# Advanced Composite High-κ Gate Stack for Mixed Anion Arsenide-Antimonide Quantum Well Transistors

A. Ali, H. Madan, R. Misra, E. Hwang, A. Agrawal, I. Ramirez, P. Schiffer, T. N. Jackson, S. E. Mohney, J. B. Boos[1], B. R. Bennett[1], I. Geppert[2], M. Eizenberg[2] and S. Datta
Penn State University, University Park, PA, USA;
[1]Naval Research Lab, Washington, DC, USA; [2]Technion - Israel Institute of Technology University, Haifa, Israel;
Tel: (814) 865-0519, Fax: (814) 865-7065, Email: aua176@psu.edu

## Abstract

This paper demonstrates the integration of a composite high-κ gate stack (3.3 nm $Al_2O_3$-1.0 nm GaSb) with a mixed anion $InAs_{0.8}Sb_{0.2}$ quantum-well field effect transistor (QWFET). The composite gate stack achieves; (i) EOT of 4.2 nm with $<10^{-7}$ A/cm$^2$ gate leakage (ii) low $D_{it}$ interface (~$1\times10^{12}$ /cm$^2$/eV) (iii) high drift μ of 3,900-5,060 cm$^2$/V-s at $N_S$ of $5\times10^{11}$-$3\times10^{12}$/cm$^2$. The $InAs_{0.8}Sb_{0.2}$ MOS-QWFETs with composite gate stack exhibit extrinsic (intrinsic) $g_m$ of 334 (502) μS/μm and drive current of 380 μA/μm at $V_{DS}$ = 0.5V for Lg=1μm.

## Introduction

Mixed anion $InAs_ySb_{1-y}$ quantum-wells (QW) with high electron mobility are candidates for integration with high hole mobility $In_xGa_{1-x}Sb$ QW for ultra-low power complementary applications[1]. With the exception of a recent $In_{0.7}Ga_{0.3}As$ QWFET with high-κ gate stack[2], nearly all QWFETs, reported to date, use Schottky gates and suffer from high gate leakage. For further scaling, a gate stack is needed for integration with $InAs_ySb_{1-y}$ QWFET, with low EOT and $J_{OX}$, good interface properties and high carrier mobility in the channel. Here, we integrate a composite high-κ gate stack ($Al_2O_3$-GaSb) with $InAs_{0.8}Sb_{0.2}$ QWFET, resulting in high performance transistors operating at 0.5V $V_{DS}$.

## Materials Characterization

MBE grown mixed anion $InAs_ySb_{1-y}$ QW exhibit room temperature electron mobility between 11,000-22,000 cm$^2$/V-s with varying electron density[3], corresponding to ballistic mean free path of ~400nm, making them promising channel material candidates for high-speed, low power electronics (**Fig. 1**). To retain the high carrier mobility in $InAs_{0.8}Sb_{0.2}$ QWFET, the high-κ dielectric is deposited on the upper barrier and not directly on the channel. We incorporated an ultra-thin (1nm) GaSb layer in the upper barrier as it avoids Al at the interface and associated surface oxidation. Using n-type and p-type GaSb(100) MOS capacitors, we evaluated both ALD and Plasma Enhanced ALD (PEALD) $Al_2O_3$ dielectrics and confirmed unpinned Fermi level in GaSb MOS system with the latter (**Fig. 2a**) [4]. By minimizing elemental Sb at the GaSb/$Al_2O_3$ interface using the low temperature PEALD $Al_2O_3$, we demonstrate low $D_{it}$ (~$1\times10^{12}$ /cm$^2$/eV) near the valence band making the composite 3.3nm $Al_2O_3$/1nm GaSb gate stack suitable for $InAs_{0.8}Sb_{0.2}$ QWFETs, where the surface Fermi level sweeps below the midgap of GaSb towards the valence band (**Fig. 2b**). From XPS measurements we estimate the valence and conduction band offsets to be 3.4eV and 2.4eV respectively, sufficient for gate leakage suppression (**Figs. 4a,b**). **Fig. 3** shows the schematic of the $InAs_{0.8}Sb_{0.2}$ MOS QWFET with GaSb and $Al_2O_3$ dielectric which forms a composite gate stack on top of the QW. **Fig. 5** shows the energy band diagram of the $InAs_{0.8}Sb_{0.2}$ QW structure with the composite $Al_2O_3$-GaSb gate stack using Schrodinger-Poisson simulation, indicating strong electron confinement in the $InAs_{0.8}Sb_{0.2}$ QW. **Figs. 6a,b** show the TEM micrographs of the $InAs_{0.8}Sb_{0.2}$ QWFET stack grown on GaAs by MBE and the active device layers. Hall measurements were performed on the device layers by varying the temperature from 4K-300K (**Figs. 7a,b**). **Table 1** shows the percentage contribution to 1/μ from individual scattering mechanisms at 300K. Near the room temperature, intra and inter sub-band acoustic deformation potential (ADP) scattering and interface defect scattering[5] dominate. Shubnikov-de Haas (SdH) oscillations (**Fig. 8a**) are observed at low temperature (2-15K) and high magnetic fields (0-9Tesla) confirming excellent channel and interface quality. An effective mass of $0.043m_0$ is extracted from the temperature dependence of the amplitude of SdH oscillations, which is lower than $0.05m_0$ reported for InAs QW due to quantization and band non-parabolicity[6]. FFT of SdH oscillations vs. 1/B at 2K (**Fig. 8b**) shows single peak confirming majority carrier transport in the first subband of the QW at $n_s$=$2\times10^{12}$/cm$^2$ and no parallel conduction.

## Device Characterization

**Figs. 9a,b** show the top view SEM and cross-section TEM of the $InAs_{0.8}Sb_{0.2}$ MOS QWFET with 100nm physical gate length ($L_G$) and the composite $Al_2O_3$-GaSb gate stack. Pd/Pt/Au metal stack was alloyed to form embedded contacts making direct contact with the QW (**Fig.10**). Circular TLM measurements before and after PEALD $Al_2O_3$ deposition are shown in **Fig. 11**. **Figs. 12a,b** show the split C-$V_G$ characteristics of $InAs_{0.8}Sb_{0.2}$ MOS-QWFET for 4.4nm and 3.3nm physically thick $Al_2O_3$ and the frequency dispersion characteristics. The EOT of the thinner stack is 4.2 nm which includes the 9 nm $Al_{0.8}In_{0.2}Sb$ barrier and 12 nm $InAs_{0.8}Sb_{0.2}$ QW capacitance. Conductance vs frequency contour plot (**Figs. 13a,b**) shows positive slope with $V_G$ indicating electron capture/emission process. This could be due to

# Report Documentation Page

*Form Approved*
*OMB No. 0704-0188*

Public reporting burden for the collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to a penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

| 1. REPORT DATE | 2. REPORT TYPE | 3. DATES COVERED |
| --- | --- | --- |
| **DEC 2010** | | **00-00-2010 to 00-00-2010** |

4. TITLE AND SUBTITLE
**Advanced Composite High-κ Gate Stack for Mixed Anion Arsenide-Antimonide Quantum Well Transistors**

5a. CONTRACT NUMBER
5b. GRANT NUMBER
5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

5d. PROJECT NUMBER
5e. TASK NUMBER
5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
**Naval Research Laboratory,4555 Overlook Avenue SW,Washington,DC,20375**

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
**Approved for public release; distribution unlimited**

13. SUPPLEMENTARY NOTES
**Proceeding of the 2010 IEEE International Electron Devices Meeting (IEDM), 6-8 Dec 2010 in San Francisco, CA**

14. ABSTRACT
**This paper demonstrates the integration of a composite high-κ gate stack (3.3 nm Al2O3-1.0 nm GaSb) with a mixed anion InAs0.8Sb0.2 quantum-well field effect transistor (QWFET). The composite gate stack achieves (i) EOT of 4.2 nm with <10-7A/cm2 gate leakage (ii) low Dit interface (~1x1012 /cm2/eV) (iii) high drift μ of 3,900-5,060 cm2/V-s at NS of 5x1011-3x1012/cm2. The InAs0.8Sb0.2 MOS-QWFETs with composite gate stack exhibit extrinsic (intrinsic) gm of 334 (502) μS/μm and drive current of 380 μA/μm at VDS = 0.5V for Lg=1μm.**

15. SUBJECT TERMS

| 16. SECURITY CLASSIFICATION OF: | | | 17. LIMITATION OF ABSTRACT | 18. NUMBER OF PAGES | 19a. NAME OF RESPONSIBLE PERSON |
| --- | --- | --- | --- | --- | --- |
| a. REPORT | b. ABSTRACT | c. THIS PAGE | | | |
| **unclassified** | **unclassified** | **unclassified** | **Same as Report (SAR)** | **4** | |

**Standard Form 298 (Rev. 8-98)**
Prescribed by ANSI Std Z39-18

the traps at the oxide-GaSb interface. **Fig. 14** plots $J_{OX}$ vs $V_G$ showing less than $10^{-7}$ A/cm$^2$ of gate leakage in $InAs_{0.8}Sb_{0.2}$ MOS-QWFET. Room temperature drift mobility values of 3,900-5,060 cm$^2$/V-s at carrier concentrations of $5x10^{11}$-$3x10^{12}$/cm$^2$ are extracted from split C-$V_G$ data (**Fig. 15**). **Figs. 16-17** show the drain current ($I_D$) vs. gate voltage ($V_G$) of $InAs_{0.8}Sb_{0.2}$ MOS-QWFET for various $L_G$ and $L_{SIDE}$. Parasitic access resistance limits the achievable on-current in the fabricated devices. For the shortest $L_{SIDE}$ of 0.25μm and $L_G$ = 1μm, the best extrinsic $g_m$ and $I_D$ at 300K are 334 μS/μm and 380 μA/μm, and at 77K are 630 μS/μm and 411 μA/μm at $V_{DS}$ = 0.5V. Peak intrinsic gm increases to 502 μS/μm (1,070μS/μm) at 300K (77K) (**Fig. 19**). **Fig. 18** shows the output characteristics of the device at 300K and 77K for $L_G$ = 1μm and $L_{SIDE}$ = 0.25 μm. The high off-state leakage of $InAs_{0.8}Sb_{0.2}$ MOS-QWFET at 300K is likely due to the hole accumulation in the $Al_{0.8}In_{0.2}Sb$ barrier layer screening the gate potential as well as the generation of holes due to impact ionization. The source side effective injection velocity, $V_{eff}$, is extracted as a function of $V_{GSi}$ - $V_T$ at 77K for $InAs_{0.8}Sb_{0.2}$ MOS-QWFET (**Fig. 20**). The highest $V_{eff}$ obtained is $1.4x10^7$ cm/s, one of the highest values ever reported for III-V MOS QWFETs.

## Conclusions

An advanced composite high-κ gate stack (3.3nm $Al_2O_3$-1.0nm GaSb) is successfully integrated in the mixed anion $InAs_{0.8}Sb_{0.2}$ QWFET with low EOT (4.2nm), negligible $J_{OX}$ ($10^{-7}$ A/cm$^2$) and high drift μ (3,900-5,060 cm$^2$/V-s). The $InAs_{0.8}Sb_{0.2}$ MOS-QWFETs with Lg = 1 μm exhibit intrinsic transconductance of 502 μS/μm and 1,070 μS/μm and drive currents of 380 μA/μm and 411 μA/μm at room temperature and 77K, respectively, all at $V_{DS}$ = 0.5V.

## References


[1]J. B. Boos et al., *IEICE Trans*. vol. E85-A/B/C/D, no. 7, July (2008) [2]M. Radosavljevic et al., *IEDM Tech. Dig*. pp. 319, Dec (2009) [3]B. P. Tinkham, et al., *J. Vac. Sci. Technol.* B 23, pp. 1441 (2005) [4]A. Ali et al., *Dev. Res. Conf.* June (2010) [5]C. Nguyen et al., Appl. Phys. Lett. pp. 1854 (1992) [6]D. Jin et al., *IEDM Tech Dig*., pp. 495 (2009)


## Acknowledgement


We acknowledge financial support from DARPA/SRC sponsored MARCO-MSD Center.

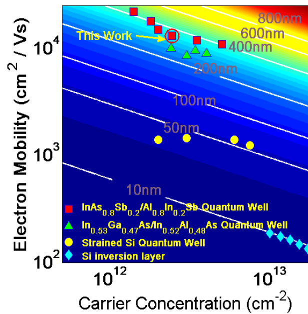




**Fig. 1** Electron mobility vs carrier concentration overlayed on a contour map of ballistic mean free path

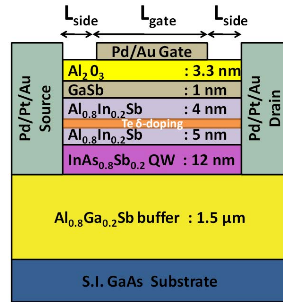



**Fig. 3** Schematic of $InAs_{0.8}Sb_{0.2}$ MOS QWFET on GaAs substrate with 1nm GaSb and 3.3nm PEALD $Al_2O_3$ dielectric which forms a composite $Al_2O_3$-GaSb gate stack on top of QW

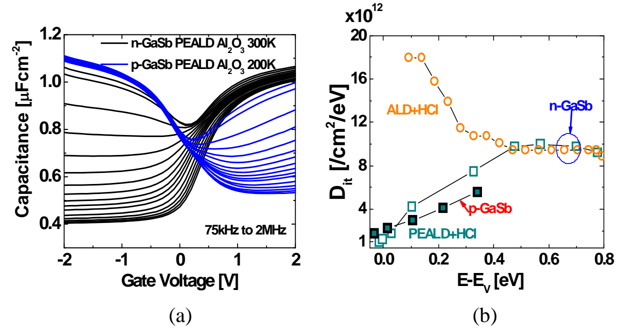



**Fig. 2** (a) Unpinned C-V characteristics of n-type and p-type GaSb (100) MOS capacitors with PEALD $Al_2O_3$ (b) $D_{it}$ of 1-3 x $10^{12}$/cm$^2$/eV near $E_V$ achieved with PEALD $Al_2O_3$ samples

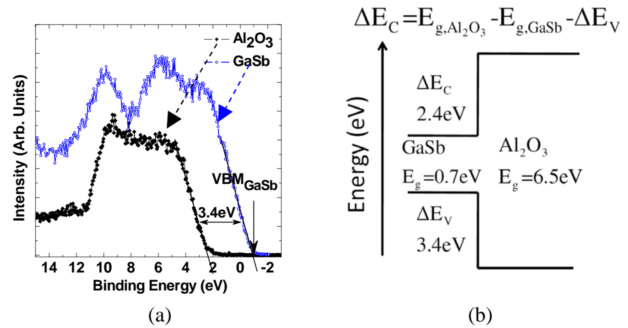



**Fig. 4** (a) Measured energy difference between the valence band spectra of $Al_2O_3$ and GaSb (100) gives valence band offset of 3.4eV (b) Valence and conduction band offsets derived from XPS analysis

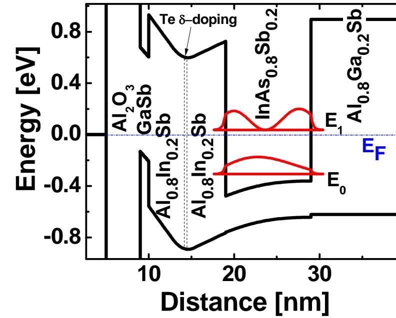



**Fig. 5** Band diagram of $InAs_{0.8}Sb_{0.2}$ MOS QWFET with 1nm GaSb and 3.3nm PEALD $Al_2O_3$ dielectric from Schrodinger-Poisson simulation

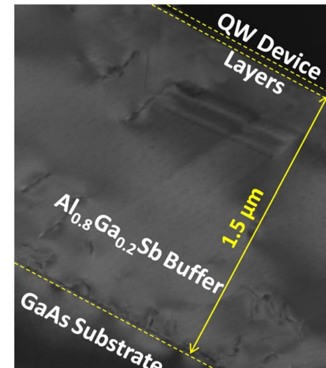



**Fig. 6** (a) Cross-sectional TEM micrograph of $InAs_{0.8}Sb_{0.2}$ QW stack on GaAs substrate using $Al_{0.8}Ga_{0.2}Sb$ relaxed buffer layer

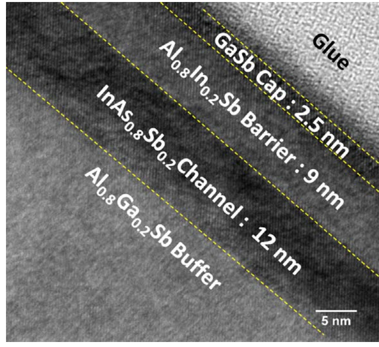
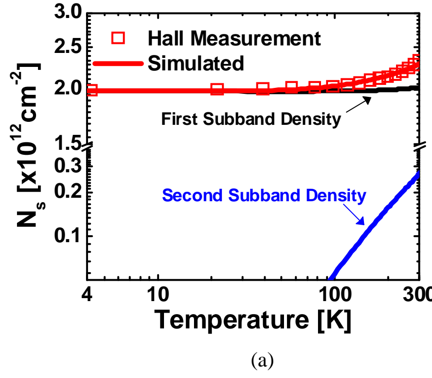
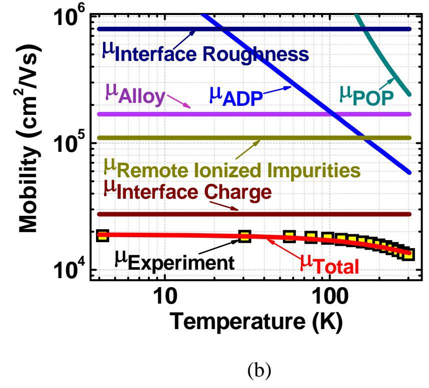



**Fig. 6** (b) High resolution TEM micrograph of $InAs_{0.8}Sb_{0.2}$ QW stack with as deposited 2.5nm GaSb (surface preparation prior to oxide deposition reduces GaSb thickness to 1nm)




(a)




(b)

**Fig. 7** (a) Carrier density ($N_s$), and (b) Hall mobility vs temperature for $InAs_{0.8}Sb_{0.2}$ QW

| | % contribution to 1/μ at 300K |
|---|---|
| Interface Charge | 50% |
| ADP Scattering | 23% |
| Remote Ionized Impurity Scattering | 13% |
| Alloy Scattering | 8% |
| Polar Optical Phonon Scattering | 6% |

**Table 1** Percentage contribution to $1/\mu_{Total}$ at 300K

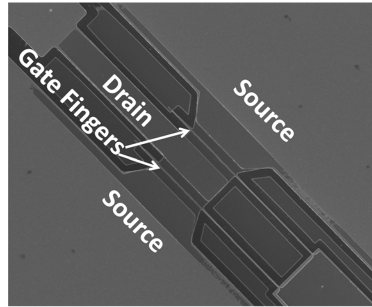



**Fig. 9** (a) Top view SEM of $InAs_{0.8}Sb_{0.2}$ QWFET with composite $Al_2O_3$-GaSb gate stack on top of the QW

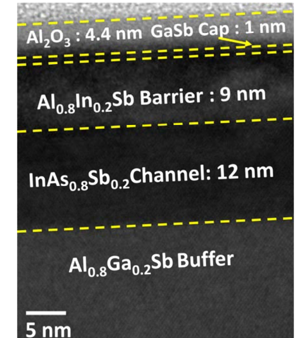
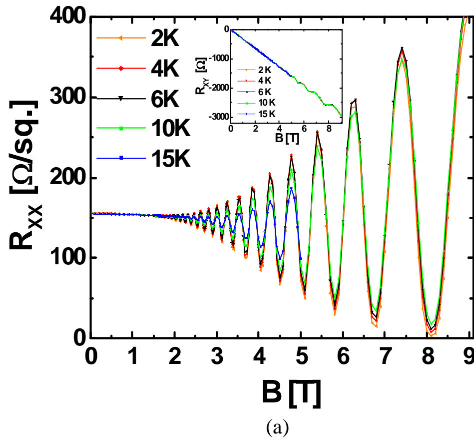
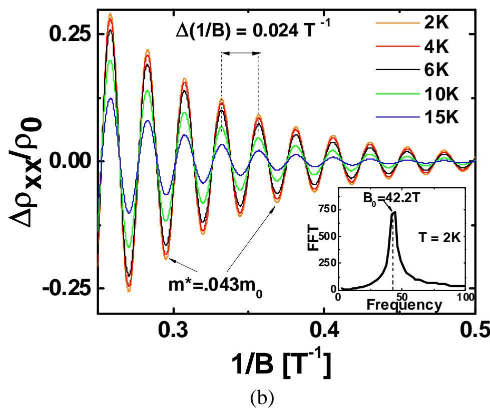



**Fig. 9** (b) Cross-section TEM of $InAs_{0.8}Sb_{0.2}$ MOS QWFET with 1.0nm GaSb-4.4nm PEALD $Al_2O_3$ composite gate stack on top of the QW

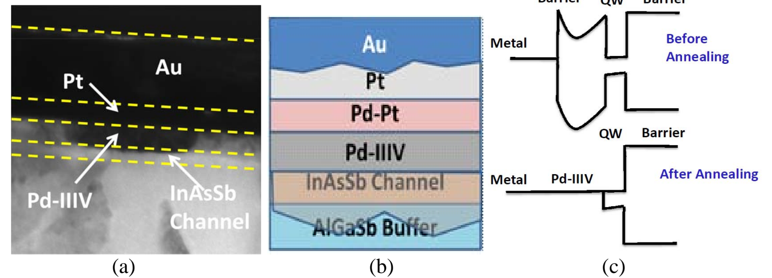



(a)




(b)

**Fig. 8** (a) Shubnikov-de Haas (SdH) oscillations in the sheet resistance. Temperature dependence of the amplitude of these oscillations is used to calculate **m*** (b) FFT of SdH oscillations vs. 1/B at 2K (inset) shows single peak confirming majority carrier transport in the first subband of the QW at $n_s$=2x$10^{12}$/cm$^2$ and no parallel conduction




(a) (b) (c)

**Fig. 10 (a)** Cross-section TEM of $InAs_{0.8}Sb_{0.2}$ MOS QWFET under the alloyed embedded contact directly contacting the $InAs_{0.8}Sb_{0.2}$ channel (b) Schematic cross-section of the region underneath the ohmic contact (c) Band diagram explaining the embedded ohmic contact formation

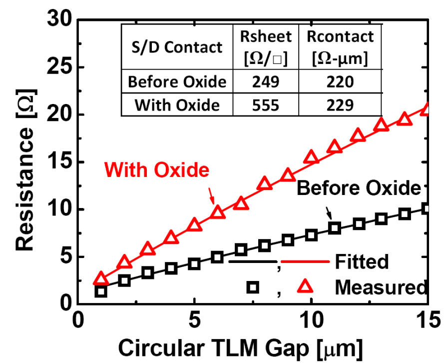



**Fig. 11** Circular TLM measurements before and after PEALD $Al_2O_3$ deposition

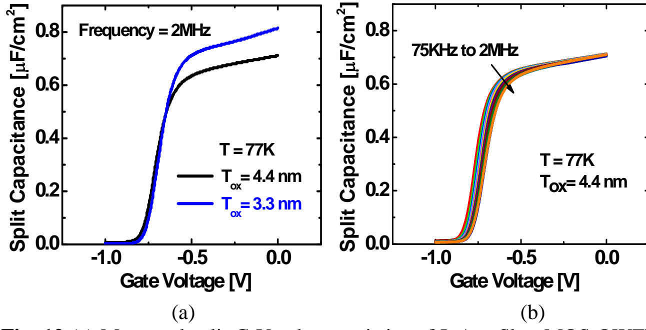



**Fig. 12** (a) Measured split C-$V_G$ characteristics of $InAs_{0.8}Sb_{0.2}$ MOS QWFET with various composite gate stack thickness (b) Frequency dispersion of the C-$V_G$ characteristics of $InAs_{0.8}Sb_{0.2}$ MOS QWFET

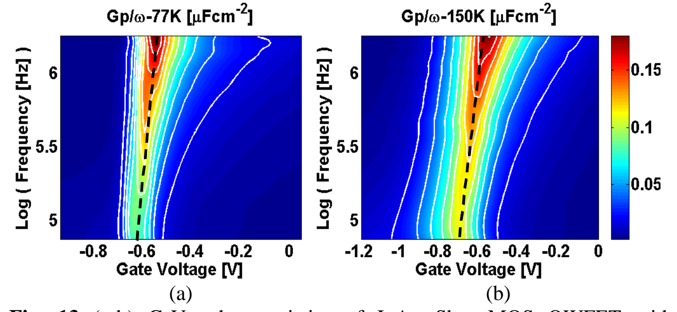



**Fig. 13** (a-b) G-$V_G$ characteristics of $InAs_{0.8}Sb_{0.2}$ MOS QWFET with composite gate stack; peak conductance trace reflects Fermi level movement in the $InAs_{0.8}Sb_{0.2}$ QW

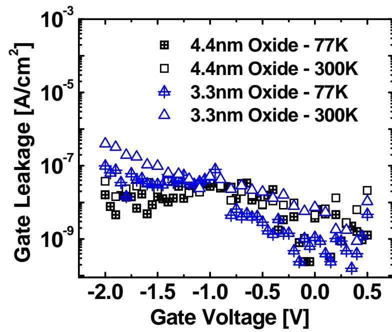
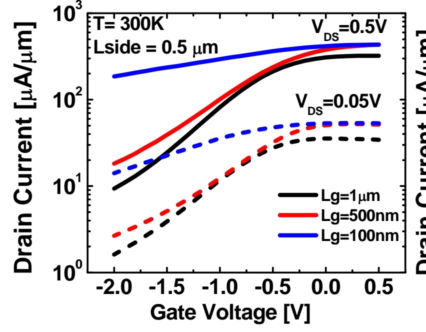



**Fig. 14** $J_{OX}$ vs $V_G$ showing lower than $10^{-7}$ A/cm² of gate leakage in $InAs_{0.8}Sb_{0.2}$ MOS-QWFET



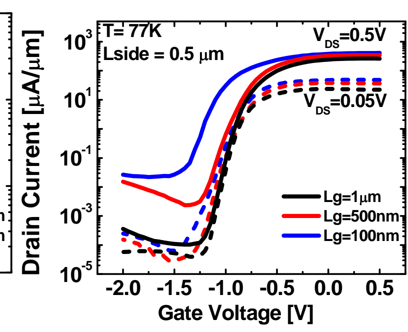




**Fig. 16 $L_G$ scaling**: Drain current ($I_D$) vs. gate voltage ($V_G$) of $InAs_{0.8}Sb_{0.2}$ MOS-QWFET with $L_G$= 1 μm, 500nm, 100nm and $Al_2O_3$-GaSb composite stack (EOT= 4.2nm) at 300K and 77K at $V_{DS}$ = 0.5V, 50mV ($L_{SIDE}$ = 0.5 μm)

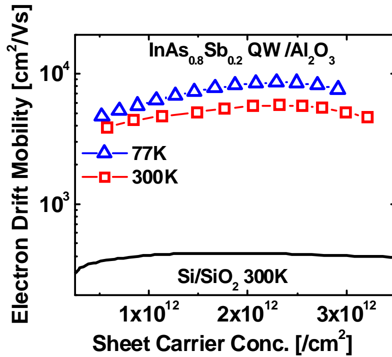



**Fig. 15** Drift μ vs $N_s$ at 77K and 300K in $InAs_{0.8}Sb_{0.2}$ MOS QWFET from split C-$V_G$ measurements

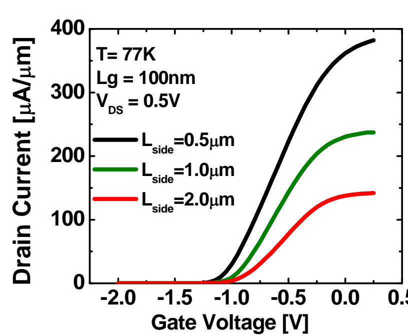



**Fig. 17 $L_{SIDE}$ scaling**: $I_D$ vs. $V_G$ of $L_G$= 100nm $InAs_{0.8}Sb_{0.2}$ MOS-QWFET with composite stack at 77K at $V_{DS}$ = 0.5Vwith $L_{SIDE}$ = 0.5, 1 and 2 μm

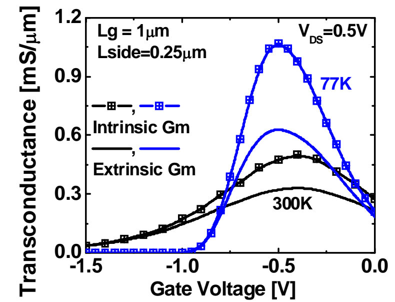
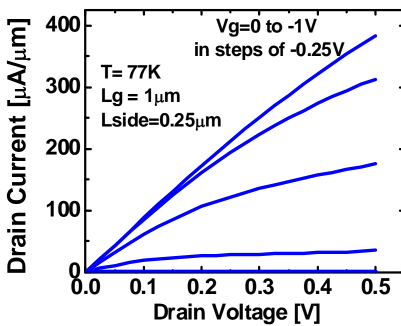



**Fig. 19** Transconductance ($g_m$) characteristics of $InAs_{0.8}Sb_{0.2}$ MOS-QWFET with $L_G$= 1 μm, $L_{SIDE}$ = 0.25 μm and $Al_2O_3$-GaSb composite stack (EOT= 4.2nm) at 300K and 77K. Intrinsic peak gm is 502 μS/ μm and 1070 μS/ μm at 300K and 77K, respectively



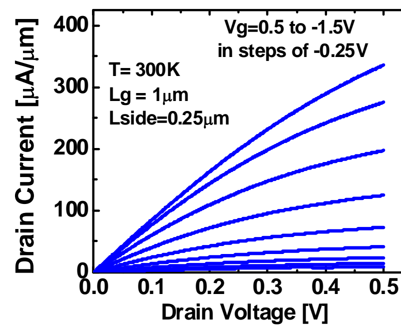




**Fig. 18 Output Charactersitics:** $I_D$ vs. $V_{DS}$ of $InAs_{0.8}Sb_{0.2}$ MOS-QWFET with $L_G$= 1 μm, $L_{SIDE}$ = 0.25 μm and $Al_2O_3$-GaSb composite stack (EOT= 4.2nm) at 300K and 77K

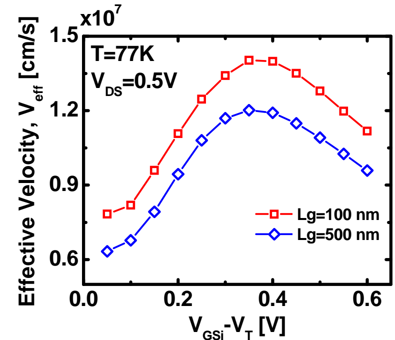



**Fig. 20** Extracted effective injection velocity, $V_{eff}$, as a function of $V_{GSi}$-$V_T$ using the charge obtained from split C-$V_G$ measurements and $I_{D,SAT}$ vs $V_{GSi}$-$V_T$. The $V_T$ from split C-$V_G$ is matched to the $V_{T,SAT}$ from $I_{D,SAT}$ vs $V_{GSi}$-$V_T$ to obtain $V_{eff}$