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Demonstration of a 10 GHz CMOS-Compatible Integrated Photonic Analog-to-Digital Converter

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Abstract: We demonstrate a photonic ADC using mostly CMOS-compatible devices integrated on silicon to optically sample and electronically digitize a 10-GHz RF signal with 37.9 dB SNR (6.0 ENOB) with a 1 GSPS optical pulse train.

OCIS codes: (070.1170) Analog optical signal processing, (250.5300) Photonic integrated circuits, (140.4050) Mode-locked lasers

Photonic sampling coupled with electrical digitization and quantization has the potential to extend the performance of analog-to-digital conversion (ADCs) orders of magnitude beyond what is possible with all-electrical ADC technology by exploiting two features: the ultralow timing jitter (< 10 fs) of modelocked lasers for sampling, and interleaving multiple lower-rate samples in parallel with high optical-to-electrical isolation. There are numerous approaches to photonic ADC architectures that have been proposed and demonstrated, including phase-encoded sampling [1], time stretching [2-4], and MSM switching [5], each exhibiting various degrees of complexity and performance (also see review article [6]). Most methods require channelizing and interleaving the high-rate optical samples to a lower rate that can be quantized with conventional ADCs, and the resolution of the system requires that each channel be carefully controlled with extreme precision. Most of the demonstrated approaches to date are difficult to scale beyond a few-to-tens of channels using bulk components. Optical sampling and channelization in a CMOS-integrated silicon substrate has the potential to alleviate both constraints. We have proposed an optically-sampled ADC architecture—GigaHertz Optical Sampling Technology (GHOST)—where most of the required devices, including the optical Mach-Zehnder modulator, filter banks, and photodetectors, are integrated on a CMOS chip developed as part of a library of Electronic Photonic Integrated Circuit (EPIC) devices as described elsewhere [7]. In this work, we demonstrate GHOST using CMOS-compatible photonic components on an EPIC chip to digitize a 10 GHz RF signal resulting in a quantized, aliased signal (sampled in this demonstration at 1 GSPS) with 37.9 dB SNR (6.0 ENOB) at -15 dBFS of the ADC and mainly limited by the available optical signal power.

In the GHOST sampling architecture, to create an effective sampling rate of 20 GSPS to digitize a 10 GHz RF waveform requires 20 pulsed wavelength channels that are each sampled and quantized at 1 GSPS and then interleaved digitally. The 20 pulsed wavelength channels are generated off chip using a modelocked laser and either a demultiplexer with time delays or an appropriate length of dispersive fiber [7] to create the proper mapping of wavelength and temporal sampling position, and quantization and digitization are achieved with twenty electronic ADCs and a computer for signal reconstruction. For these experiments, we only generated two of the twenty wavelength channels for demonstration purposes. The optical pulse train at 1.05 GHz was generated with an Erbium-doped linear-cavity fiber laser producing 200fs pulses and 10 mW output power 0. The pulse train was split, filtered, and recombined (using two 3-dB fused-fiber couplers, two 0.8-nm optical filters (Koshin Kogaku, one tuned near 1575 nm and the other to 1576 nm), and a variable time delay (Santec, ODL-330)) to produce a composite pulse train at 2.1 GHz. The pulse train was then amplified using a 45-dB gain L-band EDFA to produce ~+4 dBm average optical power and coupled to the EPIC chip with a tapered optical fiber. The EPIC chip (fabricated and packaged at Lincoln Laboratory) contains a dual-output silicon modulator with a 500-μm p-n junction operated in depletion [9]. At low bias voltages the modulator has a $V\pi L$ of 1 V·cm and a bandwidth of 10 GHz. The GHOST architecture and EPIC chip are shown in Figure 1.

The coupled 2.1 GHz sampling pulse train was modulated by an externally-applied 10 GHz waveform with an integrated dual-output modulator (reversed biased with ~ -2.0 V) and thermally biased to be in quadrature, and each of the two wavelength channels were split into two complimentary outputs and demultiplexed down to 1.05 GHz

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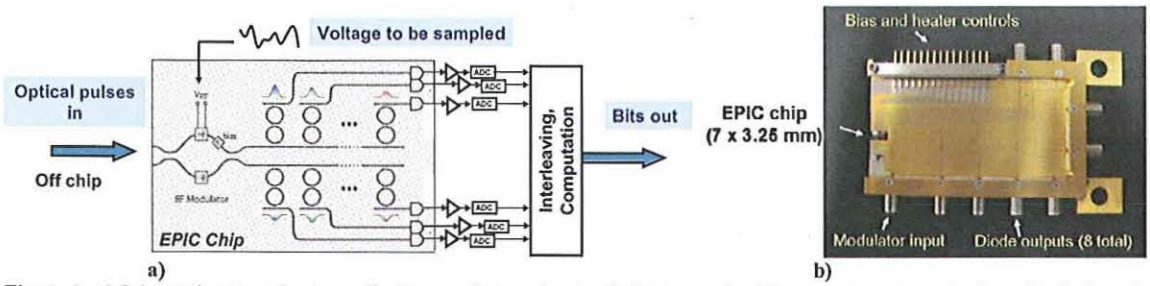

Figure 1. a) Schematic layout for the optically sampled analog-to-digital converter. The grey-box elements show the devices that were integrated onto a monolithic CMOS EPIC chip, including a dual-output optical modulator, three pairs of matched second-order microring filter banks, and four pairs of photodiodes; and b) Top-view of EPIC integrated chip and packaging with SMA connectors for the modulator input and eight output photocurrents, and 15 low-speed connections for modulator biasing and second-order microring filter tuning.

with a complimentary pair of second-order, thermally-tuned microring filters nominally 5.0 μm in diameter with Ti heaters for tuning. The demultiplexed pulse train was then detected with an integrated silicon waveguide photodiode [10] biased at +5.0 V to generate an average ~10 μA photocurrent. Post-detection electronics were used to boost the small photocurrent to span the full-scale peak-to-peak input voltage of the following ADCs (although in this experiment the full-scale voltage could not be achieved). The post-detection electronics consisted of a 3-GHz Gaussian low-pass filter, a DC block, preamplifier (H2 Com 24471, 19-dB gain), amplifier (Hittite 641, 13-dB gain), and a balun. The electronic ADCs were National Semiconductor ADC10D1000 with two 1 GSa/s differential input channels operating at 9.0 ENOB on an evaluation board with a Virtex 4 FPGA. The ADCs were synchronously clocked with an RF signal regenerated from the unmodulated optical pulse train using an amplified photodiode, RF filter, and clock distribution circuit (National Semiconductor LMK01000), and the resulting data from the FPGA was post-processed on a computer. Variable optical and RF delay lines were used to precisely align the modulated optical pulse train with the ADC sampling clock. **Error! Reference source not found.** shows the raw output spectrum from one of the modulator outputs for one of the two wavelength channels. The 10 GHz signal (effectively sampled at 1.05 GSPS) was aliased to ~430 MHz, and the resulting SNR was 37.9 dB (6.0 ENOB) with only -15 dBFS and, to our knowledge, represents one of the first demonstrations of an integrated photonic-sampled ADC. The SNR was limited by the relatively small digitized signal power available to the ADC for digitization, owing partly to the limited optical signal power at 1575 nm, and partly due to the on-chip losses that were higher than expected. Second and third harmonics of the signal were generated by the sampling process and limited the SFDR to 31 dB. Linearization has been shown [1] to dramatically reduce the SFDR when using a $LiNbO_3$ electro-optic modulator for sampling, but the proper linearization algorithm when using a silicon modulator remains under study.

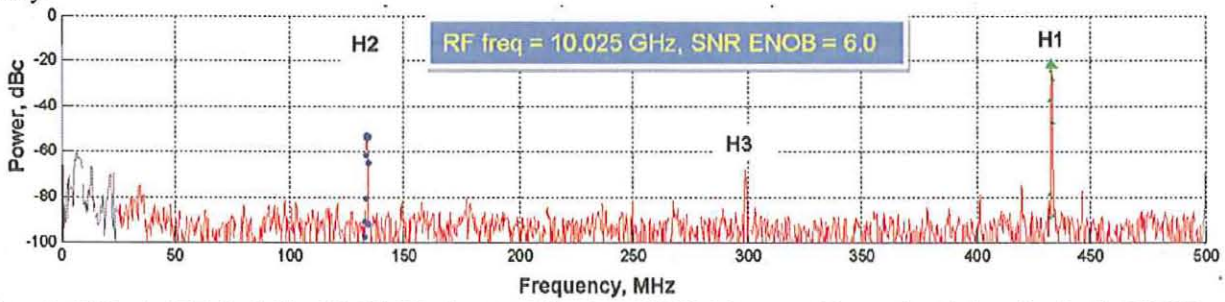

Figure 2. 1048-point FFT of a digitized 10.025 GHz sine wave (aliased to ~430 MHz) from one of the wavelength channels using the GHOST ADC with one sampling channel at ~1 GSPS where 0 dBc refers to the full-scale ADC voltage. The -15 dBFS signal (H1) has an integrated SNR of 37.9 dB (6.0 ENOB) and limited by the available optical signal power available at 1575 nm and on-chip optical losses. The second- and third-harmonic distortions (H2 and H3, respectively) limited the raw SFDR (without linearization) to 31 dB.

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