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14. ABSTRACT Lack of availability of Integrated Circuits (ICs) continues to have an adverse impact on the readiness of military systems, and is a significant cost-driver for DoD. The Defense Logistics Agency (DLA) has two successful IC manufacturing (microcircuit emulation) programs, which address these issues. The successful design, qualification and production of emulated microcircuits are dependent on hundreds to thousands of electrical tests and measurements to ensure product integrity and full compliance to QML standards. Manufacturing technology improvements to the emulation test capability to significantly reduce test cycle time by as much as 95% and increase the ability to address more complex ICs have been implemented into the emulation manufacturing flow. The benefits to the military supply chains are less pressure for life-time buys, reduction in lead-time for spare parts and a long-term source of supply for a larger number of NSNs.						
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Section I

Introduction

The low-volume demand for Integrated Circuits (ICs) by the Department of Defense (DoD), the constantly decreasing IC supplier base, the continual shortening of commercial IC product life-cycles, and the rise of counterfeit ICs in the supply chain are just a few of the challenges the Defense Logistics Agency (DLA) faces when addressing Warfighter microelectronics requirements. Lack of availability of ICs continues to have an adverse impact on the readiness of military systems, and is a significant cost-driver for DoD. DLA has two successful IC manufacturing (microcircuit emulation) programs, which address these issues. To date, these programs have supplied over 100,000 microcircuits in support of over 375 unique weapons systems applications including F-15, F/A-18, F-22, C-17, AEGIS, Phalanx, and the Bradley Fighting Vehicle. The emulation programs have saved the Government over \$700 million in costly redesign efforts. Accurate and effective testing is critical to the ability to design, manufacture, and qualify emulated microcircuits for military platforms. Manufacturing technology improvements to the emulation test capability to significantly reduce test cycle time by as much as 95% and increase the ability to address more complex ICs have been implemented into the emulation manufacturing flow.

Test Process

The design, qualification and production steps for emulated microcircuits are dependent on hundreds to thousands of electrical tests and measurements on each individual microcircuit. All military grade microelectronics requires rigorous electrical testing to validate that every specified characteristic is in strict conformance to the applicable specification. This testing is required multiple times throughout the design and production flow of emulated ICs to ensure product integrity and full compliance to QML standards (see Figure 1). At the beginning of the emulation process (“Test Sample”), electrical testing is used to evaluate a known-good, sample IC from the original manufacturer. This testing confirms that the IC performs in accordance with its documented requirements. In addition, characteristics which are critical to the correct operation or design of the IC—but not specified in the original documentation—will be measured. These measured data are used during the emulation design process to match the actual performance of the emulated IC to the original IC.

The same tests used to evaluate the original manufacturer’s known-good sample are also used to test the prototype emulated IC over the full operational range to validate the

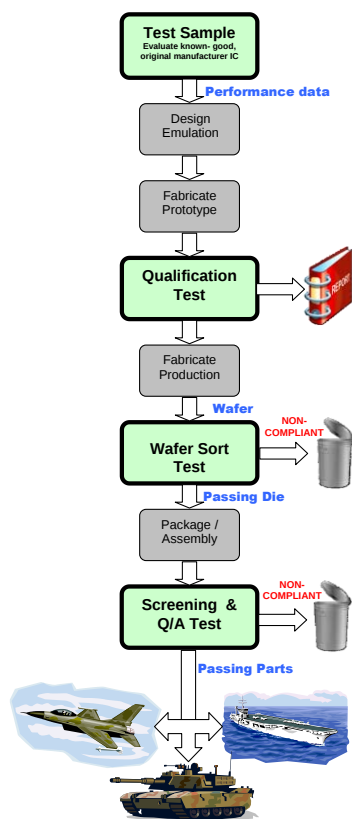


Figure 1 – TEST in the emulation process

performance (“Qualification Test”). After fabrication of production wafers, containing multiple microcircuit die, testing is used to identify any die with manufacturing defects so that downstream resources are not consumed by non-compliant die (“Wafer Sort Test”). After the assembly of production die into packages, each IC is tested over the full operating range to ensure that it is fully compliant to the required specifications (“Screening and Q/A Test”). Accurate and effective testing is critical to the ability to design, manufacture, and qualify emulated microcircuits for military platforms. As more advanced microcircuits are emulated, electrical testing must also advance to measure and validate ever higher levels of performance and complexity. To perform the necessary tests and measurements of digital microcircuits, sophisticated, computer-controlled instrumentation is required. Such instrumentation and associated control software are developed, integrated and sold as ATE systems. For each microcircuit type and package variation, customized and dedicated test fixture hardware and ATE test programs are created. Once the test programs and hardware are verified, testing of that microcircuit type again is merely a matter of mounting the appropriate test fixture and loading the associated test program into the ATE system.

Summary

To support DLA's diverse and expanding microcircuit emulation requirements in a timely manner, the emulation test capability was enhanced to improve testing performance and sustainability via deployment of more current supportable, reliable and robust Automated Test Equipment (ATE) test system for the emulation programs. This provides the improved performance to not only maintain the existing emulation production capability, but also to address DLA's demand for the emulation of more complex IC's. In addition, the improved test capability provides the flexibility and expandability to support both normal and surge demands. The approach to achieving these objectives was partitioned into three tasks.

Deployment of sustainable, emulation ATE capability:

With the rapid pace of technological advancement in the semiconductor industry, ATE systems advance to keep pace with market demands. Typical product life of an ATE system is three to five years with succeeding generations providing capability for faster and more complex ICs. Different ATE systems utilize different architectures in hardware and/or software. Therefore, the test programs developed for one ATE system cannot be used to perform the same tests on a different ATE system. The migration path to a supportable, reliable and robust ATE system is essential to preserve the emulation program's testing capability. This conversion to a modern, maintainable ATE system not only preserves the man-decades of investment in test programs developed, but must also support the testing requirements for future emulation developments of more complex, higher speed, higher pin count ICs. A viable migration path has been created and proven. This migration path enables the emulation programs to perform a cost-effective and orderly migration of the man-decades worth of existing test programs.

Installation and validation of parallel testing capability of multiple ICs:

As the emulation programs expand, testing of more advanced, higher pin count ICs is required. To support the testing of high pin count ICs, additional pin electronics have been added to the existing ATE system. The ability to test individual single ICs in excess of 400 pins has been implemented into the emulation manufacturing flow.

In addition, to address the need for increased operational flexibility to accommodate varying potential surge requirements, the ability to perform simultaneous, parallel IC testing was incorporated into the emulation test capability. The installation of parallel IC test utility software allows the added pin electronics to be used for simultaneous, parallel IC testing. A software utility automatically adapts test programs created for a single IC to support parallel, simultaneous testing. This automatic conversion virtually eliminates the additional development time and expense otherwise needed to develop and implement parallel testing.

Installation and validation of enhanced wafer testing/sorting capability:

Wafer test is performed following fabrication of the wafer to identify and remove non-compliant die before assembly into the final package. In the case of simple logic ICs using common, low pin-count packages, the cost of assembling, testing and discarding non-compliant packages can be less than the cost of performing the wafer sort test. However, as IC pin count and complexity increase, the cost of packages increases dramatically. In addition, many high-pin-count military packages are custom manufactured in limited quantities, resulting in both limited availability and high unit cost. In this situation the cost of discarding non-compliant ICs in valuable packages can become prohibitive. In the realm of complex, high-pin-count ICs, the vast majority of marginal performance issues occur at high temperature. To detect these parts on the wafer at die level, the temperature of the wafer must be raised to the worst-case temperature experienced in the package. With the wafer/die heated to this temperature, the critical performance characteristics are then measured to identify and remove marginal die.

The ability to perform wafer sort testing at worst case, high temperature condition has been implemented into the emulation manufacturing flow. With this capability in place, the most efficient consumption of the scarce, custom IC packages can be achieved. A less tangible, but equally important benefit is the ability to anticipate final product yield as many as eight weeks earlier in the manufacturing cycle. Such early detection of an unanticipated low yield enables a much higher likelihood of a timely recovery.

Conclusions

All of the objectives have been achieved. The conversion utility has successfully converted a variety of existing test programs which executed on new ATE using existing test fixtures. Parallel testing of up to eight (8) complex emulation parts was achieved using the upgraded configuration of the new ATE system which will support testing of devices with more than 400 signal pins. A hot-chuck, wafer probe system was configured, installed and validated to enable full clock-speed testing at worst case conditions. A decrease in test times by more than 30X has been demonstrated. The new capabilities remain in-place and are available for immediate use with minimal cost or delay for complete implementation into the emulation manufacturing process. The program conclusions and their resulting metrics can be seen in Table 1.

Goals for Improving DLA's IC Manufacturing (Emulation) Programs				
Program Duration	Diminishing Critical Defense Industrial Base		Surge	
	Preserve	Extend		
Develop and Implement Emulation Test Capability Improvements 11 months	Maintain >\$5M DLA investment in existing test programs by transferring test capability to a robust sustainable system	Increase capability to test more complex ICs by 3X Reduce test development time using hardware independent template on modern ATE Improve yield through improved accuracy Minimize cost and waste by detecting defective parts earlier in manufacturing cycle	Increase production capacity by 20X through use of parallel testing, reduction in test execution time and improved equipment availability/up-time	
Metrics	IC Test Capacity	Baseline	Objective	Result
	Test Capability for Higher Pin Count ICs	4 part/hour	80 parts/hour	120 parts/hour
	Test Capability for Higher Pin Count ICs	112 pins	384 pins	516 pins
	Test Capability for Higher Speed ICs	100Mhz	533 MHz	800MHz
Military Value	Reduce necessity for life-of-type-buys Reduce lead-time for spare parts Reduced system maintenance cost Long-term source of supply for a larger number of NSNs			

Table 1 – Summary of goals and metrics

Section II

Task 1 - Deployment of sustainable, emulation ATE capability

The initial task developed a conversion utility to “translate” test programs written for the installed base of unsupported, 1990’s-vintage, HP 82000 (HP82K) test systems to a supportable ATE platform. The target ATE was the V93000 (V93K) test system which is actively produced, supported, and maintained by Verigy. Verigy is the current incarnation of the former HP semiconductor test business. The DLA Advanced Microcircuit Emulation (DLA-AME) program has such a tester already in-place. An existing HP82K test program for a 40-pin, bit-slice microprocessor was selected as the demonstration vehicle since it utilized both the greatest variety and largest quantity of the test capabilities of the legacy testers.

Since the commercial semiconductor market has no need to migrate legacy products to new production facilities, no commercial utilities were available. Therefore, Verigy, (the designer and manufacturer for both systems) was sub-contracted to develop the conversion utility. The resulting utility reads HP82K configuration data and generates the corresponding V93K test program.

Results

The conversion of existing test programs from the 1990’s vintage HP 82000 test system (HP82K) to the state-of-the-art Verigy V93000 test system (V93K) was both critical to the performance of the other two tasks as well as the key technical challenge. The HP82K was originally targeted as a user-friendly, interactive system to allow semiconductor design engineers to easily evaluate and characterize the performance of new devices. It is based on an HP Unix workstation linked to the tester electronics via IEEE-488 interface. Specialized, menu-driven software allows all the test configurations to be entered using menu-like forms. This windowed software interface converts the user input into ASCII files containing the relevant settings for the test hardware. When an IC is tested, the workstation transmits these ASCII files to the test hardware over the IEEE-488 interface. This lock-step relationship between the ASCII files and the direct control of the test electronics allowed a very simple but effective test development environment appropriate for the technology of the era.

To date, this straight-forward hardware/software has effectively met the requirements of the emulation programs. However, the inexorable march of technology required more advanced capability for testing modern semiconductor technologies. HP discontinued production of the HP82K system in 1997. All related software and hardware support ceased on October 31, 2003. While still remaining effective tools for emulation activities, these aging HP82K test systems are approaching the end of their useful life.

The Verigy V93000 test system is intended to support high volume testing of advanced system-on-chip, mixed signal devices. Using advanced hardware and software, it can be configured to test IC’s exceeding 1,000 pins at clock rates exceeding 1Ghz. Unlike the

HP82K, the V93000 leverages open-source operating system and development environment on low-cost, high-performance computer hardware. The software environment uses C++ object-oriented programming methods to provide a high degree of abstraction appropriate for testing of complex, modern semiconductor devices. The test electronics contain specialized controllers to quickly change between pre-stored condition sets to maximize testing speeds.

In the normal product and economic life cycle of the semiconductor business, new technologies, design approaches, manufacturing facilities and test systems are deployed to support production of specific, high-volume microcircuits. Once the high-volume market for products from this technology are supplanted by the next generation, the products are discontinued and the associated production capability dismantled or redeployed. In this environment, there is no commercial motivation to support conversion of existing test methods to new generations of test equipment.

The DoD usage of microcircuits is distinctly different from the commercial marketplace. Beyond the obvious differences of more stringent operating environments and reliability requirements, military applications have development and usage lifetimes measured in decades versus commercial product cycles measured of months. The goals of the emulation programs further exacerbate this life-cycle difference since production capability must remain in place indefinitely irrespective of the finite life of the equipment required to perform this production.

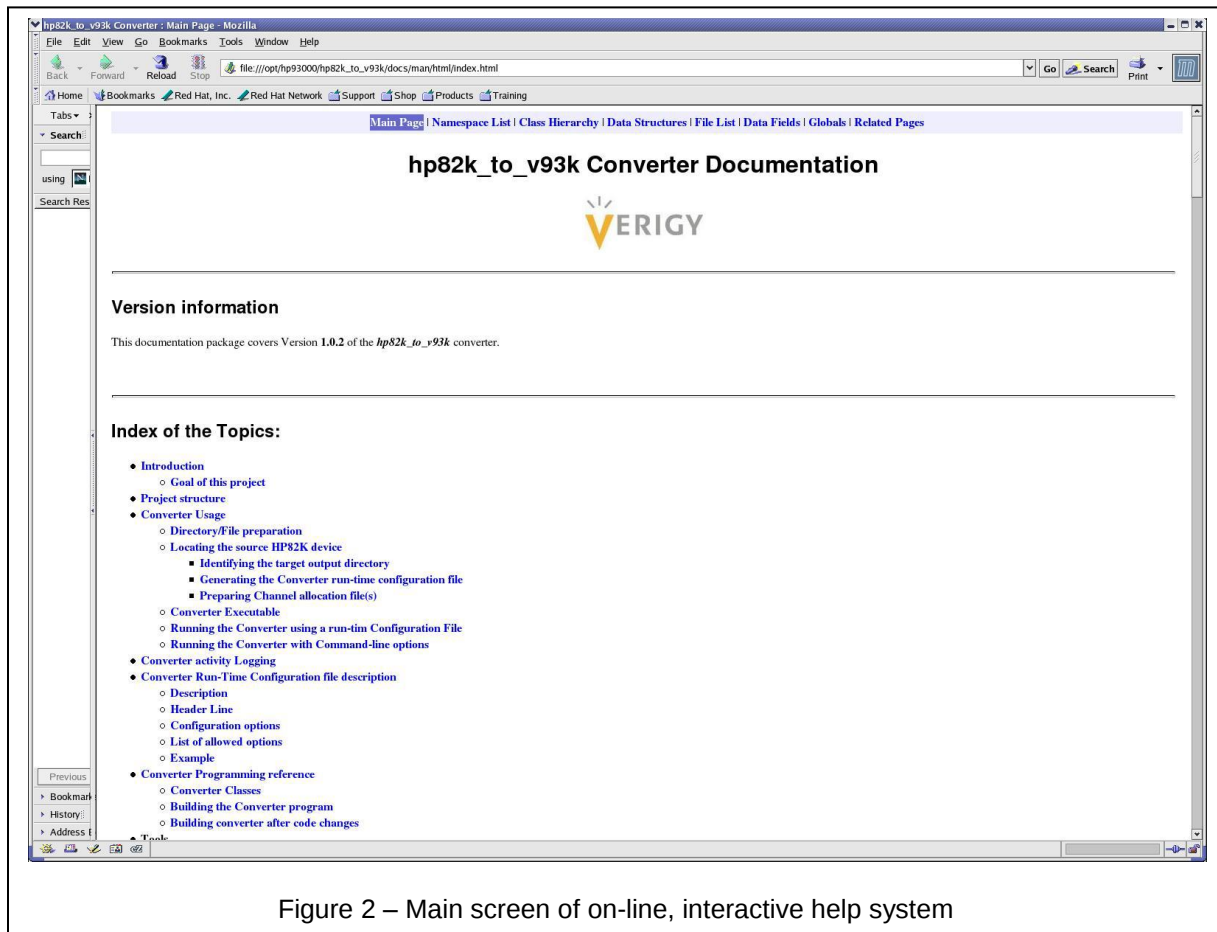


Figure 2 – Main screen of on-line, interactive help system

To maintain cost effective production of the emulation programs, it is essential to maximize reuse and preservation of more than ten years of HP82K test program development. It was determined that development of a test program conversion utility was the optimum solution. The conversion utility approach agreed between Sarnoff and Verigy was to take maximum advantage of the AIT and AIV utilities, part of the V93K ASCII Interface tool suite. The conversion would target the latest test operating system software release, Version 6.5 to ensure maximum capability and future software compatibility. All newly developed utilities were written in C++ with interactive, web-based documentation created using *doxygen* (Fig 2). The architecture of the conversion process is diagrammed in Figure 3.

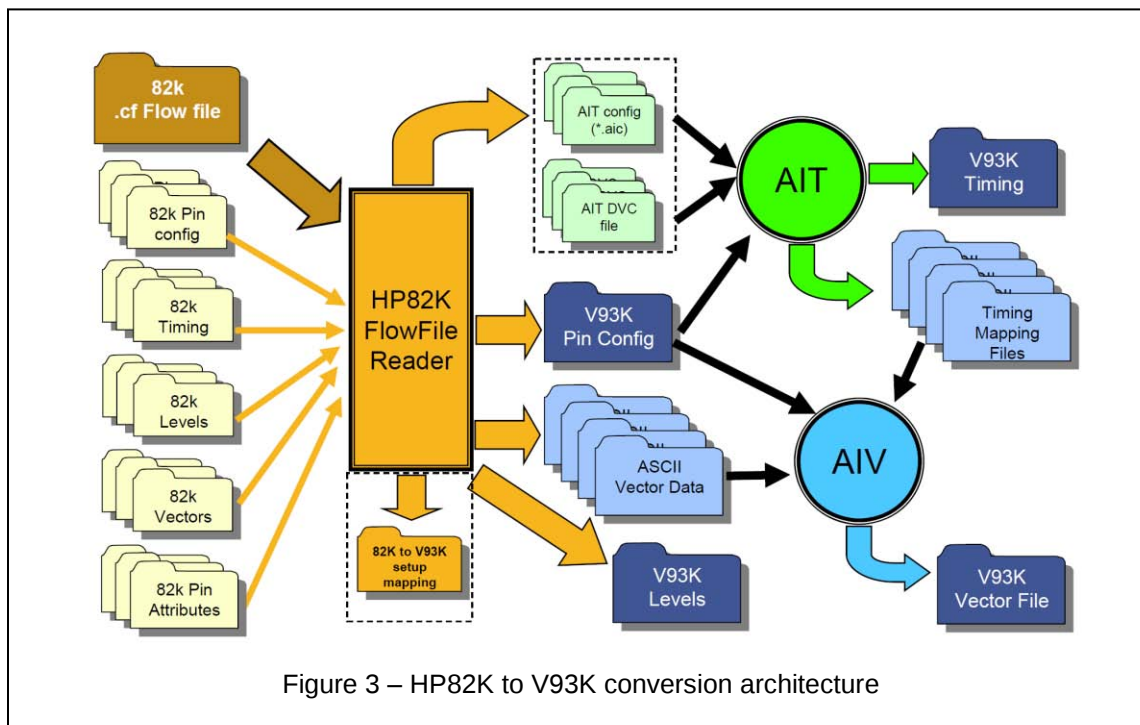


Figure 3 – HP82K to V93K conversion architecture

An existing HP82K test program for a 40-pin, bit-slice microprocessor was selected as the demonstration vehicle since it utilized the greatest variety and quantity of the conventional test capabilities of the legacy testers. This test program consisted of the directory tree of the file types above plus a top level file which links and sequences the all subsidiary files. Brief examples of the data in these files follows.

Each pin config file contains an entry for each device pin of the form:

```
dfpn 10508,"15", (cp)
conf i,std,p, (cp)
```

which relate a pin name (cp) , pin number (15) to a specific ATE hardware channel (10508), as well as defining the mode of that hardware channel (i,std,p). The timing files contain entries for each pin of the form:

```
DRTM R1,150,250, (cp)
```

Which specify the waveform format (R1) the leading (150nS) and trailing (250nS) edge timings for each pin (cp). Similarly, the levels files contain the high and low level drive levels for each pin:

```
DRLX 0,3000,3000, (cp)
```

In this case, a low level of 0mV, a high level of 3000mV (3.0V), and a total swing of 3000mV (3.0 V). Vector files contain the sequential truth-table (in binary format) for the functional test being performed.

The HP82000 electronics supports twelve (12) specific measurements used for emulation microcircuit testing: continuity, functional, general_pmu, global_search, global_search_track, hold_time, inp_volt_sensitivity, operating_current, output_dc, rise_fall_time, and setup_time. The specifics of a test are captured in a test file which contains the pin(s) to be tested, the specific measurement to be performed and the ranges/conditions for the measurement. To measure the clock pulse width, the test file is:

```

hp82000,testfunction,0.1
global_search      ← measurement type
cp                 ← pin to be measured
in/te              ← parameter to be varied (input trailing edge)
binary             ← method of variation
ns                 ← units of variation
170                ← starting value (absolute number)
150                ← ending value (absolute number)
0.1                ← step/increment value
Le                 ← reference parameter (leading edge)
Cp                 ← reference pin
.500               ← minimum passing value
14.500             ← maximum passing value

```

Finally, a test suite file associates a particular set of pin configuration, timing, level and vector file with one or more test file. Continuing the clock pulse width, the measurement and conditions are specified as:

```

tpwh_suite:
pins= config_ot;      ← pin configuration file name
timing = timing_clkh;  ← timing file name
levels = levels_45_tpd; ← levels file name
vectors = vectors_clkh; ← vector file name
tests = test_attr,test_tpwha,test_lvs50pw,test_tpwhb,
test_lvs55pw,test_tpwhc; ← test file(s) to be executed

```

The developed test conversion utility reads all the HP82K files into a temporary database to enable efficient re-formulation in to the formats required for the V93K. In the process, the converter provides a number of useful diagnostic and summary statistics:

```

-----
| hp82k_to_v93k,  Version 1.0.5 (svn r483) |
|               Build on October 22,2010 |
| (c) Copyright 2009-2010, Verigy Ltd    |
-----
Converter starting with the following parameters:
  HP82K Shell File to process = [ pkggt.cf ]
  HP82K device directory path = [ /users/art/Device_068 ]
  Target V93K file path = [ /users/art/CircuitTest/ ]
  V93K Channel Allocation File = [ /users/art/Dev068_V93K_Channel__1_site.csv ]
  Force_V93K_device = [ FALSE ]
  V93K_PinConfig_only = [ FALSE ]
  Debug Level = [ 4 ]
Extracting data from HP82K TestFlow File "/users/art/Device_068/shell/pkggt.cf"
...
  HP82K TestFlow file data extraction Done!

-----
HP82K TestFlow file Statistics:

Information  Section Data size = 6 Elements
Files        Section Data size = 1 Elements
Flags        Section Data size = 5 Elements
Pins         Section Data size = 6 Elements
Levels       Section Data size = 59 Elements
Timing       Section Data size = 25 Elements
Vectors      Section Data size = 73 Elements
Test-Function Section Data size = 276 Elements
test_flow    Section Data size = 64 Elements
binning      Section Data size = 18 Elements

TestSuite Section PinConfig list size = 6 Elements
TestSuite Section Levels list size = 24 Elements
TestSuite Section Timing list size = 25 Elements
TestSuite Section Vectors list size = 57 Elements
-----
...
TestSuite "tpwh_suite" ...
Pins label = "config_ot"
Level label = "levels_45_tpd"
Test Label[1] "test_tpwha" ...
  Creating new Level label element: "levels_45_tpd"
  Assigning new Pins label "config_ot" to new Level Element
Test Label[2] "test_lvs50pw" ...
  Changing LevelsLabel to "lvs50pw"
Test Label[3] "test_tpwhb" ...
  Creating new Level label element: "lvs50pw"
  Assigning new Pins label "config_ot" to new Level Element
Test Label[4] "test_lvs55pw" ...
  Changing LevelsLabel to "lvs55pw"
Test Label[5] "test_tpwhc" ...
  Creating new Level label element: "lvs55pw"
  Assigning new Pins label "config_ot" to new Level Element

```

In the demonstration case, this translation utility was executed in 13 seconds while generating a log file of more than 35,000 lines.

To effectively support the requirements of complex, modern microcircuits, the V93K programming environment makes extensive use of higher-level, abstracted specifications which are related more to the part being tested than to the specifics of the ATE hardware. For example, instead of the simple high and low drive level specifications of the HP82K, the V93K utilizes an equation-based approach. While this approach is highly efficient for the development of new test programs for new, complex devices, it significantly

complicates the conversion of straight-forward, legacy test programs. The specification for timing on the V93K is even more complex, as shown below in Fig. 4.

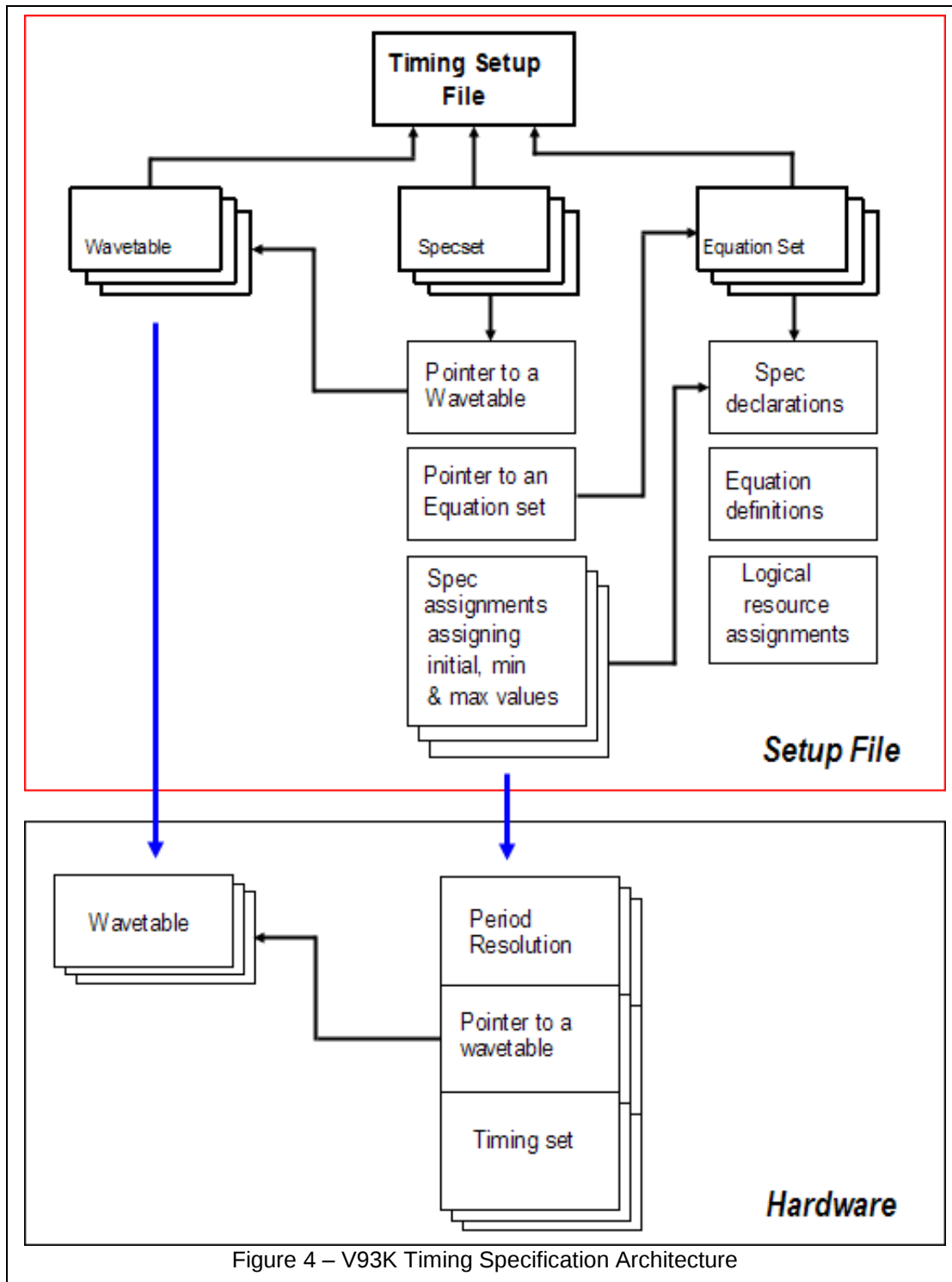


Figure 4 – V93K Timing Specification Architecture

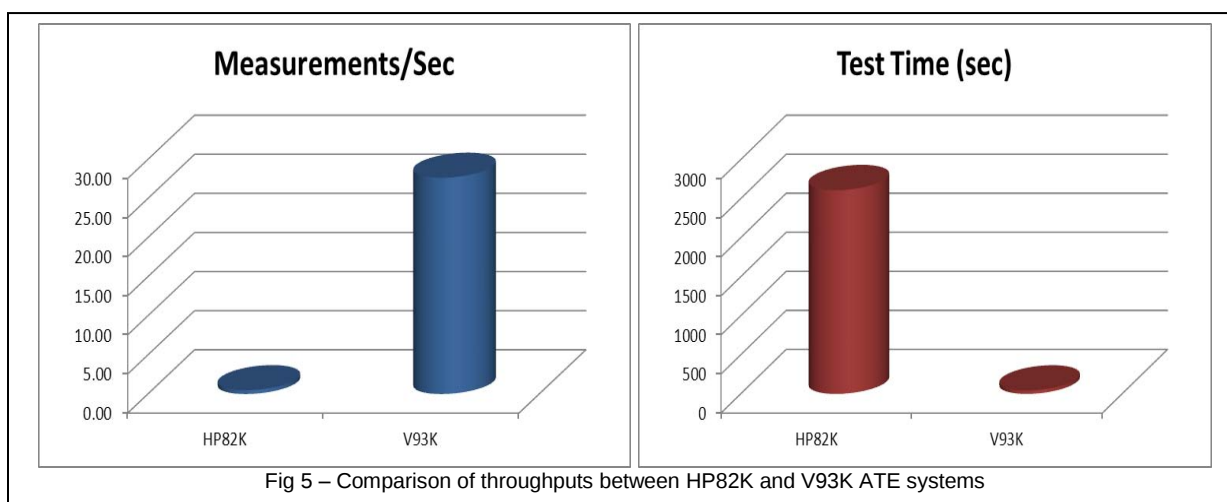
Further complicating the conversion, was the use of series impedance matching resistors on the HP82K which were not directly by V93K, as well as some customized HP82K test functions. To support these legacy HP82K requirements, customized test methods were created on the V93K to provide direct equivalence to the HP82K methods.

The converter maps HP82K to the corresponding, customized V93K functions, generates the full set of equations for timing and levels, and then creates the comparable test flow with binning. The only manual input required for the entire conversion is to create the 93K specific channel to pin mapping and specify the source and target directories for processing.

Given the complexity of this process, it is not surprising that significant, iterative debugging was required. Following initial, on-site visits from Verigy, a highly effective, network-based, collaborative environment was utilized to allow real-time, remote support from Verigy. This environment enabled timely, effective, and thorough resolution to all problems encountered.

Following the successful conversion of the test program, the high through-put capability of the V93K hardware was able to be fully utilized. The demonstration program, which fully characterized all the specified parameters of the target part required more than 40 minutes to execute on the HP82K hardware. The converted program executed in 43.1 seconds, a throughput increase of greater than 50X.

Using the converted program, five (5) sample parts were measured at -55°C, +125°C, and room temperature on both the HP82K and V93K test systems. Results were compiled and compared. Within specified accuracies of the systems, every V93K measurement agreed with the previous HP82K, a total of more than 17,500 measurements on each system. The reduction of this large quantity of data is further enhanced on the V93K by built-in data reporting utilities which eliminated the need to develop software to extract the results which was required on the HP82K.



On-site training was conducted to brief the test staff in the approach and usage of the converter utility. Both source code and an interactive help system are installed on the V93K system.

Conclusion

An automated conversion utility translates existing HP82K programs for use on V93K using the original test fixturing. Including both device specific setup and converter execution time, the time to convert a program is comparable to the time required to setup the test system to run an existing program (less than 1 hour). Test execution times were reduced by more than 98% (Figure 5) and equivalent measurement results were obtained.

Task 2 - Installation and validation of parallel testing of multiple ICs

This task added test channels to support up to eight (8) 40 pin devices simultaneously and Verigy software to convert single device test programs to multi-site testing. A customized test board accepting up to 8 HP82K test fixtures was developed and a temperature housing for controlling temperature over the military range of -55°C to $+125^{\circ}\text{C}$ was installed on an existing emulation, forced-air, temperature control system.

Results

Both a software upgrade and additional hardware were required to implement the parallel test capability. The software license, *Pin Scale Multisite Test SW, perpetual per session floating license*, was purchased to enable the parallel test capabilities of the test hardware. The parallel test mode allows a test written for n pins to be simultaneously run on multiple devices, up to the available pins in the tester. To enable meaningful parallel testing, the pin count of the V93K was expanded to 384 digital test pins which can support 8 instances of a 48 pin device. The tester was already configured with an eight (8) output device power supply (DPS) which supports independent power supplies for up to 8 parts.

The *Multisite Test Software* only requires specification of the tester channels connected to additional test site. The software automatically manages the stimulus and measurement results for each device based on a program written for a single device.

A custom test board (a/k/a *motherboard*) was designed by Dr. David Keezer of the Georgia Institute of Technology, who had previously designed the specialized HP82K fixtures routinely used by the emulation programs. The HP82K fixtures consist of a motherboard with interchangeable daughter cards which are uniquely configured for each part to be tested (Fig 6a). Previously, Dr. Keezer had also developed a V93K motherboard which accepted an HP82K type daughter card. For parallel testing, Dr. Keezer designed a motherboard which accepted eight (8) HP82K-style daughter cards. (Fig 6b).

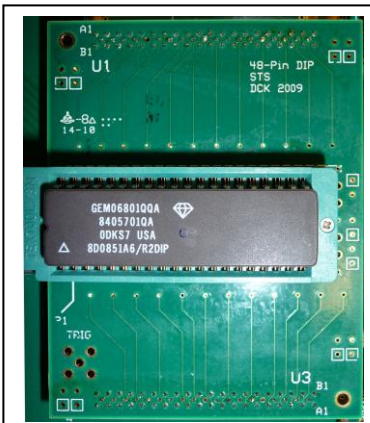


Fig. 6a - HP82K Daughter Card

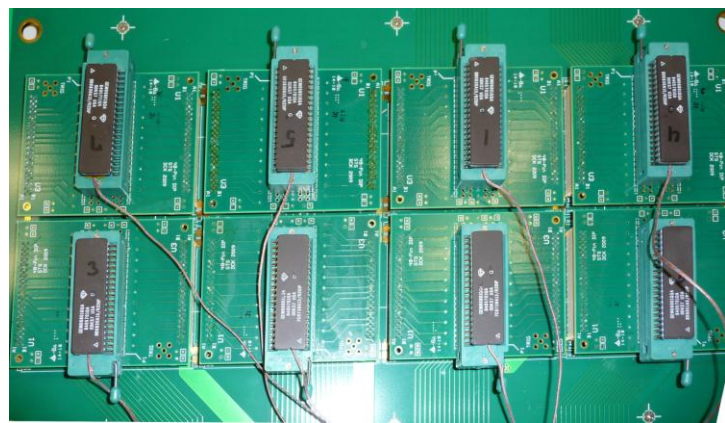


Fig. 6b – Multi-site V93K motherboard with eight (8) HP82K Daughter Cards (wires are thermo-couple leads for thermal characterization)

Eight sample parts were simultaneously tested and the execution times and results compared with single site testing. Equivalent parametric results were obtained between parallel and single testing. Test execution times presented a more complex result. The characterization test program, which performs individually, measures the actual value of each specified timing parameter, did not benefit significantly from parallel testing. This is because much of the execution time is expended performing timing measurements and the test head can only manipulate a single time searching algorithm. Alternatively, measurements of currents, voltages and functional pass/fail tests achieve full parallel operations where measurements on 8 devices are performed within the same time as one measurement in a single site test environment. Most screening for production testing can be performed using only pass/fail testing to verify conformance to the required timing specifications and would benefit fully from the 800% increase in throughput provided by parallel testing.

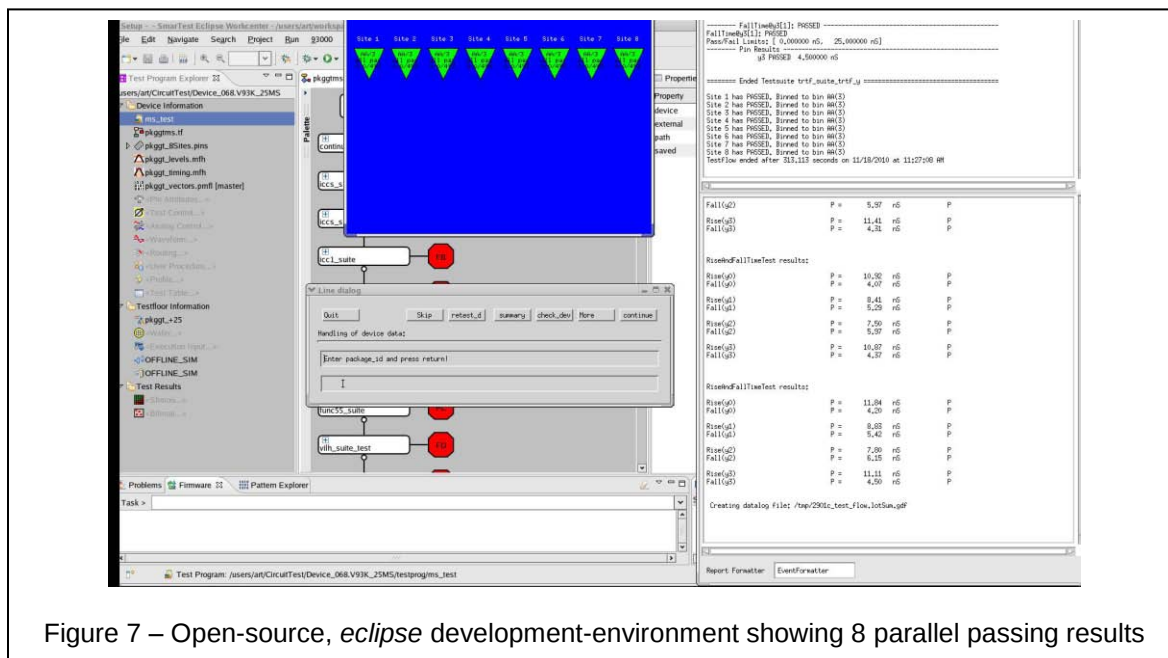


Figure 7 – Open-source, *eclipse* development-environment showing 8 parallel passing results

Lastly, a housing was installed on an existing Temptronic TP04300 forced air temperature control system. The Temptronics standard insulated hood covered the eight (8) DUT cards. Temperature was forced from -55°C to +125°C as required for screening of military quality parts. Some variation in temperature uniformity was observed across the 8 sites. Temptronics will continue to work on this issue as the capability transfers into the emulation programs.

Conclusion

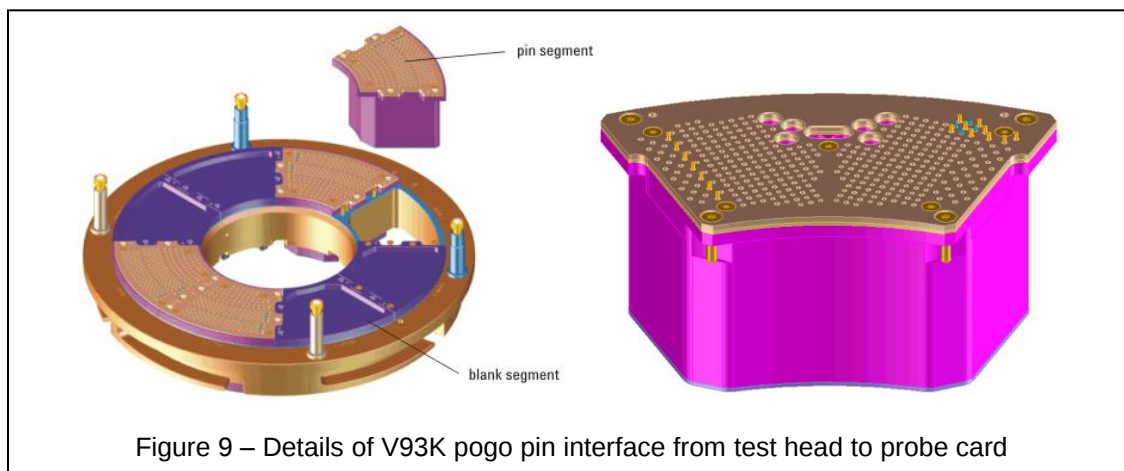
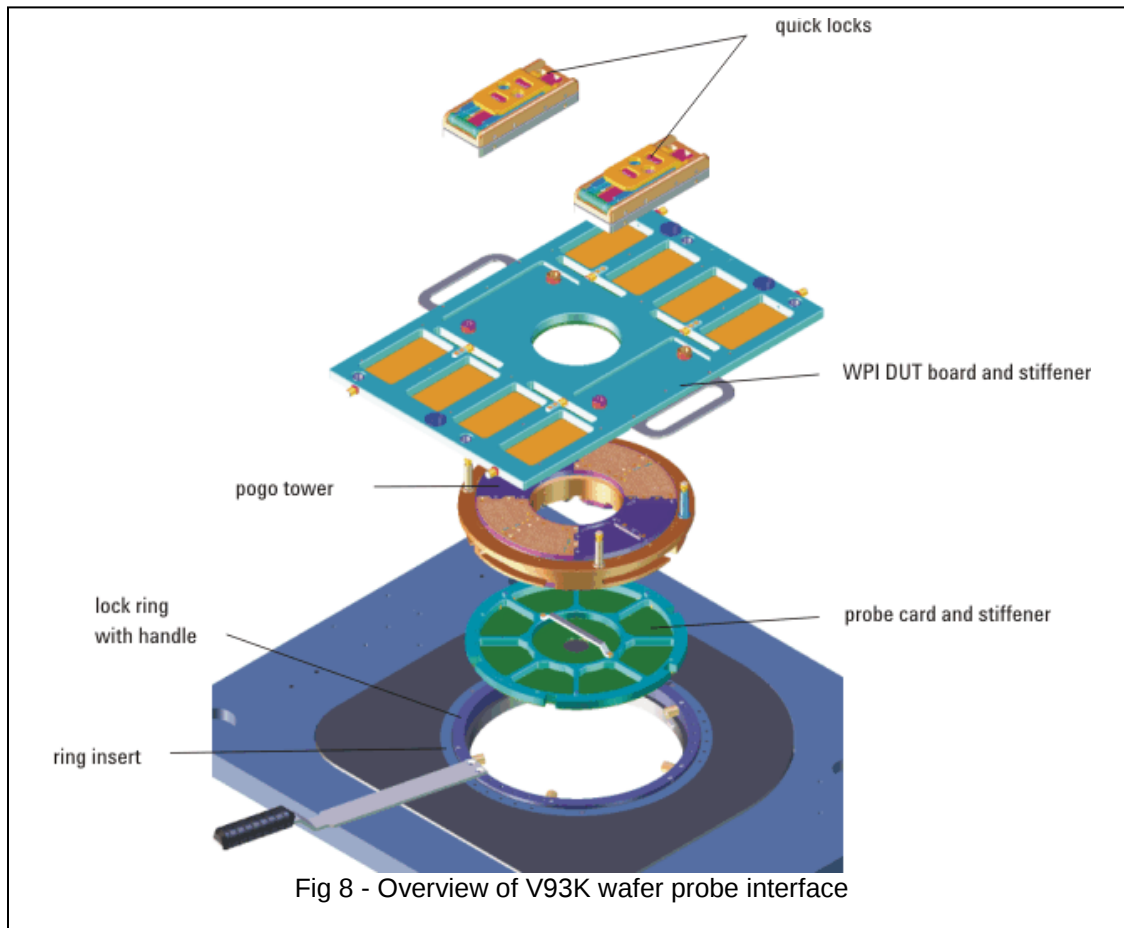
The combined hardware and software solution for parallel testing has been successfully demonstrated. MIL-STD-883 Test Method 5004/5005 screening can take full benefit of the 8X increase in capacity/throughput.

Task 3 - Installation and validation of enhanced wafer testing/sorting capability

An EG2001 specifically configured to support a high-performance interface to the V93K test system was purchased and installed. A probe card, configured for testing of high-speed signals of the target part was installed and the converted test program utilized to screen a wafer containing the target die.

Results

The V93K test system supports a high performance interface to a wafer probe system which maintains signal fidelity to the probe card. The V93K test software is also capable of control and setup of the EG2001 wafer probe system. The hardware interface is designed for the test electronics to “dock” directly on the top of the wafer probe system as shown in the figure 8:



A version of the HP82K test used for wafer probe was converted and run on the V93K. The test time for a wafer was reduced from more than 30 minutes to less than 1 minute with equivalent results.

In addition, the characterization program was also successfully run at both room temperature and at +125°C, verifying that all timing characteristics could be measured at the wafer level with performance comparable to testing at the package level. This enhanced capability will become increasingly important as emulation produces more parts in expensive and limited availability package types.

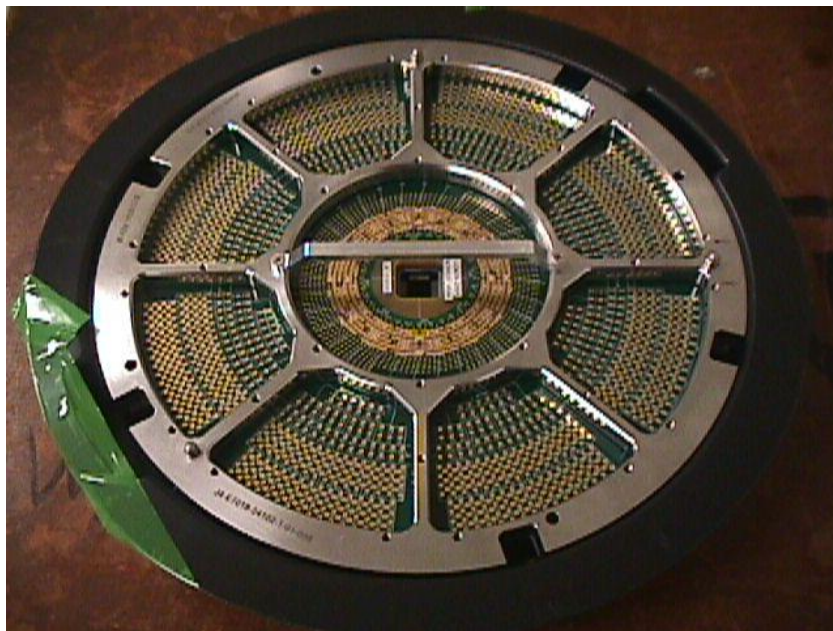


Figure 10 – Probe Card for demonstration emulation device

Conclusion

A wafer probing capability allowing high speed testing at both room and elevated temperatures has been deployed and validated on the V93K. The capability is in-place, available for immediate use by the emulation programs, providing dramatically improved throughput and test capability for high performance devices.