AFRL-AFOSR-UK-TR-2011-0015

MBE Regrowth of a Laterally-biased Double Quantum Well Tunable Detector

Rocio San Roman Alonso
Alvaro de Guzman Fernandez

Universidad Politécnica de Madrid
Instituto de Sistemas Optoelectrónicos y Microtecnología
ETSI Telecomunicación
Madrid, Spain 28040

EOARD GRANT 09-3047

June 2010

Final Report for 17 February 2009 to 17 February 2010

Distribution Statement A: Approved for public release distribution is unlimited.

Air Force Research Laboratory
Air Force Office of Scientific Research
European Office of Aerospace Research and Development
Unit 4515 Box 14, APO AE 09421

REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.
PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From – To)*
16-05-2011	Final Report	17 February 2009 – 17 February 2010

4. TITLE AND SUBTITLE

MBE Regrowth of a Laterally-biased Double Quantum Well Tunable Detector

5a. CONTRACT NUMBER
FA8655-09-1-3047

5b. GRANT NUMBER
Grant 09-3047

5c. PROGRAM ELEMENT NUMBER
61102F

6. AUTHOR(S)

Professor Alvaro Guzmán

5d. PROJECT NUMBER

5d. TASK NUMBER

5e. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Universidad Politécnica de Madrid
ETSI Telecomunicación
Madrid, Spain 28040

8. PERFORMING ORGANIZATION REPORT NUMBER
N/A

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

EOARD
Unit 4515 BOX 14
APO AE 09421

10. SPONSOR/MONITOR'S ACRONYM(S)
AFRL/AFOSR/RSW (EOARD)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
AFRL-AFOSR-UK-TR-2011-0015

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited. (approval given by local Public Affairs Office)

13. SUPPLEMENTARY NOTES

14. ABSTRACT

The main objective of this project is the development of a laterally biased QW IR detector. The structure is a double quantum well (QW) structure (fig. 1 a) consisting on a n-type doped QW tunnel-coupled with another n-type doped QW. Both wells are laterally contacted by means of two ohmic junctions (collector contacts) at the sides of the device. Furthermore, two pinch-off Schottky gates are deposited to reduce the direct conduction between the lateral contacts through the QW. This conduction is reduced applying an electric field to the pinch-off gate in a fashion similar to a field effect transistor for each one of the wells. When the electrons in the one of the wells are promoted from the ground state to the excited state (fig. 1 b), they tunnel out to the other well. The electrons in the biased well are then swept to the collector region by the lateral bias. It is also possible to apply a vertical bias (parallel to the quantum well heterostructure growth direction) using the bias gate.
The major difficulty of this scheme is the deposit of the two contacts (bias gate and pinch-off gate) in the bottom part of the device. This should lead to the regrowth of the whole structure on top of a previously etched surface where the bottom contacts are defined. Up to now, we have fulfilled the followings objectives:

- Optimization of reactive ion etching conditions for 500 nm etching.
- Optimization of reactive ion etching conditions for 10 nm etching.
- In general, regrowth of GaAs on top of patterned substrates results in very good quality material, but there are some aspects to be considered:
  - o When the etching depth is 500 nm, the pattern is reproduced in the layer regrown, and therefore it is very difficult to obtain a flat surface after the growth. We are now studying the possibility of using ion implantation to make the bottom contacts.
  - o When the etching depth is 10 nm, the result is a flat surface with very high quality of the GaAs regrown. The problem with this approach is the possible contact between QWs after the subsequent regrowth due to the low thickness of the AlGaAs barrier separating the QWs.
- Selective ion implantation of contacts
- Design and development of a photolithography mask to develop the whole device using different approaches (ion implanted contacts and selective QW etching).
- Regrowth of GaAs on previously implanted GaAs samples
- Processing of the whole device using the ion implantation scheme.
- Demonstration of practical application of the device using ion implantation. Preliminary measurements of the electrical characteristics show good agreement with the theory and are very promising to obtain IR absorption at temperatures close to RT.

The next steps we pursue are the following:

- To find the optimum annealing conditions to have high conductive layers after ion implantation, reducing the clusters observed by TEM.
- To mount an IR setup to characterize the devices at different temperatures with the possibility of accessing all the pads of the device.
- To improve the processing to develop the device using selective QW etching (in this case the regrowth is not a problem).

15. SUBJECT TERMS

EOARD, Sensor Technology, Quantum Well Devices, infrared technology

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18, NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			SCOTT DUDLEY, Lt Col, USAF
UNCLAS	UNCLAS	UNCLAS	SAR	49	**19b. TELEPHONE NUMBER** *(Include area code)* +44 (0)1895 616162

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39-18

EOARD - Award No. FA8655-09-1-3047

MBE regrowth of a laterally-biased double quantum well tunable detector

Final report

June 2010

Rocío San Román Alonso

Alvaro de Guzmán Fernández

Index (Table of contents)

Quantum Structures for Tunable Detectors

Intruduction and Summary 3

Results and discussion: Processing schemes 3

- **Growth of n+ layer/etching/regrowth** 4
- **MBE growth/ selective QW-layers etching/ regrowth** 8
- **Gate Contacts obtained from Ion Implantation** 11

Detectors Processing 15

- **GaAs contact obtained from Ion Implantation** 16
- **Selective etching of Quantum Well layers** 19

Conclusions and future work 22

APPENDIX A: Report on 500nm etching optimization 23

- **Wet etching tests** 23
- **Dry etching: Reactive Ion Etching (RIE)** 27

APPENDIX B: 10 nanometers etching 32

APPENDIX C: Ion Implantation for bottom contacts 42

Table of figures 47

References 48

Quantum Structures for Tunable Detectors

Introduction and Summary

The main objective of this project is the development of a laterally biased QW IR detector. The structure is a double quantum well (QW) structure (fig. 1 a) consisting on a n-type doped QW tunnel-coupled with another n-type doped QW. Both wells are laterally contacted by means of two ohmic junctions (collector contacts) at the sides of the device. Furthermore, two pinch-off Schottky gates are deposited to reduce the direct conduction between the lateral contacts through the QW. This conduction is reduced applying an electric field to the pinch-off gate in a fashion similar to a field effect transistor for each one of the wells. When the electrons in the one of the wells are promoted from the ground state to the excited state (fig. 1 b), they tunnel out to the other well. The electrons in the biased well are then swept to the collector region by the lateral bias. It is also possible to apply a vertical bias (parallel to the quantum well heterostructure growth direction) using the bias gate.

The major difficulty of this scheme is the deposit of the two contacts (bias gate and pinch-off gate) in the bottom part of the device. This should lead to the regrowth of the whole structure on top of a previously etched surface where the bottom contacts are defined.

In this project we propose 3 different ways to the development of the mentioned device, they are summarized below.

Results and discussion

Processing Schemes

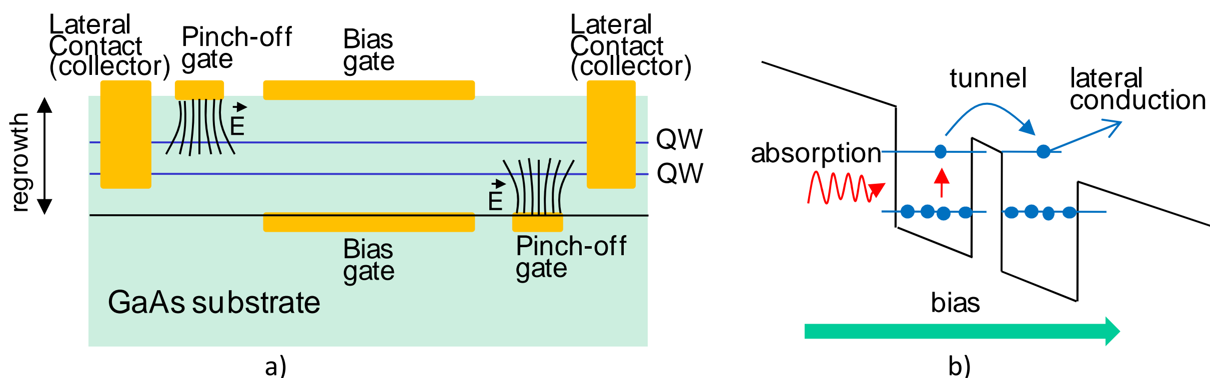


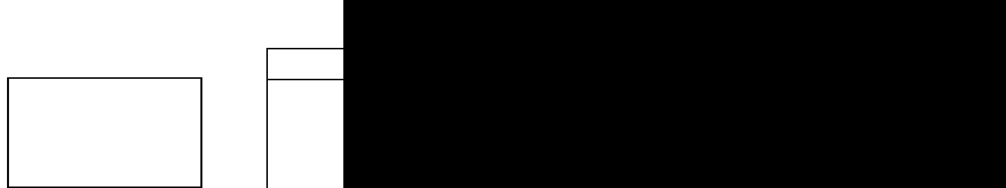
FIG. 1 Quantum Structure for Tunable Detectors

We have studied three different ways to develop this device:

- Growth n+ layer /etching/ Regrowth
- MBE growth/selective QW layers etching/regrowth
- Selective ion implantation/regrowth

Growth of n+ layer /etching/ Regrowth

This method consists on the growth of a highly foped n+ layer and the etch it to define the bottom contacts. After that, the whole device structure must be regrown on top (see figure).



In order to obtain good layers after the re-growth, the first thing to do was to optimize the etching of n+ layer trying to achieve very smooth surfaces and minimum undercutting. In our caswe we have studied both wet and dry etching methods in order to ensure a good quality of the final surface where the device is grown. In Appendix A we have included different techniques studied to etch GaAs, as well as the influence of process parameters on the final result.

The etching is followed by an oxidation process in order to protect the surface of the sample from the atmosphere prior to its loading into the chamber. This process is not necessary at the beginning since the samples are epi-ready and therefore they have a native oxide from the factory.

The best result for 500nm etchings was achieved using dry etching by Reactive Ion etching, with 9 sccm of Ar, 9 sccm of $SiCl_4$ and with a power of 107 W. With these parameters, DC Bias of 340 V was obtained and the pressure during the etching process was of 7 mTorr aprox).

Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) were used to study surface morphology and the anisotropy of the etching. After optimizing the processing we got smooth layers and good etching steps as shown in the following AFM/SEM pictures (the RMS roughness of a native GaAs substrate is 0,2 nm):

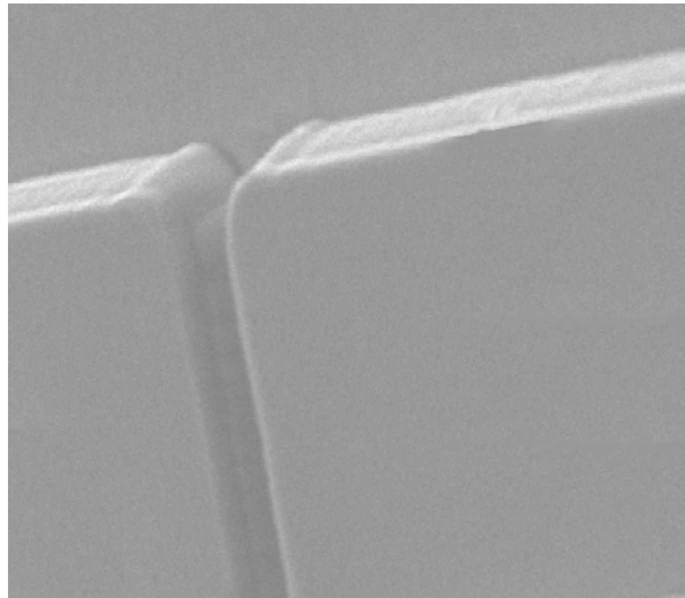


FIG. 2 SEM image of a GaAs layer etched by Reactive Ion Etching

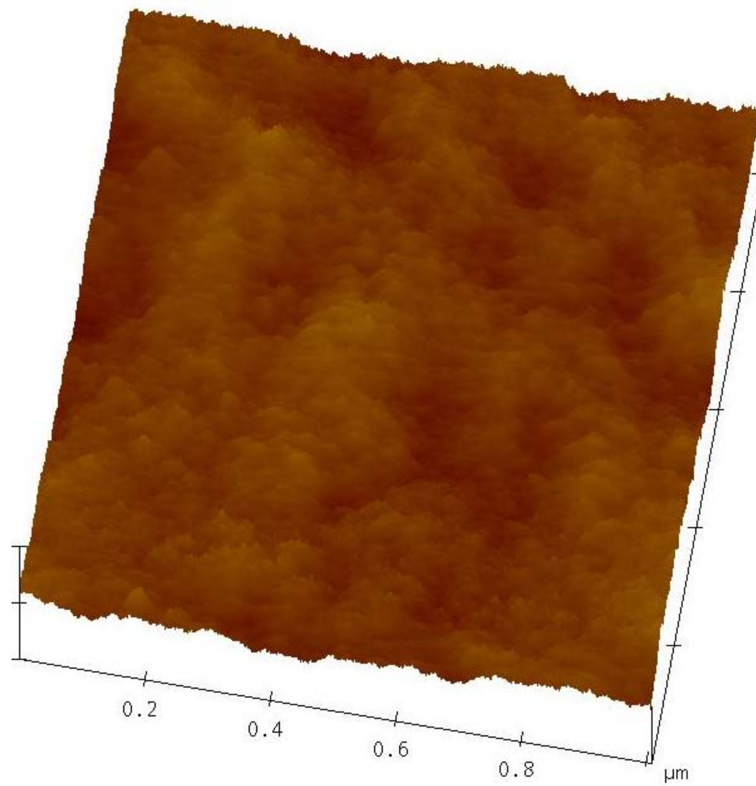


Image Statistics

Img. Rms (Rq)	0.338 nm
Img. Ra	0.269 nm

FIG. 3 AFM picture of the etched surface showing a very low roughness comparable to that of the native substrate.

We have regrown GaAs layers on top of these etched surfaces and the quality observed at a very low scale is very good in comparison with the native wafer. The figure below, shows the AFM picture of one sample with a 500 nm GaAs layer regrown on a previously etched surface. As it can be seen, the RMS roughness of the sample is 0,276 nm.

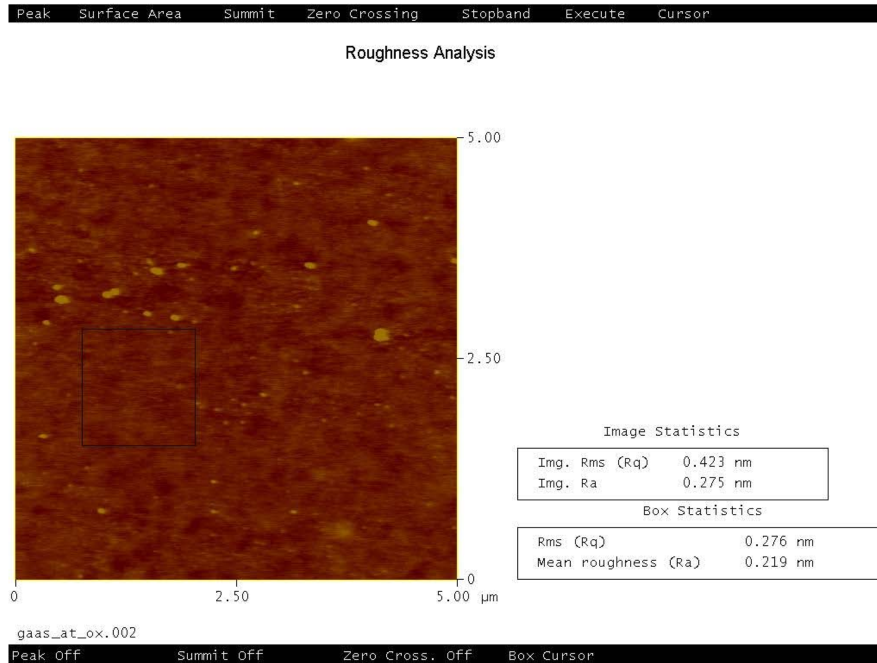


FIG. 4 AFM image of a GaAs layer regrown on a previously etched surface.

However, even when the MBE regrowth showed a good quality of the GaAs film at low scale, similar to layers grown on substrates without any processing, we found a couple of technical problems :

- Not good global uniformity in the oxidation process. The wafers were oxidized prior to loading them into the MBE chamber in order to protect them from external contamination (Appendix A). This oxidation was removed into MBE but, because of not good initial uniformity, some remains of this oxidation were found after the regrowth (FIG. 4). This problem should be solved using other ways to oxidize the samples or optimizing this process. At this respect we are now trying different ways to oxidize the sample (for example exposition to pure O_2 plasma in the etching chamber after the etching)

- The step etched to define the bottom contacts is still present after the regrowth. As it is shown in the FIG. 5 (and it is explained in Appendix 1), we transfer geometric pattern using standard photolithography process and then we etched them 500nm using RIE. We expected a complete filling of the etched patterns after re-growing, however we found that the step is still present even growing more than 1 μm of GaAs on top(FIG. 6).

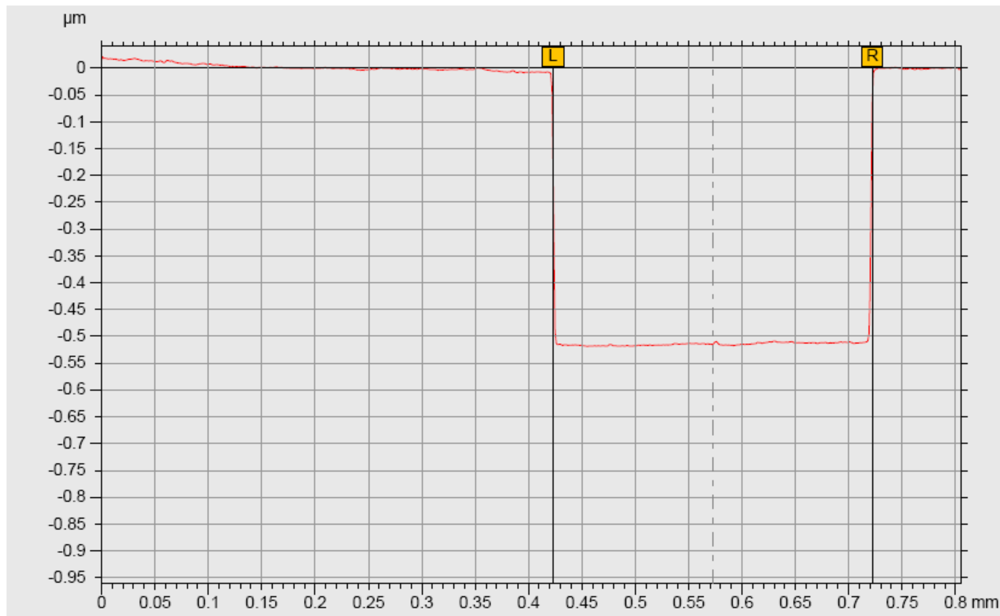


FIG. 5 Step before regrowth measured using an Alpha-Step Profiler

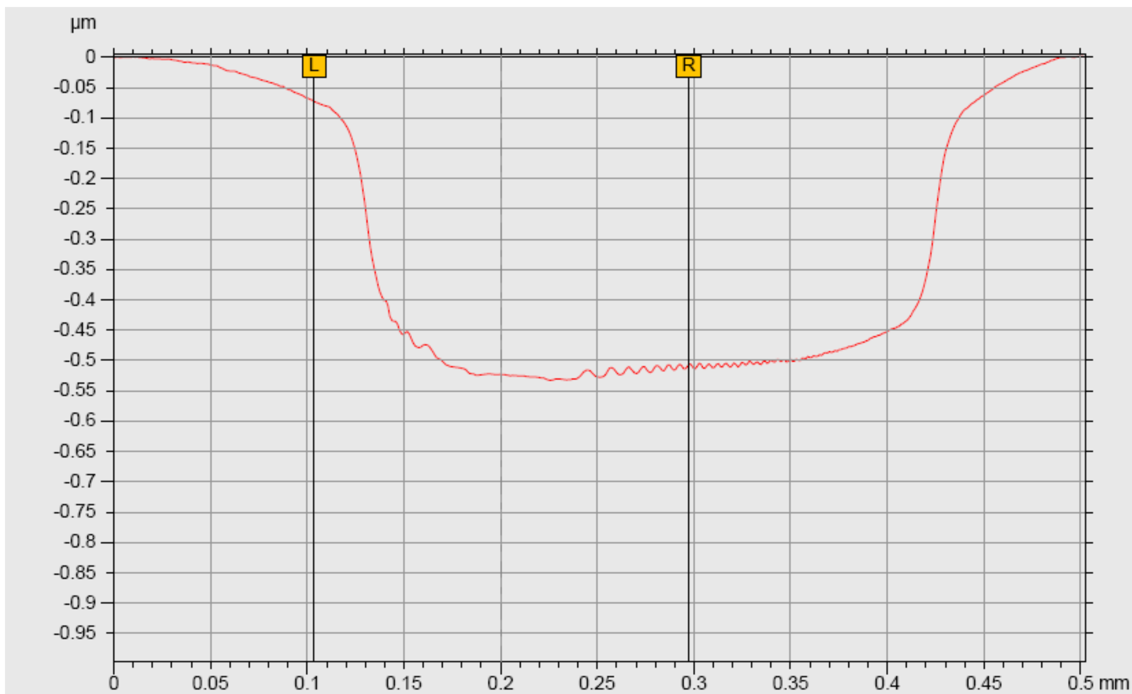


FIG. 6 Step after regrowth measured using an Alpha-Step Profiler

This problem makes very difficult the practical application of this procedure to the fabrication of the bottom contacts.

MBE growth/ selective QW-layers etching/ regrowth

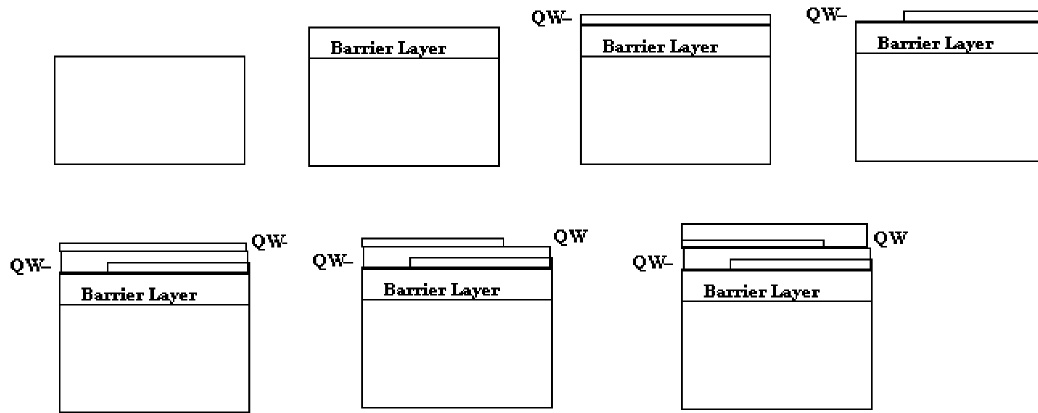


FIG. 7 MBE/selective etching/regrowth processing scheme

In this processing scheme, we avoid the use of pinch-off gates, since the quantum well are cut at the end and therefore they don't reach the opposite lateral contact (see fig. 7). To develop this structure it is necessary to first grow a barrier layer together with the first QW, then etch the edge of such QW, regrowth the middle barrier together with the second QW, etch the opposite edge of this QW and finally regrow the rest of the structure. In this case there are several disadvantages, like the very difficult precise control of etchings of less than 10nm, as well as re-growth of few nanometers layers after this etching (and making sure that QW layers are not in contact).

The optimization of parameters for nanometers etching was not easy because the conditions used for 500nm etching were not the proper ones in this case (Appendix 2). After a series of experiments we achieved to have a relatively good control of the etching rates and good results regarding the anisotropy and roughness of the layers:

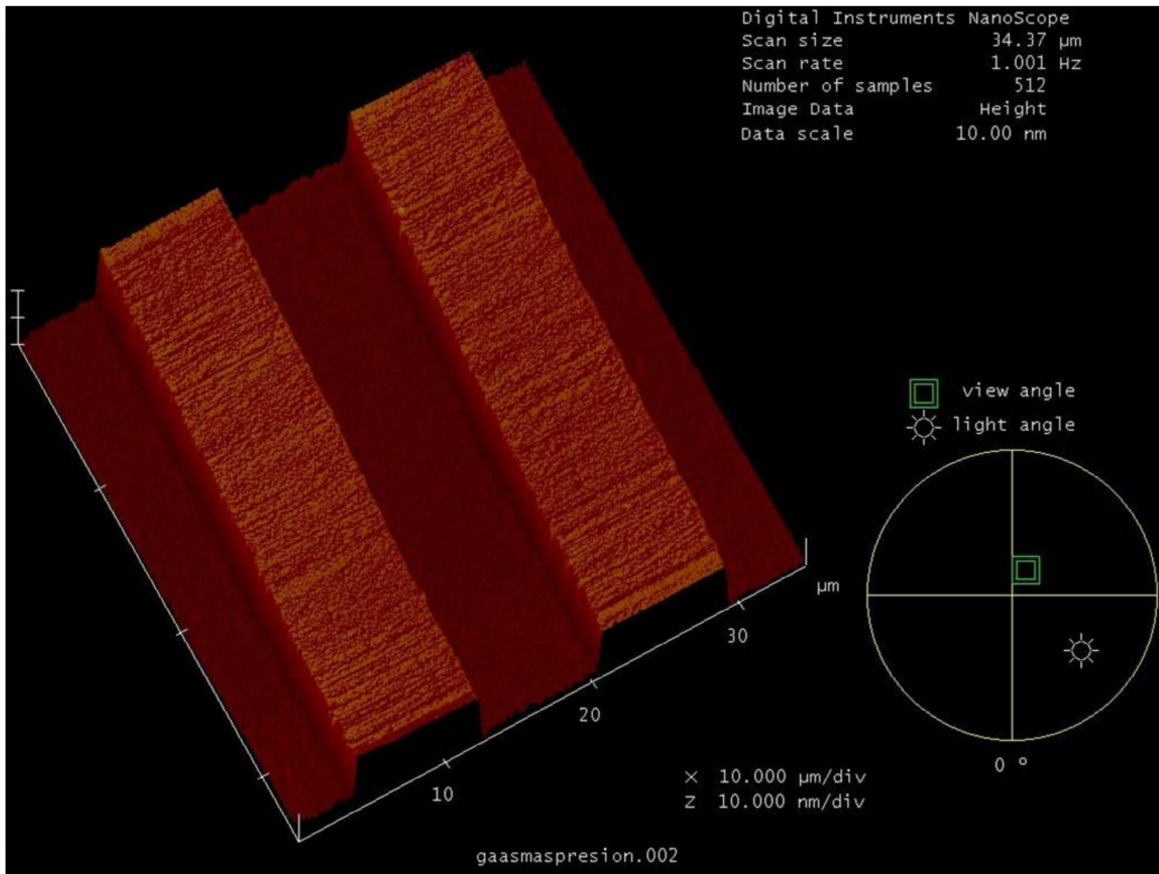


FIG. 8 Patterns of a 20 nm etching in GaAs (I)

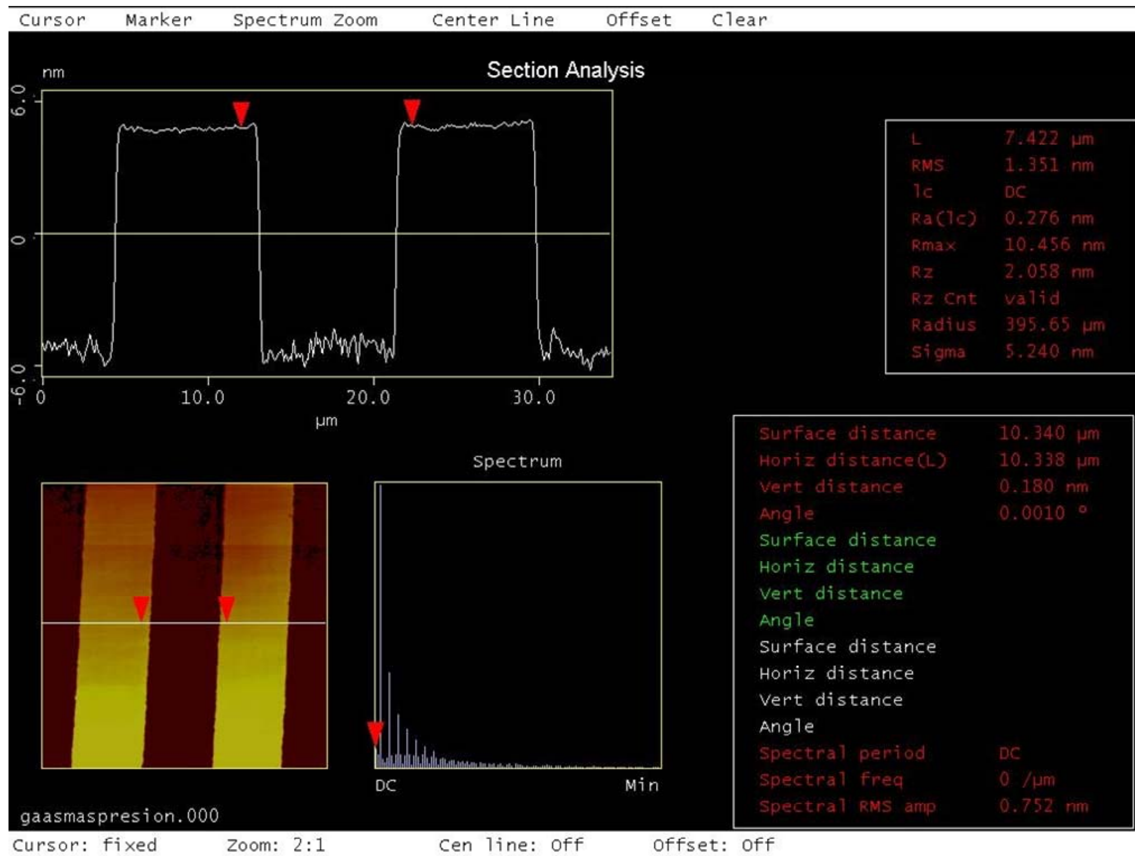


FIG. 9 Patterns of a few nanometers in GaAs (Section Analysis)

The real problem of this processing is that the re-growth is quite tricky since the AlGaAs layer between quantum Wells layers is only 2nm thick. This results in a high probability of both QW to be in contact after the second re-growth.

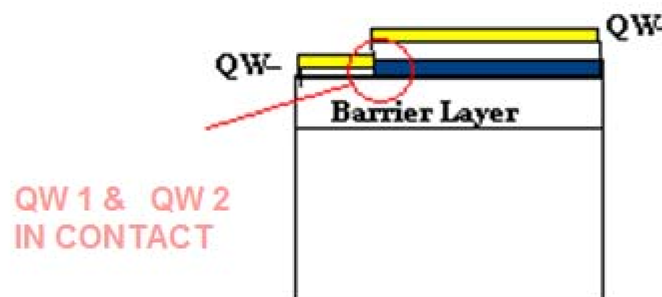


FIG. 10 Problems in the etching and re-growth in the quantum well structure

Gate Contacts obtained from Ion Implantation

The main problem of the scheme proposed in first place is the difficulty of achieving a smooth and flat surface after the regrowth. Normally, the 500 nm etched pattern remains present even after growing 1 μm GaAs on top. With respect to second scheme where the QW must be etched, the major problem arises from the very thin layer regrown on top of the etched QW. This can result in a contact between both QW in the vertical side of the etching.

To overcome these problems we propose an additional way to develop the device consisting on using ion Implantation as an alternative to obtain selective doping in the sample to develop the gate contacts.

In Appendix C we show the implantation conditions used to introduce silicon dopant in GaAs substrate in order to have an estimated doping of 10^{18} Si atoms/cm^3. We used two different implantation conditions:

- Si^+ → dose: $4 \cdot 10^{13}$ atoms/cm^2; ion energy: 180 KeV
- Si^{++}: → dose: $6.58 \cdot 10^{13}$ atoms/cm^2; equivalent ion energy: 360 KeV

The GaAs layer grown after implantation was examined by several techniques in order to check the quality relative to the same layer grown on GaAs substrate –without ion implantation-. The films examined by x-ray diffraction exhibited a full width at half maximum (FWHM) rocking curve similar in both cases –grown on an implanted substrate or a native substrate- (FIG. 11). Atomic Force Microscopy measurements indicated a surface roughness with a RMS value very low (and similar to normal growths),

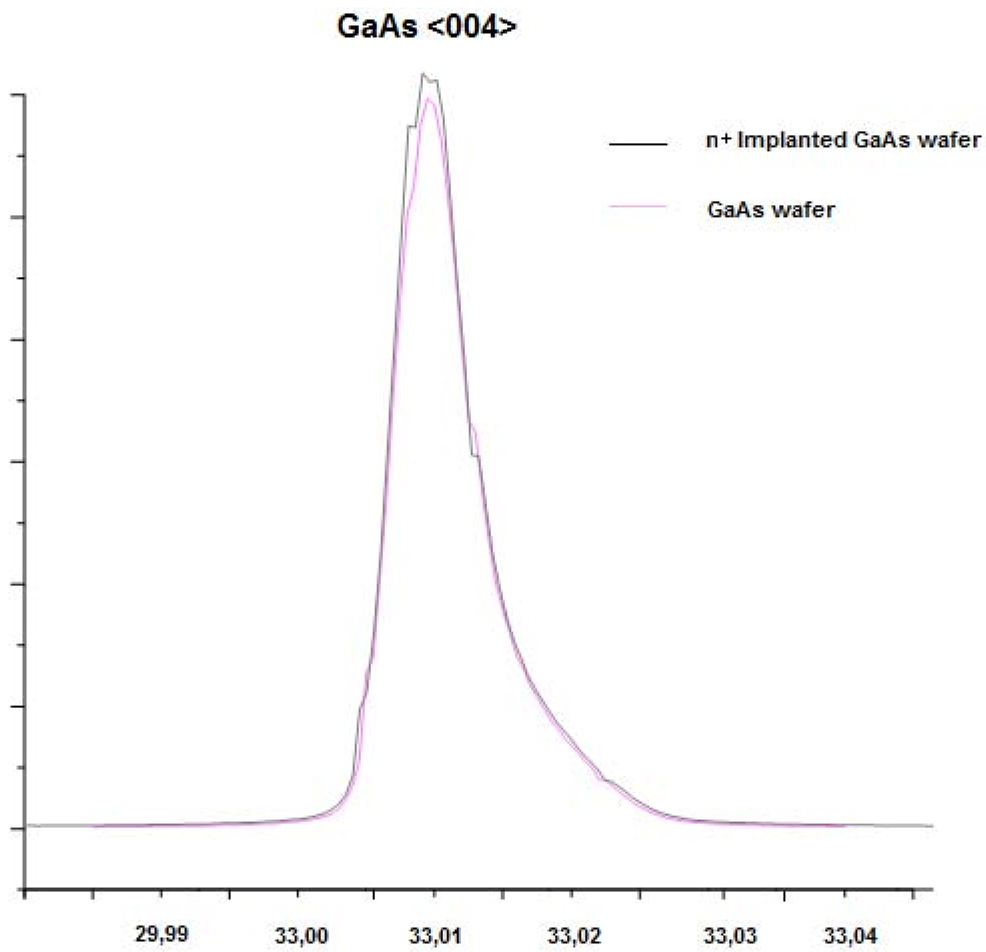


FIG. 11 Rocking Curve of GaAs layers grown on top of a epi-ready GaAs wafer and and implanted one.

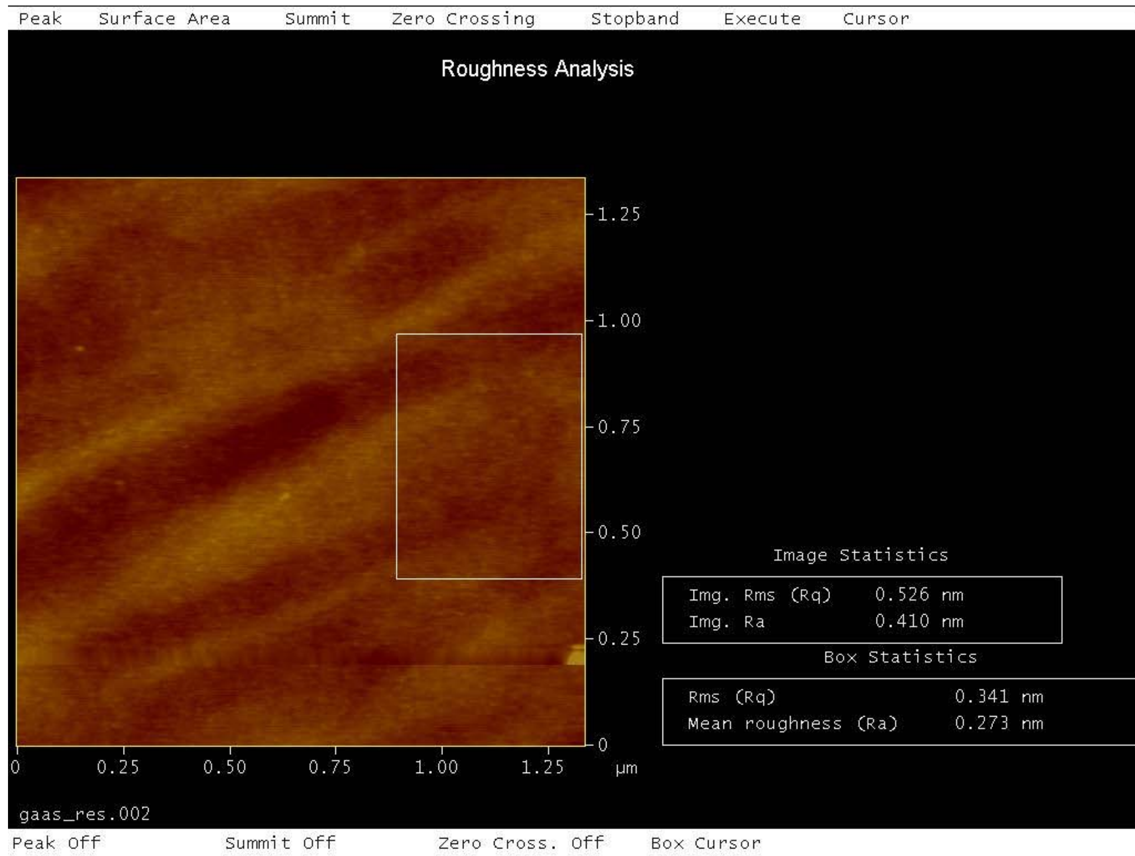


FIG. 12 AFM image of a GaAs grown in n+ implanted substrate

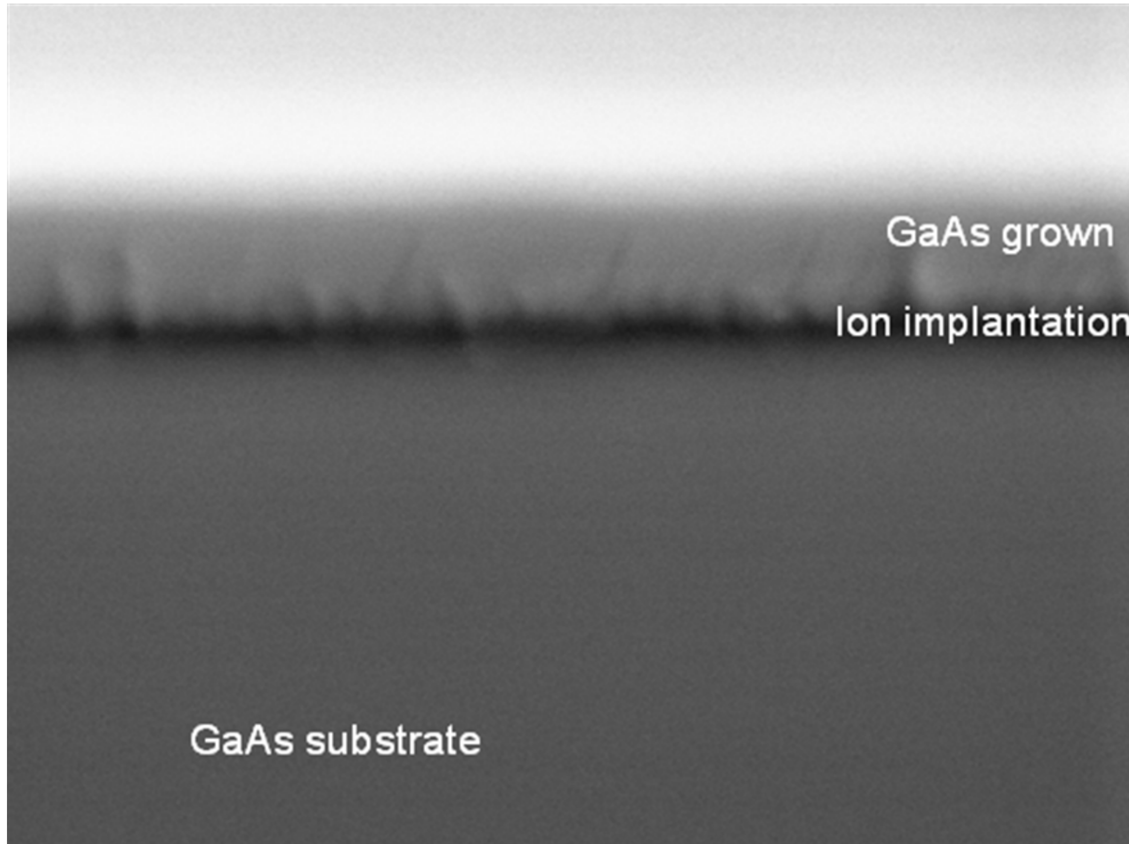
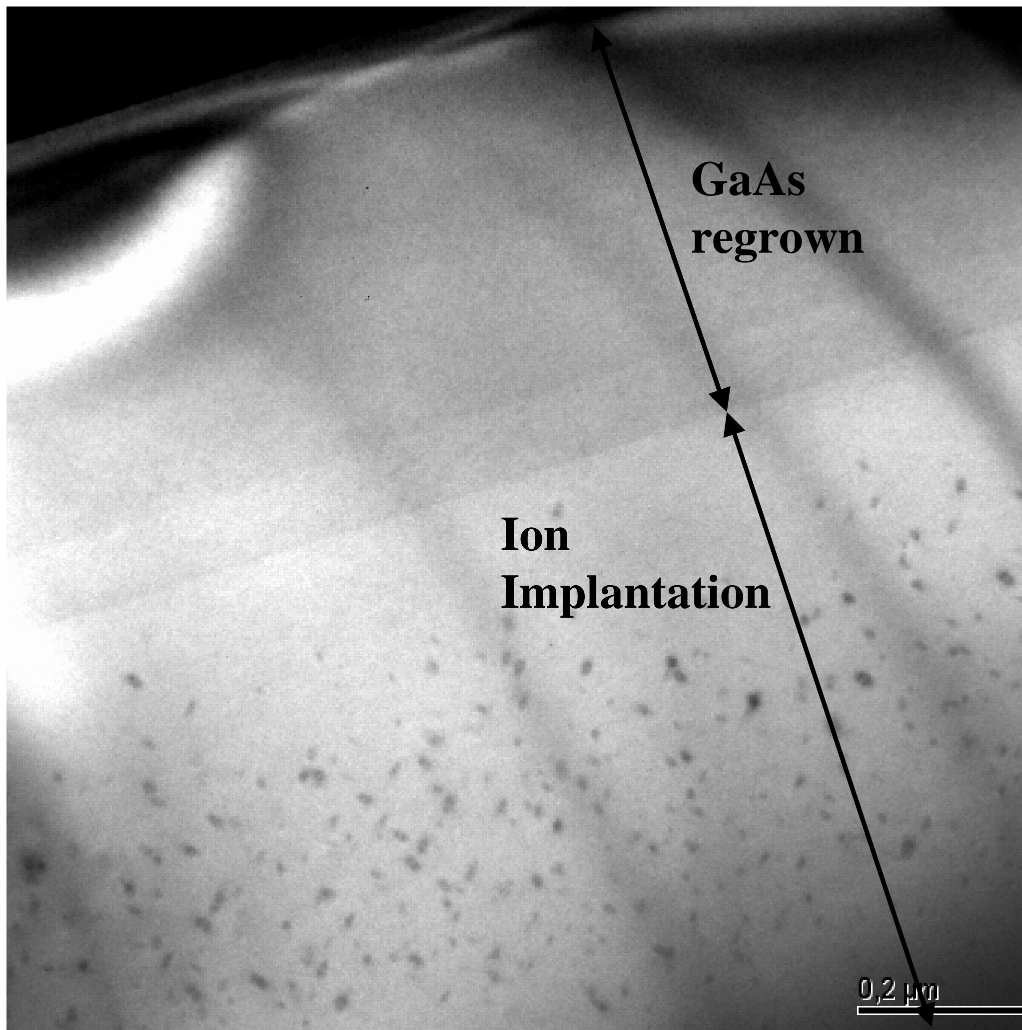


FIG. 13 SEM image of a GaAs epitaxial layer grown in n+ implanted substrate

The SEM image shown in the FIG. 13 exhibits a clear transition from GaAs substrate to n+ implanted zone (dark zone in the picture) and to the semiconductor GaAs layer grown by MBE.

We have also performed TEM measurements to analyze the crystal quality of the interface and the regrown layer. As it can be seen in the next figure, the quality of the layers is excellent, free of extended defects. Some clusters are observed in the implanted zone. Closer high resolution TEM images show that those clusters are not defects, since the crystal quality is perfect. We think they are associated with a particular distribution of the Si dopant in the crystal structure. Besides, the implanted samples show a very high resistivity (much higher than substrates with nominal $2 \cdot 10^{18}$ cm^{-3}). We expect the clusters to be the cause of this high resistivity. Our research is now focused on performing different anneal procedures in order to reduce the number of clusters and to reduce the resistivity.



TEM Micrograph of an implanted substrate and a regrown GaAs layer

Detectors Processing

Once verified the viability of the structures as well as the processing, we have designed and developed photolithography masks for the whole processing of the device. In the FIG. 14 is shown the AutoCAD design for this mask and in the FIG. 15 the mask manufactured in the company Compugraphics (UK) from that design.

This mask contains the processing steps for the two different approaches presented:

- GaAs contact obtained from Ion Implantation
- MBE growth/selective QW layers etching/regrowth

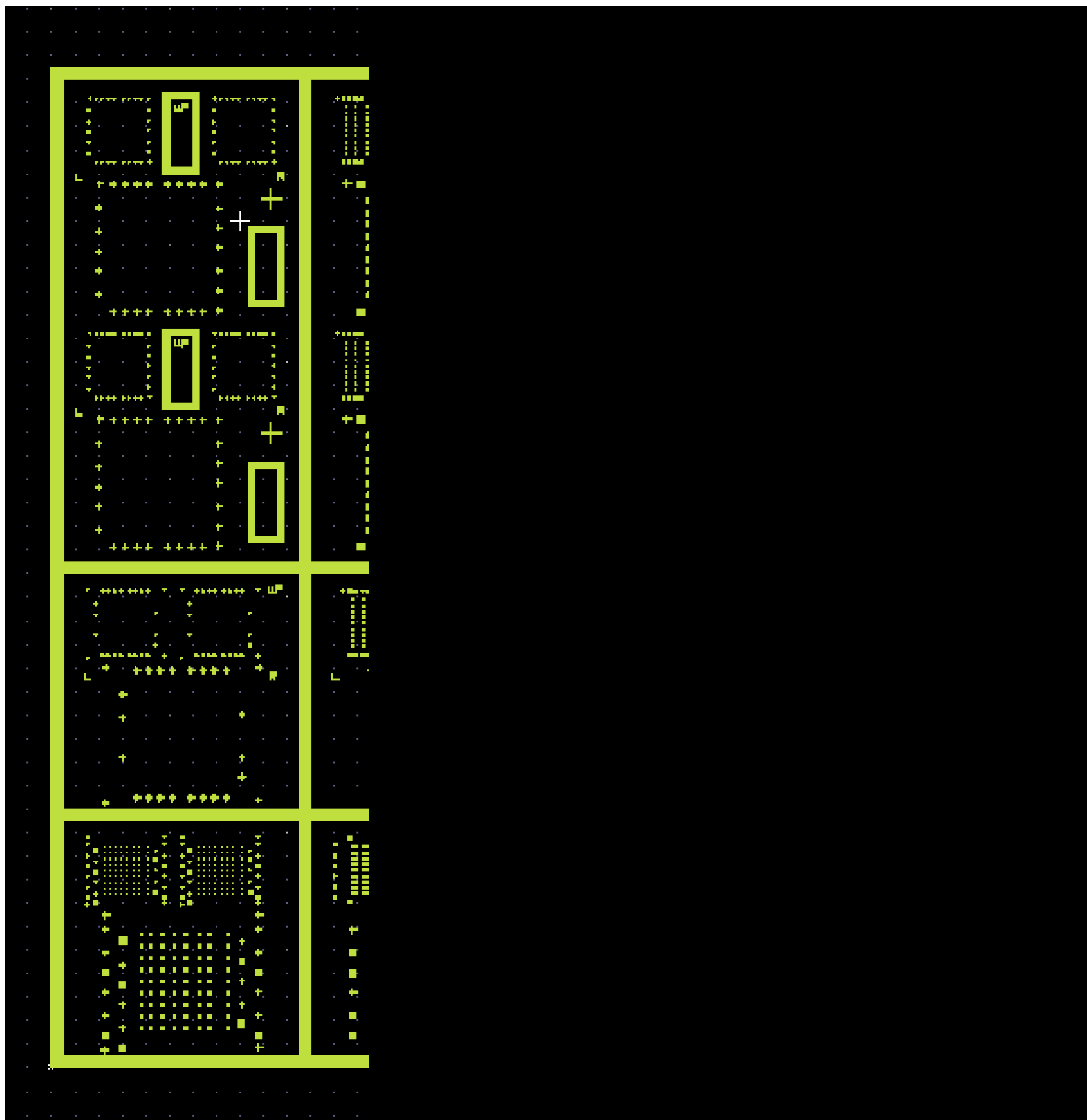


FIG. 14 Design of the lithography mask using ACAD program

FIG. 15 Optical lithography mask manufactured for this project

GaAs contact obtained from Ion Implantation

The fabrication of the final device using the ion implanted substrated comprises the following steps:

-Etching of references: Since the ion implanted zones can not be differenced from the not implanted ones, it is necessary to define alignment marks by etching (or etching + metallization) to be sure that the reference of these places are not lost after the implantation and the regrowth. For the first test we are working with 1 µm etchings, with and without metallization.

-Ion Implantation: Contacts are created by means of Si+ and Si++ ion implantation. In the following pictures (FIG. 16) taken by Nomarski microscopy it is shown a sample with photoresist prepared for the implantation process and aligned with respect to the references. The scheme of this step is in FIG. 17. We have prepared the mask to have 5 different separation gaps between the gate and the contact: 25, 50, 100, 200 and 400 microns.

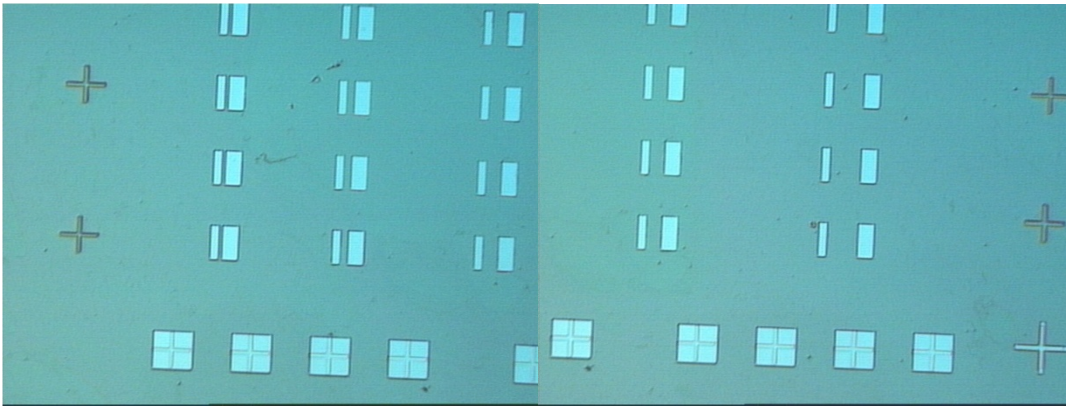


FIG. 16 Nomarski images of a GaAs sample with marks alignment prepared for the implantation process

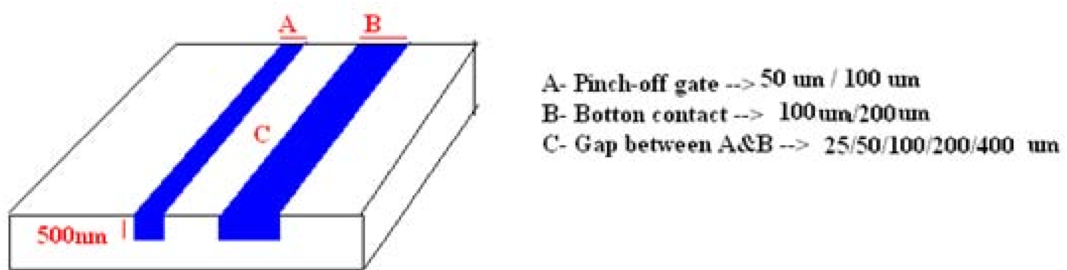


FIG. 17 Scheme of the sample after ion implantation

<u>-MBE epitaxial growth:</u> the whole structure is grown on top of the implanted substrate

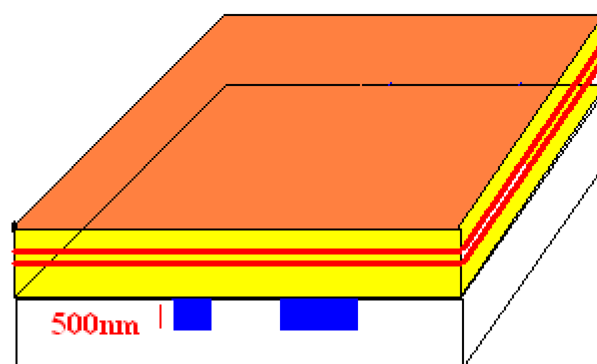


FIG. 18 Structures after MBE growth

-<u>Etching until bottom contacts</u>: the next step is to perform a mesa etching to leave access to the ion implanted contacts.

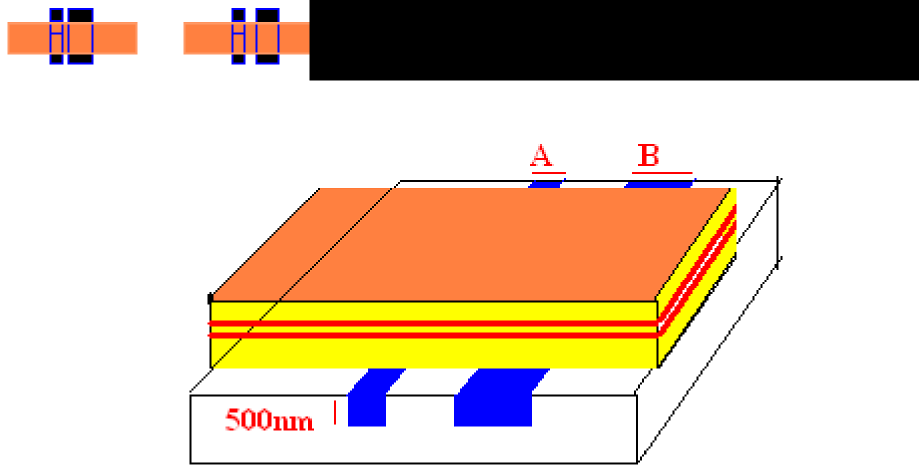


FIG. 19 Etching to free bottom contacts

-<u>Etching and metallization of side contacts:</u> Taking into account that the substrate is undoped, we etch two wells at both sides of the device and then we fill them with metal to create the lateral ohmic contacts (in magenta in the figure).

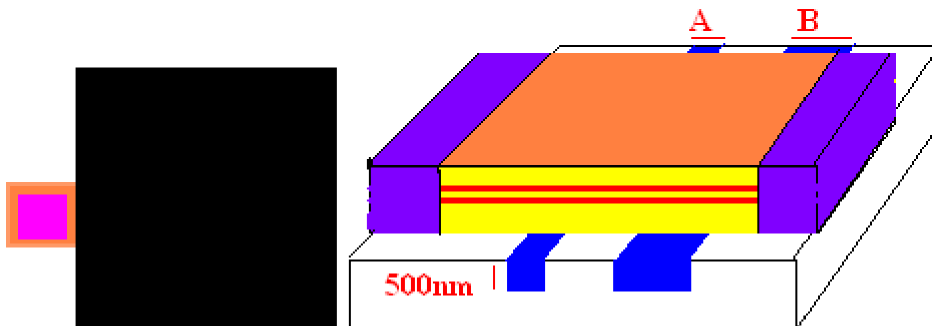


FIG. 20 Side contacts processing

-<u>Metallization of all contacts (and pinch-off gates):</u> the last step is to deposit metal on top of the different contacts and gates of the device through a mask to define all the top and bottom contacts (fig 21 in green).

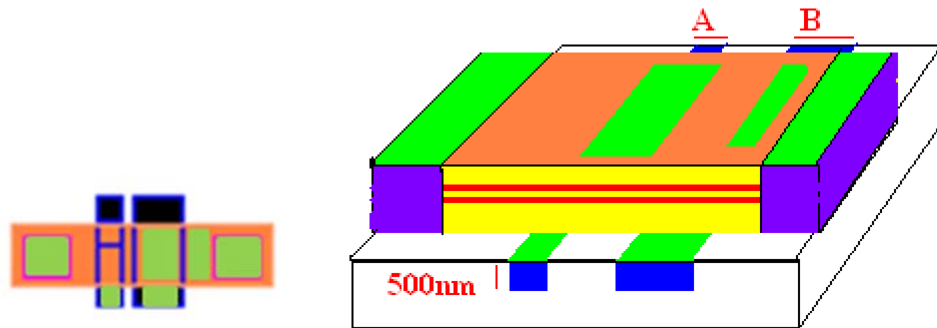
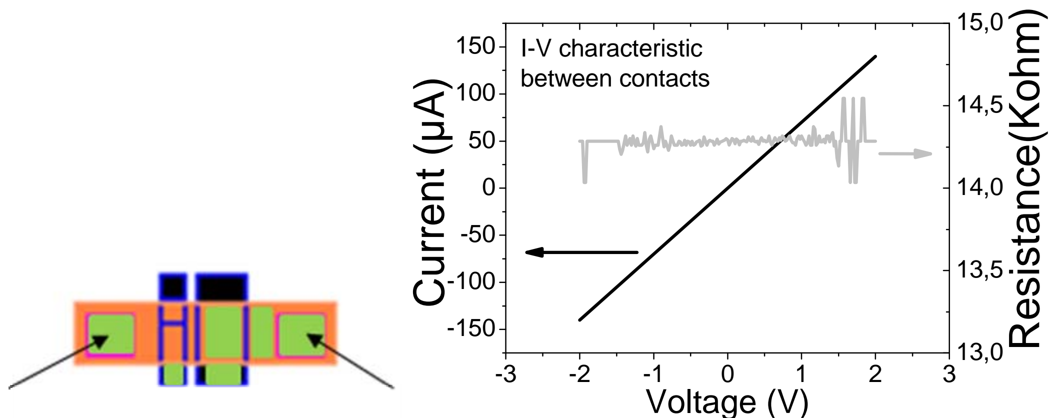


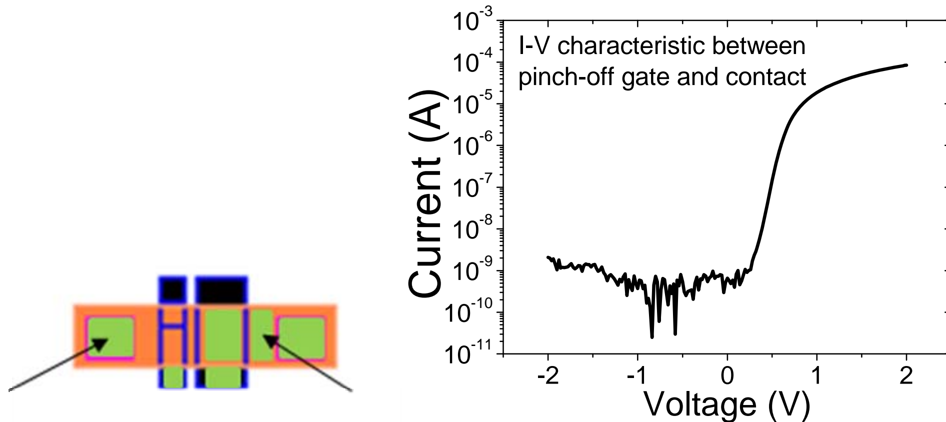
FIG. 21 Contacts metallization

Up to now, this was the best approach to develop the device, and actually <u>we have fabricated some of them and characterized some of its electrical properties</u>. We have measured the I-V characteristic between the lateral contacts and we obtained a very good agreement with the theory. The QWs have a thickness of 55 Å, the contacts have square shape with 100 x 100 µm size. The separation between contacts changes depending on the device measured (we have separations from 500 µm to 1,5 mm). Taking into account that the QW are doped and that the conductivity can be expressed as: $\sigma = n \cdot q \cdot \mu$ (n= concentration of carriers, q=electron charge and µ = electron mobility), the resistance between contacts can be written as: $R = \frac{1}{\sigma}\frac{L}{W \cdot D}$, where L is the separation between contacts, W is the contact size and D is the QW thickness. With this equations, we can obtain a value for R of 20KΩ. The next figure shows the I-V characteristic where it can be seen that the R is linear in a wide range of V and very close to the calculated value.



I-V characteristic of the measured device between lateral contacts (black arrows).

Concerning the pich-off gates, they should behave as Schottky contacts to introduce electric field in the structure avoiding a high current flux. This allows to modulate the current flowing through the QWs in a fashion similar to a field effect transistor. The next figure shows the I-V characteristic between one of the lateral contacts and the pinch-off gate, where it can be seen the clear Schottky behaviour with 5 orders of magnitude between direct and reverse bias.



I-V characteristic of the measured device between lateral contact and pinch-off gate (black arrows).

We have also demonstrated that the I-V characteristic between lateral contacts changes when an electric field is applied in the pinch-off gate. In those cases, it has been observed a change in the conductivity when the sample is exposed to the light of a lamp. Nevertheless, we have not yet measured a clear photocurrent spectrum. Our efforts are now dedicated to mount an optical IR bench to measure the above mentioned structures both at room and low temperature.

Selective etching of Quantum Well layers

-Etching of references. As in the previous structure, we need to etch some reference marks. In this case the problem come that the etchings are only of a few nanometers –QW layer size- so it is probable to lost these references after the re-growth making impossible to align the next steps.

-Growth until the first QW layer:

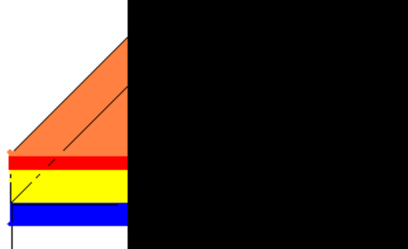


FIG. 22 Growth of n+layer, barrier layer and first QW

-Selective etching of the QW layer and regrowth

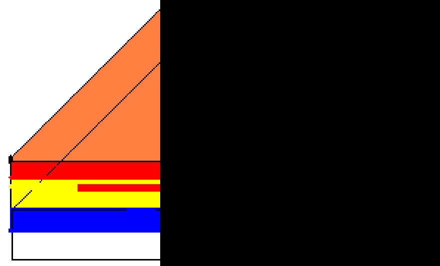


FIG. 23 Selective etching and regrowth

-<u>Selective etching of the second QW layer and regrowth</u>

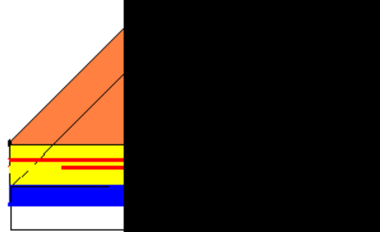


FIG. 24 Second selective etching and regrowth

-<u>Etching until n+ layer</u>

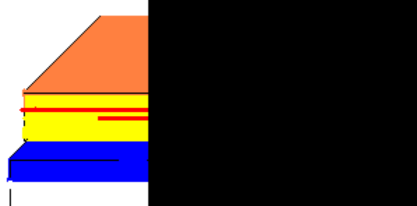


FIG. 25 Etching until n+ layer

-<u>Etching and metallization of side contacts</u>

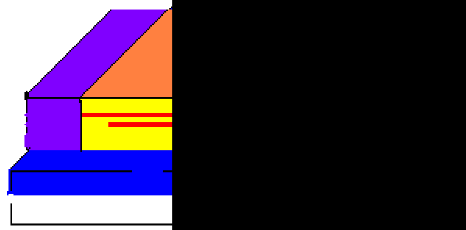


FIG. 26 Etching and metallization of side contacts

-<u>Metallization of all contacts:</u>

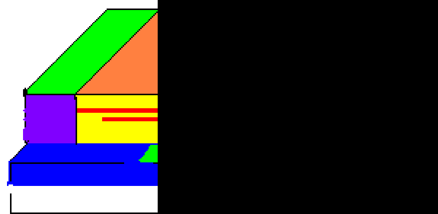


FIG. 27 Metallization and annealing of all contacts

Conclusions and future work

Up to now, we have fulfilled the followings objectives:

- Optimization of reactive ion etching conditions for 500 nm etching.
- Optimization of reactive ion etching conditions for 10 nm etching.
- In general, regrowth of GaAs on top of patterned substrates results in very good quality material, but there are some aspects to be considered:
    - When the etching depth is 500 nm, the pattern is reproduced in the layer regrown, and therefore it is very difficult to obtain a flat surface after the growth. We are now studying the possibility of using ion implantation to make the bottom contacts.
    - When the etching depth is 10 nm, the result is a flat surface with very high quality of the GaAs regrown. The problem with this approach is the possible contact between QWs after the subsequent regrowth due to the low thickness of the AlGaAs barrier separating the QWs.
- Selective ion implantation of contacts
- Design and development of a photolithography mask to develop the whole device using different approaches (ion implanted contacts and selective QW etching).
- Regrowth of GaAs on previously implanted GaAs samples
- Processing of the whole device using the ion implantation scheme.
- Demonstration of practical application of the device using ion implantation. Preliminary measurements of the electrical characteristics show good agreement with the theory and are very promising to obtain IR absorption at temperatures close to RT.

The next steps we pursue are the following:

- To find the optimum annealing conditions to have high conductive layers after ion implantation, reducing the clusters observed by TEM.
- To mount an IR setup to characterize the devices at different temperatures with the possibility of accessing all the pads of the device.
- To improve the processing to develop the device using selective QW etching (in this case the regrowth is not a problem).

APPENDIX A:

Report on 500nm etching optimization

The aim of this appendix is to show all the experiments that we made in order to optimize the etching. The final objective was looking for very low roughness, anisotropy in the etch –vertical sidewalls- and to avoid the undercutting of the masking material that could have negative effect in the subsequent growth.

GaAs substrate for testing: we first show the quality of a native GaAs substrate for comparison.

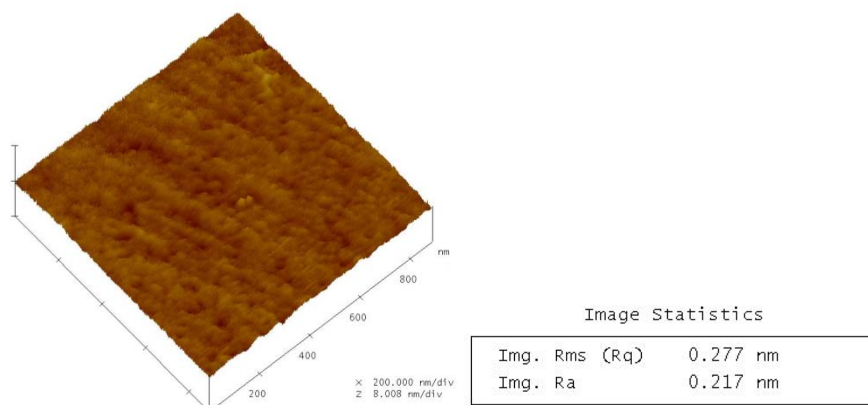


FIG. 28 GaAs Substrate

Wet etching tests:

Almost all GaAs etchants operate by first oxidizing the surface and then dissolving the oxide, thereby removing some of the gallium and arsenic atoms. Generally, the etchant contain one component that acts as the oxidizer and another that is the dissolving agent.

Before describing different chemical etchings used in the tests, we want to indicate that in the etching solutions composed of acid - H_2O_2 - H_2O it is important to add first acid to the water, waiting until the mixture is cool (at least 1 hour). The exothermic character of this reaction makes the temperature to rise up, therefore, if we add the H_2O_2 to a hot mixture it can cause the peroxide concentration to decrease and the etching cannot be performed in standard conditions. For this reason is also important to notice that the bottles open for a long time or

maintained half-empty during several months, could have varied the concentration told by the supplier. Another disadvantage of the H_20_2 etchings is that they have a tendency to form bubbles which could cause nouniform etching, and should be removed by agitation or prevented by use of wetting agents.

- **Sulfuric acid based etchings → H_2SO_4:H_20_2:H_20**

This is the more traditionally solution to etch GaAs because it is relatively possible to control the undercutting and anisotropy after etching. High sulfuric concentration mixtures are used when you need to make polishing of samples with damaged surfaces, and thanks to the high etching rates -5 microns/min- it is very anisotropic, but it is not a good way to etch step of less than 5 microns because it allows a very poor control of the step etched.

For etchings of hundreds of nanometers as in our case, concentrations of 1:8:80 and 1:8:120 were used:

H_2SO_4:H_20_2:H_20 - 1:8:80 (etching rate: 540 nm/min)

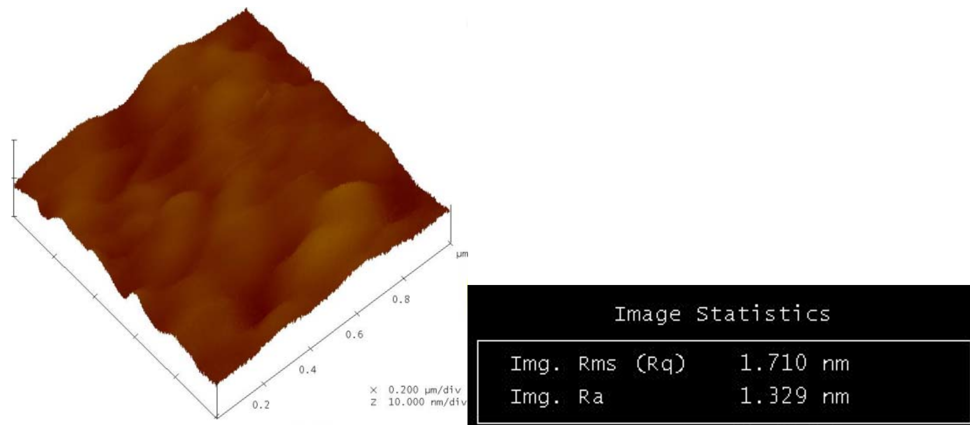


FIG. 29 AFM images of GaAs substrate etched with H2SO4:H202:H20 -- 1:8:80

H_2SO_4:H_20_2:H_20 - 1:8:120 (etching rate: 380 nm/min)

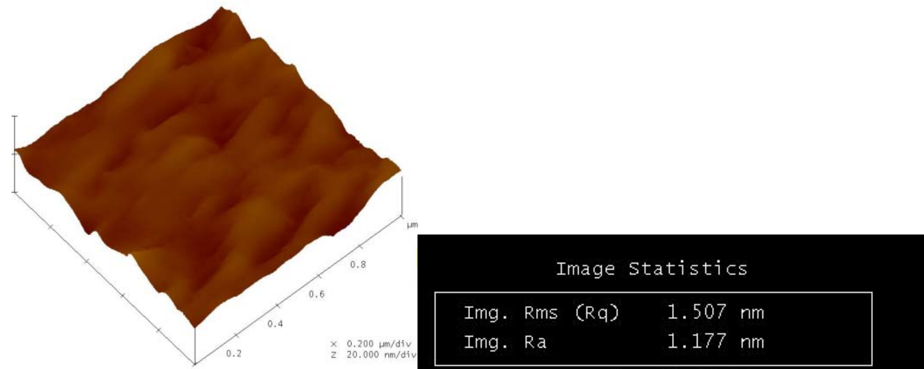


FIG. 30 AFM images of GaAs substrate etched with H2SO4:H202:H20 -- 1:8:120

- **Phosphoric acid based etchings → H_3P0_4:H_20_2:H_20**

With phosphoric etchings we obtained similar surface roughness than with sulfuric acid mixtures:

H_3P0_4:H_20_2:H_20 - 1:1:8 (etching rate: 580 nm/min)

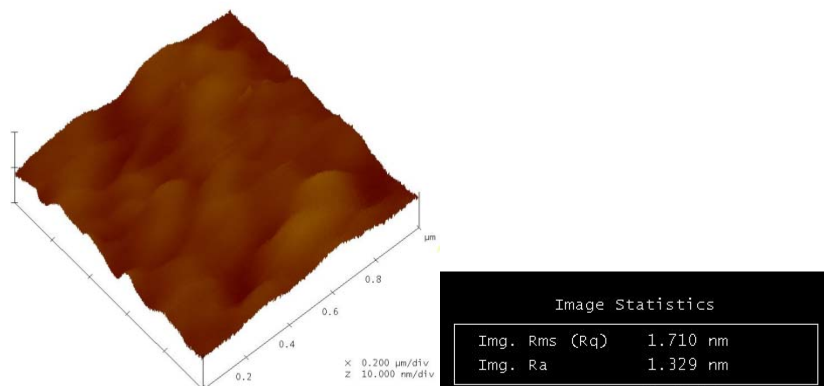


FIG. 31 AFM images of GaAs substrate etched with H3PO4:H202:H20 -- 1:1:8

H_3P0_4:H_20_2:H_20 - 1:1:12 (etching rate: 415 nm/min)

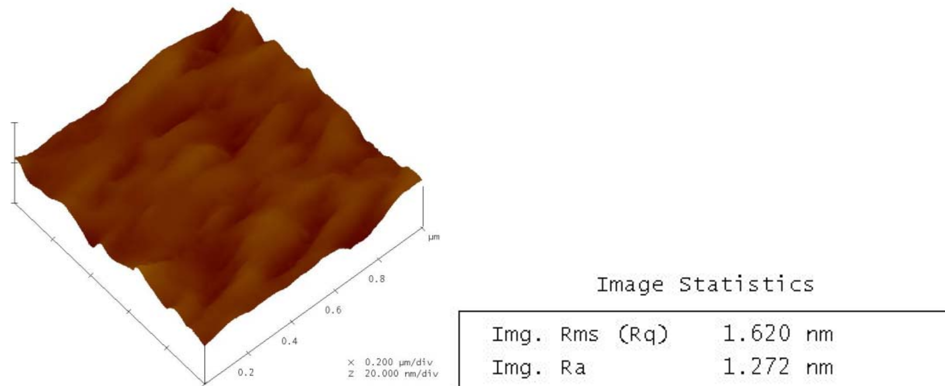


FIG. 32 AFM images of GaAs substrate etched with H2SO4:H202:H20 -- 1:1:12

- **Hydrochloric acid based etching→ HCl:H_20_2:H_20**

Although hydrochloric acid etchings are becoming very common, our experiments seem to indicate worse results than using sulfuric and phosphoric solutions:

HCl:H_20_2:H_20 - 1:1:9 (etching rate: 200 nm/min)

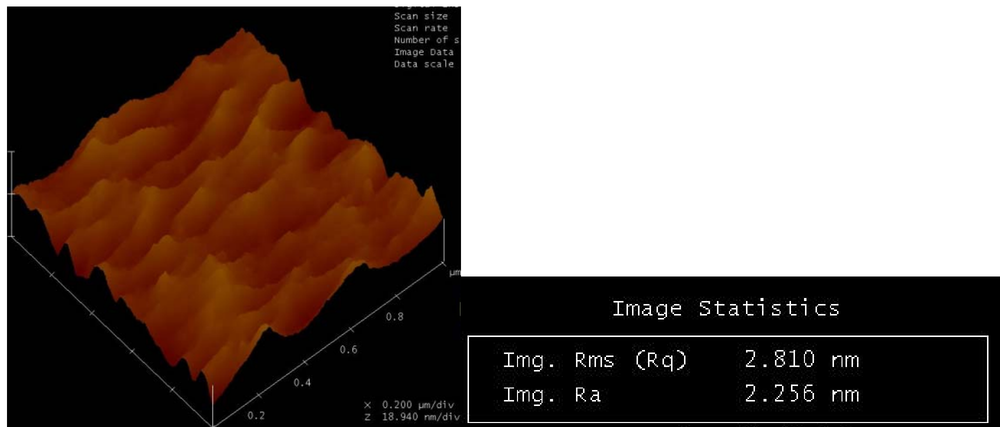


FIG. 33 AFM images of GaAs substrate etched with Hcl:H202:H20 -- 1:1:9

GaAs etching by other HCl concentrations was found in the literature, typically 40:4:1 and 80:4:1. This chemical etchings cause a smooth undercut sidewall, but they are essentially very isotropic .

CONCLUSIONS OF WET ETCHINGS EXPERIMENTS:

The major limitation in GaAs wet etching is that there is considerable undercutting of the masking material, that is, lateral etch rate is a significant fraction of the vertical rate. According to our experiments we can conclude that the roughness and the degree of mask undercut were undesirably large, and it is quite isotropic which caused inaccurate patterns transfer.

Dry etchings: Reactive Ion Etchings (RIE)

Reactive Ion Etching is a technology that uses chemically reactive plasma to remove material. The plasma is generated under low pressure by RF electromagnetic fields and the high-energy ions etch the sample and react with it. Etch conditions in a RIE system depend strongly on process parameters such as pressure, gas flows and RF power. The ions react chemically with the materials on the surface (chemical process), but can also remove some material by kinetic energy (physics mechanism).

The main factor to consider is the voltage difference between electrodes (DC Bias). This factor is directly proportional to the RF power and inversely proportional to pressure. In order to achieve the wished anisotropy, the way is to work with very higher DC-bias (which implies low pressures and high powers) but it can suppose rough surfaces and other damages induced by the ions bombardment. Lowering the power can improve the surface roughness, but probably it results in worse vertical side walls.

Etching steps and conditions

The previous cleaning of the samples is essential for the right etching. Otherwise, some rests of the photoresist of the lithography can appear. In order to solve this problem it is advisable to use an oxygen plasma during some minutes to clean organic contaminations previously to the GaAs etching. Oxygen causes a reaction with organic agents, giving as result the volatilization and diffusion of them towards the plasma of the chamber and later absorbed by the vacuum pumps.

- **O_2 Plasma characteristics**

  Φ_{O2}→ 10 sccm
  Power→ 37 W
  Pressure →35 mTorr
  Time→ 3 minutes
  Etching rate (of resist) → 10nm /min
- **Etching process**

The etching can be performed using only $SiCl_4$, but by means of argon addition it is possible to reduce DC Bias keeping the etching rate, which affects to the roughness of the sample in a very positive way. After optimization of the parameters –gas flows, power, pressure, etc- we obtained very good results with the conditions that are described below:

Φ_{Ar} (sccm)	Φ_{SiCl_4} (sccm)	POWER (W)	Rate (nm/min)
1.5	**15**	**125**	**92**
9	**9**	**125**	**93**
3	**15**	**107**	**73**
9	**9**	**107**	**79**

In all of these cases we obtained similar results. The surface roughness seems to improve with lower power.

The following AFM images show GaAs surfaces after an etching of 500nm:

125 W, 1,5 sccm Ar, 15 sccm $SiCl_4$

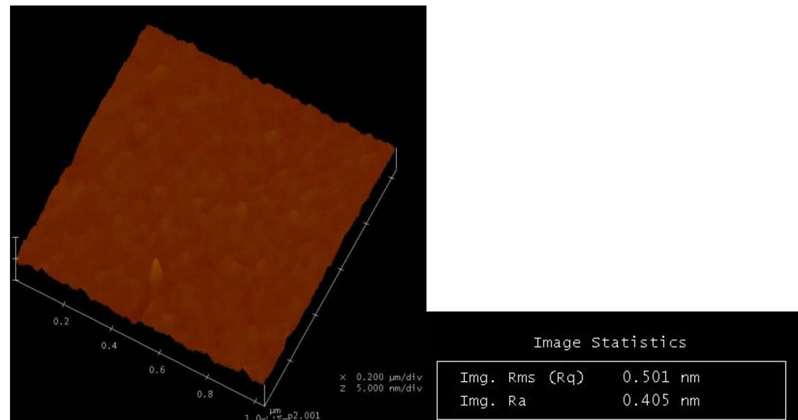


FIG. 34 AFM images of GaAs sample etched 500nm with RIE using SiCl4:Ar (1,5:15) mixture and 125 W

125 W, 9 sccm Ar, 9 sccm $SiCl_4$

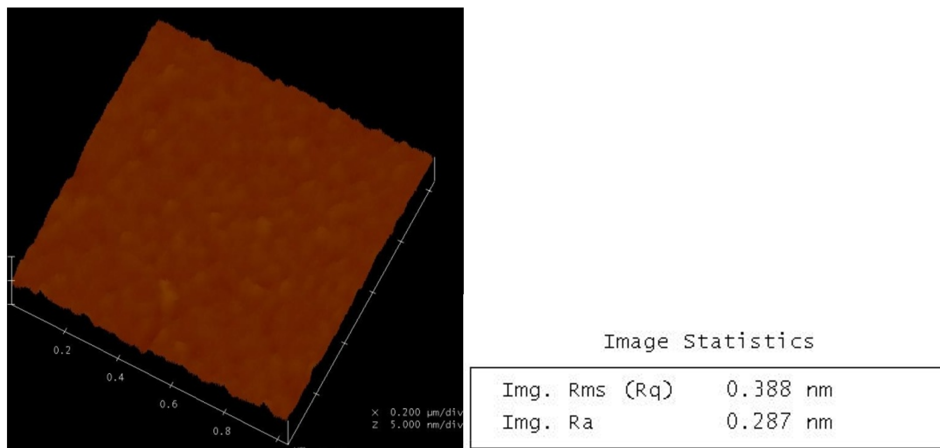


FIG. 35 AFM images of GaAs sample eteched 500nm with RIE using SiCl4:Ar (9:9) mixture and 125 W

125 W, 1,5 sccm Ar, 15 sccm $SiCl_4$

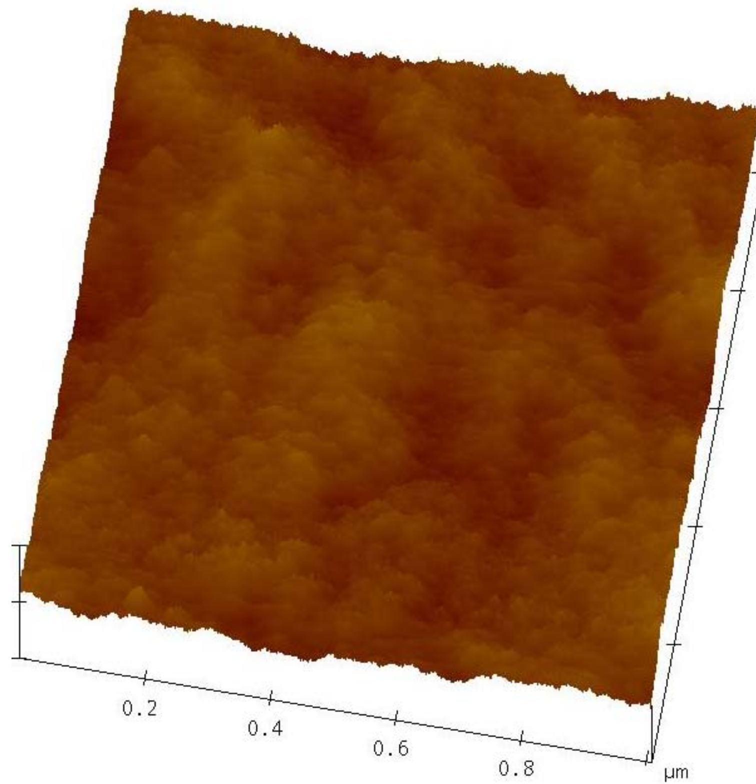


Image Statistics

Img. Rms (Rq)	0.338 nm
Img. Ra	0.269 nm

FIG. 36 AFM images of GaAs sample eteched 500nm with RIE using SiCl4:Ar (9:9) mixture and 107 W

The best result for 500nm etchings was achieved with 9 sccm of Ar, 9 sccm of $SiCl_4$ and with a power of 107 W. With these parameters, DC Bias of 340 V was obtained and the pressure during the etching was of 7 mTorr aprox (FIG. 36).

In the FIG. 37 it is shown a SEM image of a sample etched in the conditions mentioned before.

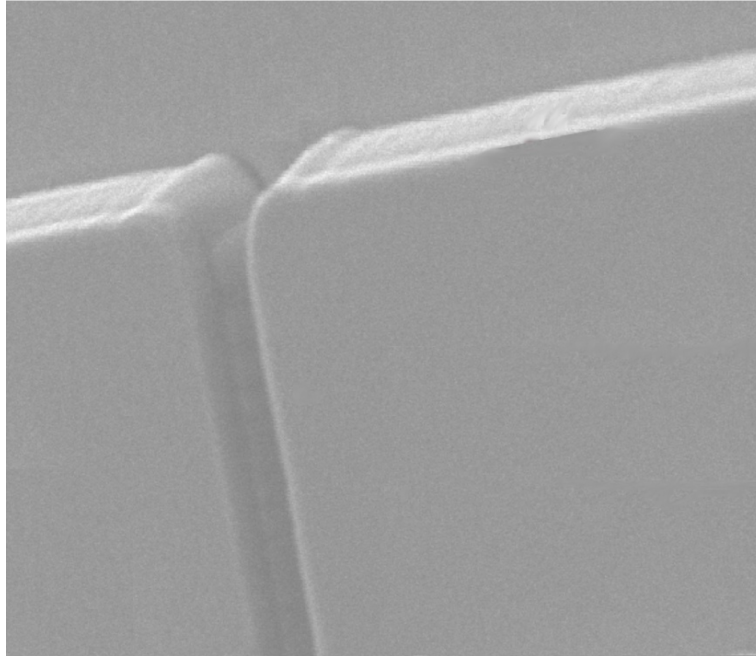


FIG. 37 SEM image after 500nm etching in GaAs

Conclusions: Very vertical sidewalls, negligible undercutting and very smooth surfaces (less than 1 Angstrom of nominal roughness in 500nm etchings).

After etching process:

Before loading sample in the MBE, it is necessary to clean and oxide the surface to protect it from external agents.

In this etching high proportion of sulfuric acid is used. Combinations of 4:1:1 or 3:1:1 are commonly used because they tend to be diffusion limited in character. Etch rate is rapid (6 μm/min) so the sample should be immersed in the solution during not more than 5 seconds.

The oxidation process is made by a very simple method: 15 minutes in running desionized water –i.e. keeping the water flowing during all the process-, agitating continuously –not ultrasonic agitation, because it could crack the sample-

APPENDIX B:

10 nanometers etching

Considering the high etchings rates obtained with wet etching (aprox. 600 nm/min) it would be impossible to control only a few nanometers, so in this case we have only used RIE etching to optimize this processing.

- **Best conditions for 500 nm etchings:**

First tests were performed using the optimized parameters for 500 nm etchings, i.e.:

- Power: 107 W
- Ar flow: 9 sccm
- $SiCl_4$ flow: 9 sccm
- DC Bias: 340 V
- Pressure: 7mTorr
- Etching rate: 79 nm/min (1,32 nm/s)

While these conditions were suitable for 500nm etchings, we found difficulties to extrapolate the results for 10 nm. Performing tests with 8 s (the time that theoretically we should keep the etching for 10 nm) it was verified that not etching at all occurred. We then decided to increase progressively the etching time.

In the next six images (FIG. 38-FIG. 43) are shown different etchings performed in the same conditions above mentioned but during 25 seconds. As it is possible to see in the AFM images, the step etched varies from 8 nm to 40 nm.

The origin of the low reproducibility was found in the plasma creation. With low pressure (lower than 5 mTorr) it is very difficult to produce plasma, so our RIE machine responds closing the throttle valve in order to increase the pressure until a current between electrodes is detected. When plasma is formed, the valve is opened again. The movement of valve closing and opening spends a few seconds (15-30 seconds according to our tests), as well as stabilization of pressure. This explains why, etching during 25 seconds, we obtain different depths from 8 nm to 40nm, because this time it is not enough to be sure that the processing is been performed at the same conditions.

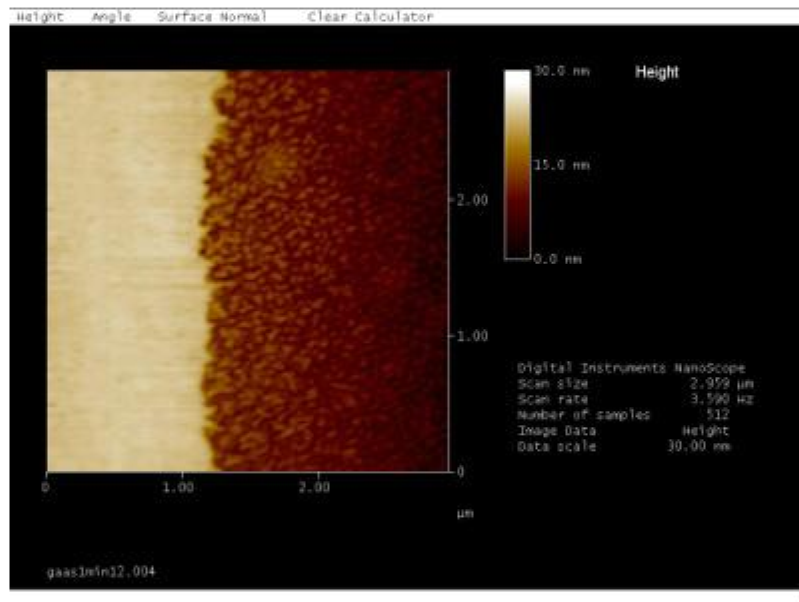


FIG. 38 high power-low pressure etching (I)

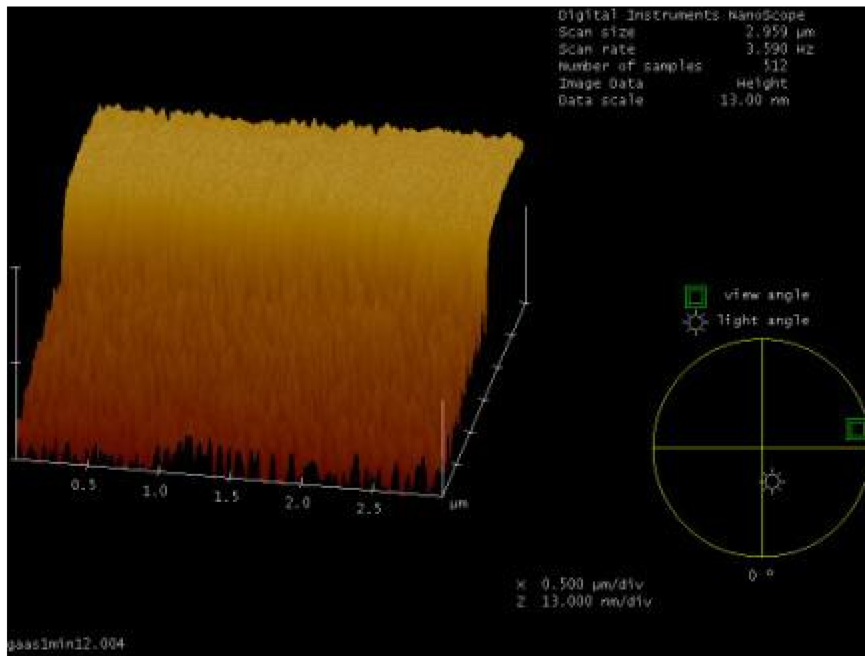


FIG. 39 high power-low pressure etching (II)

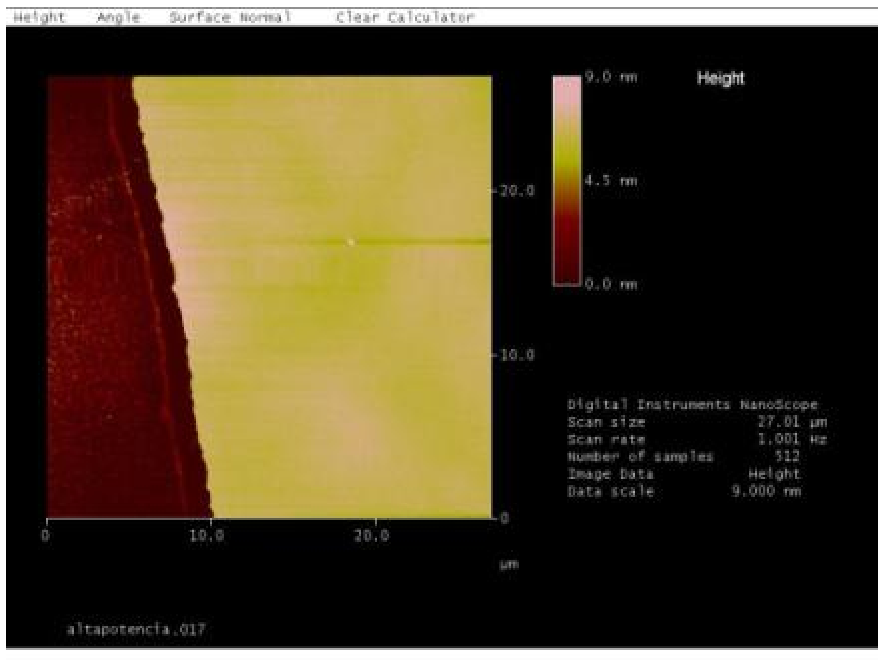


FIG. 40 high power-low pressure etching (III)

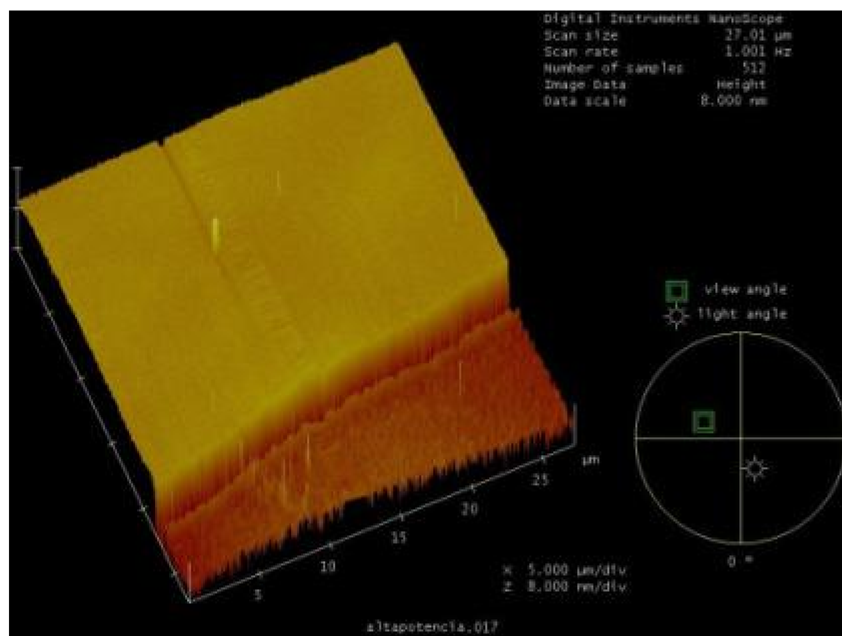


FIG. 41 high power-low pressure etching (IV)

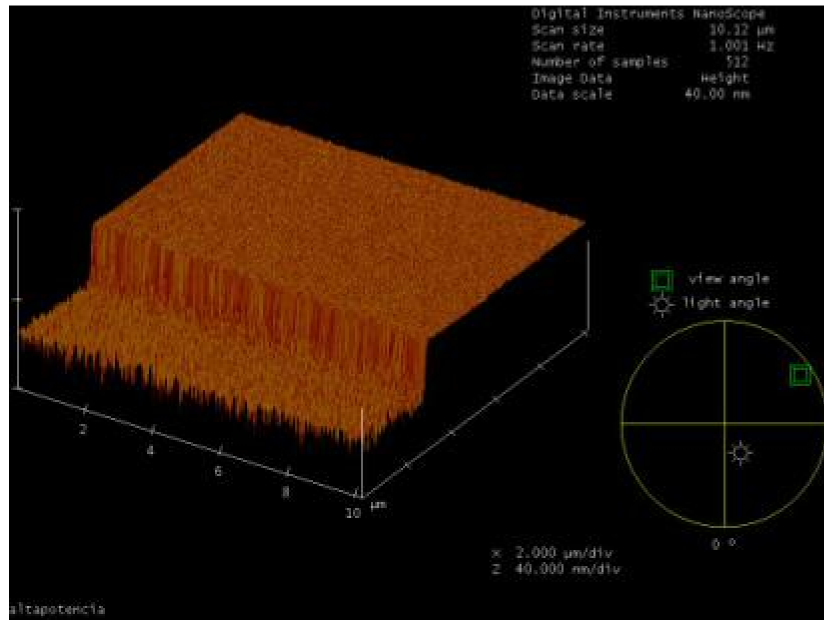


FIG. 42 high power-low pressure etching (V)

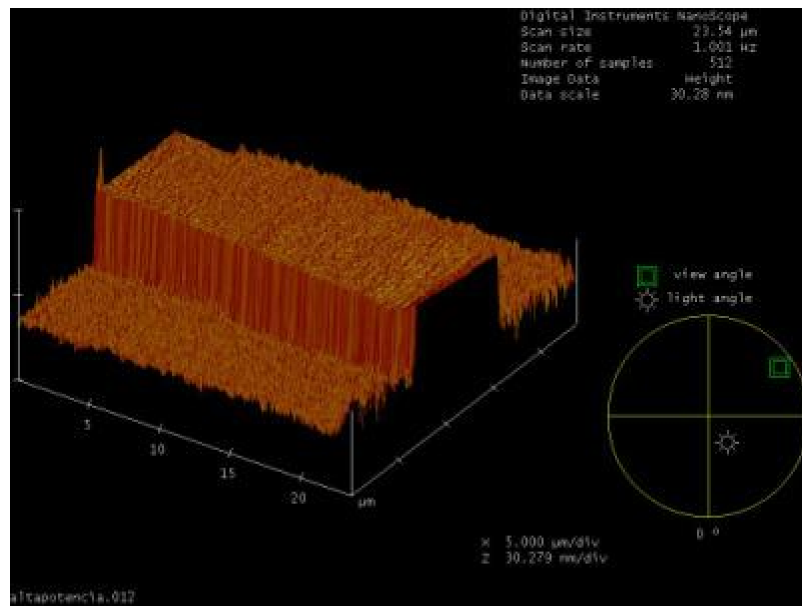


FIG. 43 high power-low pressure etching (VI)

- ### Etchings with lower power

The following step was focussed to calibrate the etching using lower powers, but keeping the pressure used in our first tests.

We found that with power higher than 60 W, we still have the problem according to the reproducibiliy of the results, achieving good etching in some samples (FIG. 44) but not in all the testings performed.

The lower the power, the better reproducibility (because we increased the etching time as well). However the results were not completely satisfactory, noting a deterioration of the surface (roughness), with not good uniformity and worse results near of the pattern sidewalls (FIG. 45, FIG. 46).

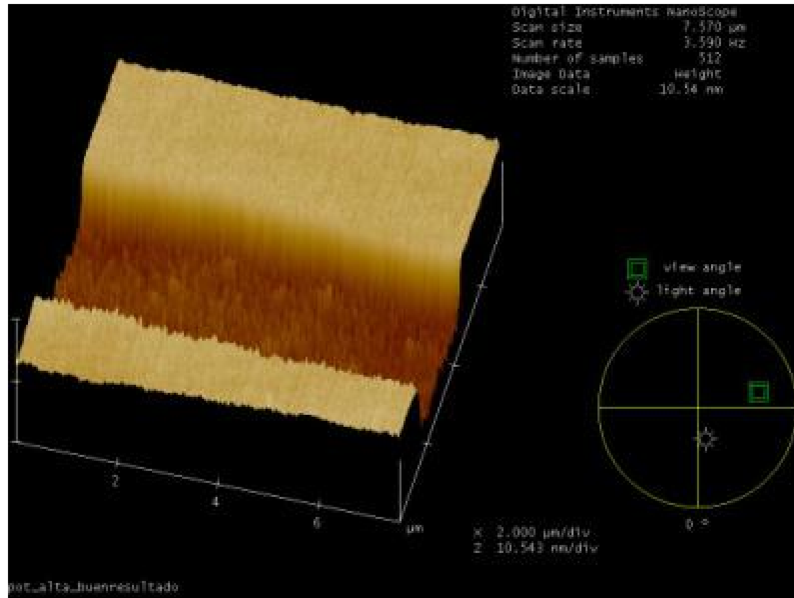


FIG. 44 60 W etching, low pressure

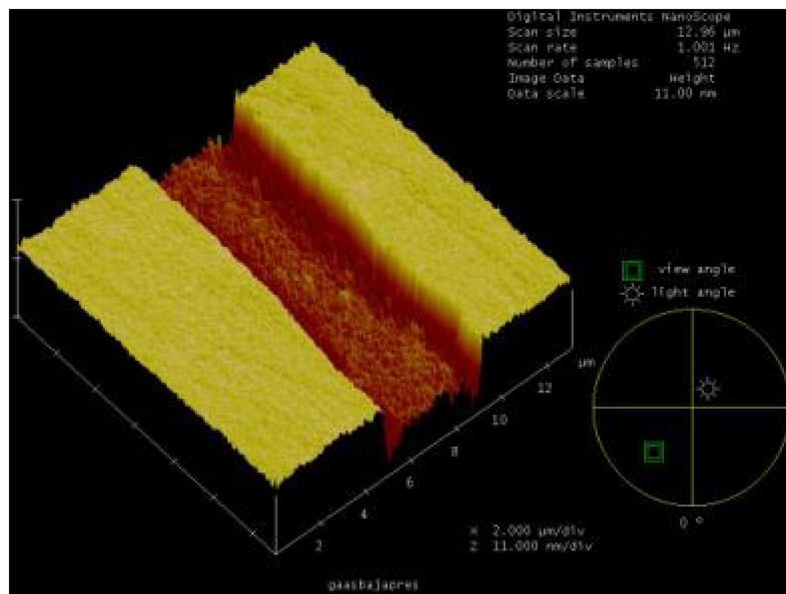


FIG. 45 40 W etching, low pressure

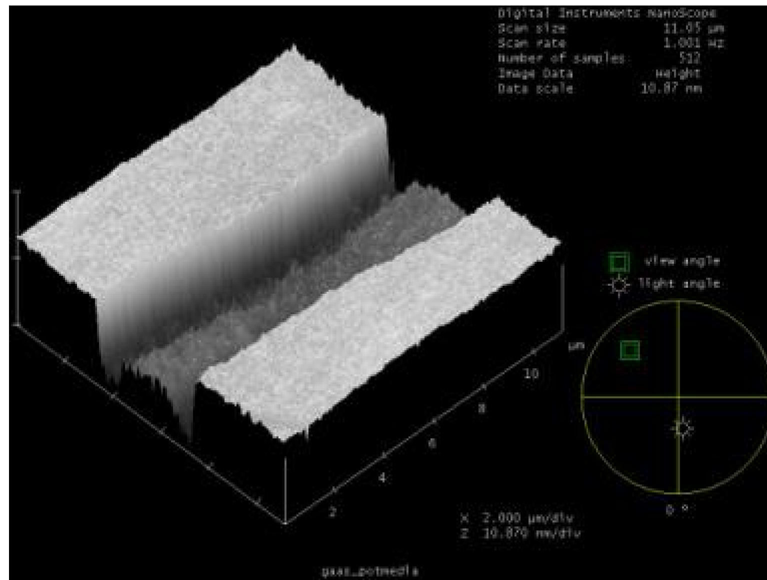


FIG. 46 50 W etching, low pressure

o Etchings with lower power and higher pressures:

We performed new tests increasing the pressure (i.e. increasing the gasses flows). In principle, it should improve the results because the discharge can be sustained without the needed of closing the valve to increase the pressure (i.e. quick plasma estabilization) and with a lower rates, resulting in a better control of the process. This new conditions led to a less anisotropic etching (close to the results obtained by wet etching), anyway in this case this is not so important because of the short thickness of material we need to remove.

In this conditions, homogeneity, roughness and reproducibility in etched samples improved:

Parameters used in the etching:

- Power: 45 W
- Argon flow: 7,5 sccm-13.5sccm
- $SiCl_4$ flow: 11sccm-17 sccm
- DC BIAS: 100 V

Following AFM images shown some of the successful 10 nm etching performed in the mentioned condition.

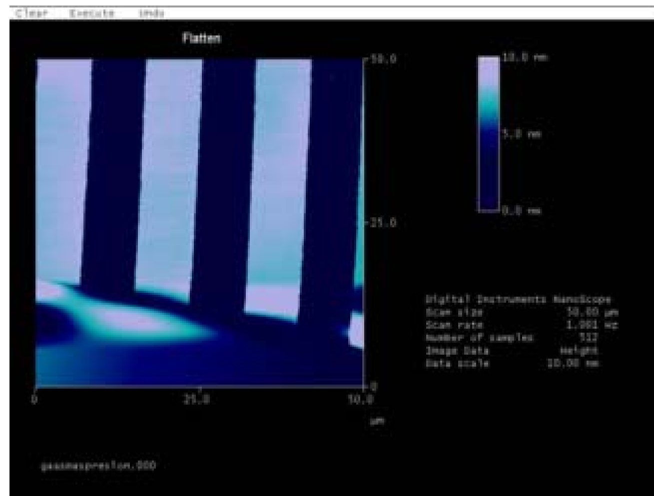


FIG. 47 2D Analysis of a 10nm etched sample

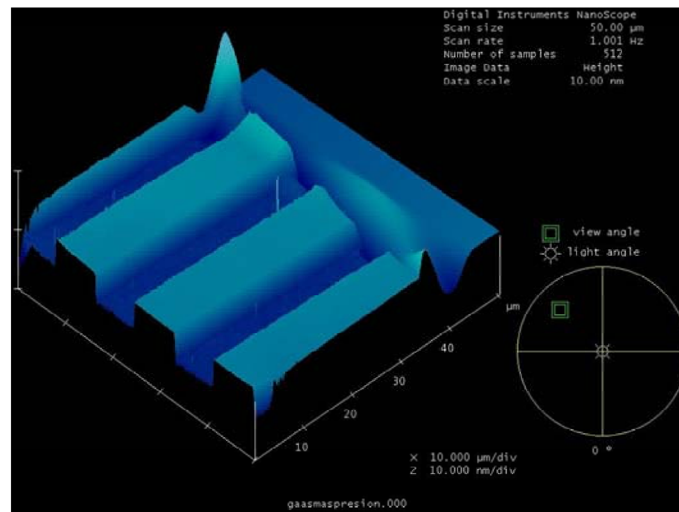


FIG. 48 Etching with 13 sccm Ar flow, 11 sccm $SiCl_4$ flow, power 45 W

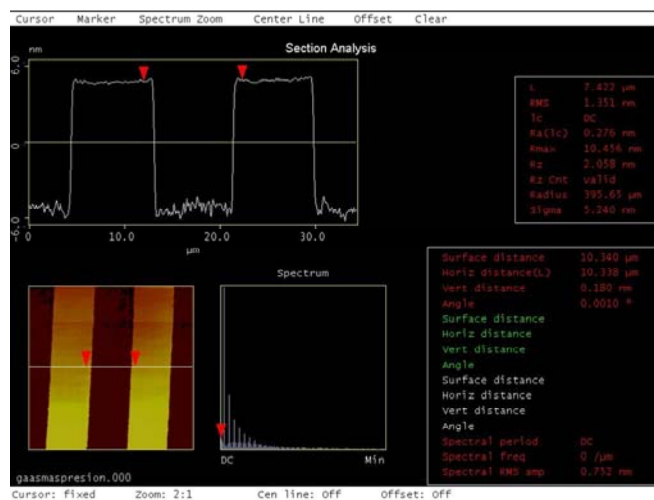


FIG. 49 Section Analysis of a sample etched 10 nm (I)

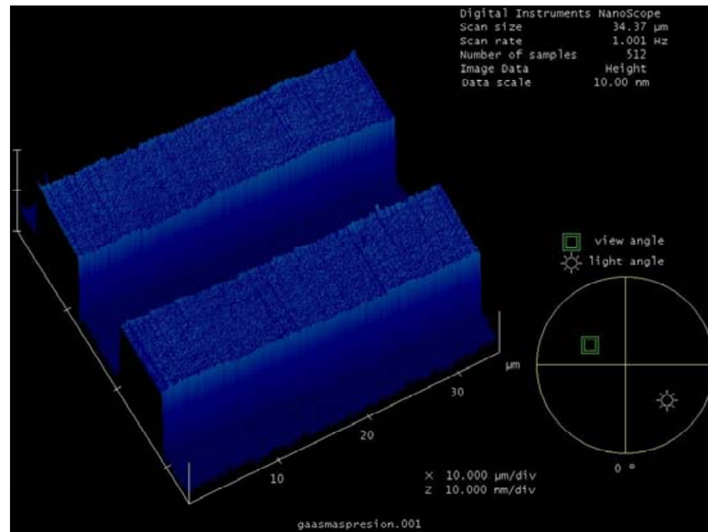


FIG. 50 Etching with 9 sccm Ar flow, 15 sccm $SiCl_4$ flow, power 45 W (I)

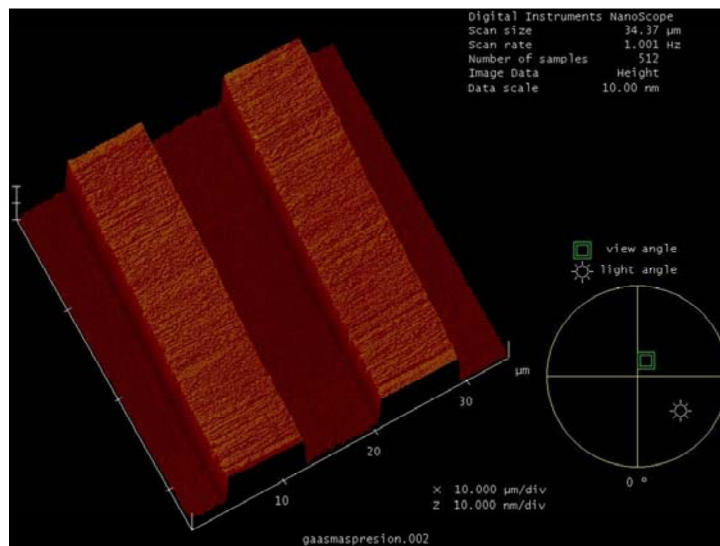


FIG. 51 Etching with 9 sccm Ar flow, 15 sccm $SiCl_4$ flow, power 45 W (I)

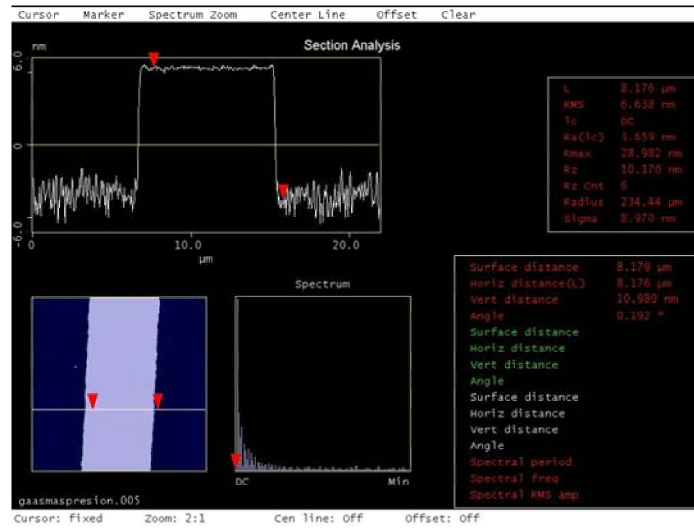


FIG. 52 Section Analysis of a sample etched 10 nm (II)

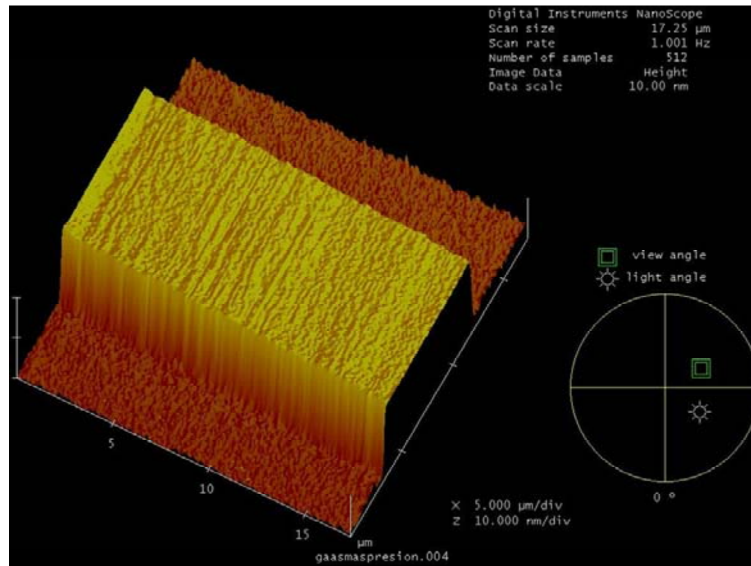


FIG. 53 Etching with 12 sccm Ar flow, 15 sccm $SiCl_4$ flow, power 45 W

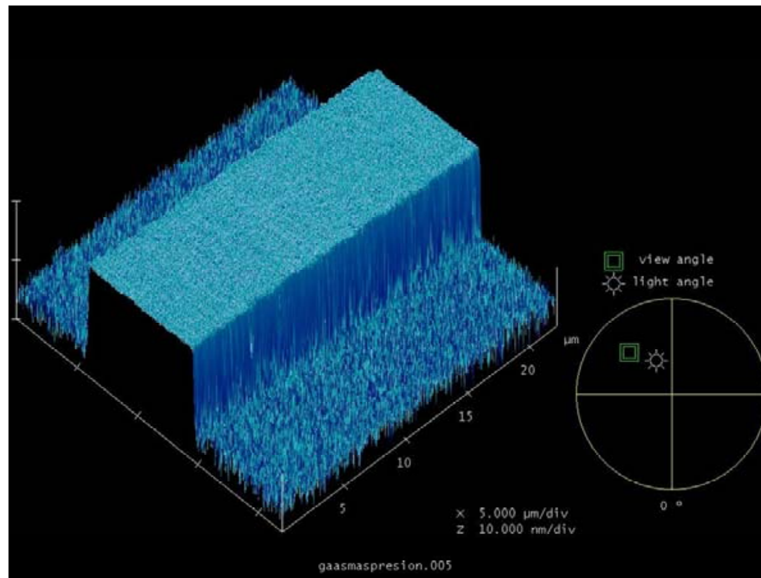


FIG. 54 Etching with 7,5 sccm Ar flow, 17 sccm $SiCl_4$ flow, power 45 W

Appendix C: Ion Implantation for bottom contacts

Ion implantation is the introduction of ionized dopant atoms into a substrate with enough energy to penetrate beyond the surface. The depth of implantation is function of the dose and the ion energy. The major advantage of ion implantation technology is that doping can be performed locally by selectively masking the wafer so that ion implantation occurs only at desired locations.

This method is very useful to form conductive materials from semiconductor or insulator samples keeping the flat surface of the initial wafer, although it is not free of problems:

- Generally, the quality of the material decreases with the ion implantations

- Ions bombardment usually increases the density of nucleation sites. This effect is related to the appearance of defects in the surface and other textures or preferred orientations.

- Normally, the magnitude of compressive stress increases drastically with the ion implantations.

- Even though the more important effect of the introduction of ions appears in vertical directions, it can also take place in horizontal way, so that in implanted zones very near to each other, it is possible that they are connected after implantation process.

In order to obtain similar contacts that making use of n+ layers grown by MBE –i.e. 10^{18} atoms/cm^3-. the conditions to achieve this doping level were obtained by means of simulation program SRIM.

The distribution of impurities with depth follows a Gaussian law: $N(x) = \frac{\Phi}{\Delta R_p \cdot \sqrt{2\pi}} e^{\frac{-(x-R_p)^2}{2\Delta R_p^2}}$

Where Φ is the dose, Rp is the projected range and ΔRp is the longitudinal straggling. These latter values (Rp and ΔRp) are obtained by simulation considering the ion (Si) and the implantation energy. The dose is calculated to have 10^{18} atoms/cm^3 at x=Rp.

We used two different implantation conditions: Si^+ implanted at 180 KV and Si^{++} implanted at 180 KV. Figures 55 and 56, show the doping profile and simulated data used in this work to obtain a doping concentration of 10^{18} atoms/cm^3 at 150 nm and 300 nm in depth respectively.

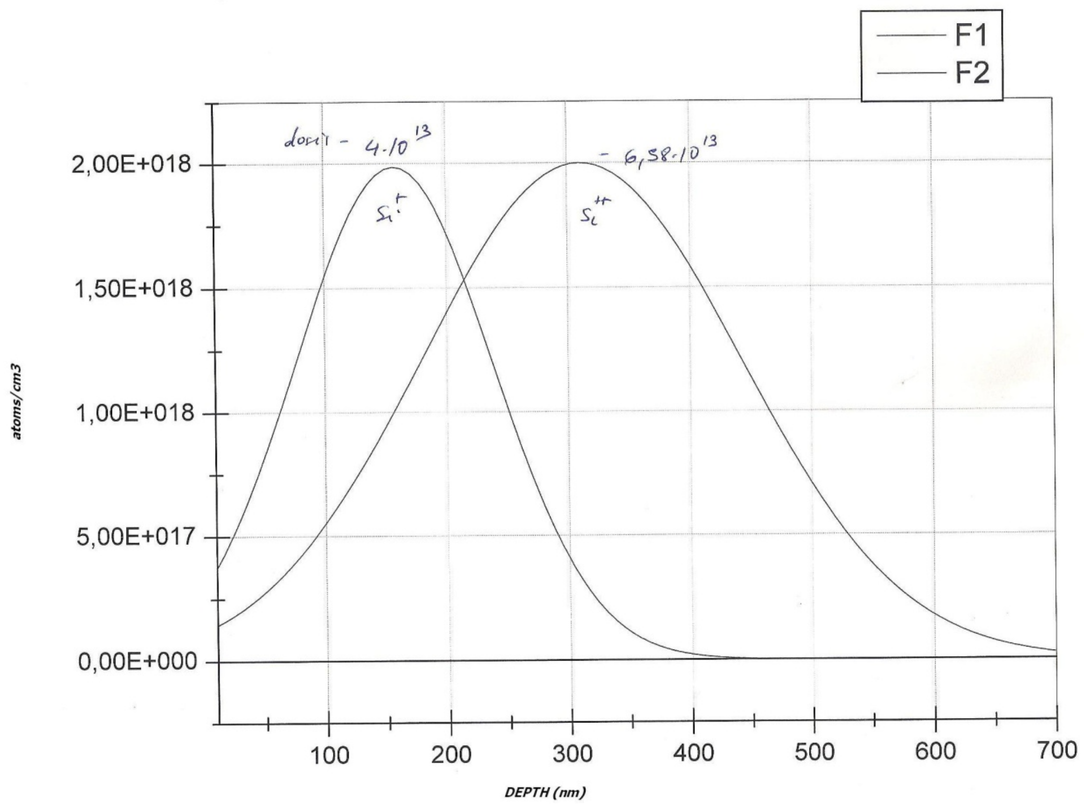


FIG. 55 Doping profile after ion implantation for two different species

Ion Energy	dE/dx Elec.	dE/dx Nuclear	Projected Range	Longitudinal Straggling	Lateral Straggling
80,00 keV	5,410E-01	6,791E-01	696 A	427 A	316 A
90,00 keV	5,784E-01	6,610E-01	782 A	468 A	348 A
100,00 keV	6,125E-01	6,438E-01	868 A	509 A	380 A
110,00 keV	6,432E-01	6,273E-01	954 A	548 A	411 A
120,00 keV	6,706E-01	6,117E-01	1040 A	587 A	442 A
130,00 keV	6,952E-01	5,969E-01	1127 A	625 A	473 A
140,00 keV	7,175E-01	5,828E-01	1215 A	662 A	503 A
150,00 keV	7,380E-01	5,695E-01	1303 A	698 A	532 A
160,00 keV	7,570E-01	5,568E-01	1391 A	734 A	562 A
170,00 keV	7,749E-01	5,447E-01	1480 A	769 A	591 A
180,00 keV	7,920E-01	5,333E-01	1569 A	804 A	620 A
200,00 keV	8,246E-01	5,119E-01	1748 A	871 A	677 A
225,00 keV	8,638E-01	4,879E-01	1975 A	952 A	748 A
250,00 keV	9,027E-01	4,664E-01	2202 A	1031 A	818 A

FIG. 56. Simulated data for ion implantation

Another item to consider is that implantation takes also place in the photoresist. We simulated the depth until which they penetrate to be sure that the ions did not affect the GaAs layer. We proved that 1,5 microns of photoresist is enough to avoid the ions to reach the GaAs..

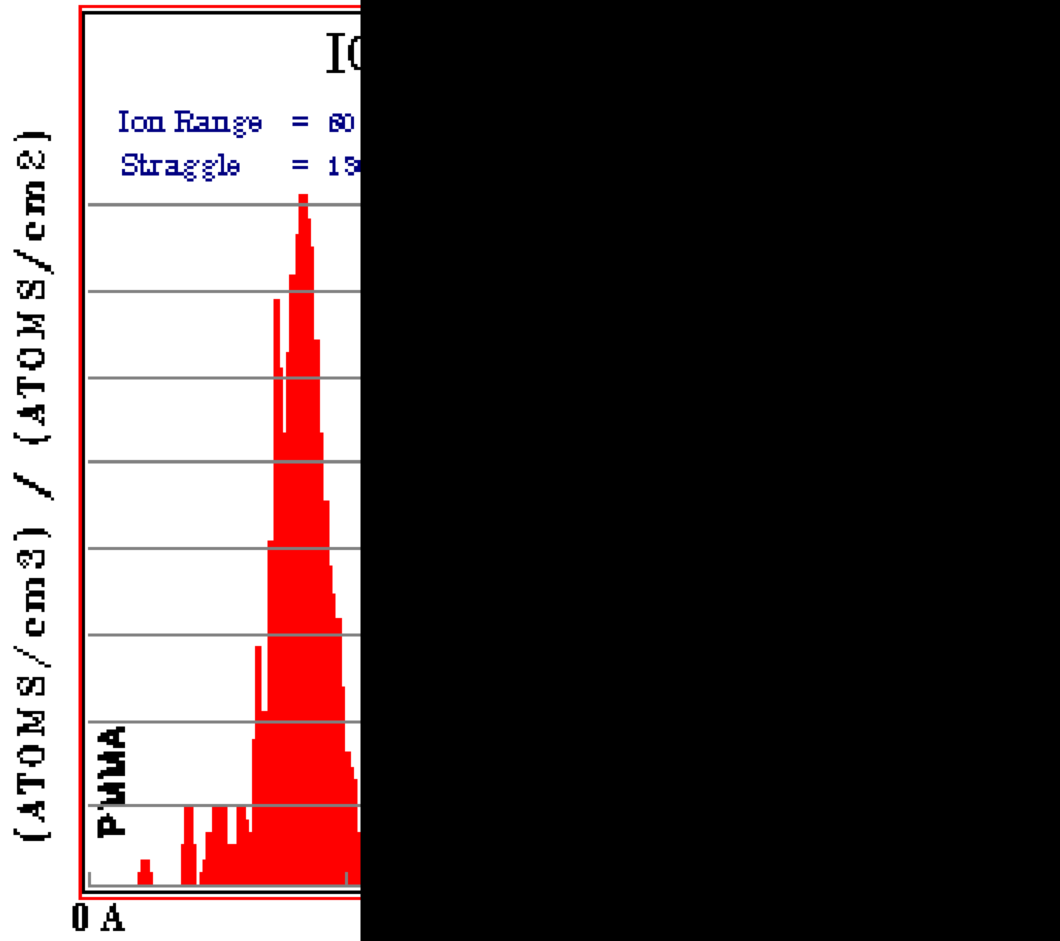


FIG. 57 Penetration of the ion implanted species in the photoresist

Table of figures

FIG. 1 Quantum Structure for Tunable Detectors
FIG. 2 SEM image of a GaAs layer etched by Reactive Ion Etching
FIG. 3 AFM picture of the etched surface showing a very low roughness comparable to that of the native substrate.
FIG. 4 AFM image of a GaAs layer regrown on a previously etched surface.
FIG. 5 Step before regrowth measured using an Alpha-Step Profiler
FIG. 6 Step after regrowth measured using an Alpha-Step Profiler
FIG. 7 MBE/selective etching/regrowth processing scheme
FIG. 8 Patterns of a 20 nm etching in GaAs (I)
FIG. 9 Patterns of a few nanometers in GaAs (Section Analysis)
FIG. 10 Problems in the etching and re-growth in the quantum well structure
FIG. 11 Rocking Curve of GaAs layers grown on top of a epi-ready GaAs wafer and and implanted one.
FIG. 12 AFM image of a GaAs grown in n+ implanted substrate
FIG. 13 SEM image of a GaAs epitaxial layer grown in n+ implanted substrate
FIG. 14 Design of the lithography mask using ACAD program
FIG. 15 Optical lithography mask manufactured for this project
FIG. 16 Nomarski images of a GaAs sample with marks alignment prepared for the implantation process
FIG. 17 Scheme of the sample after ion implantation
FIG. 18 Structures after MBE growth
FIG. 19 Etching to free bottom contacts
FIG. 20 Side contacts processing
FIG. 21 Contacts metallization
FIG. 22 Growth of n+layer, barrier layer and first QW
FIG. 23 Selective etching and regrowth
FIG. 24 Second selective etching and regrowth
FIG. 25 Etching until n+ layer
FIG. 26 Etching and metallization of side contacts
FIG. 27 Metallization and annealing of all contacts
FIG. 28 GaAs Substrate
FIG. 29 AFM images of GaAs substrate etched with H2SO4:H202:H20 -- 1:8:80
FIG. 30 AFM images of GaAs substrate etched with H2SO4:H202:H20 -- 1:8:120
FIG. 31 AFM images of GaAs substrate etched with H3PO4:H202:H20 -- 1:1:8
FIG. 32 AFM images of GaAs substrate etched with H2SO4:H202:H20 -- 1:1:12
FIG. 33 AFM images of GaAs substrate etched with Hcl:H202:H20 -- 1:1:9
FIG. 34 AFM images of GaAs sample etched 500nm with RIE using SiCl4:Ar (1,5:15) mixture and 125 W
FIG. 35 AFM images of GaAs sample eteched 500nm with RIE using SiCl4:Ar (9:9) mixture and 125 W
FIG. 36 AFM images of GaAs sample eteched 500nm with RIE using SiCl4:Ar (9:9) mixture and 107 W
FIG. 37 SEM image after 500nm etching in GaAs
FIG. 38 high power-low pressure etching (I)
FIG. 39 high power-low pressure etching (II)
FIG. 40 high power-low pressure etching (III)
FIG. 41 high power-low pressure etching (IV)

FIG. 42 high power-low pressure etching (V)
FIG. 43 high power-low pressure etching (VI)
FIG. 44 60 W etching, low pressure
FIG. 45 40 W etching, low pressure
FIG. 46 50 W etching, low pressure
FIG. 47 2D Analysis of a 10nm etched sample
FIG. 48 Etching with 13 sccm Ar flow, 11 sccm SiCl4 flow, power 45 W
FIG. 49 Section Analysis of a sample etched 10 nm (I)
FIG. 50 Etching with 9 sccm Ar flow, 15 sccm SiCl4 flow, power 45 W (I)
FIG. 51 Etching with 9 sccm Ar flow, 15 sccm SiCl4 flow, power 45 W (I)
FIG. 52 Section Analysis of a sample etched 10 nm (II)
FIG. 53 Etching with 12 sccm Ar flow, 15 sccm SiCl4 flow, power 45 W
FIG. 54 Etching with 7,5 sccm Ar flow, 17 sccm SiCl4 flow, power 45 W
FIG. 55 Doping profile after ion implantation for two different species
FIG. 56. Simulated data for ion implantation
FIG. 57 Penetration of the ion implanted species in the photoresist

References

P.M. Alsing, D.A. Cardimona, D.H. Huang, T. Apostolova, W.R. Glass, C.D. Castillo, Infrared Physics & Technology 50 (2007) 89–94