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ABSTRACT

The feasibility of integrating RF communication subsystems into system-on-a-chip devices to form covert sensor networks was investigated. The research vision and vehicle was an M&M(TM) candy-sized, low power, affordable (a few dollars) CMOS micronode device. The goals were to investigate approaches for realization of small on-chip antenna, define circuitry and techniques for wireless activation of a micronode device before deployment, and define low power circuitry for key functional blocks within the micronode. The antenna research concluded that on-chip antennas at ~5 GHz were easily realizable, but additional investigations were needed to establish more optimal on-chip 2.4 GHz antennas. Integrated low power designs were devised and verified for a transceiver and for wireless activation. Communication ranges that were feasible when limiting the available power source to 10's of mAh were 20 m node to node and 1 km node to base station. Device power dissipation, available power/energy and desired physical size and operating life place tight constraints on the design. The battery dimensions determine the size of the assembly. The micronode assembly will consist of only a small battery and one chip in a sealed rugged unit.

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INTRODUCTION AND SUMMARY

MOTIVATION

For more than a decade the University of Florida (UFL) has been conducting research for various sponsors (primarily DARPA) on small communication nodes that could serve as links in a mesh network or simple single point nodes that communicate with a base station. The intent has been to utilize these nodes in conjunction with sensors to form wireless sensor networks. The UFL approach has been to attempt to realize entire nodes within single chips produced using mainstream bulk silicon CMOS. Previous work established proof of concept circuitry for a node (called a μ Node) that operated using a 24 GHz carrier frequency. In the project reported here, funded by the Army Research Office, the intent was to increase the μ Node communication range, to reduce the device power dissipation, and to provide circuitry that would allow a node to be wirelessly activated before placing it into service.

The primary approach to power reduction and range increase was to change the carrier frequency from 24 GHz to a lower frequency – preferably to 5.2 GHz or 2.4 GHz if it proves feasible. Figure 1 shows conceptual diagrams of μ Node assemblies [1]-[5]. Figure 2 shows a version of a μ Node (a μ Node marble) operating at 24 GHz that could be packaged with a battery in a volume about the size of an M&M™ candy. Unfortunately the high operating frequency resulted high power consumption that limited the size and reduced operating life time.

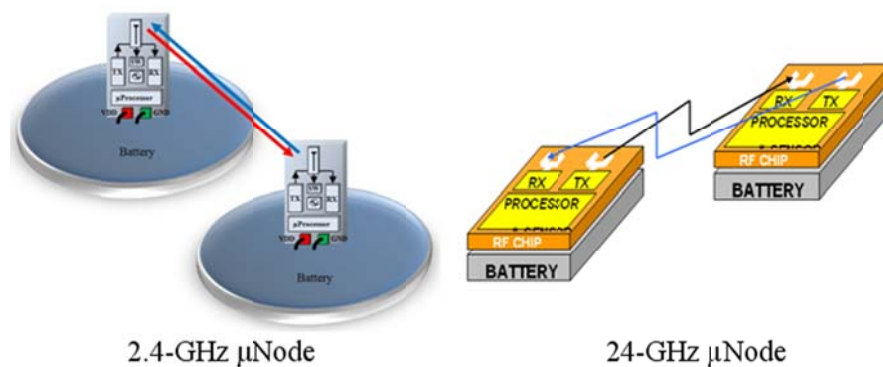


Figure 1: Recent μ Node system concept diagrams

For a μ Node device power dissipation is a critical issue. Each node is assembled with a battery as a single rugged unit. The physical size of the assembly is determined primarily by the size of the battery. The assembly power dissipation, the limited energy available from the battery and the desired operating life of the unit combine to determine the particular size of battery that can be used. To make the node more power efficient, approaches to lower the operating frequencies were investigated. Lowering the frequency from 24 GHz to 2.4 GHz provides several advantages. The power consumption of the entire system can be reduced by a factor of ~ 3 and the communication range was expected to increase by a factor of ~ 10 due to lower path loss at 2.4 GHz [6]. With longer communication range, the node density required to monitor a given

area (nodes per km or per km²) can be reduced. This leads to lower system cost. Furthermore, the lower power consumption increases the life time of μ Node as well.

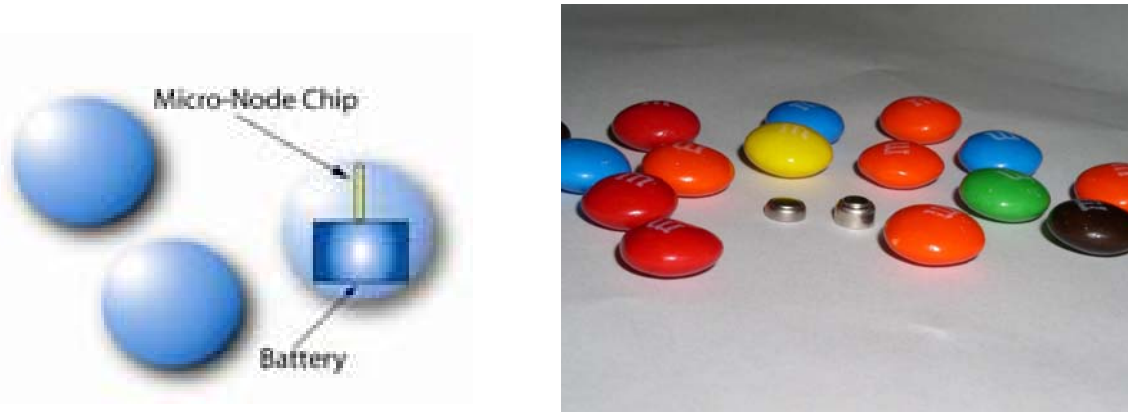


Figure 2: Assembly concept for M&M size μ Node

Like the vision of previous research, package size target of this new μ Node is still that of an M&M™ candy. A major challenge is to realize a compact antenna operating at 2.4 GHz. Since the wavelength is longer at lower frequencies, it is challenging to implement an antenna which can fit inside the μ Node package while still providing reasonable performance. Furthermore, because of the small size it is difficult to power up each node individually by flipping a mechanical switch. In addition, a subsystem which can rapidly activate many nodes simultaneously is required. Finally, since a μ Node system is deployed in remote areas where no additional supply sources except a coin cell battery attached on each node are available, a system with low power consumption is necessary.

RESEARCH GOALS AND RESULTS

Simplified radio architecture of a μ Node chip is shown in Figure 3. This new system architecture consists of an antenna, a wireless switch, a transceiver front-end (transmitter and receiver chains), a frequency generator, a demodulator and a baseband processor. Unlike the previous μ Node version, this new system employs only one antenna to reduce the chip area. A wireless switch is introduced to provide the ability of activating the μ Node after it is assembled with a battery. The goals for this RF subsystem integration research project were (1) to investigate approaches for realization of small on-chip antennas, (2) define circuitry and techniques for wireless activation of a μ Node before deployment, and (3) define low power circuitry for key functional blocks within the μ Node.

More specifically, the research objective was to enable realization of small (M&M™ candy size), low power and low cost micro-nodes which can communicate from node to node at increased distances. The 24 GHz design was capable of communicating at 5 m node to node and 100 m node to base station distances. The initial target for this effort was to achieve about 50 m from

node to node and from node to base station at distances of ~ 1 km. This research effort demonstrated that 20 m node to node and 100 m node to base station was readily achievable with on-chip antennas where the power supply is limited to a small coin cell. The targeted longer ranges can obviously be achieved provided more power can be expended, but that leads to either reduced operating life because the battery is depleted or requires a larger battery and thus larger assembly size. The research also explored in more detail the impact of placing the μ Node device very close to the ground. In that case ground reflections reduced the node to node range to about 5 m.

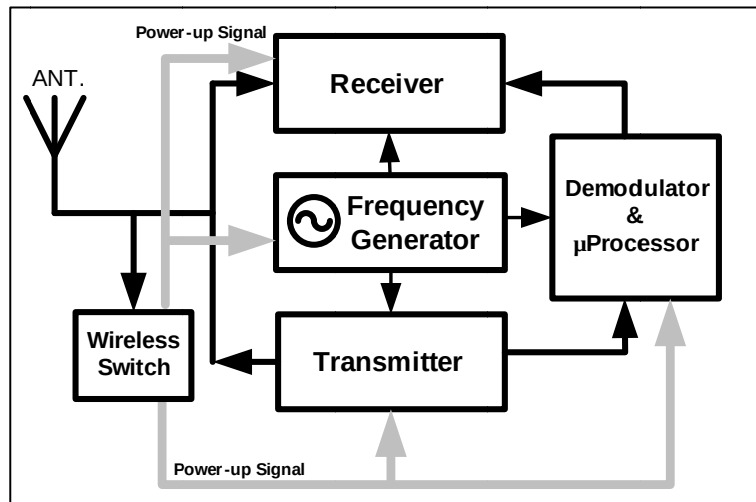


Figure 3: Simplified μ Node radio architecture

Due to the small volume of μ Node, a compact antenna that can fit inside the package while achieving reasonable performance at 2.4 GHz is important and challenging. Investigation of the off-chip and on-chip antenna characteristics especially at low operating frequencies such as 2.4 GHz was required. Figure 4 shows some off-chip and on-chip antennas which were investigated in this research.



Figure 4: Size comparison of off-chip and on-chip antennas

Since a μ Node system requires post fabrication calibration [7], an ability to turn the battery power on and off the system is required. Also, there will be a period of time after the μ Node and battery assembly has been fabricated, and it is desirable that the battery connection to the active circuitry be held open in such a manner as to minimize leakage currents that would drain the battery. As mentioned before, it is difficult to place a physical switch in a node which has a small form factor. Therefore, the concept of wireless activation switch has been utilized to accomplish this function. Figure 5 shows a conceptual diagram for a non-contact switch to turn on single chip radios [8]. It consists of an input matching network, rectifying element, low-pass filter and regulator, and a switch and control circuit. This wireless switch is added between the antenna and the transceiver front-end, and will provide a power-up signal to turn on the whole system. A goal of this proposed method is to incorporate the wireless switch function into the μ Node utilizing as much of the infrastructure available in the single chip radio while not significantly degrading the performance of radio link.

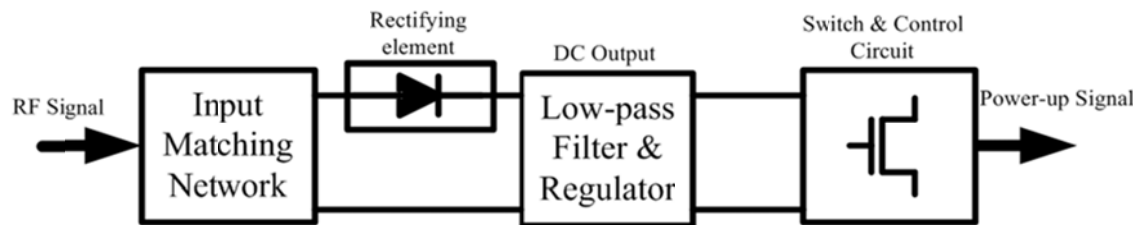


Figure 5: Concept for μ Node wireless activation switch

COMMUNICATION SUBSYSTEM OVERVIEW

A μ Node is a low data rate and low power communication system. Figure 6 shows a simplified μ Node transceiver block diagram. This new μ Node system utilizes only one antenna for both receiver and transmitter to reduce the overall chip area. The operating frequency of the system has been moved from 24 GHz down to 2.4 GHz so the communication range can be increased due to lower propagation loss at 2.4 GHz, and to lower power consumption. Furthermore, the 2.4 GHz band is high enough to allow integration of all the necessary components.

A wireless activation switch is added in this μ Node to allow turning the system on and off. When a μ Node chip is first assembled with a battery all on-chip circuits should by design be in an off state where even leakage current is suppressed. This allows the assembled device to be stored before deployment without draining the supply. Immediately prior to deployment an activation procedure should be performed where on-chip control circuitry receives power and takes command of the device. This wireless switch can power up the system using a strong RF signal from an external source such as that used in passive radio frequency identification (RFID) systems. This external RF power source can be placed very close to the node (~ 10 cm or less). The operating frequency of wireless switch is chosen to be 5.8 GHz (well separated from the

2.4 GHz carrier frequency) so the switch will not significantly degrade the performance of the main transceiver.

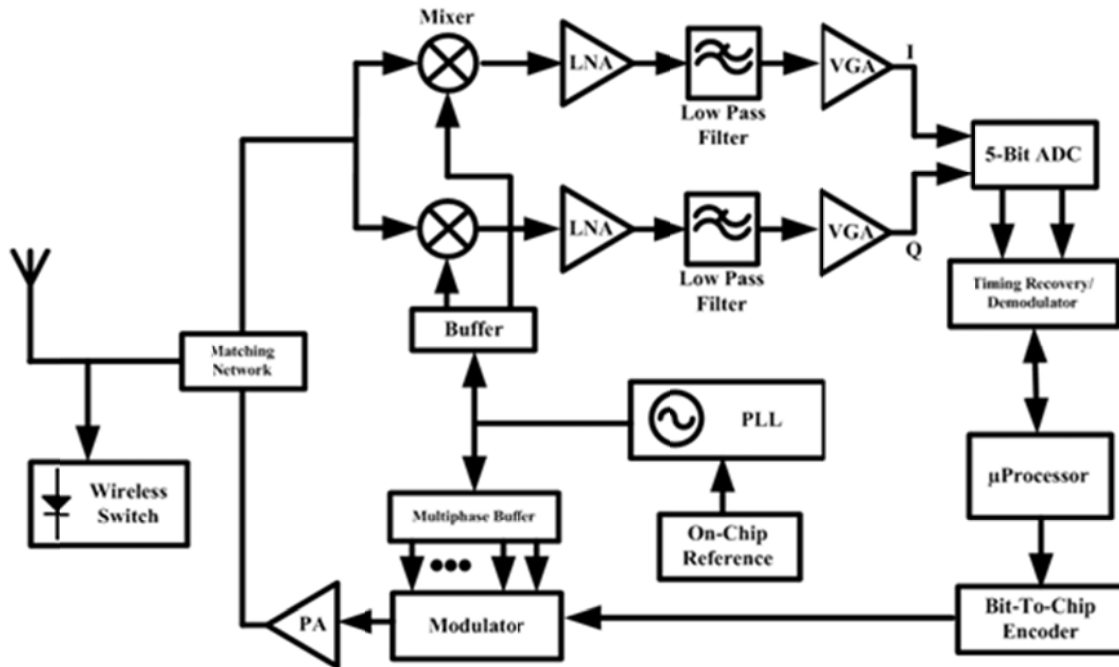


Figure 6: Simplified μ Node transceiver functional diagram

The receiver consists of a matching network followed by I&Q mixers and low noise amplifiers (LNAs). A passive receiver front-end configuration is employed in order to improve the linearity as well as to eliminate the power consumption of LNAs working at the RF frequency. The noise figure of this configuration tends to be higher than that of the traditional receiver. However, with careful design of the matching network, mixers and the buffer, the noise performance of this front-end can be maintained within an acceptable range. After passing through the LNAs, down-converted signals are filtered by low pass filters (LPFs), amplified again by the variable gain amplifiers (VGAs) and then fed through a baseband demodulator consisting of a 5-bit analog-to-digital converter (ADC), a timing recovery and demodulator, and a microprocessor. On the transmitter side, baseband I and Q signals modulate the 2.4 GHz carrier, implementing an MSK-like constant envelope phase-shift modulation [5]. The modulated signal is directly fed to a power amplifier followed by the matching network and an antenna to transmit the signal. Since a μ Node system does not require an ultra-stable crystal-based frequency reference, an on-chip frequency reference incorporated into a 2.4 GHz-frequency synthesizer provides the reference frequency. Although this on-chip reference tends to have poor phase noise and larger frequency offset, direct sequence spread spectrum (DSSS) differential chip detection can be

used to mitigate this problem as in the previous μ Node system [2]. Table 2-1 summarizes the link analyses for the 2.4-GHz and 24-GHz μ Node systems.

The communication range target for node-to-node communication at 2.4 GHz has been increased from 5 m to 20 m. Although, the free space path loss at 2.4 GHz is 100 times lower than that at 24 GHz, the performance of compact antennas such as on-chip monopoles and dipoles are significantly degraded. Hence, the communication range target is only ~ 4 times instead of 10 times longer as initially expected. However, this communication range is still sufficient for a wide variety of applications and the density of the nodes can be reduced as well as cost of the whole system. Power consumption is another concern for the μ Node system because μ Nodes need to be employed in remote areas without any power sources except a battery attached on each node. Lowering the operating frequency to 2.4 GHz reduces the power consumption and also increases the life time of the entire system.

Table 1: Link analyses summary for 2.4 GHz and 24 GHz μ Node systems.

Parameter	2.4 GHz μ Node	24 GHz μ Node [2], [3]
Operating Frequency	2.4-2.5 GHz	24 GHz
Architecture	Direct Conversion	Dual Conversion
Modulation	O-QPSK (MSK)	O-QPSK (MSK)
Coding	DSSS DCD	DSSS DCD
# of Channel	1	1
Range (N-to-N)	20 m	5 m
Antenna Pair Gain, G_a	-90 dB	-99 dB
TX output power	7 dBm	10 dBm
RX input power	-83 dBm	-89 dBm
Thermal Noise	-174 dBm/Hz	-174 dBm/Hz
Data Rate	100 kbps	100 kbps
E_b/N_o	18 dB	18 dB
RX Noise Figure	10 dB	10 dB
Sensitivity	-96 dBm	-96 dBm
Link Margin	13 dB	7 dB

ON-CHIP ANTENNA RESEARCH

An antenna is a key element in wireless communication systems. It converts electromagnetic waves into electrical currents and vice versa. The performance of antennas can be characterized by various parameters such as input impedance, antenna gain and radiation pattern. These parameters are related to each other, and normally depend on the physical dimensions and operating frequency as well. Typically, their physical size should be on the order of a wavelength, (i.e. half-wave for a dipole antenna, quarter-wave for a monopole

antenna over infinite ground plane). Thus, the size of antenna is dependent on its operating frequency. This indicates that, as the operating frequency is lowered, the antenna size should become larger. As can be seen in the Friis equation below, at lower operating frequencies a longer communication range can be achieved if the performance of the antennas can be kept the same as those at higher operating frequencies.

$$\frac{P_r}{P_t} = G_r G_t \left(\frac{\lambda}{4\pi R} \right)^2 = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} = G_a \quad (1)$$

When P_r , P_t , G_r and G_t are fixed, a longer wavelength will increase the communication range [3]. G_a is the antenna “pair gain” that can be measured by de-embedding the mismatch loss of the pair of antennas. Unfortunately, for a radio which requires a small form factor a large antenna is not suitable. Reducing the antenna size below the natural resonant length can dramatically degrade the antenna performance. Several approaches have been presented to minimize the antenna size especially at lower operating frequencies in [12]-[16]. Compact antenna design for low operating frequency is challenging. The previous effort for μ Node [1] showed that use of a 3-mm long on-chip antenna is possible at 20-24 GHz. This makes an M&M™ candy size feasible. However, for the new μ Node, due to its low operating frequency (target 5.2 or 2.4 GHz), use of an on-chip antenna becomes a challenge. Thus, more studies of on-chip antennas, especially at lower operating frequencies were necessary.

The antenna research reported here was focused on practical issues related to realization of small antennas that can perform adequately in a μ Node-battery assembly. Commercially available small off-chip ceramic antennas were examined briefly to define the critical issues for that technology option. On-chip antennas formed on a 20 ohm-cm silicon substrate were examined by design, fabrication and evaluation of sample devices. Linear and zigzag monopole geometries were treated. Performance at different frequencies and at different elevations above the ground plane was evaluated. A short range wireless communication formed by a pair of on-chip antennas located ~5 mm above ground in a grass field and a wireless link using an on-chip monopole antenna in a 5.2 GHz 802.11a WLAN were also demonstrated. Finally, other studies for increasing the effective length for on-chip antennas by utilizing dielectric coatings were performed.

OFF-CHIP MONOPOLE ANTENNAS

Numerous commercial antennas are available. However, most of them come in a size which is unsuitable for a small package. A ceramic chip antenna is popular due to its compact size and reasonable performance. This class of antenna is based on helix, meander or patch geometries covered by some dielectric materials such as low temperature co-fired ceramic (LTCC) which has a high dielectric constant and low loss [24]-[26]. Hence, electromagnetic waves traveling in this antenna experience shorter wavelength than that travelling in air. Figure 7 depicts the structure for a helix-based ceramic chip antenna. As mentioned above, this type of antenna looks promising for systems requiring a small package such as a μ Node.

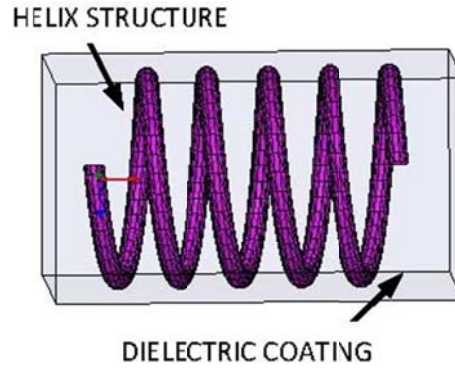


Figure 7: Helix based chip antenna

For chip antenna evaluation, a ceramic chip antenna, AN3216, from RainSun Company was chosen due to its very compact size ($\sim 3\text{mm}$). Figure 8 shows the physical dimensions of this antenna and the recommended PCB (printed circuit board) size from the manufacturer [27]. This PCB serves as a ground plane for the antenna. It is evident that the size of this chip antenna is small enough for the μNode package but, according to the datasheet, the size of the PCB or ground plane is too large to fit in the μNode package. To understand the effect of smaller ground plane, various sizes of PCBs were fabricated and tested with this antenna.

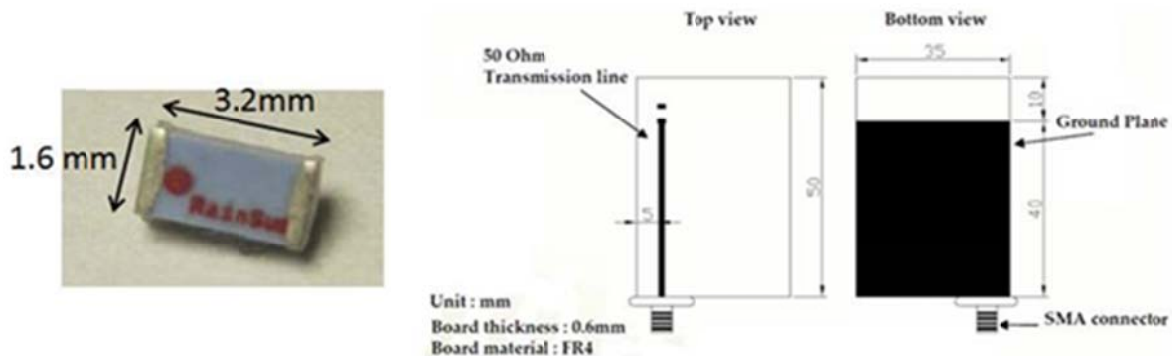


Figure 8: Ceramic chip antenna (AN3216) and recommended PCBs [27]

Figure 9 shows antennas with different ground sizes and associated measurement results for the return loss, $|S_{11}|$. The measured results show that the tuning frequency and $|S_{11}|$ for the chip antennas was sensitive to the size of ground plane. Therefore, in order to have a chip antenna working at 2.4 GHz as mentioned in the datasheet, it requires a large ground plane or a large PCB which is unsuitable for the μNode .

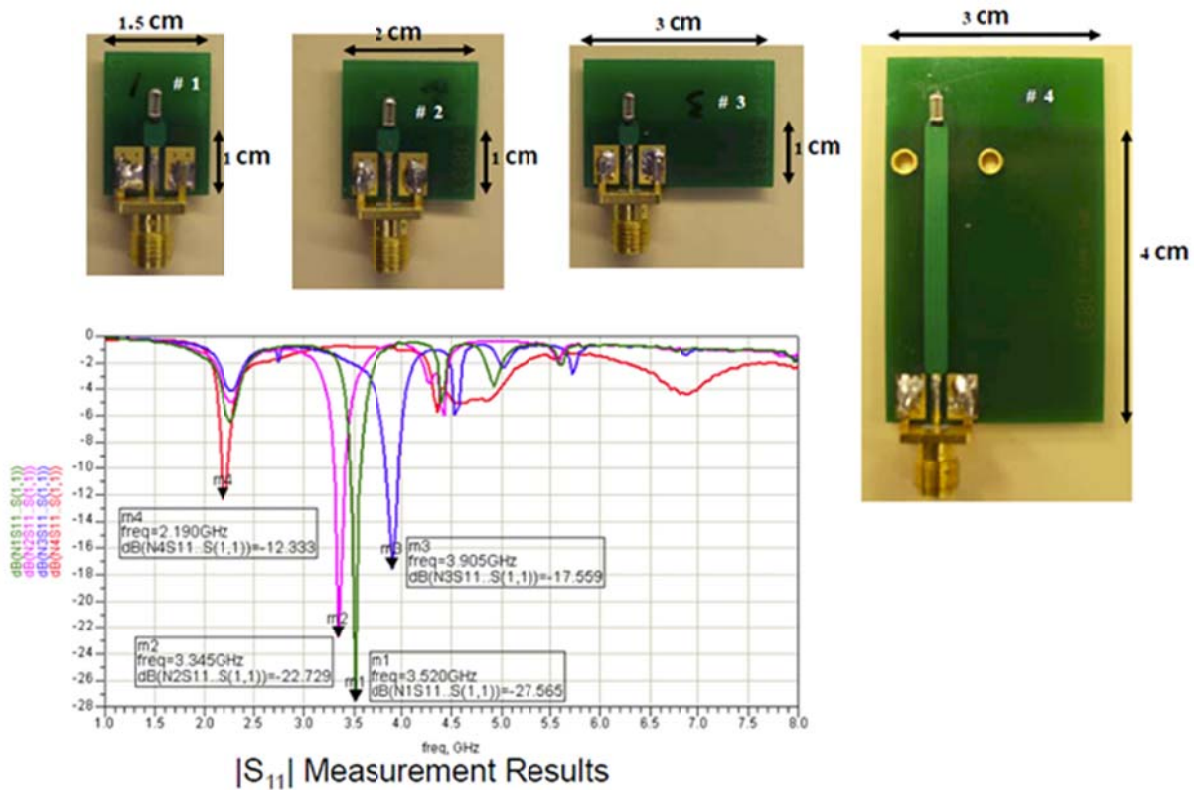


Figure 9: Chip antennas with different PCB sizes and return loss characteristic

More measurements were conducted to investigate the performance of these chip antennas. Figure 10 shows the antenna pair gain G_a measurement setup and the results. The antenna gain can be estimated from the measurements as also shown in this figure. Two samples of antennas with PCBs, (sample #1 and #4), are chosen to compare the two cases of ground sizes, 1.5 cm^2 and 12 cm^2 . The loss through setup is also measured and has been de-embedded. This data shows that the antenna pair gain G_a of these antennas is substantially lower than the calculated ideal case based on the antenna gain specified in the datasheet (antenna gain $\sim 0.5 \text{ dBi}$). Even though the size of a ceramic chip antenna is compact by itself, it still requires a large ground plane resulting in a large PCB to achieve good performance at the desired frequency. Therefore, it is difficult to incorporate ceramic chip antennas into the desired small package size.

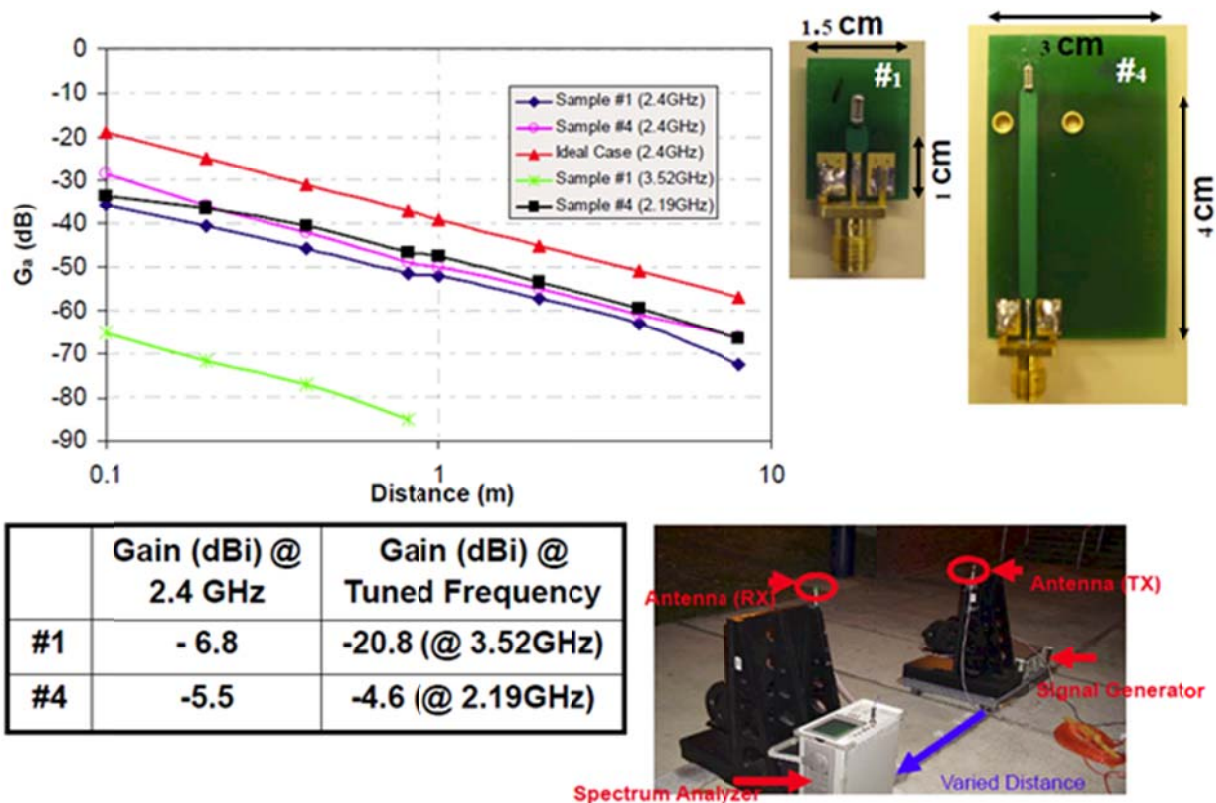


Figure 10: Antenna pair gain (G_a), measurement setup and results

ON-CHIP MONOPOLE ANTENNAS

The motivation for using on-chip monopole antennas in a standard CMOS process arises from high integration, simplicity and lower cost. The possibility of using on-chip monopole antennas operating at 5.8 GHz was previously demonstrated [3]. To investigate the feasibility at even lower frequencies, on-chip antenna test structures were fabricated and evaluated.

MONOPOLE TEST STRUCTURES

Figure 11 shows some antenna test structures. These antennas are based on the co-planar waveguide (CPW) feed micro-strip monopole [14] due to its compact ground size and simplicity. Figure 12 shows fabricated on-chip antenna test structures. These structures were fabricated with aluminum-copper (thickness = 3 μm , metal width = 30 μm) over 3- μm Tetra Ethyl Ortho Silicate (TEOS) and 20- $\Omega\text{-cm}$ silicon substrate (thickness = 670 μm). Note that the different structures were labeled Z1 through Z6 for zigzag antennas and L1 through L6 for linear antennas as identified in the figure.

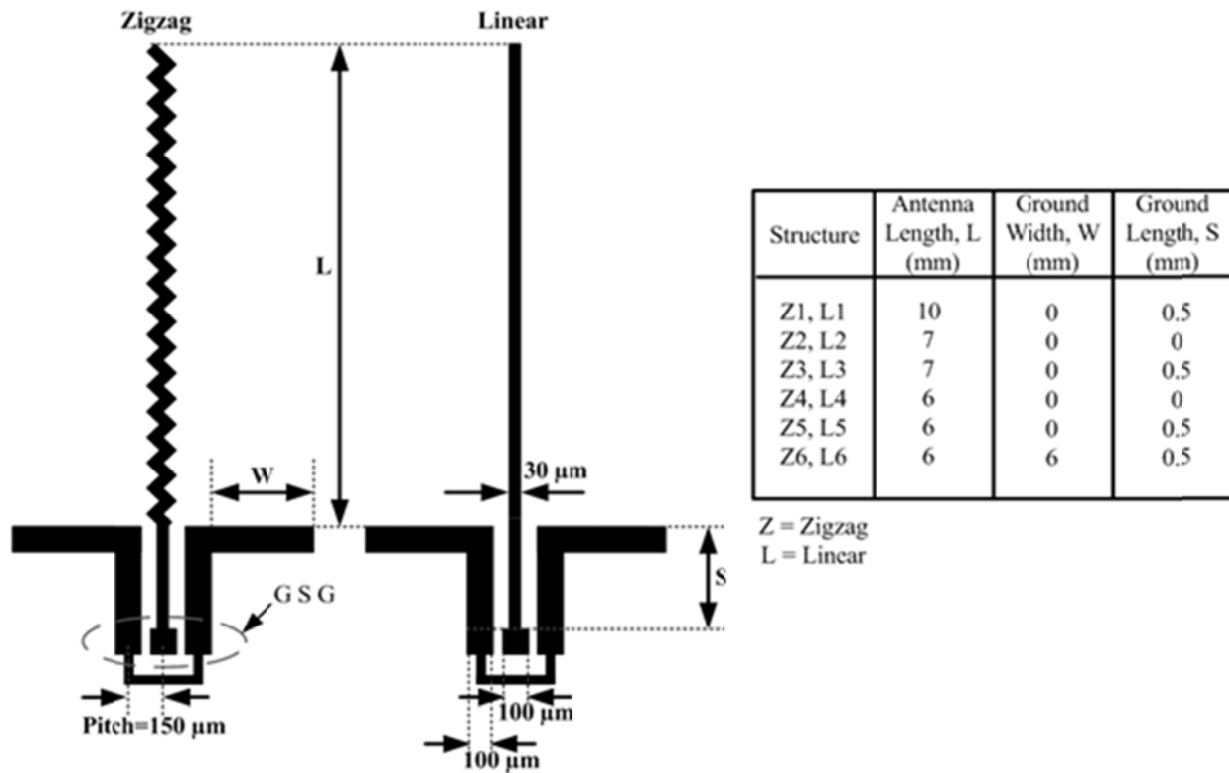


Figure 11: On-chip monopole test structures (Not to scale)



Figure 12: Fabricated antenna test structures

MONOPOLE CHARACTERISTICS

The input matching parameters or $|S_{11}|$ of the antennas were characterized. An on-chip antenna was mounted on a glass slide and placed on a mobile probe stand (Delrin plastic with $\epsilon_r \sim 3.7$). Figure 13 shows this measurement setup. The probe stand was equipped with a

Cascade MPH-F4 probe holder which was connected to a network analyzer using an SMA cable. The purpose of using this mobile probe stand for antenna $|S_{11}|$ measurement instead of a metal chuck inside the cage was to avoid reflections from the metal chuck.

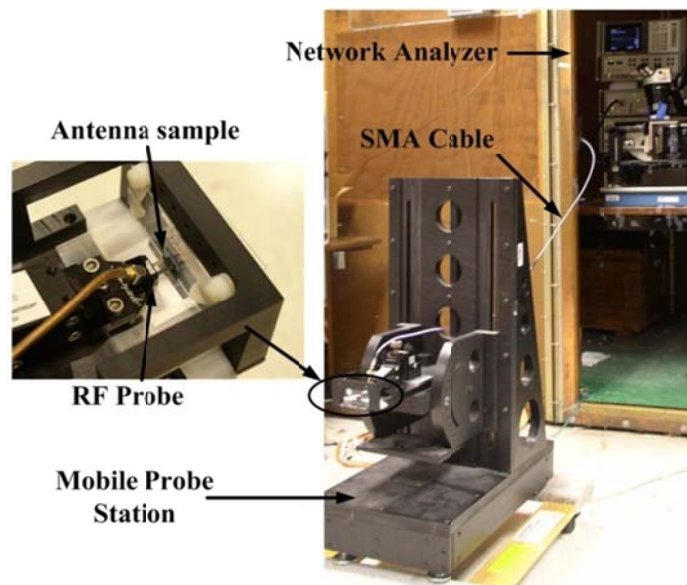


Figure 13: $|S_{11}|$ measurement setup for on-chip antennas

Figure 14 and Figure 15 show the $|S_{11}|$ measurement results for both linear and zigzag structures, respectively. Unlike ideal short monopoles, these antennas show reasonable input matching even at frequencies below ~ 2 GHz due to the losses from silicon substrate. Also, the zigzag-type antennas show better input matching than the linear-type antennas do because the zigzag line increases the antenna effective length resulting in lower resonant frequency [29]-[31]. Furthermore, antenna input matching can be improved by increasing antenna length (L), ground length (S) and ground width (W). This suggests that the input matching characteristic of the on-chip antennas can be tuned by modifying these three parameters as well as using a zigzag line instead of the linear line.

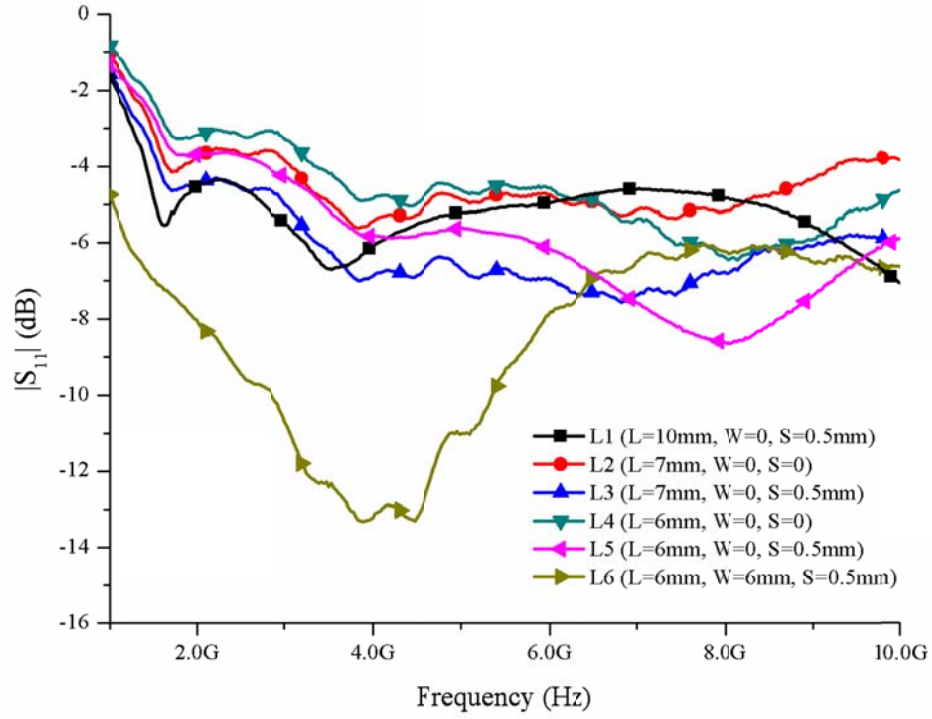


Figure 14: Measured $|S_{11}|$ for linear on-chip monopoles (height = 52 cm)

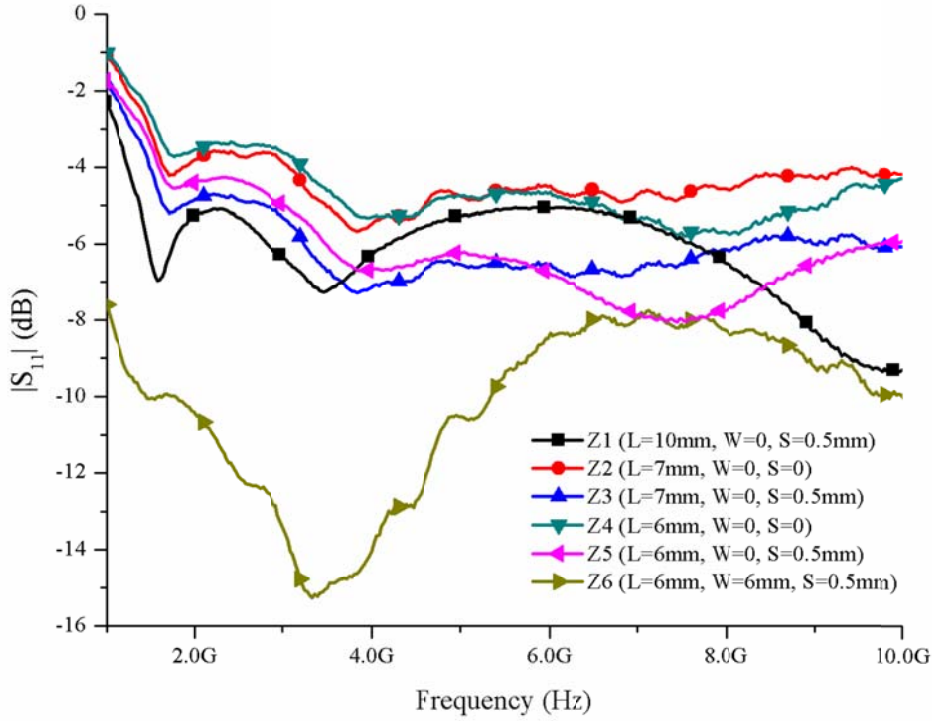


Figure 15: Measured $|S_{11}|$ for zigzag on-chip monopoles (height = 52 cm)

Figure 16 and Figure 17 plot the real part of antenna input impedance for a linear monopole and a zigzag monopole respectively. Figure 18 and Figure 19 plot the imaginary part of the antenna input impedance for a linear and zigzag monopole respectively. Due to the losses as mentioned above, these impedance values are in the range (~ 70 to $\sim 180 \Omega$ for the real part) which is possible to be matched by using matching networks at 2.4 GHz. Antennas with ground width ($W=6$) have better input matching but require larger area for the ground width portion.

Antenna pair gain G_a was characterized next. The G_a was calculated using equation (1). The measurement setup, which is similar to that for measuring chip antennas described in the previous section, is shown in Figure 20. In this setup, a pair of identical antennas was placed on both mobile probe stations with a height of ~ 52 cm above ground.

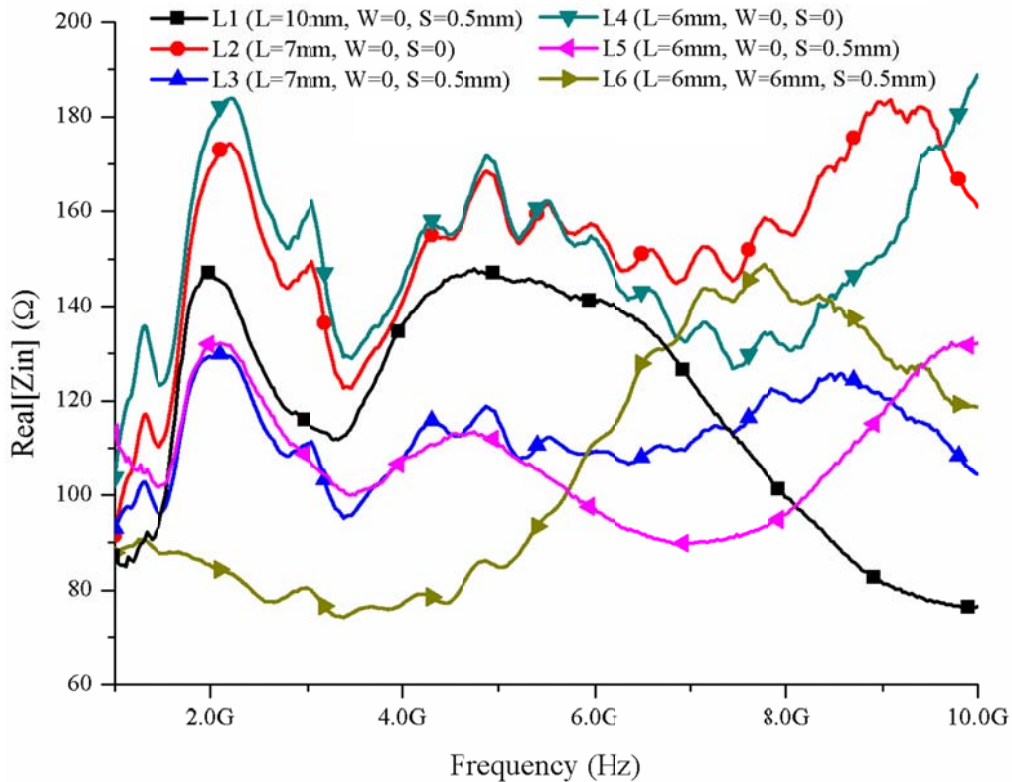


Figure 16: Measured linear antenna real part of input impedance

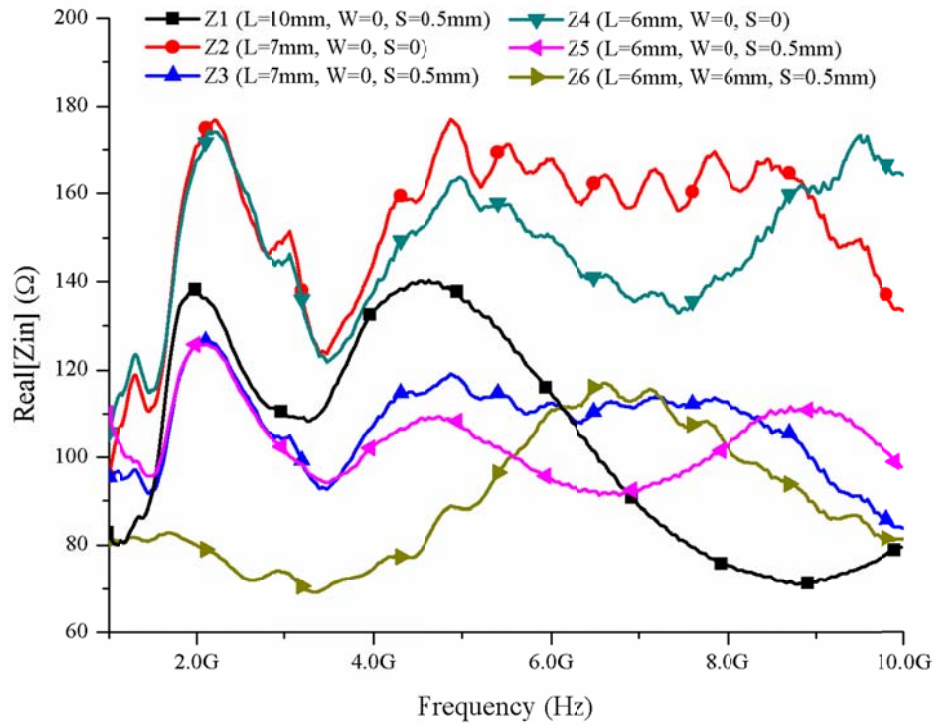


Figure 17: Measured zigzag antenna real part of input impedance

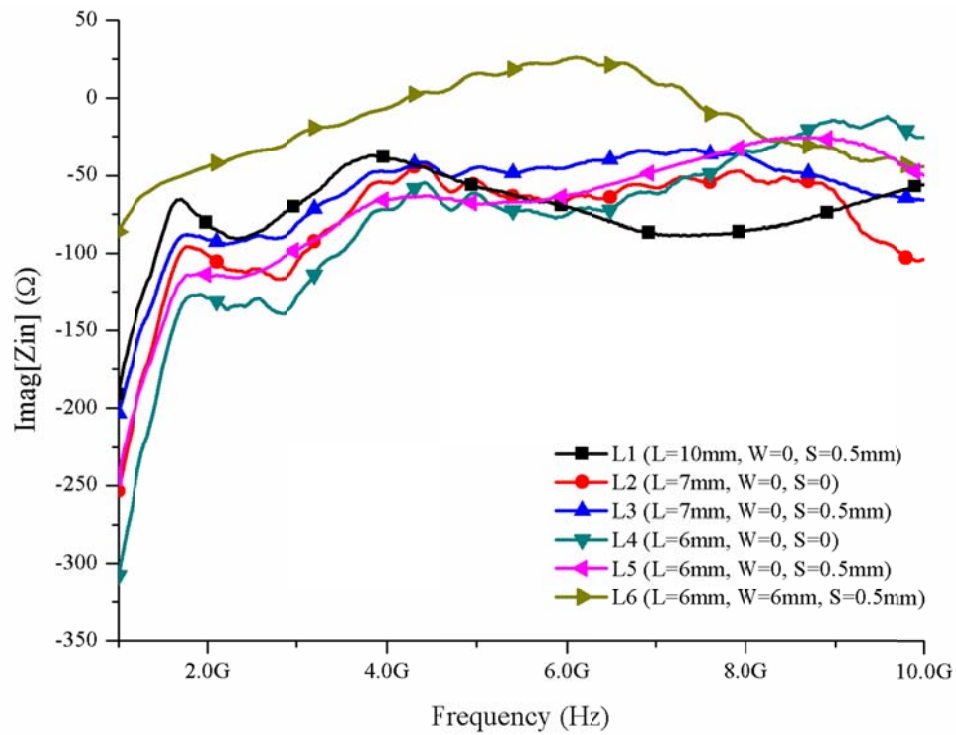


Figure 18: Measured linear antenna imaginary part of input impedance

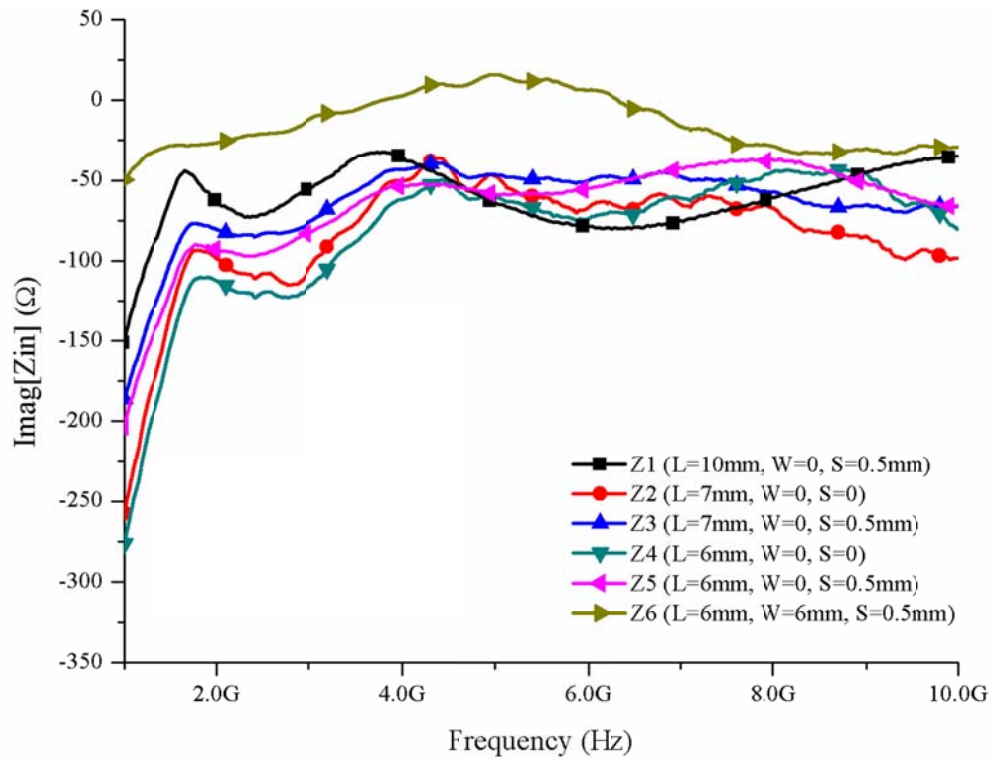


Figure 19: Measured zigzag antenna imaginary part of input impedance

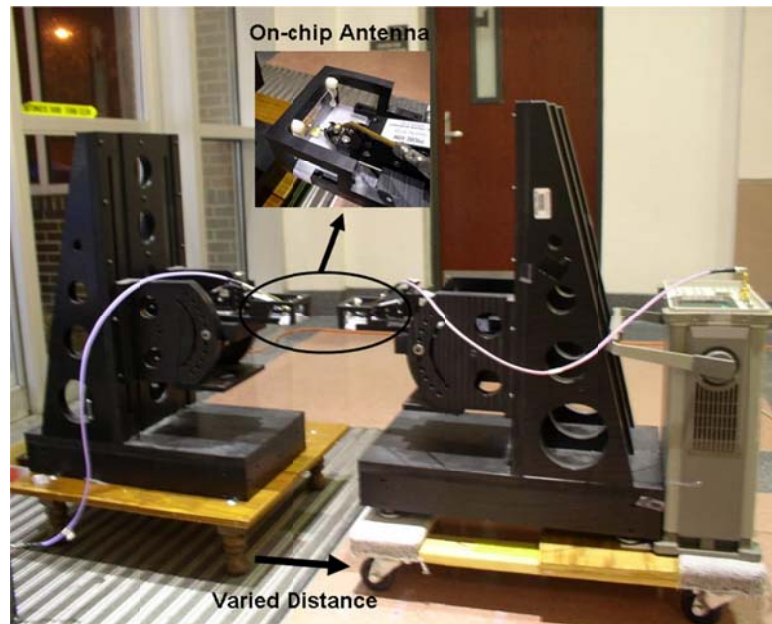


Figure 20: G_a measurement setup for on-chip antennas

The pair-gain for both linear and zigzag antennas was measured at 5.8 GHz. Figure 21 and Figure 22 show the G_a measurement results for linear and zigzag antennas. The theoretical value in the plots is the pair-gain for ideal (zero loss) half-wave dipoles (Gain = 2.15 dBi). Measurement results show that both linear and zigzag antennas with the same dimension have similar G_a 's. This means that G_a weakly depends on the type of antenna structure. Furthermore, G_a is weakly dependent on the ground length (S) and the ground width (W) of antennas [3] and only increases with the antenna length (L). Moreover, the G_a results at 5.8 GHz for the antenna with 6 mm length are consistent with previous antenna research [3], [32].

From the measurements and discussions above, G_a of the antennas weakly depend on the feeding structure of the antenna. Therefore, it is feasible to use the compact sleeve type on-chip antenna without an on-chip ground width (W=0). This can reduce the area of the chip for implementing on-chip antenna.

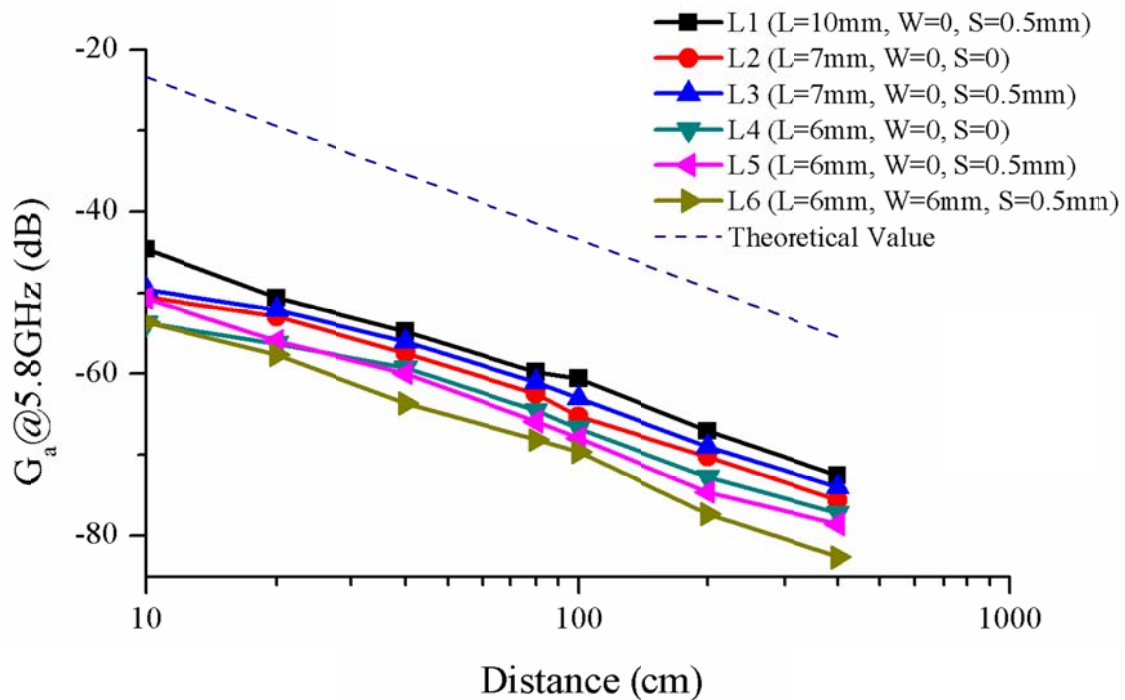


Figure 21: Measured linear antenna pair gain (G_a) at 5.8 GHz vs. distance (height ~52 cm)

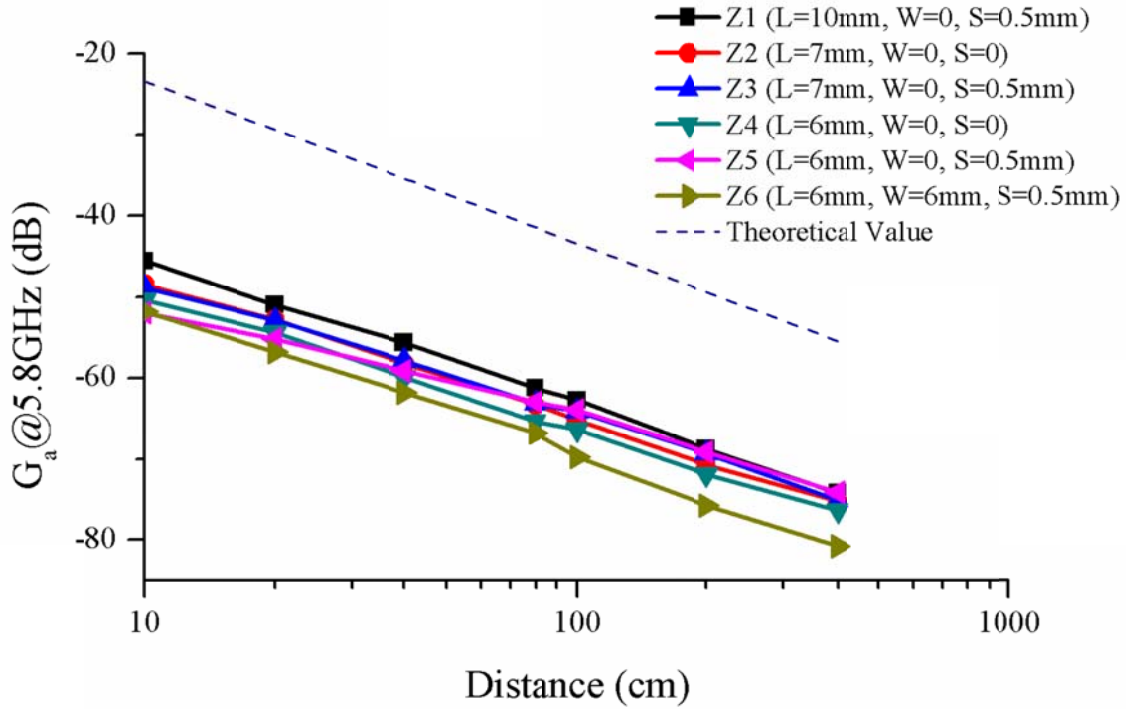


Figure 22: Measured zigzag antenna pair gain (G_a) at 5.8 GHz vs. distance (height ~52 cm)

To characterize antenna G_a at lower operating frequencies, test structures with maximum and minimum antenna length (L1 (L=10mm, W=0, S=0.5mm), L5 (L=6mm, W=0, S=0.5mm) for linear structures and Z1 (L=10mm, W=0, S=0.5mm), Z5 (L=6mm, W=0, S=0.5mm) for zigzag structures) were used. Figure 23 and Figure 24 show the pair-gain at six different frequencies (0.9, 1.4, 1.8, 2.4, 5.2 and 5.8 GHz) for linear and zigzag antennas, respectively. Measurement results show that the antenna G_a 's do not monotonically decrease as the operating frequency goes lower. More specifically, antenna G_a at 2.4 GHz slightly degrades compared to that at 5.2 and 5.8 GHz but, at 1.8 and 1.4 GHz, the G_a improves and eventually degrades again at 0.9 GHz. This is believed to be because the antenna gain does not monotonically decrease like the path loss does. Therefore, at certain frequencies, the path loss over-compensates the antenna gain degradation resulting improvement of the antenna pair gain, G_a .

As mentioned before, the antenna G_a 's for both linear and zigzag antennas are similar. Furthermore, the G_a curves have some deviation from the Friis equation, especially at 0.9 GHz (G_a should decrease by 6 dB when distance increases by a factor of 2). This is due to the multi-path reflection from the environment surrounding the antennas. Compared to the measurements using chip antennas with PCB size of $1.5 \times 1.5 \text{ cm}^2$, G_a of antenna Z5 at 2.4 GHz is ~15 dB lower.

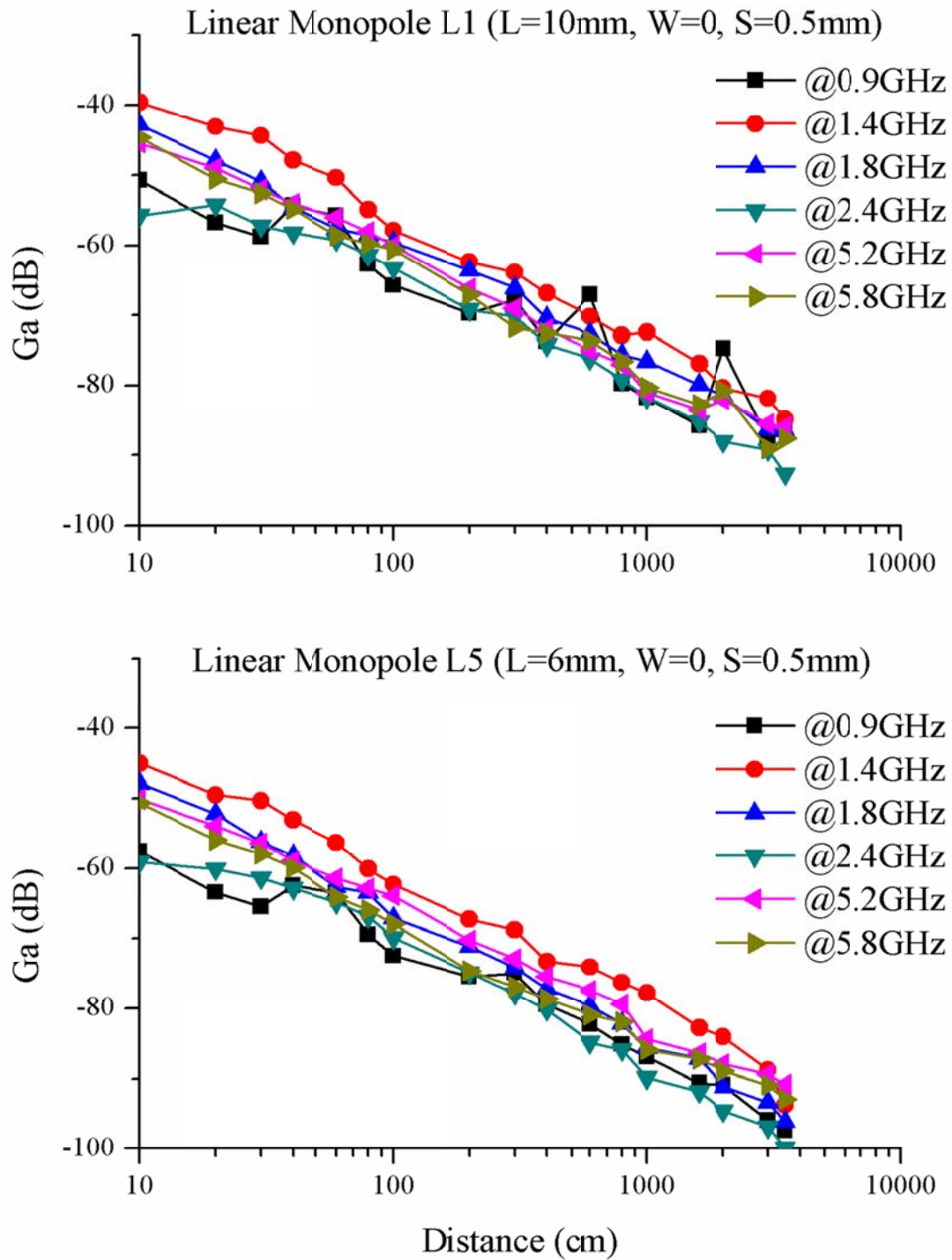


Figure 23: Measured antenna pair gain (G_a) vs. distance for linear-type antennas (height = 52 cm)

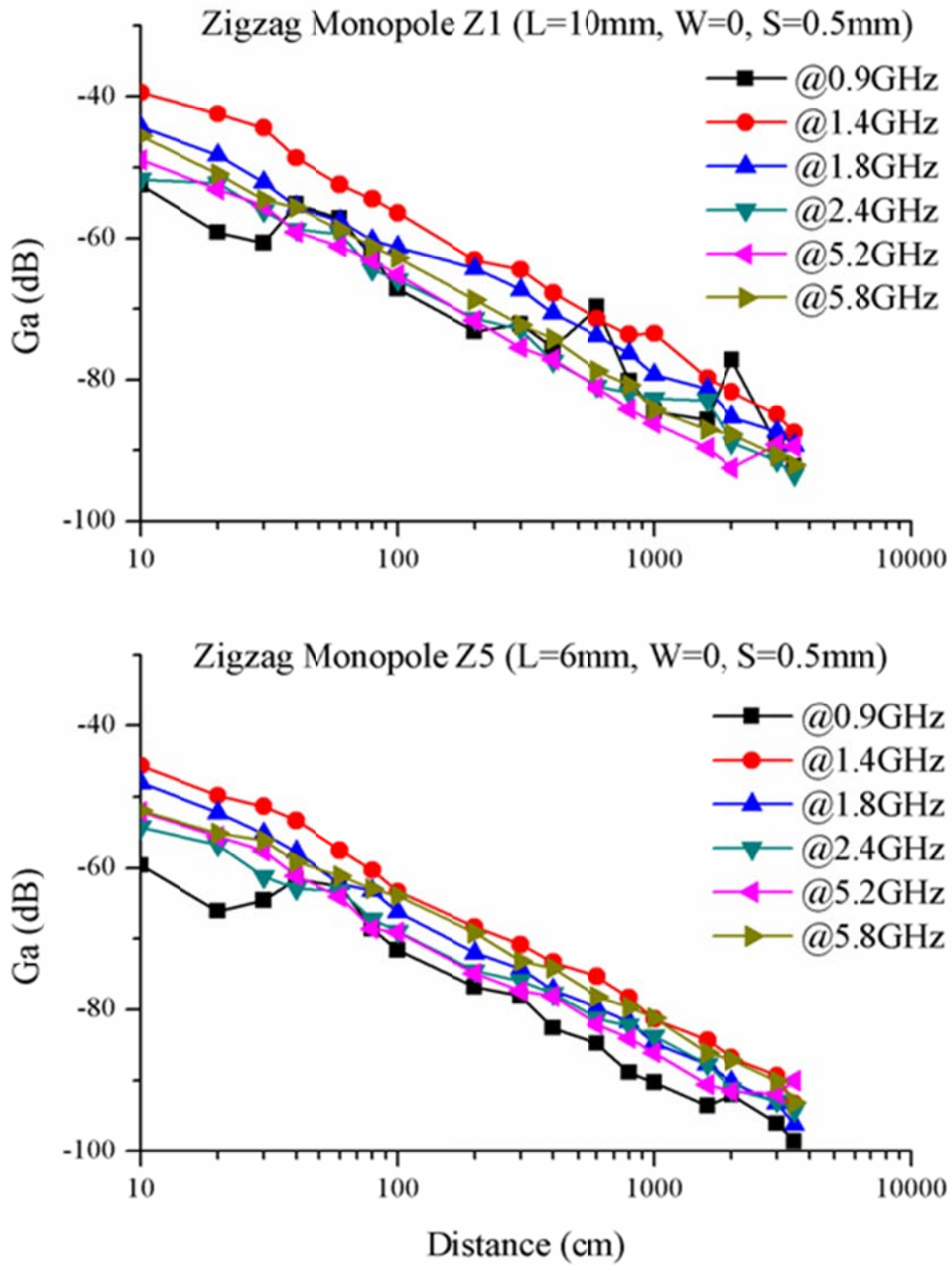


Figure 24: Measured antenna pair gain (G_a) vs. distance for zigzag-type antennas (height = 52 cm)

The radiation pattern of the antennas is shown in Figure 25 for 5.8 and 2.4 GHz. The chuck of the measurement setup is replaced with two pieces of glass slides glued together at $\sim 90^\circ$ degrees for mounting the on-chip antenna. In the receiver side, commercial patch antennas (5.8 and 2.4 GHz) are used to rotate around the transmitter in a half circle. The normalized radiation patterns are calculated and plotted. The radiation patterns at 5.8 GHz are similar to the theoretical monopole pattern. However, at 2.4 GHz, the patterns are slightly asymmetrical. This may be due to the fact that the wavelength at 2.4 GHz is longer than that at 5.8 GHz, and the multi-path reflections from the asymmetrical structure of the probe holder.

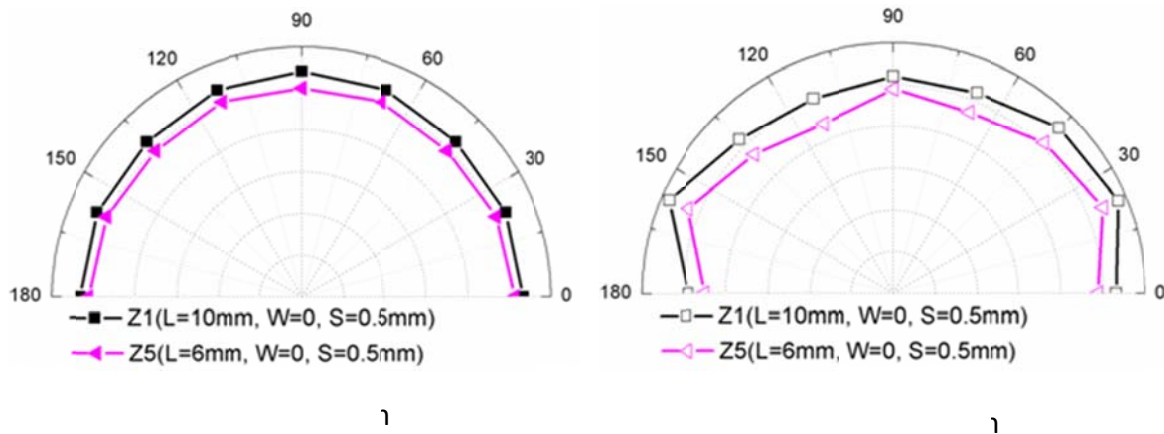


Figure 25: Measured radiation patterns of structure Z1 and Z5

In some use scenarios, μ Nodes can be placed close to ground, therefore G_a near ground is of great interest. Figure 26 shows the measurement setup. Antennas are located at about 5 mm from ground by placing small PCBs underneath. Small pieces of PCBs represent the situation when the μ Node chip sits on a 1-mm thick battery. The measurement results at 5.8, 5.2 and 2.4 GHz are shown in Figure 27, Figure 28 and Figure 29 respectively.

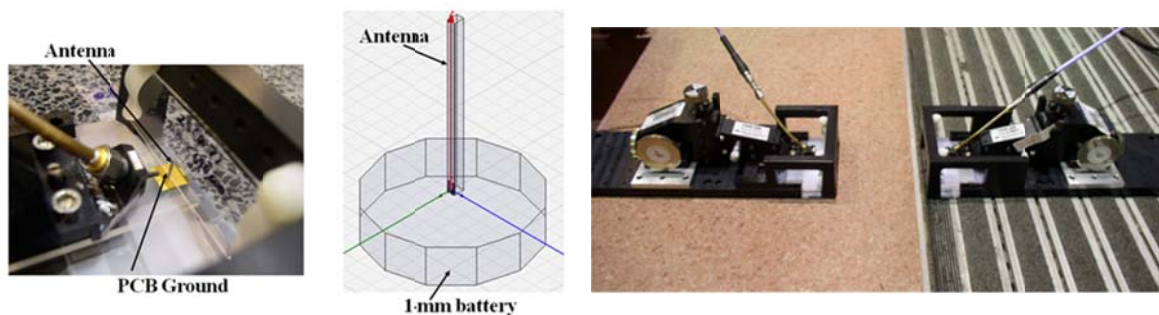


Figure 26: G_a measurement setup with antennas placed about 5 mm from ground

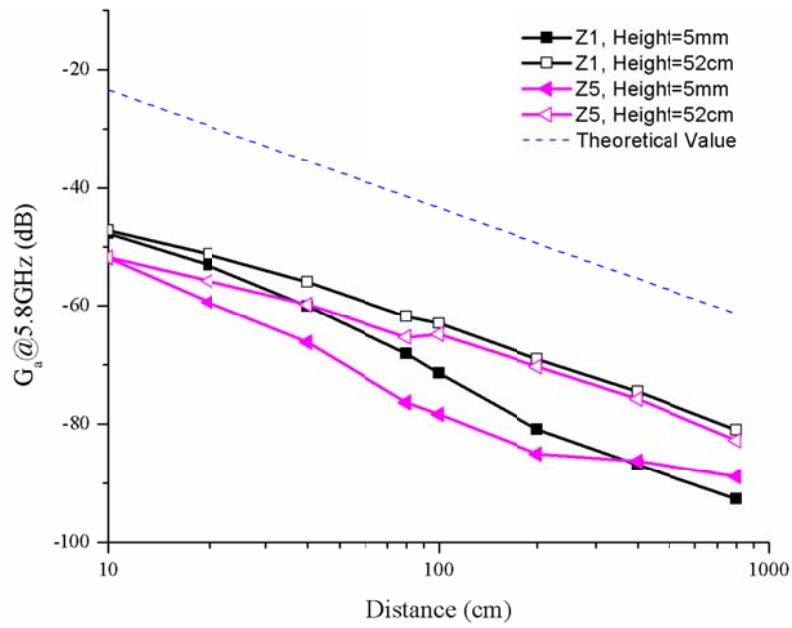


Figure 27: Measured G_a at 5.8 GHz vs. distance for antennas Z1 and Z5 (with PCB, height = 52 cm and 5 mm)

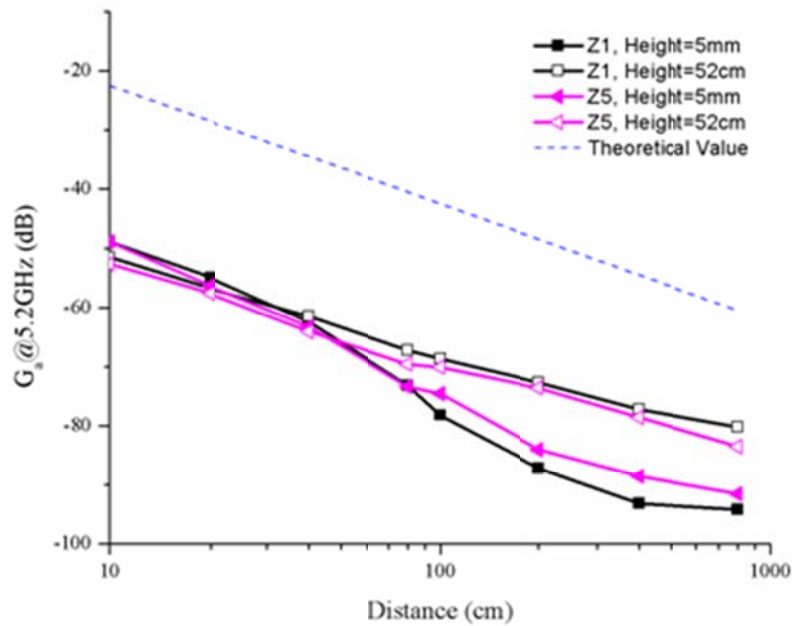


Figure 28: Measured G_a at 5.2GHz vs. distance for antennas Z1 and Z5 (with PCB, height = 52 cm and 5 mm)

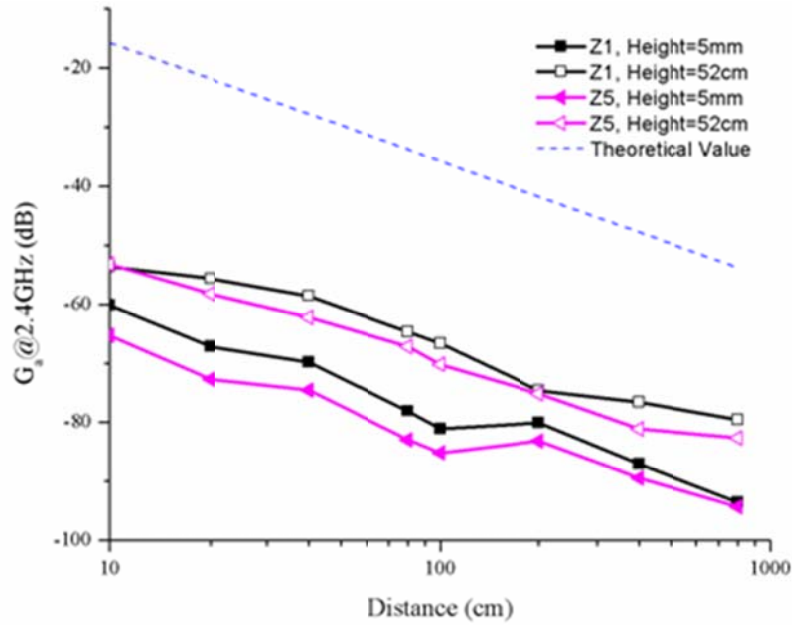


Figure 29: Measured G_a at 2.4 GHz vs. distance for antennas Z1 and Z5 (with PCB, height = 52 cm and 5 mm)

The results show that G_a decreases when antennas are placed close to the ground due to reflections from ground. Furthermore, compared to the antennas without a PCB at 52 cm height from ground in previous section, the G_a of the antenna is not strongly dependent on the small floating PCB ground underneath the antennas. According to these measurements, assuming that the target sensitivity is ~ -90 dBm, it is possible to form a 2.4 GHz wireless communication link using a pair of Z5 type antennas at distances of ~ 6 m and ~ 25 m with the heights of ~ 5 mm and ~ 52 cm above ground, respectively. This is sufficient for short range wireless communication.

ON-CHIP MONOPOLE ANTENNA DEMONSTRATION

Two on-chip antennas (antenna structure Z5) were placed ~ 5 mm above ground in a grass field separated 6 m from each other as shown in Figure 30. A 0-dBm single tone signal was transmitted by the on-chip antenna and was picked up by the other antenna at the receiver side. This demonstration was repeated at three different frequencies: 5.8, 5.2 and 2.4 GHz. Figure 31 shows that the received power level was ~ -106 , ~ -105 and ~ -103 dBm at 5.8, 5.2 and 2.4 GHz, respectively. When 10 dBm or higher is transmitted the received power is greater than -96 dBm. This is sufficient to form a communication link. This demonstration confirmed that short range communications (~ 6 m node to node) using on-chip antennas positioned close to the ground are feasible.



Figure 30: Short range communication demonstration set-up

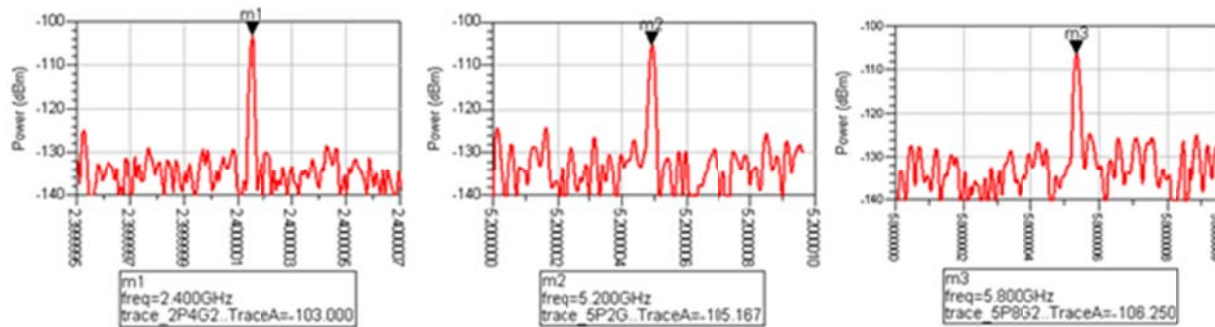


Figure 31: Received power level for signal at 2.4, 5.2 and 5.8GHz, respectively

The on-chip antennas were also used as part of an 802.11a WLAN (wireless local area network). The setup is shown in Figure 32. At the transmitter, the 802.11a wireless router is connected to an on-chip antenna through a 3.5-mm cable and an RF GSG probe, while the second antenna port is terminated with 50-Ω. The on-chip antenna used in this demonstration was a zigzag-line antenna with 6 mm ground width on each side (antenna structure Z6). This transmitter was located on the second floor of a building and wireless signal was transmitted at 5.3 GHz (Channel 60). At the receiver, the 802.11a Super Range card bus from Ubiquiti Networks, Inc. equipped with a 5 dBi commercial antenna was connected with a laptop. The receiver was located outside the building in the parking area and ~100 m away from the transmitter. To verify this wireless link, the network name (SSID) was setup on the wireless router. Using software installed on the laptop, the strength of the wireless signal was checked. Figure 33 shows the results displayed on the laptop. This confirmed that the receiver picked up the signal transmitted by the wireless router through an on-chip antenna. Even though the on-chip antenna is small, this clearly demonstrates its usefulness for wireless communication at 5.3 GHz.

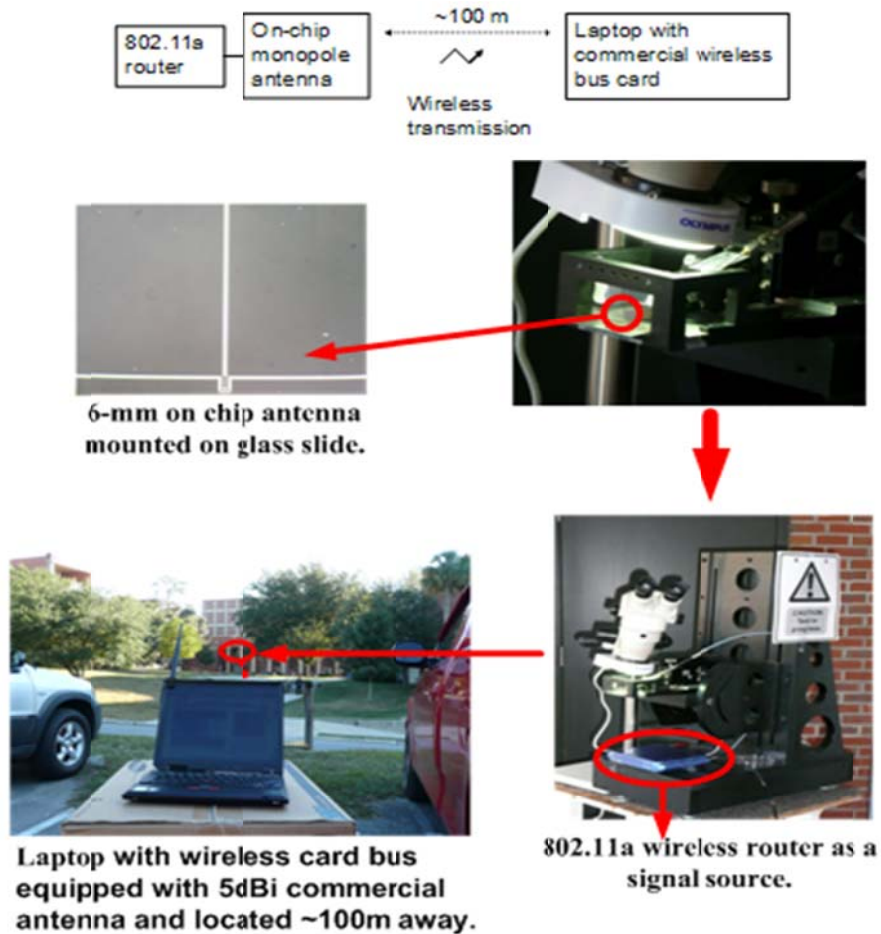


Figure 32: Demonstration setup for long range communication with an on-chip antenna

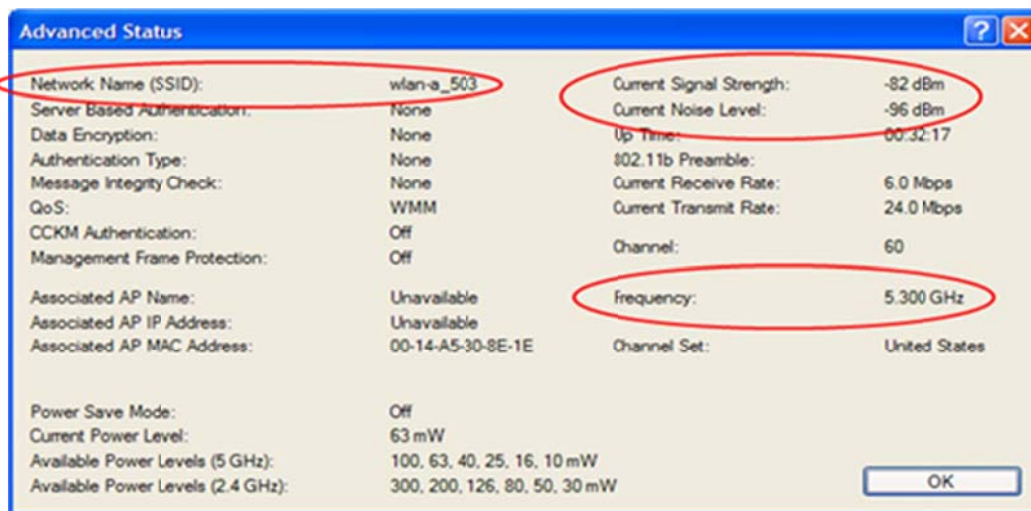


Figure 33: Characterization of received signal displayed on the laptop

ANTENNA WITH DIELECTRIC COATINGS

From the measurement results reported above, although a pair of on-chip antennas operating at 2.4 GHz can form a wireless communication link for ~20 m with the height of 52 cm and ~6 m with the height of ~5 mm above ground, it is important to investigate and study approaches which can improve the on-chip antenna performance. From system level studies, an antenna with a gain of ~-2 dBi, a real value for the input impedance of ~10 Ω or higher and compact size is desirable for the envisioned μ Node type systems.

This subsection presents several approaches to improve the antenna performance for a compact antenna such as an on-chip antenna. The 3-D full-wave electromagnetic field simulation, HFSSTM from Ansoft was used as the primary antenna modeling tool in this study.

One important aspect of the feasibility of an on-chip antenna is the relative size of the antenna compared to the associated wavelength. Obviously, it is desirable that the electrical wavelength of the antenna be comparable to the wavelength (half or quarter wavelength) so the natural resonances can be exploited.

The wavelength λ of an electromagnetic wave traveling in free space is simply $\lambda_0 = c/f$ where c is the speed of light and f is the wave frequency. It is possible to adjust the wavelength by covering the antenna with a high dielectric constant (ϵ_r) material so that the effective wavelength becomes $\lambda_{eff} = \lambda_0 / \sqrt{\epsilon_r}$. This fundamental concept will be considered as a starting approach throughout this antenna study.

ON-CHIP ANTENNA WITH SINGLE LAYER DIELECTRIC COATING

The characteristics of on-chip antennas were investigated for specific geometric configurations and specific on-chip antenna structures. The μ Node marble configuration with the approximate size of an M&MTM candy was taken as the desired geometry. Figure 34 points out the critical elements within the marble that will be considered.

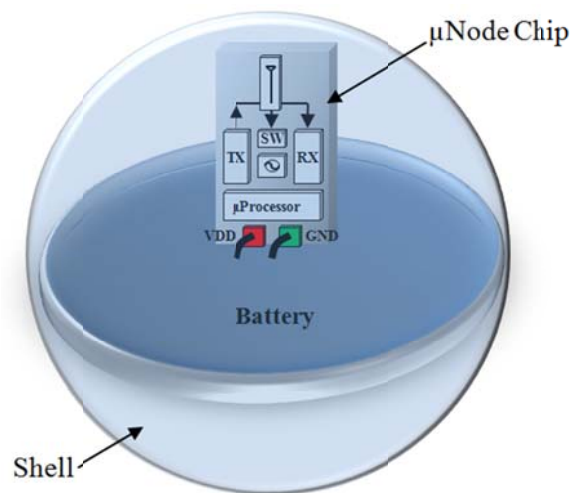


Figure 34: μ Node Marble assembly

A series of simulations were constructed assuming a specific length for the metal antenna, and an antenna location perpendicular to a metal cylindrical shape representing a battery. Encapsulation materials will cover the antenna as well as fill the internal portion of the shell. The model structure includes (1) a battery (230 μm thickness and 1 cm diameter), (2) a linear monopole on-chip antenna (formed using 30 μm wide metal on a 20 $\Omega\text{-cm}$ silicon substrate 10 μm thick), and (3) an encapsulation material with a dielectric constant greater than 1. The metal thickness for the antenna structure is 3 μm as well as the thickness of the silicon dioxide. Figure 35 shows the structure details used in these simulations. Table 2 summarizes the simulated performance of the antenna test structures for their gain and input impedance at 5.2 and 2.4 GHz. The effect of introducing an air gap under the metal line using silicon etching was also investigated.

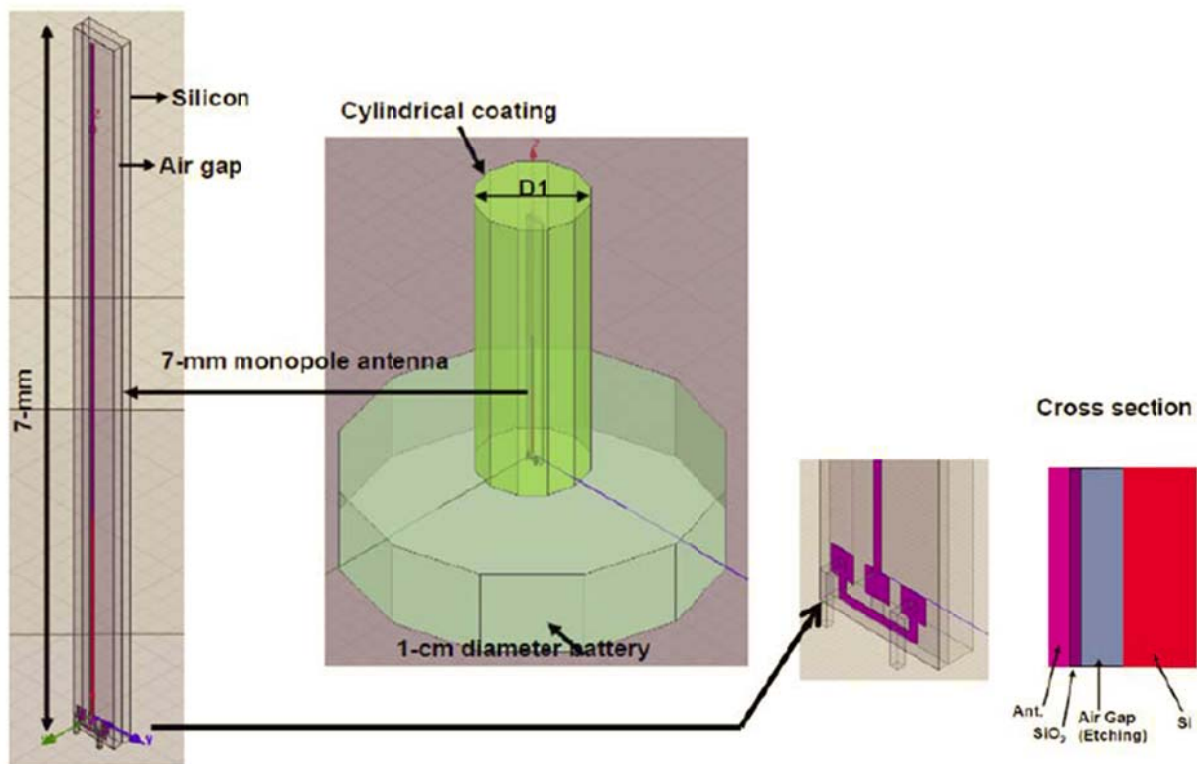


Figure 35: An on-chip antenna with a single-layer dielectric coating

Table 2: On-chip antennas with single-layer dielectric coating simulation results

Structure	Metal	Antenna	Air Gap (μm)	Si Thickness (μm)	Encapsulation $\epsilon_r=4, H=8\text{mm}$	Gain (dBi)		Impedance (Ω)	
						2.4GHz	5.2GHz	2.4GHz	5.2GHz
1	PEC	Length=7mm Metal Width=30 μm Metal Thickness=3 μm	None	None	None	1.3	1.9	0.8-j811	4.9-j320
2	Al					-1	1.1	1.4-j800	6-j320
3	PEC					-1.6	1.7	0.9-j228	5.4-j32
4	Al					-17.9	-3.8	40.7-j158	22.3-j15
5	Al		100	100 (20- $\Omega\text{-cm}$)	D1=2mm	-9.6	0.2	8.4-j330	7.9-j96
6	Al				D1=6mm	-8.1	-0.1	4.3-j223	6.9-j55

Structure #1 was intended to establish an idealized baseline for the small antenna without any losses. The metal trace was specified to have zero resistivity (i.e. perfect electrical conducting (PEC) metal), and was hanging unsupported in free space (i.e. no air gap under the metal and no silicon substrate). The idealized antenna showed adequate gain but low input impedance at both frequencies

Structure #2 introduced a realistic metal (aluminum) into the model configuration. As a result the gain degraded and the real portion of the impedance increased. The introduction of metal losses reduces the gain down to +1.1 and -1 dBi for 5.2 and 2.4 GHz, respectively, while the real portion of the impedance increases to 6 and 1.4 Ω for 5.2 and 2.4 GHz, respectively.

Structure #3 introduced an encapsulating material into the ideal structure #1 configuration. This 5 mm diameter cylinder of FR-4 (relative dielectric constant assumed to be 4) is expected to alter the effective wavelength thus changing any resonance effects, and to introduce losses in the material. The free space quarter wavelength at 5.2 GHz is ~ 14.4 mm. In a material of $\epsilon_r=4$ the effective quarter wavelength should approach 7.2 mm. The simulation results showed a gain of +1.7 dBi with an input impedance of $5.4-j32 \Omega$ and -1.6 dBi gain and $0.9-j288 \Omega$ at 5.2 and 2.4 GHz, respectively. The encapsulation material losses degraded the gain and increased the real portion of the impedance at both operating frequencies.

Structure #4 was the first realistic configuration. Here aluminum metal, a silicon substrate and a coating material were included. The diameter of the coating cylinder was reduced to 3 mm from the 5 mm used in structure #3, so the results are not directly comparable. Simulation results are -3.8 dBi with $22.3-j15 \Omega$ and -17.9 dBi with $40.7-j158 \Omega$ for 5.2 and 2.4 GHz, respectively. This was lower gain than desired, especially at 2.4 GHz, but still a usable value that could readily be improved.

Structure #5 introduced a silicon etching or air gap underneath the antenna in order to reduce silicon losses. It also used a 2 mm diameter coating. The air gap improved the gain for both operating frequencies (increased to +0.2 and -9.6 dBi for 2.4 and 5.8 GHz, respectively). It also altered the input impedance to $7.9-j96 \Omega$ (5.2 GHz) and $8.4-j330 \Omega$ (2.4 GHz). The performance of the antenna for 2.4 GHz is far below the -2dBi design target. However, for 5.2 GHz, this combination meets the μ Node target of > -2 dBi and real portion of the input impedance of about 10 Ω .

Structure #6 repeated the conditions of structure #5 with an increase of the coating cylinder diameter from 2 mm to 6 mm. This change reduced the gain by 0.3 dB to -0.1 dBi at 5.2 GHz but it improved the gain by 1.5 dB to -8.1 dBi at 2.4 GHz. The input impedance was altered to $6.9-j55 \Omega$ and $4.3-j223 \Omega$ at 5.2 and 2.4 GHz, respectively. These simulation exercises for fixed antenna length with single layer coatings demonstrated the complex interplay between antenna gain and input impedance when measures are taken to reduce losses. Etching out the silicon substrate under the antenna improves gain but degrades the input impedance for matching purposes. The simulation results did confirm that a small simple monopole on-chip antenna can be made to work at 5.2 GHz in a μ Node marble type configuration.

ON-CHIP ANTENNA WITH DOUBLE LAYER DIELECTRIC COATING

The simulation results from previous subsection show that the antenna performance at 2.4 GHz is far below the design target. This indicates that measures beyond the single coating with an air gap are required to achieve the desired performance. One alternative option is the use of a double-layer encapsulation in order to alter the antenna effective length.

A series of four models were constructed to examine the potential for double layer coatings as a method to achieve acceptable operation at 2.4 GHz. Figure 36 shows the structural details of the models. The concept was to use a first coating that has a high dielectric constant combined with a second coating that represented typical packaging encapsulants. The second layer also acts as an impedance transformer designed to maximize transmission and minimize reflections at the interfaces.

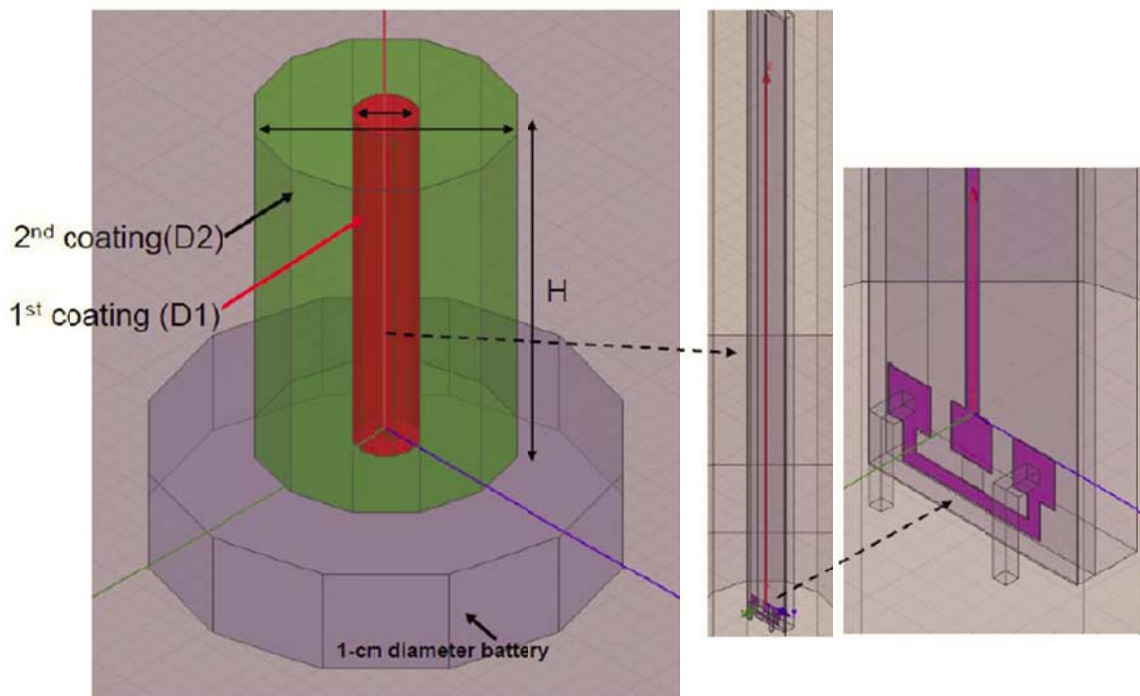


Figure 36: On-chip antenna with a double-layer dielectric coating.

The structure is almost the same as that for the previous case except that the first coating cylinder was a material with permittivity of 10 and diameter of 2.4 mm. The permittivity for second coating cylinder was 4 and the diameter was 7.8 mm. Table 3 presents the simulation results at 2.4 GHz only.

Table 3: On-chip antennas with double-layer dielectric coating simulation results.

Structure	Metal	Antenna	Air Gap (μm)	Si Thickness (μm)	Encapsulation 1 $\epsilon_r=10$	Encapsulation 2 $\epsilon_r=4$	Gain (dBi)	Impedance (Ω)
1	PEC	Length=7mm	None	None	D1=2.4mm	D2=7.8mm, H=10mm	0.1	0.5-j97
2	Cu		100	100			-6	2.2-j133
3	PEC	Length=10mm	None	None		D2=7.8mm, H=11.5mm	0.3	1.1-j67
4	Cu		100	100			-3.5	2.8-j94

Structure #1 shows the gain and impedance achievable for a 7 mm long antenna without metal and silicon substrate losses. The gain of 0.1 dBi is acceptable, but the $0.5-j97 \Omega$ impedance is difficult to match. As shown in structure #2, including metal and silicon losses deteriorates the gain down to -6 dBi and increases the impedance to $2.2-j133 \Omega$. Note that the double coating is effective in raising the gain versus the gain achievable with one coating (i.e. -6 dBi double coating versus -8.1 and -9.6 dBi for single coatings). Structures #3 and #4 examine the impact of increasing the antenna length to 10 mm. The height of the coatings has to be increased to 11.5 mm to accommodate the larger antenna. The idealized structure #3 shows a 0.3 dBi gain, and $1.1-j67 \Omega$ impedance. Structure #4 which includes metal and silicon losses shows a gain of -3.5 dBi and impedance of $2.8-j94 \Omega$. These four models confirmed that performance at 2.4 GHz could be improved by using a double coating approach, but the desired target gain of >-2 dBi was not achieved for the permittivity levels investigated. Before concluding the investigation of double layer coating potential it was decided to examine the option of using a higher permittivity first coating and modification of the second level coating to represent the spherical shape of the μNode marble. Figure 37 shows the structure and Table 4 summarizes the data.

This brief exercise showed a gain of -7.1 dBi at 2.4 GHz. Since this gain was slightly lower than the simpler lower dielectric ϵ_r (10 versus 50) of structure #2, this line of investigation was terminated in favor of more promising approaches.

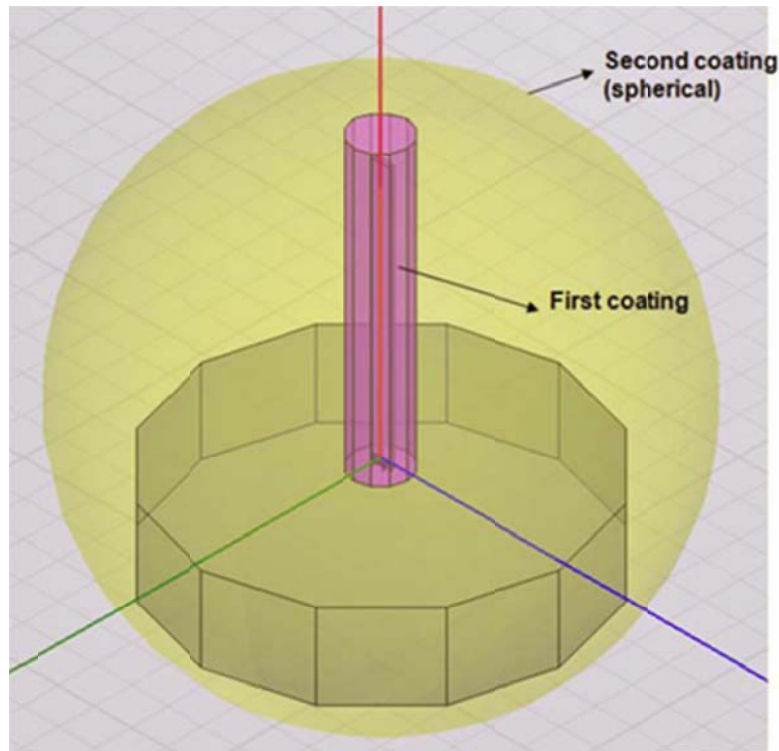


Figure 37: On-chip antenna with a spherical coating

Table 4: On-chip antennas with spherical coating simulation results

Structure	Metal	Antenna	Air Gap (μm)	Si Thickness (μm)	Encapsulation 1 $\epsilon_r=50$, Cylinder D1=2.4mm	Encapsulation 2 $\epsilon_r=2$, Sphere D2=14mm	Gain (dBi)	Impedance (Ω)
1	Cu	Length=7mm	40	100			-7.1	2.2-j133

ON-CHIP ANTENNA WITH INDUCTIVE AND CAPACITIVE LOADING

Figure 38 shows two antenna structures with inductive loading. Both antennas have the same physical length, and both are loaded on the end with an inductive coil. The body of one antenna is a straight metal line, and the other antenna employs a meander-line shape. These antennas are also covered by a single-layer dielectric coating. Table 5 shows the simulation results for these antennas at 2.4 GHz. These devices exhibit performance slightly better than the previously modeled single coating 7 mm antennas.

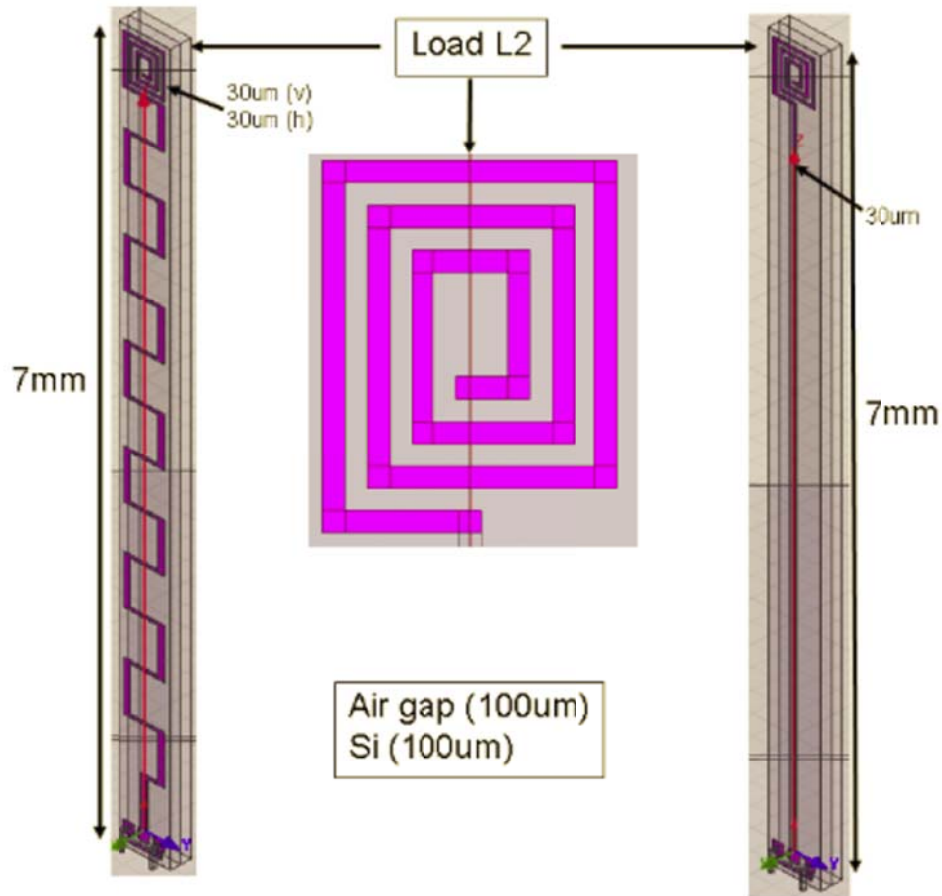


Figure 38: On-chip antennas with inductive loading.

Table 5: On-chip antennas with inductive loading simulation results

Structure	Metal Al (3μm)	Antenna	Air Gap (μm)	Si Thickness (μm)	Encapsulation 1 $\epsilon_r=4$, Cylinder	Gain (dBi)	Impedance
1	Meander	Length=7mm,	100	100	D1=2.4mm, H=8mm	-7.5	4.6-j197
2	Linear	Metal Width=30μm		20-Ω-cm		-7.7	4.8-j260

Another approach is to load the antenna with both capacitive and inductive elements. This structure of antenna is also called a "slow-wave structure". Figure 39 shows the slow-wave antenna.

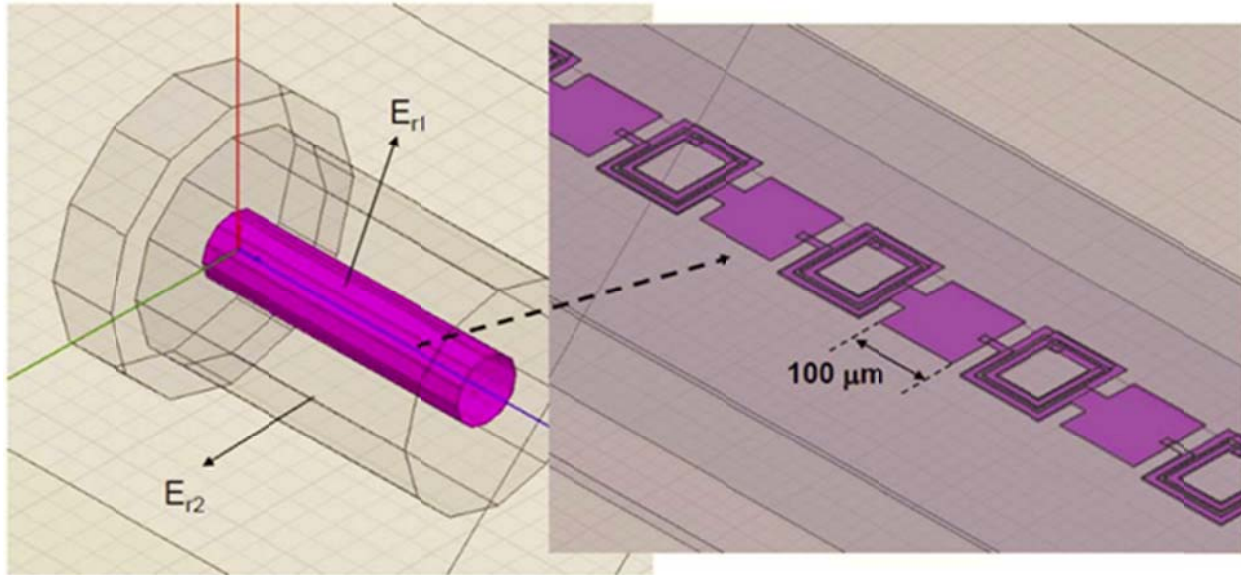


Figure 39: On-chip antennas with inductive and capacitive loading

The slow-wave antenna consists of inductive loops for the top layer and capacitive patches for the bottom layers. This provides inductive and capacitive loading for the antenna. A ground shield is included underneath the signal pad. Table 6 presents simulation results at 2.4 GHz for some slow-wave antennas and some slow-wave antennas connected with linear antennas (for increasing the antenna length). The slow-wave structures give higher input impedance but antenna gain is lower. This is because most of the impedance comes from various losses (from silicon substrate, dielectric, antenna material and etc.).

Table 6: On-chip antennas with inductive and capacitive loading simulation results

Structure	Metal, Thickness	Antenna	Air Gap (μm)	Si Thickness (μm)	Encapsulation 1 $\epsilon_r=10$	Encapsulation 2 $\epsilon_r=4$	Gain (dBi)	Impedance (Ω)
1	Cu, 2μm	6mm slow wave	100	100	D1=2.4mm	D2=7.8mm, H=10mm	-18.26	170+j194
2	Al, 1μm	6mm slow wave				D2=7.8mm, H=11.5mm	-16.01	191-j424
3	PEC, 2μm	+			None	None	-16.14	14.2-j294.5
4	PEC, 1μm	4mm linear			D1=2.4mm	D2=7.8mm, H=11.5mm	-6.31	9.9+j189.9

ANTENNA RESEARCH SUMMARY

In portion of the research the characteristics of on-chip antennas in μ Node systems at lower operating frequencies such as 5.2, 2.4, 1.8, 1.4 and 0.9 GHz was demonstrated. Using simple monopole on-chip antennas, it is possible to form 2.4 GHz wireless communication links at distances up to ~ 6 m and ~ 25 m with the heights of ~ 5 mm and 52 cm above ground, respectively. The demonstration using a monopole in an 802.11a WLAN showed that the on-chip monopole also useful for longer range wireless communication (~ 100 m). Although the performance of a simple on-chip antenna is not as good as that of chip antennas, its size is

more compact and it does not require a large ground plane. Finally, it is practical to match the input impedance of on-chip antennas at 2.4 GHz using integrated matching networks.

More complex on-chip antenna structures were also investigated. Simulation models were prepared that examined several schemes of dielectric coating, inductive loading and capacitive loading. For the single-layer dielectric coating, the antenna can meet the design target for μ Node operating at 5.2 GHz (>-2 dBi gain and about $10\ \Omega$ for the real part of the input impedance). However, for the antenna to operate at lower frequencies such as 2.4 GHz, its performance is still far below the desired target even with the several techniques employed. More studies and investigations to improve the on-chip antenna performance at 2.4 GHz are required.

WIRELESS WAKE-UP (ACTIVATION) CIRCUIT

The μ Node system requires post fabrication calibration [7]. This implies an ability to turn the battery power on and off to store the system settings before and after calibration. Making the battery connection using a mechanically activated switch is not a practical solution because it conflicts with objective of achieving a small form factor for the assembly. A reasonable solution is to incorporate a wireless switch. Several approaches have been reported for wake-up receivers [34]-[36]. For this particular application, a passive RFID (Radio Frequency Identification) architecture was chosen for no standby power consumption. To keep the chip area and system size overheads small, the wireless switch function should share as much of the infrastructure for the main receiver, while not significantly affecting its performance. This research devised an approach for integrating a wireless switch into a single chip radio. It included a circuit that protects against RF signals with amplitude higher than the normal operation range.

WIRELESS CIRCUIT ARCHITECTURE

Figure 40 shows the architecture of a μ Node system that includes a wireless activation mechanism. The wireless switch and main transceiver share the same antenna to reduce the system overhead. Energy to perform the wake-up activation function is coupled into the antenna and directly to wireless switch functional block. The switch is placed in between the antenna and main transceiver since no signal is available to turn on the T/R (Transmit/Receive) switch and main transceiver for TDD (Time Division Duplex) operation before the power-up operation is completed. The wireless switch must be designed to avoid loading the input of the transceiver in such a manner that the antenna and transceiver become mismatched.

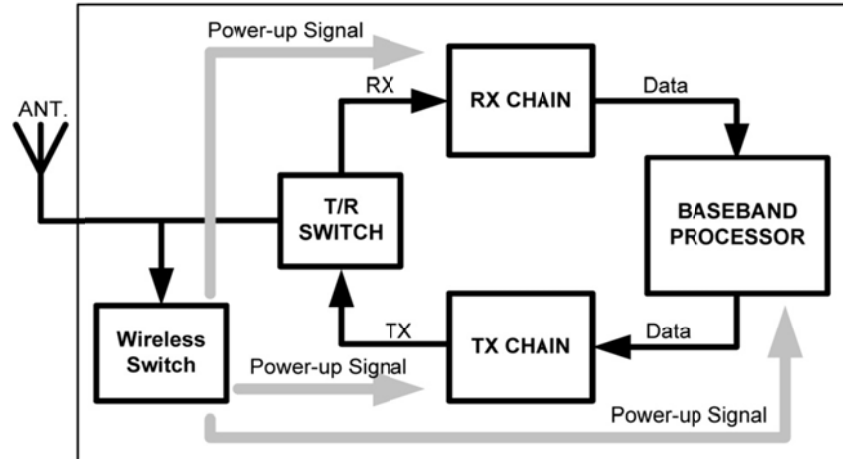


Figure 40: Architecture of μ Node system used to evaluate the impact of wireless switch

A way to mitigate this problem is to make the wireless switch and the radio operate at two different frequencies while utilizing an antenna that can operate at both frequency bands. More specifically, the operating frequency of 5.8 GHz was chosen for the wireless switch and 2.4 GHz for the transceiver. Several dual-band antennas have already been reported [37]-[40]. These antennas provide excellent performance, i.e. gain >0dBi for both frequency bands as well as being compact. The impedance looking into the switch should be high at 2.4 GHz, while the impedance looking into the main transceiver should be high at 5.8 GHz in order to reduce the impact on each other.

Figure 41 shows a simplified schematic of the wireless switch. It is similar to that of a passive transponder in an RFID system. This subsystem consists of a matching network, an RF clamp, an RF-to-DC converter, a limiter, a power-on-reset circuit (POR), an envelope detector, a comparator with control logic, and a power switch to connect the battery. The comparator/control logic and the power switch were not treated in this work. The wireless switch receives energy through the antenna and converts the sinusoid wave to DC using an RF-to-DC converter. An envelope detector was used to recover the coded signal for authentication of the power-up signal [43]. The comparator/control logic provides a power-up signal for the power switch to connect the battery to the transceiver. The power switch includes a latch that holds its on-state after receiving the power-up signal. This means once the main transceiver is turned on, the power-up signal is no longer needed. For turning the transceiver off, the 2.4 GHz radio link is used.

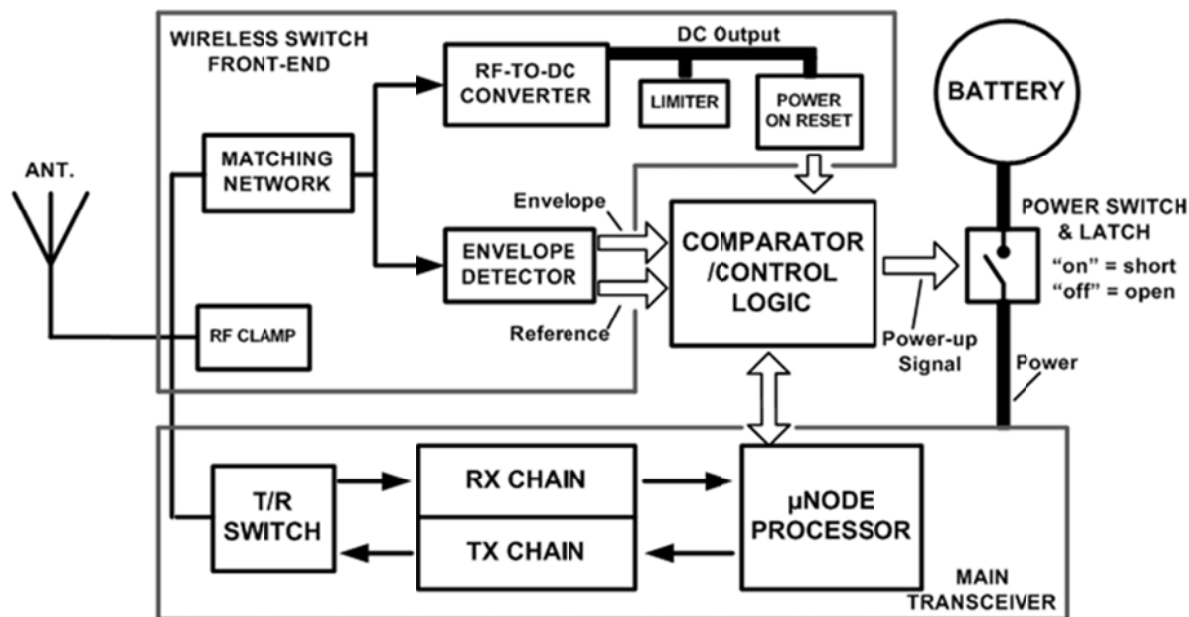


Figure 41: Schematic for wireless switch for μ Node system

To evaluate the performance of the wireless switch as well as its impact on the transceiver performance, the wireless switch was integrated with a T/R switch. By evaluating the performance of T/R switch with and without the wireless switch, the expected impact of wireless switch on the transceiver was estimated. As a matter of fact, if the receiver, transmitter and antenna are all matched to $50\ \Omega$ at 2.4 GHz, the insertion loss degradation of a T/R switch after integrating a wireless switch will be exactly the gain and noise figure degradation of the receiver and the output power degradation of the transmitter. This approach removed the need for a full transceiver model and greatly simplified the task of quantifying the impact of wireless switch.

OPERATING MODES

The RF power source for activation can be placed close to the μ Node chip so propagation loss is not an important concern, and a high frequency can be used. Distances between the source antenna and the μ Node antenna can be assumed to be less than 10 cm. Therefore, using an operating frequency of 5.8 GHz which has higher propagation loss than the 2.4 GHz transceiver frequency is a practical choice.

The operation modes (power-up (PUx) and transceiver (TRx) modes) for a matching network of wireless switch are shown in Figure 42. In PUx mode (Figure 42(a)), the main transceiver is turned off, thus its input impedance looking at the input of the T/R switch, is high. The matching network of the wireless switch is designed so that its input impedance is $50\ \Omega$ at 5.8 GHz. Therefore, essentially all the available power of the RF power-up signal at 5.8 GHz picked up by the antenna is delivered to the wireless switch circuit.

In TRx mode as shown in Figure 42(b), the transceiver is turned on and the RF signal frequency is 2.4 GHz. The input impedance of the wireless switch is close to open at 2.4 GHz. Therefore, only a small amount of RF power at 2.4 GHz is diverted to the wireless switch. This ensures that the wireless switch is not powered up by the signal at 2.4 GHz and, the loading effect introduced by the switch is reduced.

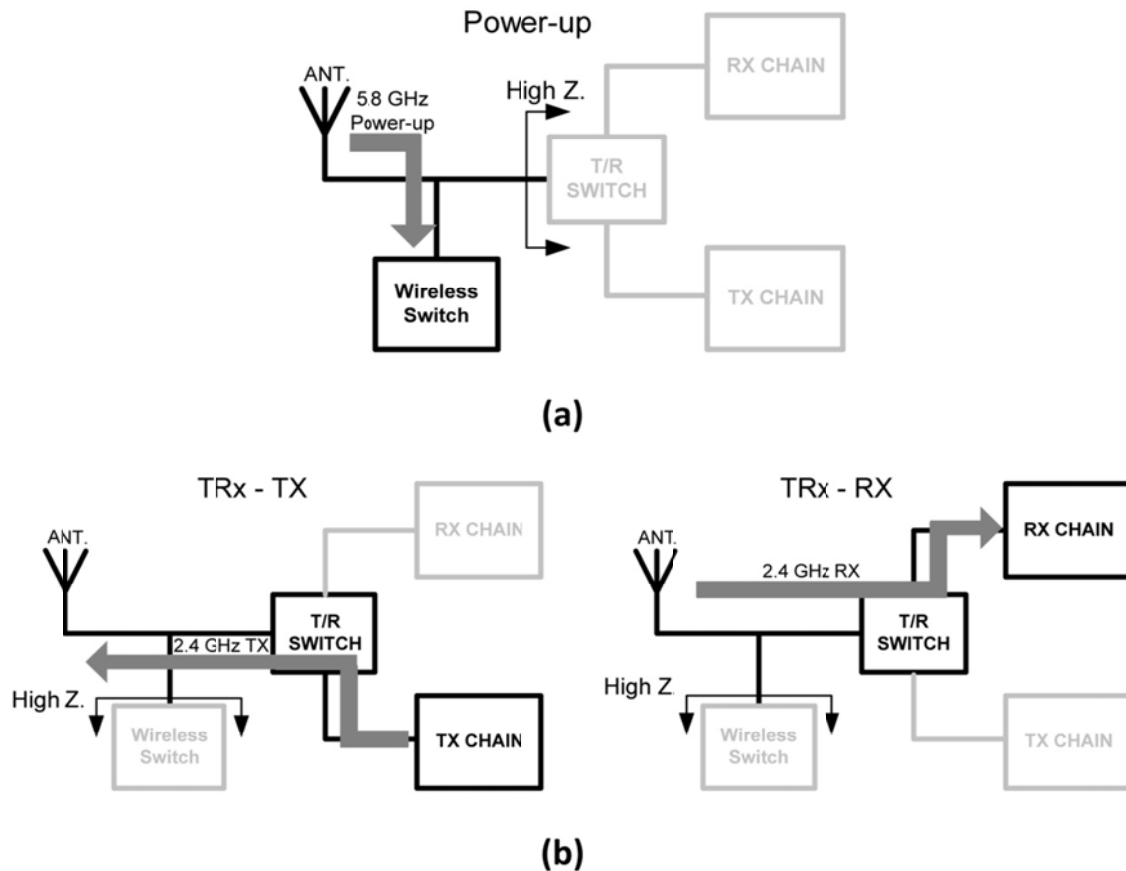


Figure 42: (a) Power-up (PUx) mode. (b) Transceiver (TRx) Modes

CIRCUIT BLOCK DESIGNS

In this section, the designs for the wireless switch front-end including an RF-to-DC converter, a matching network, an envelope detector, protection circuits, a power-on-reset circuit and T/R switch for evaluation of the impact of wireless switch to the transceiver performance are described.

RF TO DC CONVERTER

The DC power of wireless switch circuit is generated from the incident RF signal by an RF-to-DC converter or voltage multiplier [41]-[48]. Figure 43 shows the RF-to-DC converter integrated with the input matching network. The RF-to-DC converter consists of a cascade of voltage multiplier circuits. For the RF signal, all capacitors can be considered as shorted thus, all diodes

are connected in parallel (or anti-parallel) to the input. For the DC, all capacitors can be considered as an open circuit so that all diodes are connected in series with the output. The DC output generated by the RF-to-DC converter is approximately equal to [41]

$$V_{DC} \approx N \cdot (V_{InRF, peak} - V_{fwd}) \quad (2)$$

where N is the number of diodes, $V_{InRF, peak}$ is the amplitude of input RF signal (V_{InRF} in Figure 43) and V_{fwd} is the forward bias voltage of the diode. A critical figure of merit for RF-to-DC converters is power conversion efficiency [42], [46]

$$\eta_c = \frac{P_{DC}}{P_{RF, in}} \quad (3)$$

$$P_{RF, in} = \text{Incident RF Power} - \text{Reflected RF Power} = P_{RF, Avail} \cdot (1 - |S_{11}|^2) \quad (4)$$

where P_{DC} is the DC power measured at the output of the converter, $P_{RF, Avail}$ is the available power provided by the RF input source, $|S_{11}|$ is the return loss and $P_{RF, in}$ is the power delivered into the RF-to-DC converter.

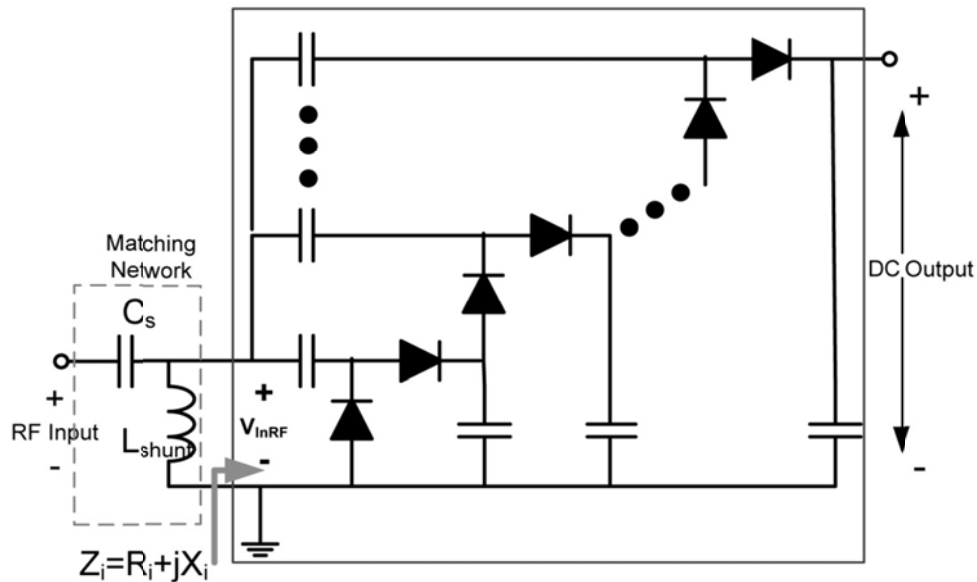


Figure 43: RF-to-DC converter integrated with the input matching network

The required RF input power should be as small as possible for longer operating range. This requires low power consumption circuits connected at the converter output and high input impedance (Z_i in Figure 43) which further reduces the required RF input power by increasing the conversion efficiency. Typical power consumption of an RFID baseband circuit is in the order of

~1-2 μW [41], [54]. Since the function of baseband for the wireless switch is much simpler than that of an RFID, its power consumption should be significantly lower.

Ideally, the highest efficiency is achieved with a single stage. However, generation of sufficiently high DC output voltage with only one stage requires large input voltage amplitude and, hence, a very high-Q matching network to transform the antenna impedance which is typically around 50 Ω . To relax this, multiple stages are needed. In this wireless switch design, an RF-to-DC converter with 5 stages was chosen. To achieve high Q, an on-chip metal-oxide-metal capacitor, C_{series} and a bond wire inductor, L_{shunt} are used for matching (Figure 43). A concern for a bond wire inductor is its variation. The length of bond wire inductor can be controlled within $\sim \pm 50 \mu\text{m}$. With the variations of bond wire inductor and on-chip capacitor, the tuning frequency is expected to vary $\sim \pm 100 \text{ MHz}$ and $|S_{11}|$ at 5.8 GHz is expected to be less than -10 dB over these variations. An on-chip inductor with lower Q can also be used at the expense of more loss and degraded efficiency. Since for the applications of interest, the range and transmitted power can be selected with a great deal of flexibility, the degradation of efficiency can be tolerated.

The diode sizing along with the number of stages for the RF-to-DC converter also needs to be considered to improve the efficiency. Since diodes with higher saturation current, a lower forward bias voltage drop and faster switching time are desirable for better efficiency, Schottky Barrier diodes (SBD's) have been chosen [41], [44]. These SBD's are created without process modifications by using the layout layers available in the standard design kit [49], [50]. In this design, SBD's with measured characteristics have been used to optimize the power efficiency. Figure 44 shows an n-type Schottky diode layout, cross section, and Figure 45 presents the diode equivalent circuit model including its parasitics. An n-well-to-p-substrate diode, $D_{\text{nwell-sub}}$, has been added to account its junction breakdown. For the series resistance R_s , it includes all the resistances between the Schottky Barrier contact and ohmic contact. The series resistance R_s [51] is

$$R_s \approx R_1 + R_2 + R_3 + R_C$$

$$\approx \frac{R_{\text{sh-nwell}}}{29} + R_{\text{sh-nwell}} \left(\frac{d_{\text{STI}} \cdot x_j}{l_s^2} \right) + R_{\text{sh-STI}} \left(\frac{l_1}{4l_s} \right) + R_{\text{sa-n+}} \left(\frac{l_2}{2(l_s + 2l_1)} \right) + R_C \quad (5)$$

where $R_{\text{sh-nwell}}$ is the n-well sheet resistance, $R_{\text{sh-STI}}$ is the n-well sheet resistance under the shallow trench isolation (STI), $R_{\text{sa-n+}}$ is the salicided n^+ sheet resistance, R_C is the resistance associated with the contacts and vias. l_s is the length of the Schottky, l_1 is the STI width and l_2 is the separation between the edge of STI and n-well metal contact. d_{STI} is the STI thickness and x_j is the n-well depth.

For the junction capacitance for SBD, its expression is similar to that a p-n diode. The difference is that SBD does not have diffusion capacitance when it is forward biased because the minority-charge storage effect is not present [52].

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V}{V_{bi}}\right)^{m_j}} \quad (6)$$

$$C_{j0} = l_s^2 \left(\frac{qN_D \epsilon_{si}}{2V_{bi}} \right)^{1/2}$$

where C_{j0} is the zero bias junction capacitance, q is the charge of an electron, N_D is the n-well doping density, ϵ_{si} is the permittivity of silicon, V_{bi} is the built-in potential and m_j is the junction grading coefficient.

Because the operating frequency of RF-to-DC converter (5.8 GHz) is low compared to the cut-off frequency of diode, the main trade-off for sizing the diodes is between increasing the saturation current which leads to higher direct current slope and higher DC output voltage, and decreasing n-well-to-substrate parasitics which introduces loss and degrades efficiency. This loss can be approximated by [41]

$$P_{loss,sub} \approx \frac{1}{2} v^2 (2\pi f_o C_{sub})^2 R_{sub} \quad (7)$$

where v is the RF peak voltage at a node referenced to ground, C_{sub} is the substrate parasitic capacitance, R_{sub} is the series resistance of C_{sub} , and f_o is the frequency of RF input. A single diode cell with a larger area that has a smaller n-well to Schottky diode area ratio should be better than a structure with multiple minimum area diode cells connected in parallel.

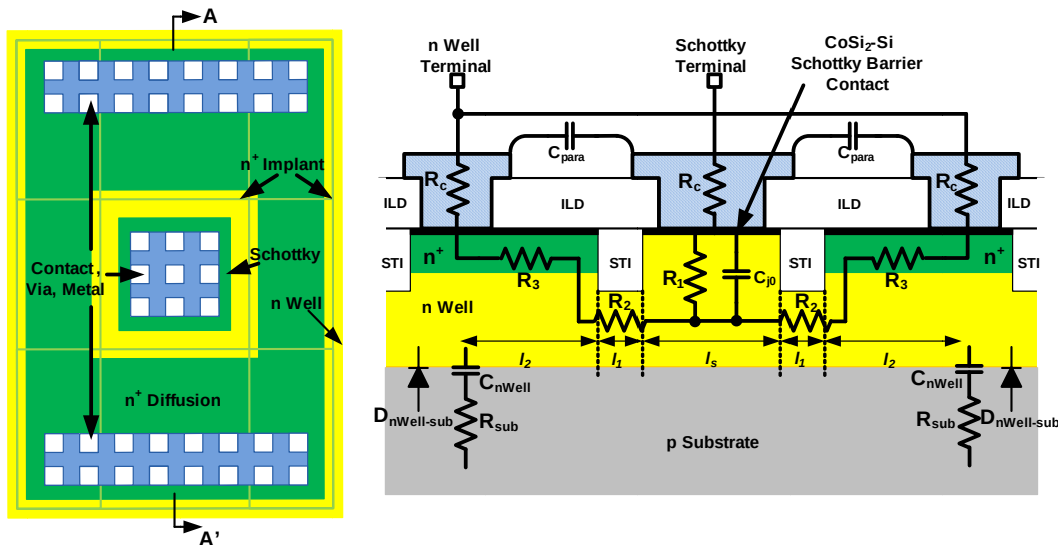


Figure 44: N-type Schottky barrier diode layout and its cross section

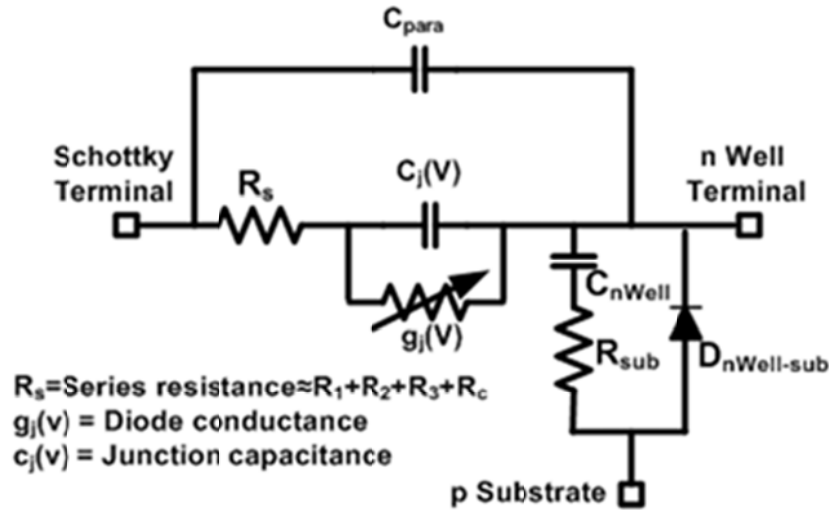


Figure 45: Diode model with associated parasitics

Figure 46 plots simulation results for the power efficiency of 5-stage RF-to-DC converters constructed with the different diode structures. It shows that a Schottky diode with a unit area of $1.28 \times 1.28 \mu\text{m}^2$ and the corresponding n-well size of $4.88 \times 3.24 \mu\text{m}^2$, and the space between the Schottky contact and n^+ diffusion of $1.16 \mu\text{m}$ is well suited for this particular application.

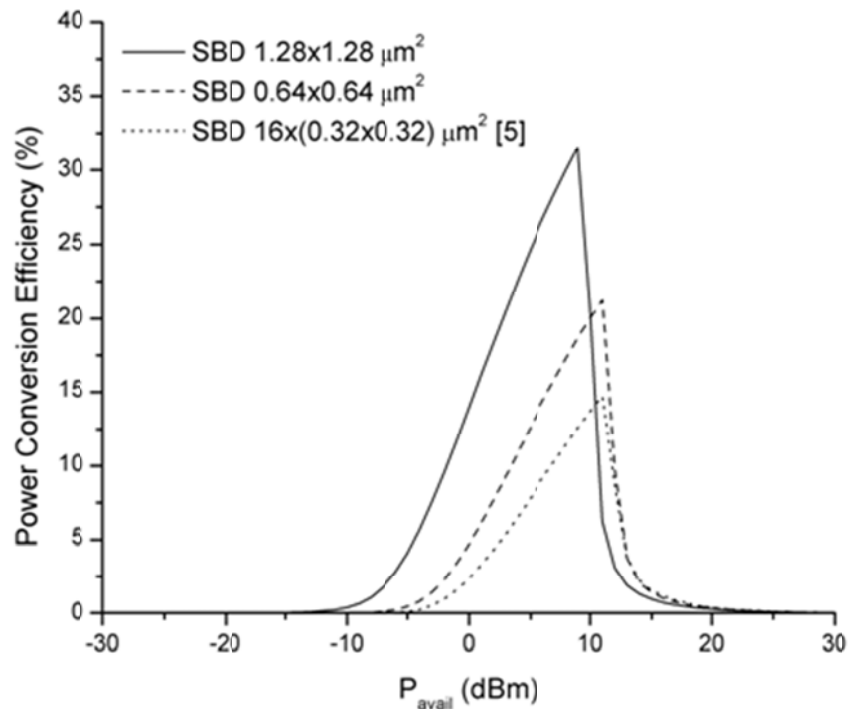


Figure 46: Simulated power conversion efficiency for a 5-stage RF-to-DC converter

ENVELOPE DETECTOR, LIMITER AND RF CLAMP AND POWER ON RESET

The circuit diagram of envelope detector is shown in Figure 47 (a). This structure is the same as that of the RF-to-DC converter except that only one diode stage has been used. The capacitors, C_1 - C_2 , and resistors, R_1 - R_2 are used to provide appropriate time constant to generate envelope signal and reference signal for the comparator. These component values depend on the RF input signal data rate. Two outputs, envelope signal and reference signal are fed to a comparator to generate the demodulated data that can be used to authenticate wake up request. Having the reference signal enables proper operation even when the envelope signal does not swing down all the way to zero.

The DC output voltage as well as input voltage of the RF-to-DC converter can be unacceptably high. This can damage the converter and circuit connected to its output. To prevent this, a limiter and an RF clamp have been included. Figure 47 (b) shows the limiter and RF clamp circuits. The locations of these elements in the transceiver are shown in Figure 41Figure 42. The limiter consists of 3 p^+ -to-n-well diodes connected in series at the output of RF-to-DC converter. The RF clamp consisting of a p^+ -to-n-well diode and an n^+ -to-p-substrate diode in an anti-parallel configuration is connected to the antenna port. The junction areas of p^+ -to-n-well and n^+ -to-p-substrate diodes are $100 \mu m^2$. The total parasitic capacitance of the clamp is $\sim 110 fF$. Once the DC output voltage is higher than $3v_{d,p+}$, (where $v_{d,p+}$ is the turn-on voltage for the p^+ -to-n-well diode), the diodes turn on and limit the DC output voltage. For the RF input signal with amplitude greater than $v_{d,p+}$ for positive side and $v_{d,n+}$ (where $v_{d,n+}$ is the turn-on voltage for the n^+ -to-p-substrate diode) for negative side, the diodes turn on and limit the input signal level.

The power-on-reset circuit for the wireless switch is shown in Figure 47 (c). It is composed of a cross-coupled pair of NMOS transistors and a NOR gate [43]. When the DC output voltage from the RF-to-DC converter is sufficiently high, one branch of the cross-coupled pair over powers the other and latches the value. Long channel devices that increase the gain of inverters [56], and damping capacitor, C , [43] are used to reduce the probability of cross-coupled pair being in a meta-stable state. The NOR gate compares the two signals and generates a pulse (power-on-reset signal) to initialize a logic block (not included) that determines whether the rest of circuits should be powered up.

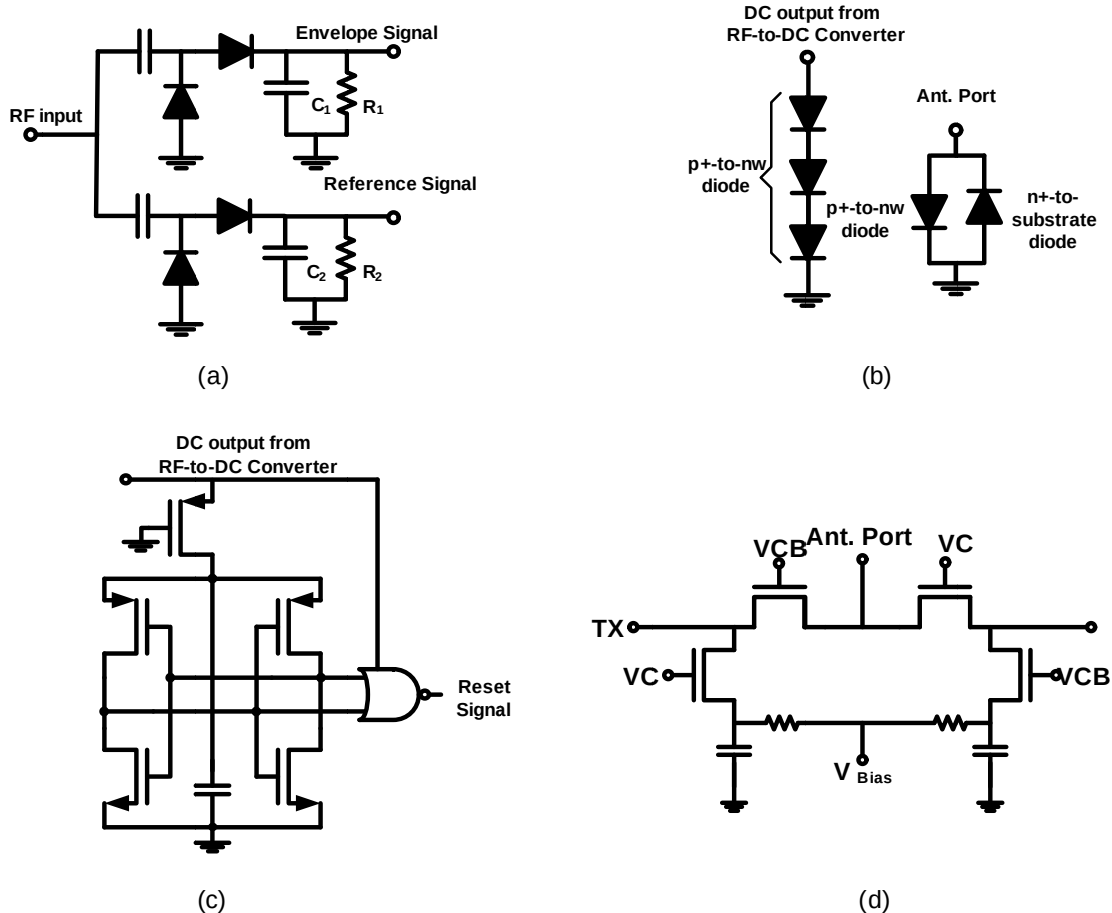


Figure 47: (a) Envelope Detector, (b) Limiter and RF Clamp, (c) Power-on Reset, (d) Simplified T/R switch [55]

T/R SWITCH

To evaluate the performance of wireless switch and transceiver in the presence of the other, a T/R switch for TDD communication system is connected at the input of the wireless switch. Figure 47 (d) shows a simplified schematic of broad band T/R switch. The T/R switch [55] achieves insertion loss of ~ 0.7 dB, return loss of ~ 20 dB and isolation greater than 30 dB at 2.4 GHz.

To combine the wireless switch and transceiver chain together, as mentioned in previous section, the input impedance looking into the wireless switch must be high impedance at 2.4 GHz to prevent loading, while matched at 5.8 GHz. This is realized by using the same shunt inductor and series capacitor input matching network that transforms $50\ \Omega$ to higher input impedance of the RF-to-DC converter. The series capacitor, C_s increases the input impedance at 2.4 GHz to reduce the loading of the converter. Figure 48 shows the frequency dependence of input impedance for the entire system on a Smith chart in both PUX and TRx modes.

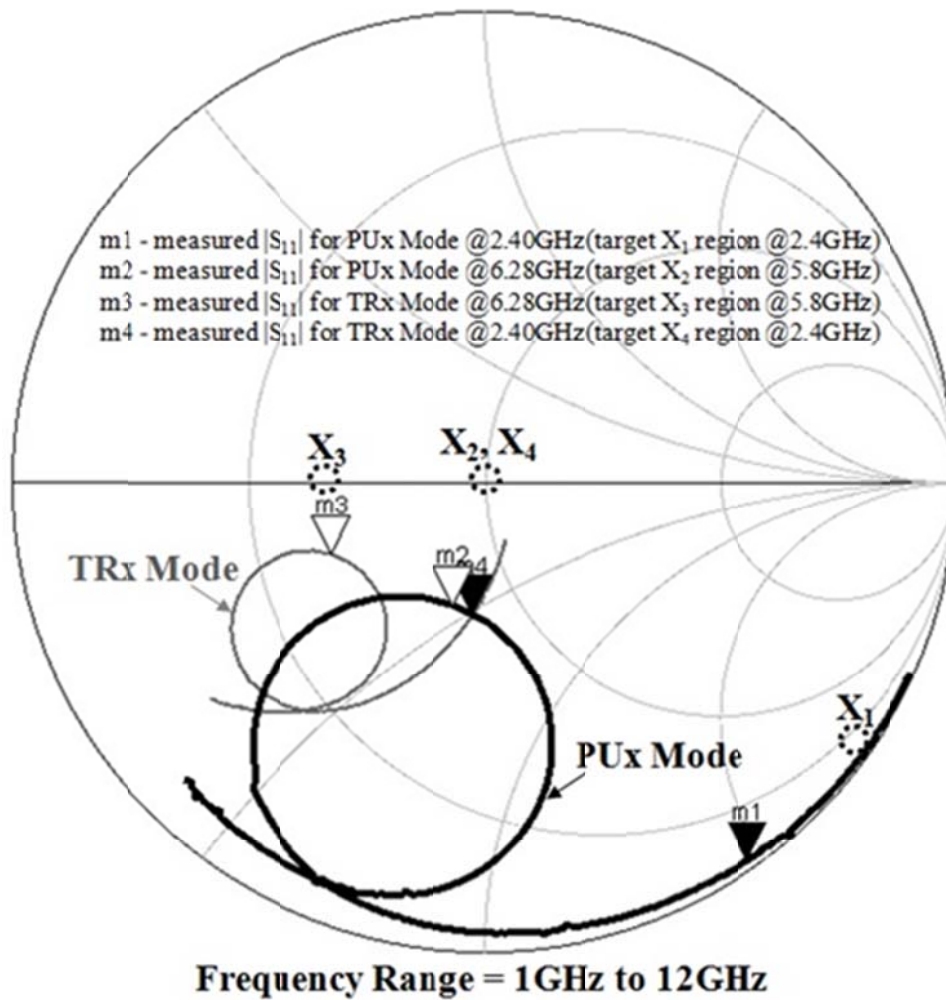


Figure 48: Input impedance of the entire system for PUX and TRx operating modes (design targets and measurement results).

In PUX mode, the T/R switch is turned off so its input impedance is capacitive and high. Since the matching circuit of the wireless switch is tuned at 5.8 GHz, the total input impedance is at the center of Smith chart (X_2) at 5.8 GHz and at the lower-right-hand side at 2.4 GHz (X_1). In TRx mode, due to the broad band response of T/R switch, its input impedance is $\sim 50 \Omega$ at both 2.4 and 5.8 GHz. Because the input matching network of wireless switch is high impedance at 2.4 GHz and matched to 50Ω at 5.8 GHz, the total input impedance is 50Ω (X_4) at 2.4 GHz and 25Ω (X_3) at 5.8 GHz.

EXPERIMENTAL RESULTS

A die micrograph for an integrated circuit including both wireless switch and T/R switch is shown in Figure 49. The chip size is $\sim 1400 \times 730 \mu\text{m}^2$ including bond pads. The area of the wireless switch excluding bond pads is $\sim 400 \times 590 \mu\text{m}^2$. This circuit is fabricated in a 130-nm digital CMOS process. The wireless switch and T/R switch are connected on-chip for

characterization of the T/R switch and wireless switch combination. More specifically, the antenna bond pads of T/R switch and input bond pads of wireless switch are connected at the center of the chip. The bond pads on the wireless switch side, including a ground pad, are used to make the bond wire connections for L_{shunt} in Figure 49. These bond pads in combination with laser cuts also allow separate characterization of the RF-to-DC converter with and without a matching network, and the T/R switch by itself.

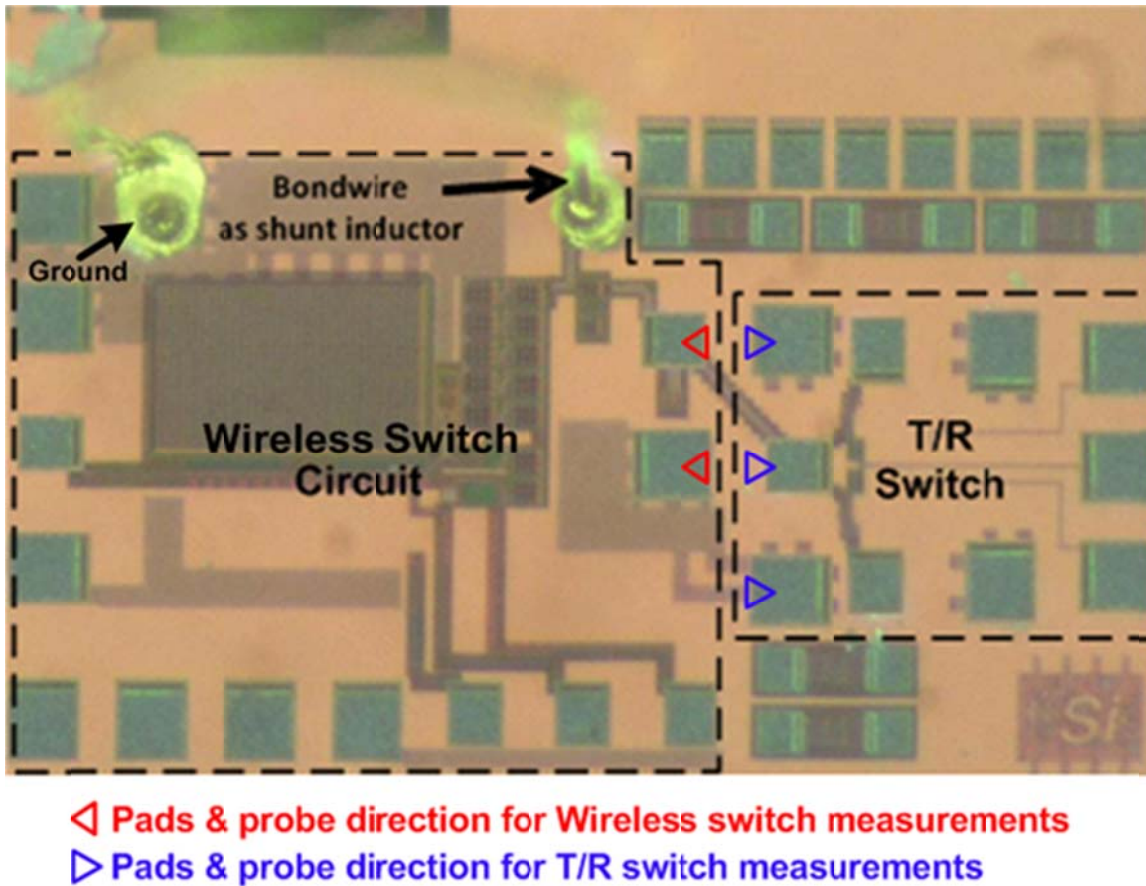
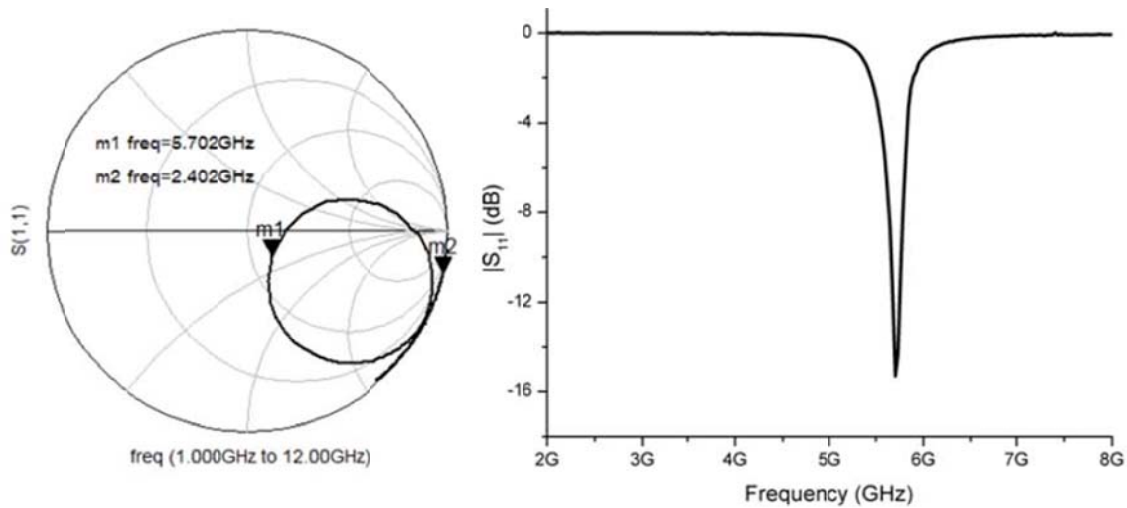


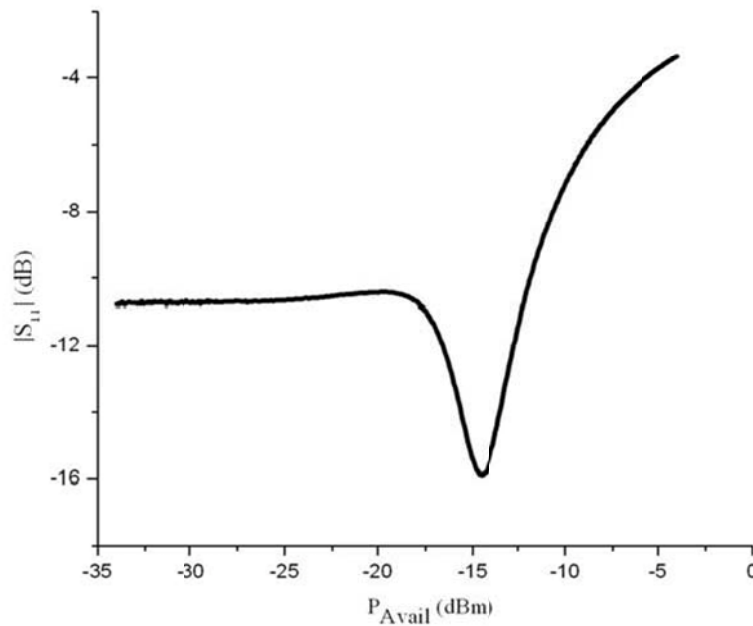
Figure 49: Die micrograph of wireless switch integrated with T/R switch

The input return loss, DC output voltage and the power conversion efficiency of the RF-to-DC converter were measured with a 1-M Ω load. Figure 50 (a) and (b) show the measured small-signal and large-signal $|S_{11}|$'s of the converter with the matching network, respectively. In Figure 50 (a), the matching network is tuned at ~ 5.7 GHz. The input impedance is high at 2.4 GHz. The resonant frequency is slightly below the target, because of errors in modeling the matching network and the previously discussed variations of the passive components. The large-signal $|S_{11}|$, DC output voltage, and the power conversion efficiency (also without matching network) are measured at the tuned frequency of 5.702 GHz. Figure 50 (b) shows that $|S_{11}|$ is below -10 dB for input power less than ~ -12 dBm and over -10 dB for input power greater than -10 dBm. The high $|S_{11}|$ at high input RF power (greater than -10 dBm) is not a

serious issue since the power level is already large enough to turn on the wireless switch although the return loss is high.



(a)



(b)

Figure 50: $|S_{11}|$ of RF-to-DC converter and matching network. (a) small-signal, (b) large-signal

Figure 51 and Figure 52 show measured and simulated DC output voltage and power conversion efficiency of the RF-to-DC converter (with and without a matching network), respectively. The limiter at the output was laser cut for these measurements. The power

efficiency is calculated using equations (3) and (4). These two figures are plotted versus the available power, P_{Avail} , of an external RF signal generator. In Figure 51, at the same P_{Avail} ~ -13 dBm, the converter with a matching network generates DC output voltage of around 1 V instead of ~ 0 V for the converter without the matching network. This clearly demonstrates that the matching network improves the sensitivity of wireless switch. The measurements also agree well with the simulation results overlaid in the same figures. At high available power levels, the DC output voltage saturates around 10 V because of the breakdown voltage associated with the n-well to p-substrate junction of Schottky diodes. When the limiter circuit is connected, the DC output voltage of the converter is clamped at $3v_{d,p+}$ (~ 2 V), where $v_{d,p+}$ is the turn-on voltage for the p^+ -to-n-well diode.

The efficiency peaks and falls beyond a certain input power level due to the n-well-to-substrate junction breakdown that saturates the output voltage. At $P_{\text{Avail}} < 0$ dBm, the converter with the matching network provides higher conversion efficiency. However, its efficiency increases at a slower rate than the one without the network and reaches the maximum of around 14 % at P_{Avail} of ~ 0 dBm while the converter without the matching network shows the peak efficiency of around 34 % at $P_{\text{Avail}} \sim 9$ dBm. The degradation of power conversion efficiency is due to the loss of the matching network resulting from the finite Q of on-chip capacitor and bond wire (estimated Q of ~ 50 at 5.8 GHz). The measured and simulated results agree well.

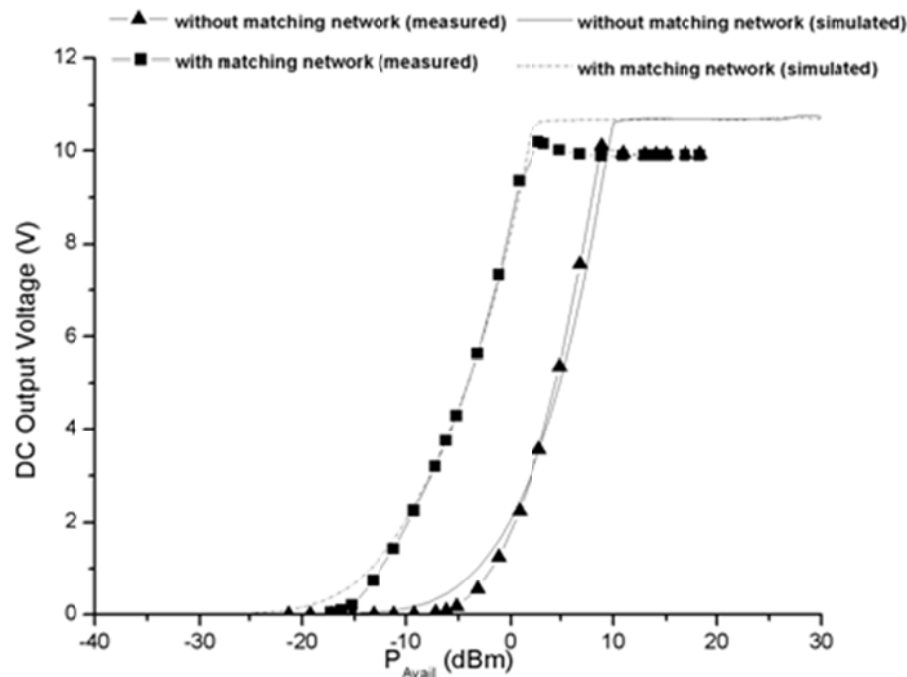


Figure 51: DC output voltage vs. available power, P_{Avail}

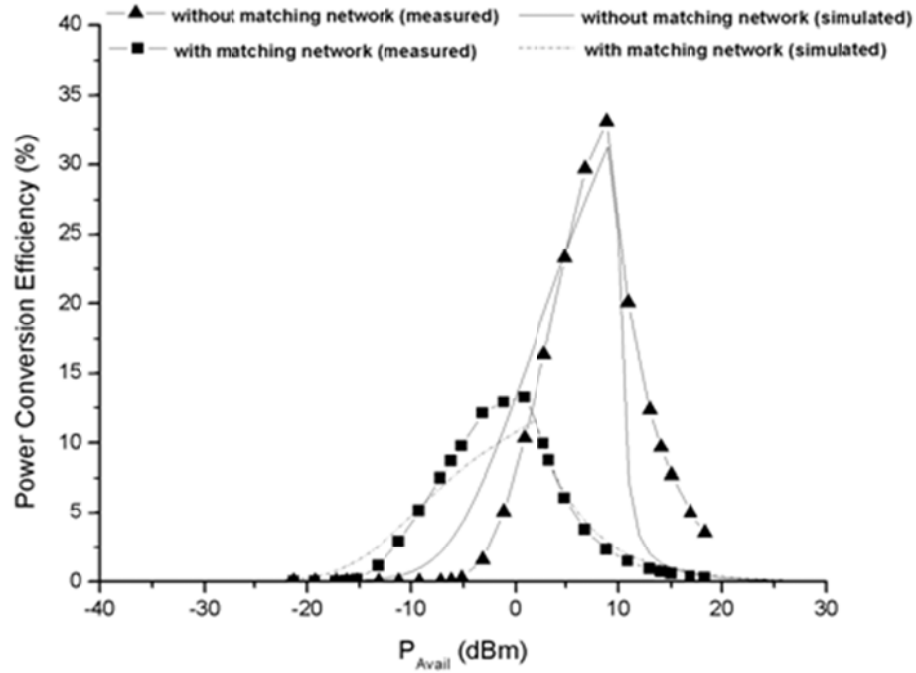


Figure 52: Power conversion efficiency vs. available power, P_{Avail}

For the T/R switch characterization, since only a small battery with supply voltage of around 1.2 V is expected to be available in μNode , the DC bias voltage (V_{Bias}) for the shunt transistors of the switch has been connected to ground instead of 1.8V in [55]. Figure 53 shows the measured performance of the T/R switch with zero bias voltage alone. At 2.4 GHz, the T/R switch has 0.7 dB insertion loss, around 24 dB isolation (from antenna port to TX or RX port), and less than -15 dB $|S_{11}|$ and $|S_{22}|$.

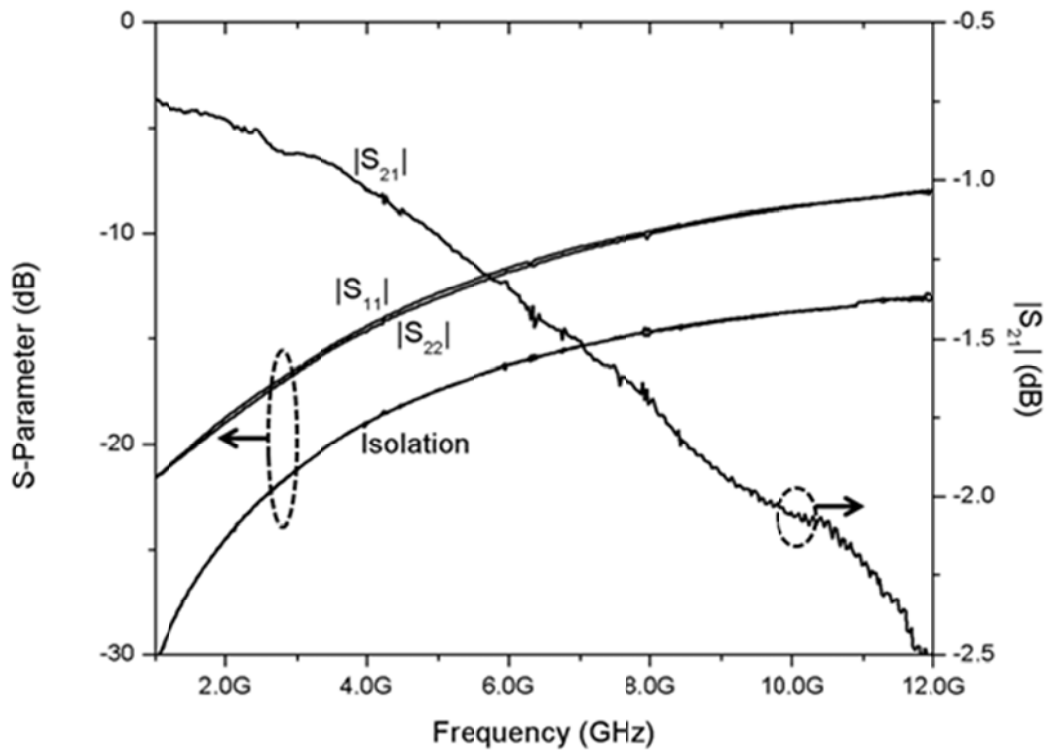


Figure 53: Measured performance of a T/R switch with zero bias voltage

Figure 48 also shows the measured input impedance of wireless switch integrated with the T/R switch at both PUX and TRx modes. In PUX mode, the input impedance is capacitive at 2.4 GHz, (marker m1) and close to the center of Smith chart at 6.28 GHz, (marker m2). There is a frequency shift from 5.7 to 6.28 GHz. This is due to the difference of position for the RF probe compared to that for the RF-to-DC converter measurement alone (Figure 49). The probe is much closer to the bond wire, and the mutual coupling with the probe reduces the effective length of bond wire, increasing the tuning frequency from 5.7 to 6.28 GHz. In the actual μ Node implementation the circuits can be rearranged to reduce this mutual coupling and thus the discrepancy. In TRx mode, when the T/R switch is turned on, the input impedance of circuit is close to the center of Smith chart at 2.4 GHz, (marker m4), and the input impedance at 6.28 GHz moves toward the 25 Ω constant resistance circle (marker m3) due to the broad band response of T/R switch and loading of the wireless switch as discussed in the previous section.

The performance of T/R switch after integrating the RF wireless switch is also shown in Figure 54 and Figure 55 in PUX and TRx mode, respectively. In PUX mode, the isolation from the antenna port to TX or RX port at frequency 2.4 GHz is around 24 dB and $|S_{11}|$ is less than -11 dB at 6.28 GHz. In TRx mode, at 2.4 GHz, the insertion loss of the switch is degraded by ~0.3 dB to 1 dB, and $|S_{11}|$ and $|S_{22}|$ are less than -10 dB. Figure 56 shows the measured 1 dB compression point (P_{1dB}) for the T/R switch before and after integrating the wireless switch. The input referred P_{1dB} of T/R switch degrades 0.5 dB when the wireless switch is added due to the RF

clamp circuit that was added at the input (antenna port). This also indicates that the RF clamp will limit the input power larger than ~12 dBm to protect the wireless switch and transceiver. These measurement results show that the deleterious effect of adding a wireless switch into a transceiver can be limited.

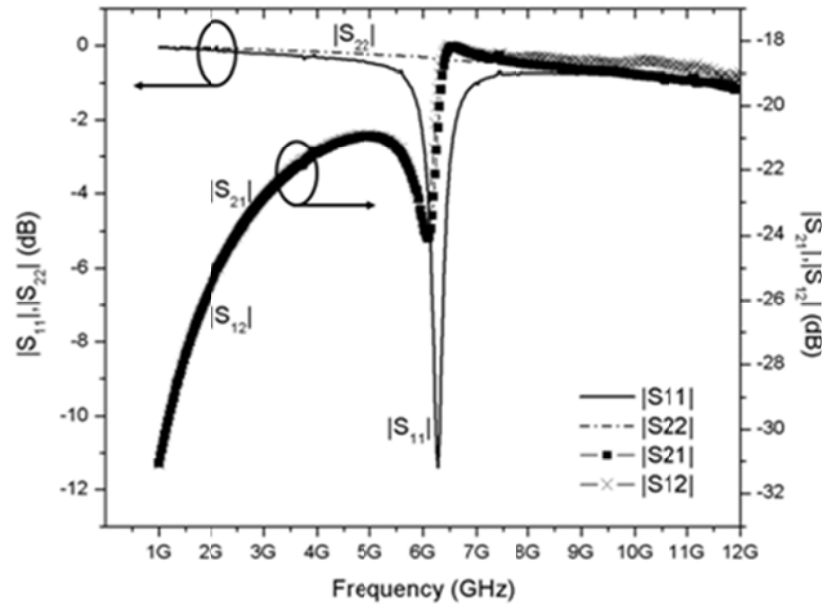


Figure 54: Measured S parameters T/R switch and wireless switch in Power-up (PUx) mode

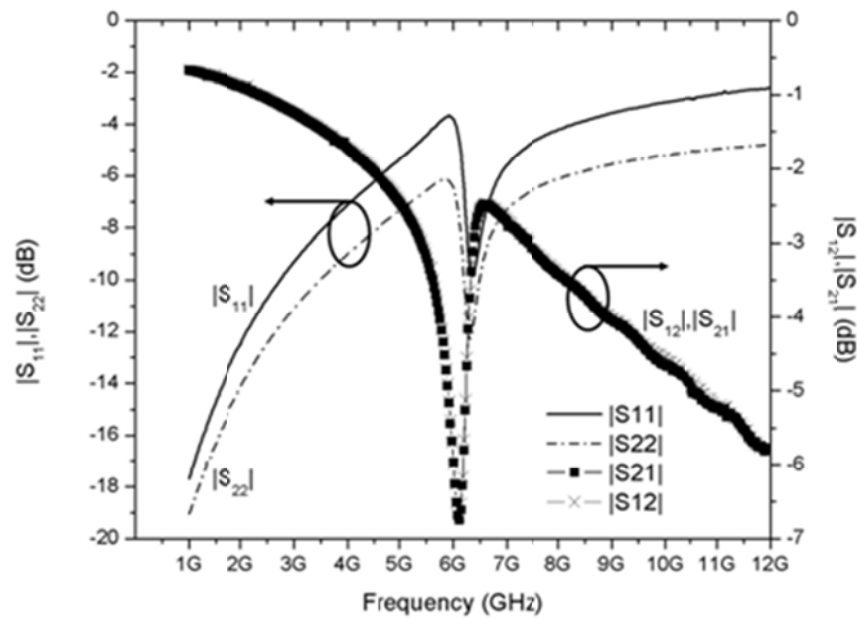


Figure 55: Measured S parameters T/R switch and wireless switch in Transceiver (TRx) mode

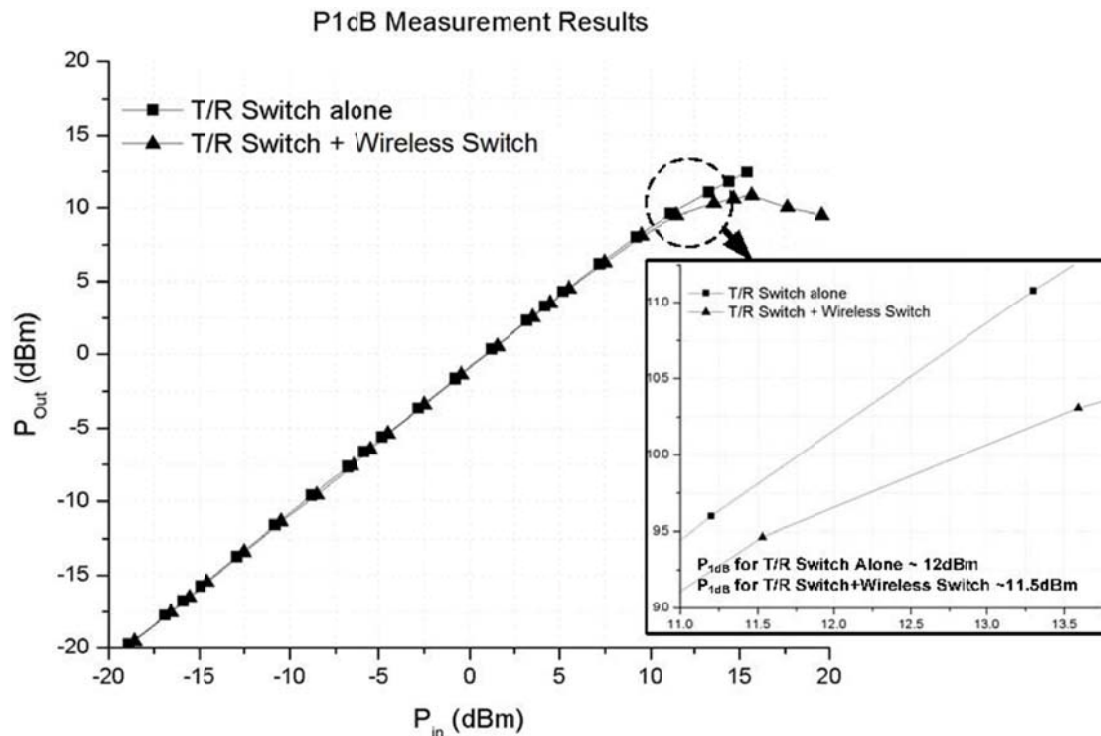


Figure 56: Measured 1 dB compression points of T/R switches with and without wireless switch

ACTIVATION CIRCUIT SUMMARY

A dual frequency band approach for integrating a wireless switch using an RF-to-DC converter (5.8 GHz) with a transceiver (2.4 GHz) was devised. The RF-to-DC converter is the first fully integrated converter operating at 5.8 GHz. The approach was validated by evaluating the performance impact of adding the switch to a T/R switch. In a 130-nm digital CMOS process, a T/R switch integrated with the wireless switch achieves ~0.3 dB higher insertion loss and 0.5 dB lower 1 dB compression point compared to that without the wireless switch, 24 dB isolation and less than -10 dB for the matching at 2.4 GHz. The maximum power efficiency of RF-to-DC converter using Schottky diodes and a bond wire inductor for matching/impedance transformation is 14% at 5.7 GHz. The maximum occurs when the available input power is 0 dBm. This indicates that integration of a wireless switch for turning on and off a transceiver of M&M size or smaller communication nodes by using RF signals can be accomplished with minimal performance degradation for the transceiver.

LOW POWER RECEIVER FRONT END DESIGN

In a μ Node system, the power consumption of radio communication subsystem is a dominant factor determining its size and life time. To lower the power consumption of μ Node system, low power RF front-end circuits are thus necessary. However, the performance of the system

normally varies with the power consumption, so careful design of the RF front-end is critical to lower the total power consumption while maintain the acceptable system performance. This section discusses the architecture and circuit design issues for reducing the power consumption of an RF receiver front-end employed in this μ Node system.

RECEIVER ARCHITECTURE

A simplified block diagram of the receiver architecture for a μ Node system is shown in Figure 57. It uses direct conversion receiver architecture. To improve the linearity constraints and power consumption of this system, a passive receiver front-end topology has been devised. The first RF stage of this receiver is an impedance transformation network instead of a low noise amplifier (LNA). The output of this network is fed into I and Q passive mixers that perform down conversion. This passive structure is well suited for low power application because it is highly linear and has moderate RF voltage gain with reasonable noise performance [57].

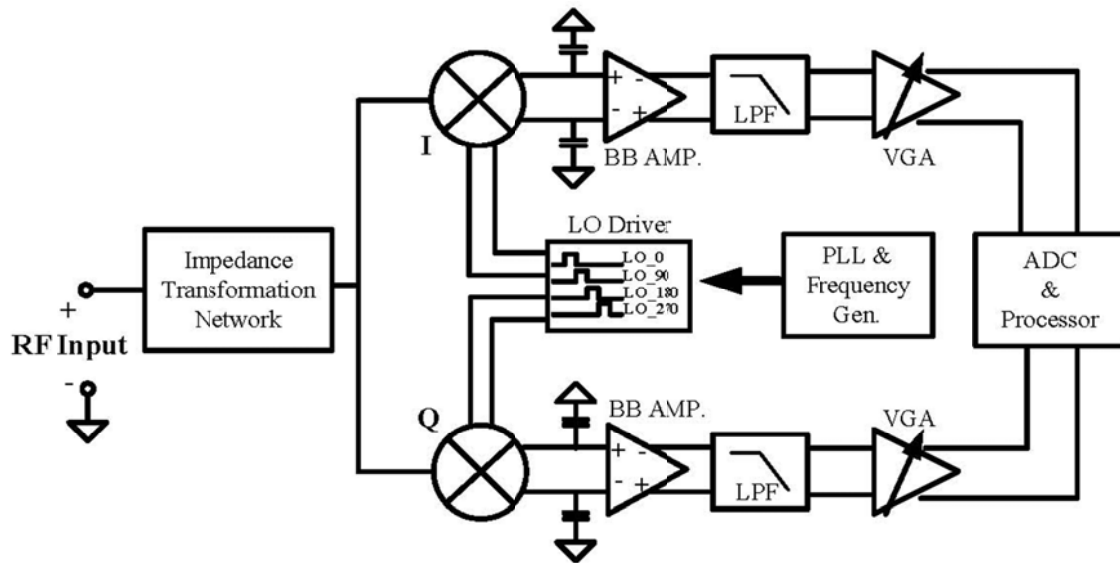


Figure 57: Receiver architecture simplified diagram

This receiver consists of an impedance transformation network (ITN), I-Q passive mixers, phase-locked loop, frequency generator, LO driver, baseband amplifiers, low-pass filters, variable gain amplifiers (VGAs), analog-to-digital converter (ADC) and a baseband processor. At the RF front-end the incoming RF signal gets amplified by the tapped capacitor resonator and down converted by I-Q passive mixers. The high frequency component is filtered at the output of the mixers so that only the baseband signal is fed into baseband amplifier (BB Amp.). This is followed by a low pass filter and variable gain amplifiers (VGAs). The final output signal is fed into the analog-to-digital converter (ADC) and microprocessor for data demodulation.

CIRCUIT DESIGNS

This subsection discusses the circuit structures, and circuit design issues for the RF front-end consisting of impedance transformation network, passive mixers, baseband amplifiers and the LO driver.

IMPEDANCE TRANSFORMATION NETWORK

A simplified structure for the impedance transformation network or tapped capacitor resonator is shown in Figure 58. This tapped resonator consists of capacitors (C_1 and C_2) and shunt inductor (L_1). This circuit has the ability to set the center frequency, quality factor (Q) of the network, and impedance transformation ratio. To simplify the analysis, some parasitic capacitance associated with capacitors and inductors are neglected and the inductor is assumed to have sufficiently high self-resonant frequency (SRF). This subsection presents the effect of quality factor of passive components on matching, noise performance and voltage gain of this network.

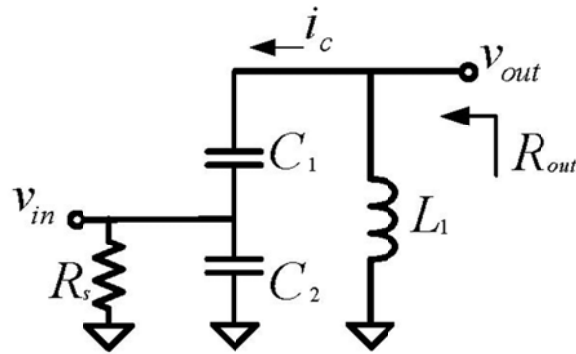


Figure 58: Tapped capacitor resonator as an impedance transformation network

To achieve high voltage gain and low noise figure from this network, passive components with high quality factor, Q , are necessary. However, Q for on-chip components is normally limited by the integrated circuit (IC) process. Careful consideration and design for passive components are really necessary. Assuming that negligible current flows into the source resistance R_s , the voltage gain of this network can be approximated as

$$v_{out} \approx v_{in} \left(1 + \frac{C_2}{C_1}\right) \quad (8)$$

For a lossless network, the impedance transformation ratio can also be approximated as

$$R_{out} \approx \left(1 + \frac{C_2}{C_1}\right)^2 R_s \quad (9)$$

To better understand the effect of Q on the performance of this circuit, by transforming shunt circuit to series and transforming the net series circuit to a shunt circuit (Figure 59).

$$R_{out} = \frac{1 + Q_s^2}{1 + Q_2^2} R_s \quad (10)$$

where $Q_2 = \frac{R_s}{X_2} = \omega C_2 R_s$

and $Q_s = \frac{X_s}{R_s} (1 + Q_2^2) = \omega R_s \frac{C_2}{C_1} (C_1 + C_2) + \frac{1}{\omega R_s C_1}$ (11)

where $X_s = X_1 \parallel X_2'$, $X_1 = \frac{1}{\omega C_1}$, $X_2' = \frac{1}{\omega C_2'}$ and $C_2' = C_2 (1 + Q_2^{-2})$

After some algebra and assumption that $X_2 \ll R_s$, the impedance transformation ratio in (7) is approximately equal to that in (6). In order to resonate at the desired frequency, the output impedance of composite RC network must present an imaginary part of equal magnitude but opposite sign to that of the inductor at the resonant frequency. Since the input of this network is connected at the node between C_1 and C_2 , the parasitic capacitance associated with interconnect lines and additional components such as a bond pad, a bond wire and etc. must be carefully taken into account in the design.

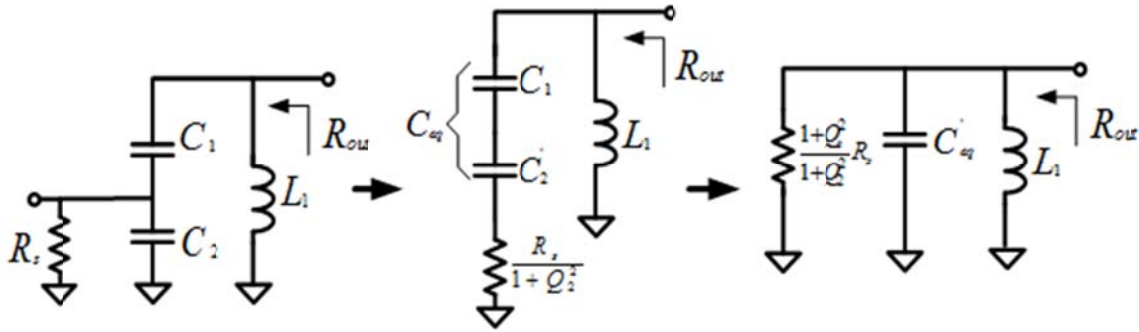


Figure 59: Transformation of tapped capacitor resonator

By using the circuit in Figure 59, the resonant frequency of this network is

$$f_o = \frac{1}{2\pi \sqrt{L_1 C_{eq}}} \quad (12)$$

where $C_{eq} = \frac{C_1 C_2 (1 + Q_2^2)}{(C_1 + C_2) Q_2^2 + C_2}$

Figure 60 shows a plot of resonant frequency of this resonator with varying value of C_2 while C_1 and L_1 are kept constant. The initial value of C_1 , C_2 and L_1 needed to achieve the resonant frequency at 2.4 GHz are 340 fF, 320 fF and 13.5 nH, respectively. Note that these are not the actual values used in real design since more parasitics associated with passive components and interconnect lines must be included in final design. This plot shows that the resonant frequency of this tapped capacitor resonator is relatively insensitive to the variation of C_2 . This is one of the major advantages of this transformation network that simplifies the design.

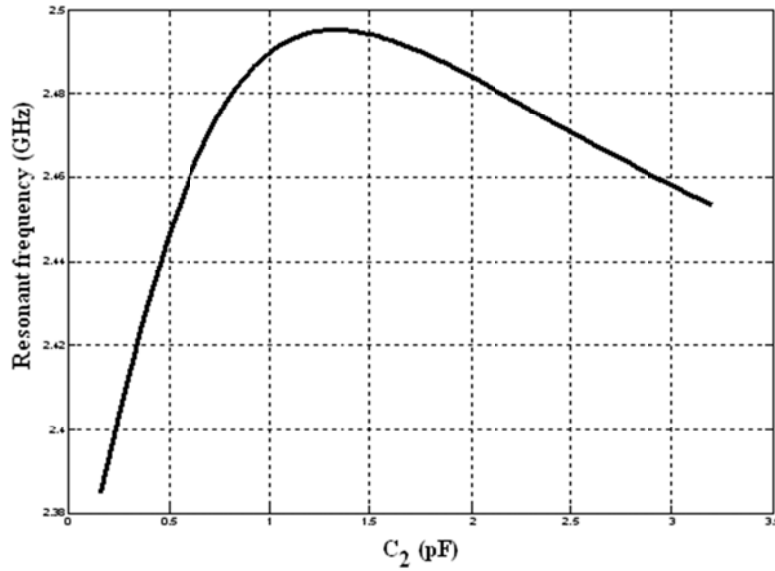


Figure 60: Resonant frequency, f_o , of tapped capacitor resonator vs. variation of C_2

The noise contribution of this network is mostly from both source resistance R_s and series resistance R_L associated with the shunt inductor L_1 (not shown in Figure 58 and Figure 59). Therefore, to analyze the noise performance, the series resistance is included in the following analysis. To achieve good noise factor, the total output noise due to R_L should be minimized, or high Q_L is desirable. The relationship between noise factor of this network and quality factor of the passive component can be considered by using the shunt $\leftrightarrow$ series for R_L and assuming $Q_s^2 \gg 1$, $Q_2^2 \gg 1$ and $Q_L^2 \gg 1$. Hence, the noise factor of can be approximated as:

$$\text{Noise factor} = 1 + \frac{R_s \left(\frac{Q_s^2 + 1}{Q_2^2 + 1} \right)}{R_L (Q_L^2 + 1)} \approx 1 + \frac{R_s \left(\frac{Q_s}{Q_2} \right)^2}{R_L Q_L^2} \approx 1 + \frac{X_s Q_s}{R_L Q_L^2} = 1 + \frac{Q_s}{Q_L} \quad (13)$$

where $|X_s| = |X_L|$ at resonant frequency.

This analysis clearly shows that a high quality factor of inductor, Q_L improves the noise performance. At the matched condition, $Q_L = Q_s$, noise factor from (13) is equal to 2 (or 3 dB NF). However, in actual design, Q_s can be less than Q_L to improve the noise performance while trading some voltage gain due to the mismatch. Simulated performance of this matching network with varied Q_L is shown in Figure 61 and Figure 62. In this design, the impedance is transformed from $50\ \Omega$ to $1\text{k}\ \Omega$ for R_s and R_{out} , respectively. From these simulation results, high Q_L is desirable for this kind of matching network because it gives lower noise factor (or noise figure), and higher voltage. However, high Q for on-chip components, especially for inductor, is difficult to achieve. Therefore, other types of inductors with higher Q such as bond wire or off-chip inductors are used to improve the performance of this matching network.

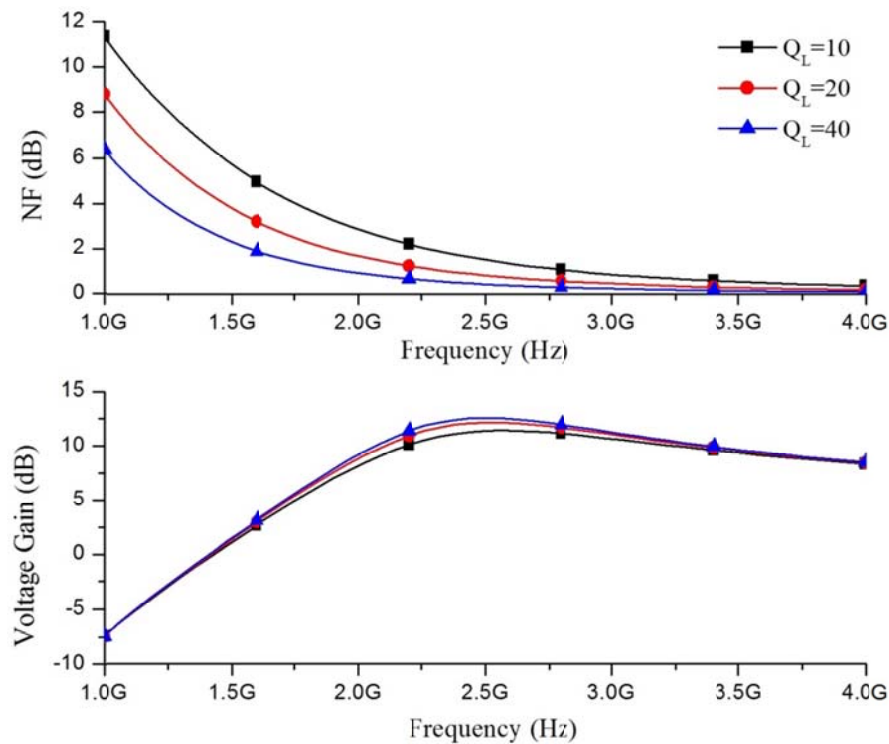


Figure 61: Simulated Noise Figure and Voltage Gain of matching network with varying Q_L

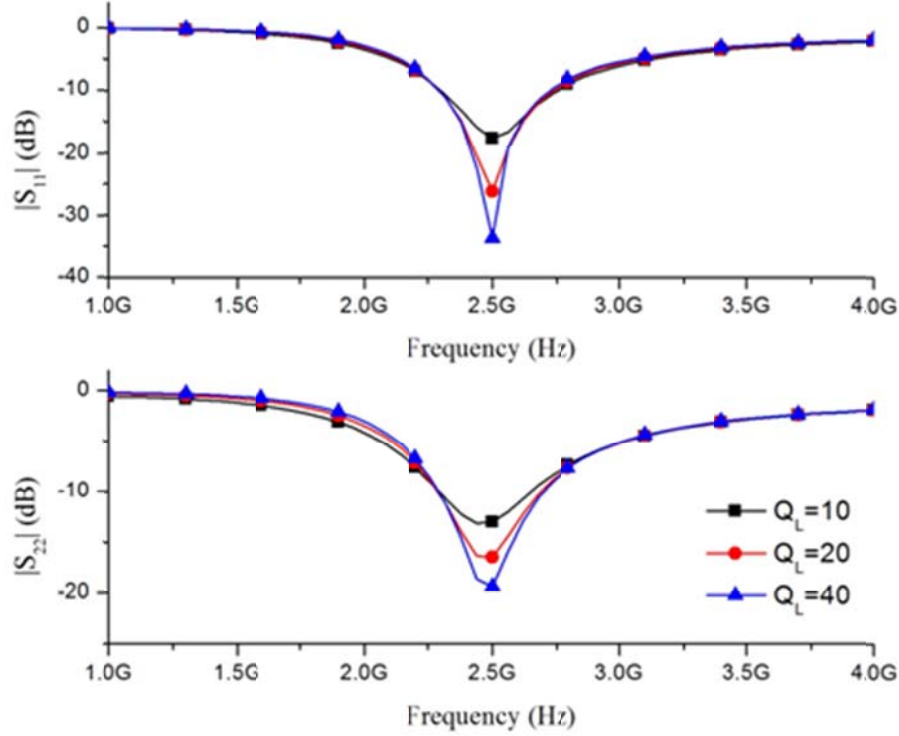


Figure 62: Simulated $|S_{11}|$ and $|S_{22}|$ matching network for various Q_L ($|S_{22}|$ normalized to 1 k Ω source resistance)

PASSIVE MIXERS

In this μ Node system, only one mixer performs frequency translation from RF to baseband signals. Therefore, the mixer is directly connected to the output of the impedance transformation network. The passive mixer has been chosen in this design due to its high linearity, no dc power consumption and low flicker noise. This subsection describes the details of the design of passive mixer, especially its input impedance, conversion gain, noise performance.

A single-balanced passive mixer has been chosen over a double-balanced passive mixer because the former requires a fewer number of LO drivers which reduces power consumption. Furthermore, the conversion gain of a single-balanced passive mixer is 6 dB higher than that of the double-balanced passive mixer [57], [58]. A circuit schematic and the small-signal equivalent circuit for a single-balanced passive mixer are shown in Figure 63. This circuit consists of two switching transistors (M_1 - M_2), input capacitor (C_{in}), bias resistors (R_{Bias}), LO ac-coupling capacitors (C_{LO}) and loading capacitors (C_L). The LO ac-coupling capacitors are added to prevent low frequency noise flowing into the gates of switching transistors and to provide the flexibility for gate bias. V_{CM} and V_{Bias} at the gate set the gate bias of the transistors. For the small-signal equivalent circuit, $\overline{g(t)}$ and $\overline{g(t-T/2)}$ represent the switch conductance of the transistors associated with the LO and $\overline{LO}$, respectively [58]-[59].

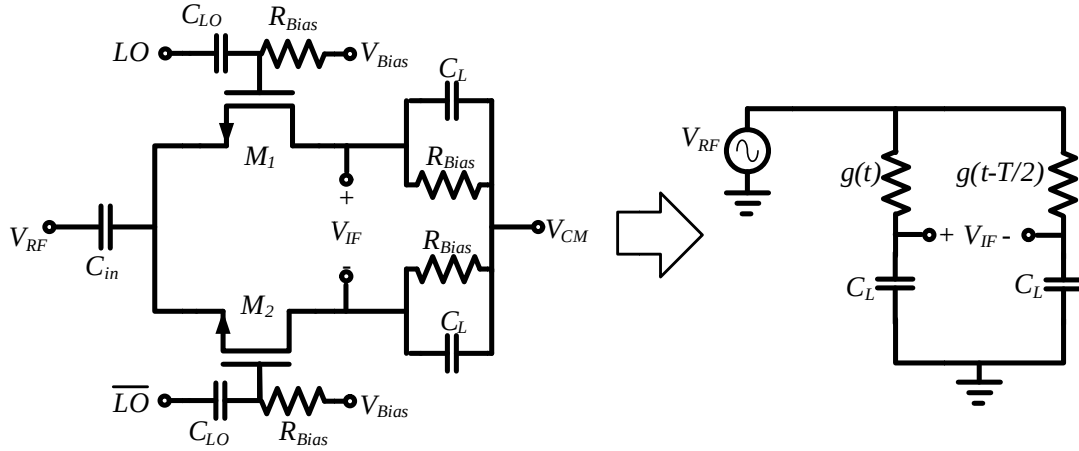


Figure 63: Schematic and small-signal equivalent circuit for a single-balanced passive mixer

To calculate the voltage conversion gain of a single-balanced passive mixer, a technique of square wave approximation for the conductance of switching transistors has been employed to simplify the analysis [57], [58] as shown in Figure 64. This square approximation consists of two out of phase switch conductance associated with the LO and $\overline{\text{LO}}$ driving at the gates of transistors M_1 and M_2 , respectively.

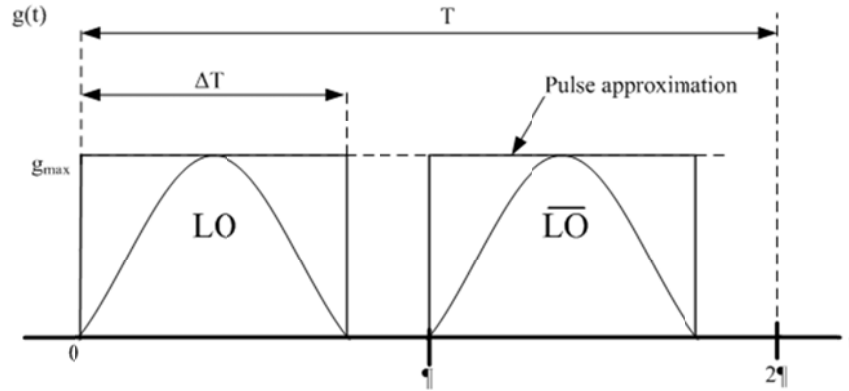


Figure 64: Pulse approximation for the conductance of the transistors

By using this technique and considering only the fundamental tone for the LO signal, the voltage conversion gain of the single-balanced passive mixer and its single-pole at the output can be approximated as [57]-[58], respectively:

$$G_{\text{conv, sin gle}} = \frac{2}{\pi} \sin\left(\frac{\pi \Delta T}{T}\right) \frac{T}{\Delta T} \quad (11)$$

$$\omega_{3dB} = \frac{\Delta T \cdot g_{\max}}{T \cdot C_L} \quad (15)$$

The input impedance of the passive mixer is another important factor since the output of the impedance transformation network is directly connected to the input of the passive mixer. Therefore, the input impedance of the mixer must be relatively high so that the impedance transformation network can provide enough voltage gain and appropriate impedance transformation ratio. The input impedance of the mixer depends on the frequency offset between the RF input signal and the LO switching waveform, the duty cycle and the characteristics of LO signal, the size of the switching transistors and the size of the load capacitors. Higher input impedance leads to smaller size of switching transistors and hence, lower power consumption in the LO driver circuit. However, the mixer noise performance degrades because the ON resistance is higher. Therefore, the optimum input impedance must be found. Figure 65 shows the simulated input impedance of a single-balanced passive mixer with varied RF input signal from 2.35 to 2.45 GHz.

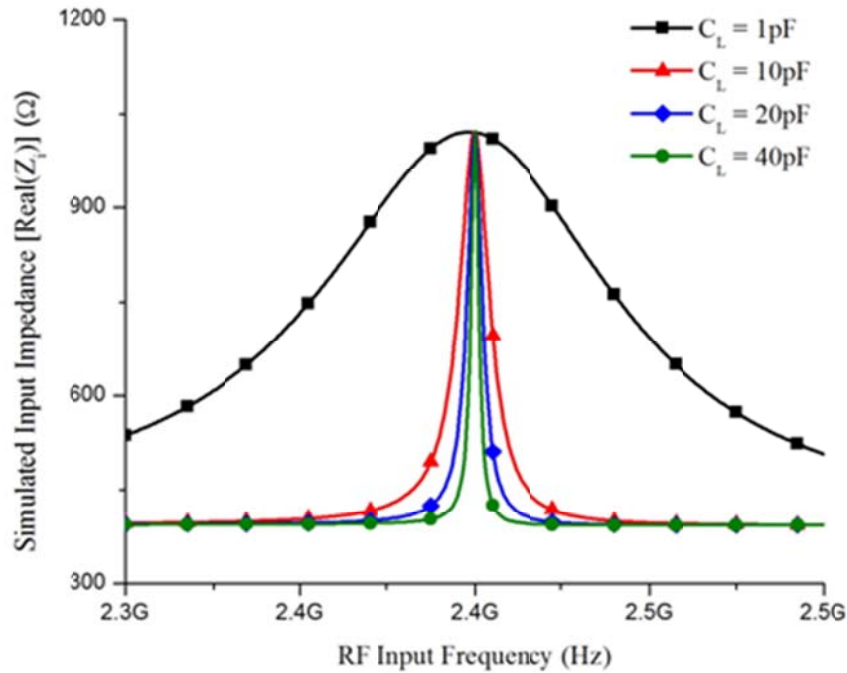


Figure 65: Simulated $\text{Real}(Z_i)$, of a single-balanced passive mixer vs. frequency ($W/L_{\text{Mixer}} = 1.6 \mu\text{m}/0.04 \mu\text{m}$, ideal LO drive with 0.5 duty, LO frequency = 2.4 GHz)

The source impedance used in this simulation is 1 kΩ which represents the output impedance of the impedance transformation network. This simulation result shows that the input impedance profile of the single-balanced passive mixer resembles that of an RLC resonator circuit with the center frequency and 3 dB bandwidth set by the frequency of LO switching signal and mixer output pole, respectively. The maximum input impedance occurs when the

frequency of the RF input signal is exactly the same as that of the LO signal and decreases to the minimum value as the frequency offset becomes larger. This frequency dependence is due to the attenuation from the output pole of the mixer (defined in equation (15)) when the frequency offset is much greater than this dominant pole [57]. Therefore, the signals at small frequency offsets can pass through the mixer but those at large offsets are attenuated at both the output and input of the mixer. The minimum level of the input impedance is determined by the size of the switching transistors. Due to the power consumption constraint in the oscillator and its output driver circuit, the minimum input impedance of the mixer is limited at $\sim 400 \Omega$. Although, the minimum impedance is not as low as a short circuit, some wideband interferers will still be filtered out at the mixer input, and it will improve the wideband linearity.

The other important factor for the passive receiver front-end is the noise performance. A mixer is a linear periodically time varying (LPTV) system which with a single frequency excitation can produce responses at a number of different frequencies [58]-[60]. Hence, all harmonics from the LO signal (mLO , where m is an integer) can down convert the associated RF noise, especially the thermal noise, and generate low frequency noise at the mixer output. Figure 66 shows the simulation result of the noise figure for a single-balanced passive mixer driven by an ideal LO square wave. It shows that as the size of the transistors increase, the noise figure decreases. At low frequency, noise figure increases due to the low frequency noise contributions described above.

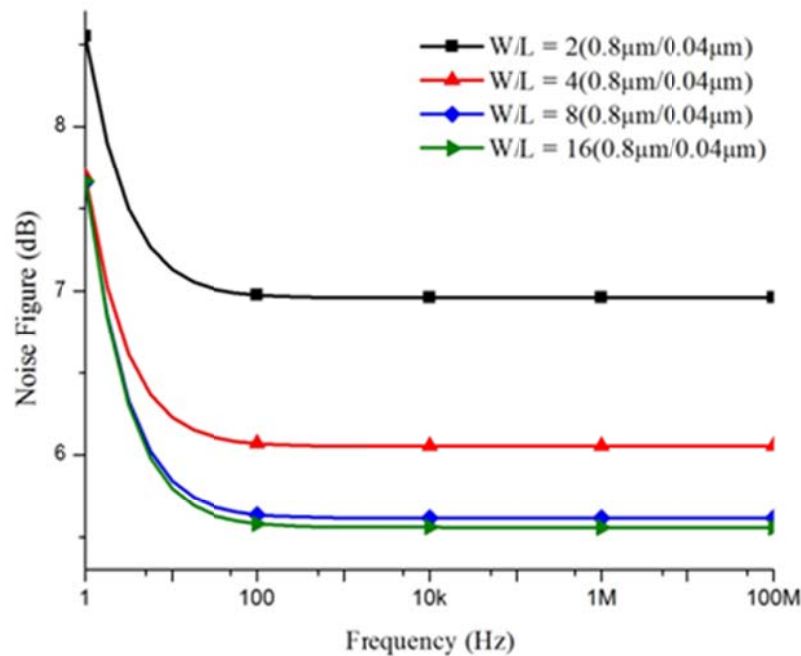


Figure 66: Simulated noise figure of a single-balanced passive mixer with various transistor sizes (ideal LO drive with 0.5 duty, LO frequency = 2.4 GHz, source impedance = 1 k Ω)

In general, the noise contribution of the passive mixer is mainly from the switches [59]; therefore, it is desirable to have very wide switches to reduce the on-resistance and associated thermal noise. However, once again, with the power consumption constraint, the size of the switches cannot be very wide. Fortunately, combining the passive mixer with the impedance transformation network can allow use of a smaller size for the switches while keeping the noise contribution from the mixer not too high due to the 50 Ω -to-1 k Ω impedance transformation ratio.

BASEBAND AMPLIFIER

The baseband amplifier is the first baseband stage following the mixer. A schematic of the baseband amplifier with gain control is shown in Figure 67. This circuit is based on an inverter amplifier with self-bias. Utilizing the current reuse technique, NMOS and PMOS transistors share the same bias current while increasing the total transconductance of the amplifier, $G_M = g_{mn} + g_{mp}$. Switches SW_1 - SW_4 are implemented by transistors and resistors R_1 - R_4 provide gain control step (6 dB per step) for the amplifier by applying bias voltage, 0 or V_{dd} , at the gates of these transistors.

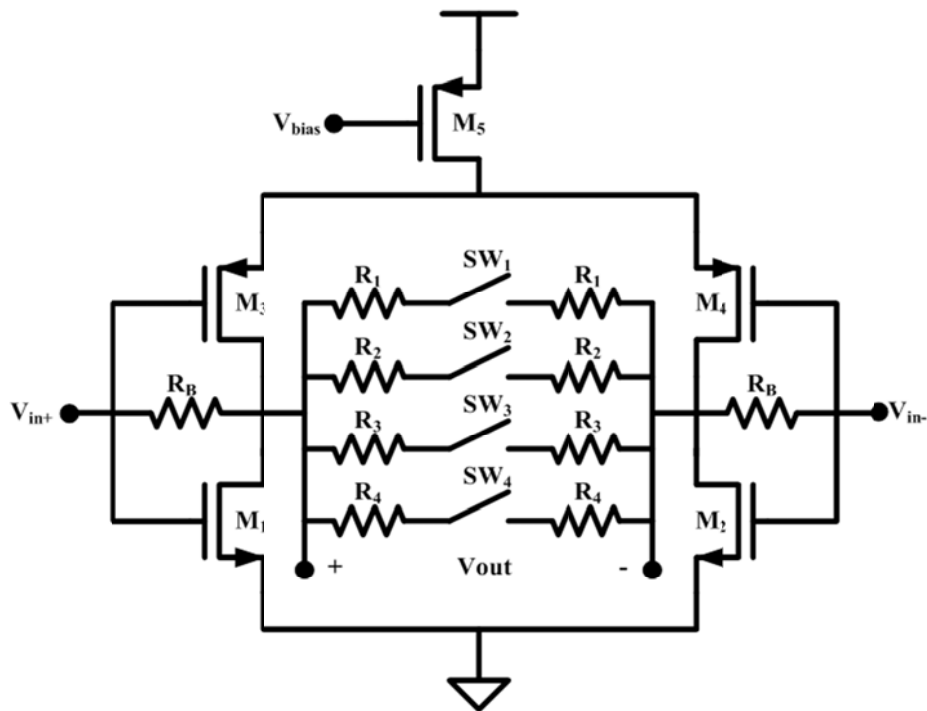


Figure 67: Baseband amplifier with gain control

Since the preceding stage of the baseband amplifier is purely passive, the noise contribution from the baseband amplifier becomes important, especially the low-frequency noise component, e.g. flicker noise. The current reuse technique to increase the total transconductance in combination with a larger device size ($W/L_{NMOS} = W/L_{PMOS} = 1689.6 \mu\text{m}/0.1$

μm) can mitigate the noise contributed by this stage without significantly increasing the power consumption.

LOCAL OSCILLATOR DRIVER

Due to the quadrature structure of the mixer as shown in Figure 57, an LO driver with 25 % duty cycle waveform is required to prevent the overlap in the switching waveform of the I-Q mixers and to improve the noise figure of the quadrature mixers [57], [61]. The inverter driver is chosen for the LO driver because of its compactness. Furthermore, with careful sizing the size of the mixers, the power consumption of the inverter driver can be maintained within an acceptable limit.

The circuit diagram of the LO driver and its input and output waveforms are shown in Figure 68 and Figure 69, respectively. Input of LO driver is a 50 %-duty-cycle quadrature signal provided by a ring oscillator. At the output, 25 %-duty-cycle LO waveforms are generated and used to drive the quadrature passive mixers. At the input, V_A , two cascaded inverters provide additional time delay to reduce the overlapping period for the output signals.

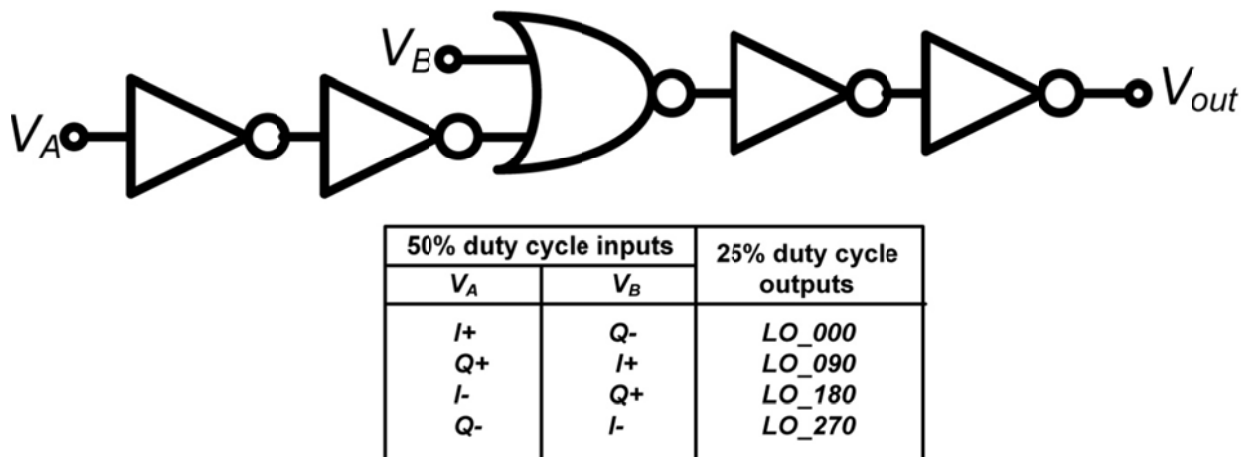


Figure 68: Circuit diagram of LO driver

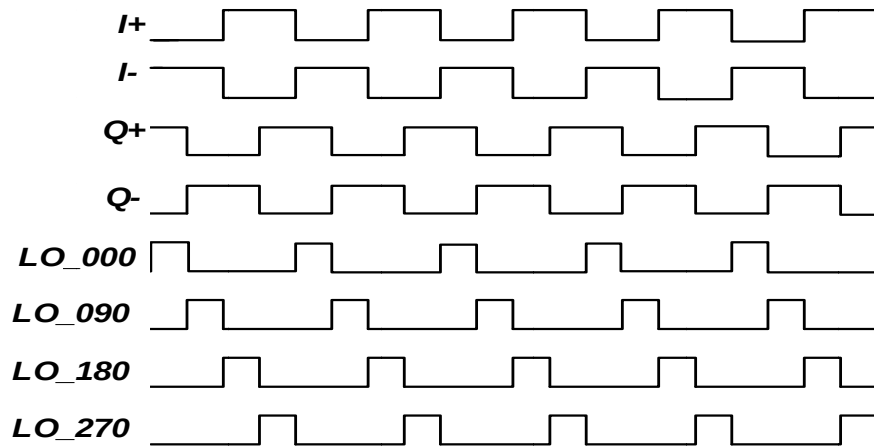


Figure 69: LO driver input and output waveforms

RECEIVER INTEGRATION AND SIMULATION

Figure 70 shows the simplified schematic of the μ Node receiver front-end used in the simulation. In this simulation, the LO driver is driven by the output stage of a phase-locked loop (PLL). The RF input is fed between capacitors C_1 and C_2 which form the impedance transformation network. The inductor in the matching network, L_1 , is an off-chip component implemented by a bond wire, printed circuit board (PCB) line and a high-Q chip inductor for tuning. Transistors M_1 - M_4 form the quadrature mixer for down converting RF input signal. The down-converted signal is passed through a low-pass filter formed by the output impedance of the mixer and the load capacitors (C_L 's) to filter out the high frequency component. These load capacitors are formed by the parasitic gate capacitance of the input transistors in the baseband amplifier stage. The baseband amplifiers are directly connected to the output of I-Q mixers. The DC voltage set by the baseband amplifiers and the DC bias for the LO signal, V_{BiasLO} , at the gates of the switching transistors determine the gate-source bias voltage for the mixers. The amplifiers with gain control capability amplify the baseband signal.

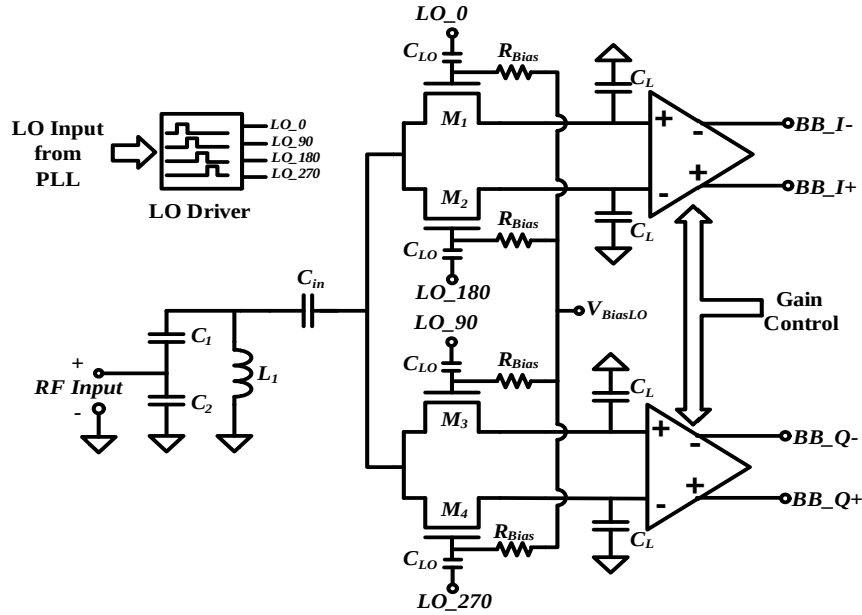


Figure 70: Simplified schematic of the μ Node receiver front-end

Figure 71 shows simulated SSB noise figure of the μ Node receiver front-end. At low offset frequencies, the noise figure is high due to the flicker noise contributed by the baseband amplifiers. As the offset frequency increases, the noise figure decreases and approaches the flat region which is determined by the thermal noise of passive mixers. The simulated noise figures are around 7.7 dB and 7.5 dB at 1 MHz and 10 MHz offset frequencies, respectively. Figure 72 shows the simulated voltage conversion gain of receiver front-end. The RF input signal frequencies varied from 2.4 GHz (-10 MHz offset) and 2.42 GHz (10 MHz offset) while the LO frequency is centered at 2.41 GHz. The voltage conversion gain profile of receiver is similar to that of a band-pass filter. This is due to the input impedance characteristic of passive mixer which provides only high impedance to the matching network when the frequency offset between the RF input signal and the LO is small. The maximum voltage gain of this receiver front-end is around 42.7 dB when $f_{LO}=f_{RF}$.

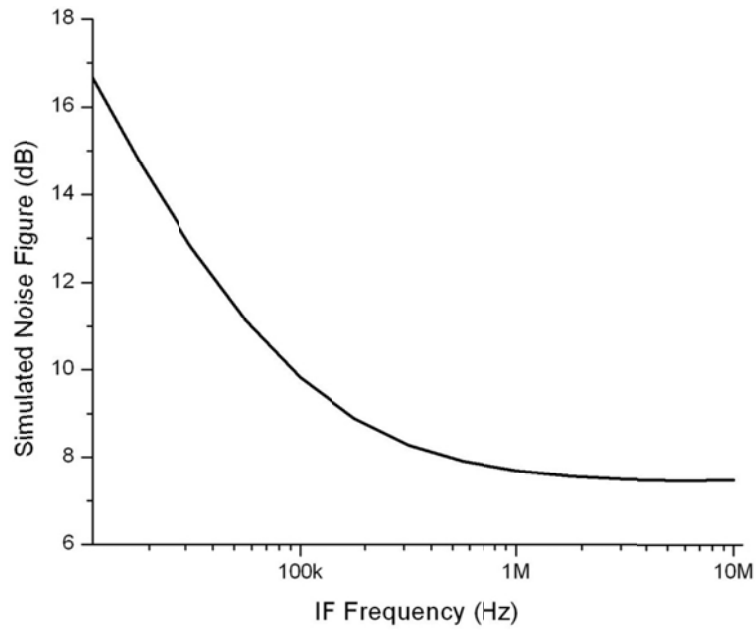


Figure 71: Simulated noise figure of the μ Node receiver front-end

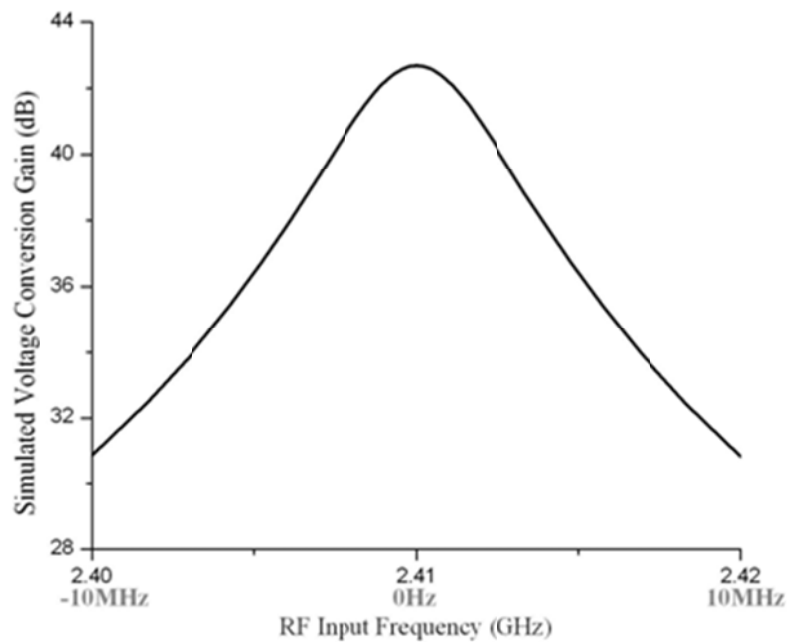


Figure 72: Simulated voltage conversion gain of the μ Node receiver front-end

Table 7 summarizes the simulated performance of the receiver as well as its power consumption. The total power consumption of the receiver front-end is around 1 mW with a 1.1 V power supply.

Table 7: Simulated performance summary of the μ Node receiver front-end

Specification	Simulated Result
Process Technology	45 nm CMOS
Supply Voltage	1.1 V
Bias Current:	
LO Driver (I&Q)	462 μ A
Baseband Amplifiers (I&Q)	438 μ A
Total	900 μ A
Operating Frequency	2.4-2.5 GHz
SSB Noise Figure @ 1 MHz	7.7 dB
Voltage Conversion Gain	42.7 dB
Gain Step	6 dB

INTEGRATED RECEIVER SUMMARY

The circuit designs and simulation results for the μ Node receiver front-end were presented and discussed above. Starting with the impedance transformation network in cascade with a passive mixer makes the receiver front-end fully passive. This reduces the power consumption of the receiver and provides acceptable receiver performance. The receiver front-end achieves simulated 7.7 dB noise figure at 1 MHz offset and 42.7 dB voltage conversion at total power consumption of less than 1 mW.

CLASS F POWER AMPLIFIER

Class-F power amplifiers use output resonators to control the output impedance to be open or short at harmonic frequencies. Figure 73 shows the schematic of the generic class-F power amplifier. For example, at odd harmonic frequencies the resonator impedance is infinite, and at even harmonic frequencies the input impedance is zero. In this case, the drain voltage waveform will add odd harmonics to build a square wave, and the drain current waveform will add even harmonics to build a half sine wave. Since there is 180 degree shift between drain voltage and current, there will be no harmonic power generated. Theoretically, a class-F power amplifier could achieve 100 % efficiency if transistor loss could be excluded. Waveforms for an ideal class-F PA are shown in Figure 74.

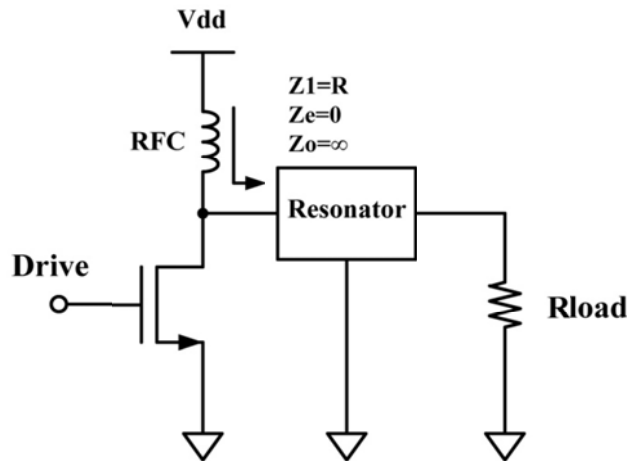


Figure 73: Generic class-F power amplifier

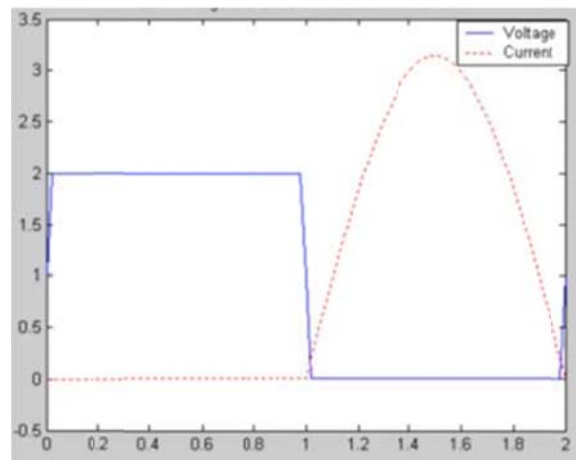


Figure 74: Voltage and current waveform of ideal class-F PA

CLASS F POWER AMPLIFIER CIRCUIT DESIGN

In CMOS PA design it is impractical to achieve a short-circuit for all voltage even harmonics and open-circuit for all odd current harmonics using only lumped passive elements because it requires many inductors which cost excessive chip area, and the efficiency improvement for higher order terminations is marginal. At the same time there will be power and efficiency loss associated with the relatively low Q on-chip inductors, thus using higher order resonator networks don't necessarily mean high efficiency. The present design uses only a third order harmonic peaking resonator, that is to say, ideally, the resonator impedance will be zero for $2f_0$ and infinity for $3f_0$. Figure 75 shows the schematic of the output resonator.

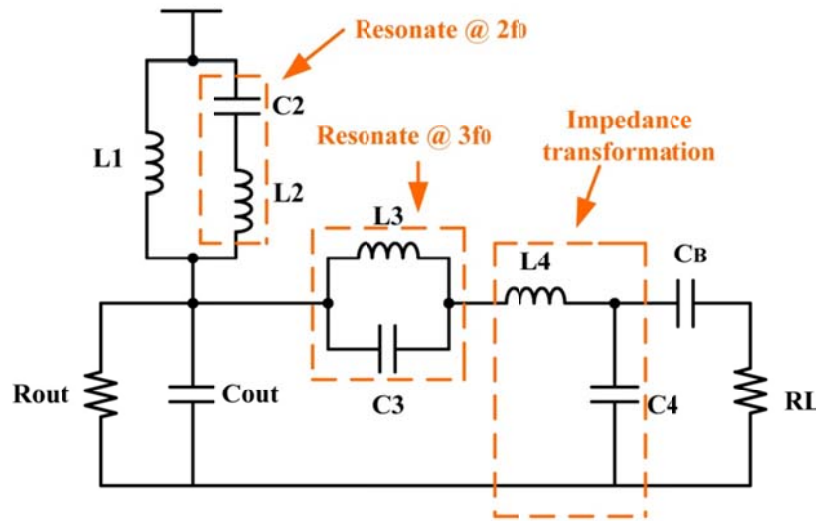


Figure 75: Output resonator circuit for a class-F PA

R_{out} and C_{out} form the drive transistor equivalent circuit. $L1 \sim L3$, $C2 \sim C3$ form the third harmonic peaking network. $L4$, $C4$ form the output impedance transformation network. $C2$ and $L2$ resonate at $2f_0$, while $C3$ and $L3$ will resonate at $3f_0$. At the fundamental frequency, the series combination of $L2$ and $C2$ behaves like a capacitor. Proper values are chosen for the combination so that it resonates with $L1$ and C_{out} , so the input impedance of $L1$, $L2$ and $C2$ is infinite and the drain of the transistor will only see the transformed impedance. At $2f_0$, $L2$ and $C2$ resonate to present zero impedance. At $3f_0$, the series combination of $L2$ and $C2$ behaves like an inductor, and proper values are chosen to make it resonate with $L1$ and C_{out} . At the same time $L3$ and $C3$ will also resonate, so the impedance looking into the resonator will be infinite at third harmonic.

Figure 76 shows the complete schematic of the 2.4 GHz class-F PA design. Four inverters were inserted as the PA driver. R_I (50Ω) and C_I were used to achieve input matching. There are two separate supply voltages, one for the output stage and the other one for the inverter driver. R_B is a bias resistor. The diode $D1$ is used as ESD (electro static discharge) protection. By-pass capacitors were also connected at the DC voltage supply and bias nodes.

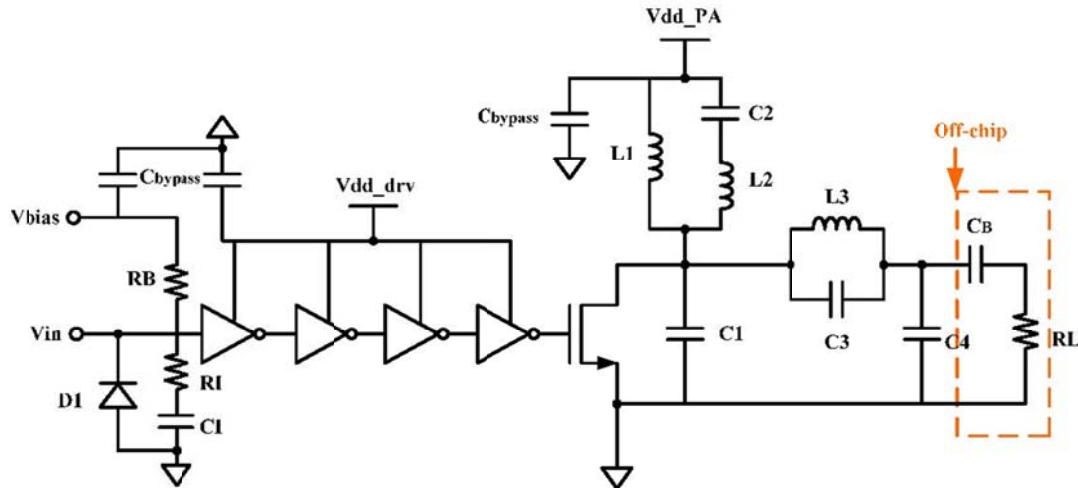


Figure 76: Class F power amplifier schematic

CLASS F POWER AMPLIFIER TEST CHIP

The output drive transistor must be sized wide enough to safely handle the output current. On the other hand, a wider transistor has larger parasitic capacitances. From load-pull simulations, the optimum width and length of PA transistor are 250 and 0.12 μm , with a finger width of 1 μm . The output capacitance C_{out} approximately equals to $C_{db} + C_{gd}$. As previously mentioned, C_{out} should be accurately estimated to set the component values in the output network. The parasitic capacitance of metal lines for transistor connections is significant and must be taken into account. The polysilicon gate is contacted from both sides to decrease the gate resistance. Since the transistor source is grounded, the source diffusion length is increased to 0.56 μm . This increases the separation between the source and drain metal connections and that between the source and polysilicon gate connections, which in turn reduces the parasitic capacitance. Figure 77 shows the layout cell for the PA output transistor.

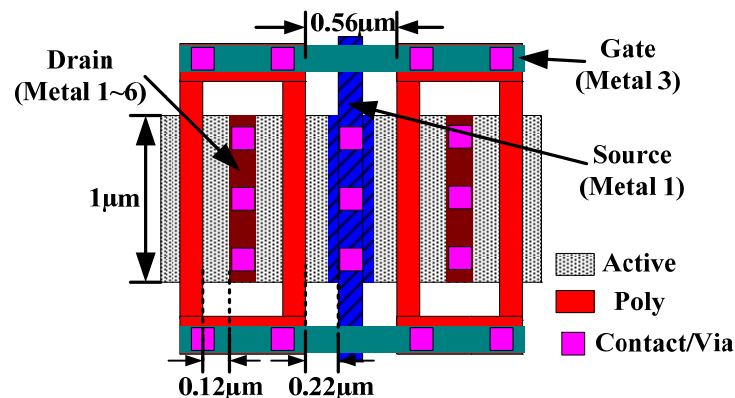


Figure 77: Layout cell for the PA output transistor

The transformed impedance at the fundamental frequency depends on the target output power and efficiency. There is a tradeoff between the output power and efficiency. To increase the output power, R_L should be smaller. This however lowers the efficiency because the ratio between the series resistance of inductor and R_L increases and the loss of the impedance transformation network increases. In the design, the target output power is 10 dBm. The maximum voltage at the drain node is limited by the transistor breakdown and reliability limit. For $V_{DD}=1.2$ V and 10 dBm output power, R_L of $36\ \Omega$ is chosen to maximize the efficiency.

The quality (Q) factors of the on chip inductors are critical. To decrease the inductor series resistance (thus increasing Q), the top two copper metal layers and Al-cap aluminum layer are shunted to form inductors L1, L2 and L3. The metal width is chosen to be $10\ \mu\text{m}$. The metal trace is $\sim 4\ \mu\text{m}$ above a polysilicon patterned ground shield. From ADS Momentum simulations, the quality factors of L1, L2 and L3 at 2.4 GHz are 7.6, 7 and 5, respectively.

A test chip was fabricated using the UMC 130-nm digital CMOS process with eight-layer copper metallization. Figure 78 shows the die micrograph of the power amplifier. The chip size is $0.6\ \text{mm} \times 0.7\ \text{mm}$ including bond pads.

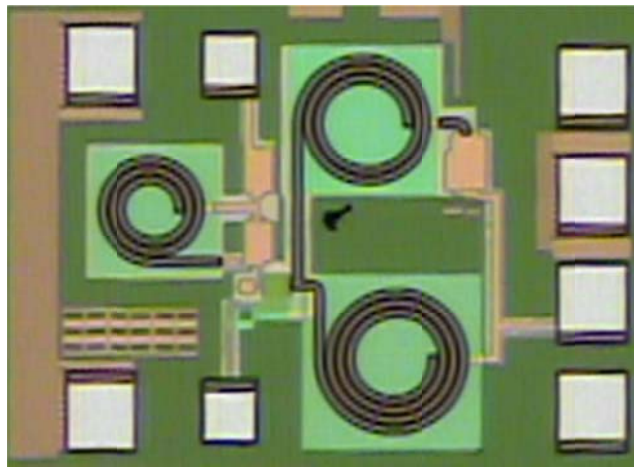


Figure 78: Die micrograph of the power amplifier test chip

MEASUREMENT RESULTS FOR THE 2.4 GHz CLASS F POWER AMPLIFIER

Measurements were performed on the power amplifier test chip to verify power out versus frequency and power out for different bias conditions. An HP8495A 50 MHz - 26.5 GHz power sensor was used to observe the output. The power losses associated with the measurement set-up and cabling were de-embedded. Figure 79 shows the simulated and measured PA saturated output power versus input frequency at $V_{DD}=1.2$ V for the driver and output stage and $V_{bias} = 0.5$ V. The output power peaks between 2.4 and 2.5 GHz, which was the design target. Figure 80 shows the saturated PA output power and power added efficiency (PAE) for varied bias conditions. The maximum output power of 10.9 dBm was obtained at $V_{DD} = 1.2$ V

for the driver and output stage with 0.54 V input bias voltage. The maximum power added efficiency was 31% at 10.5 dBm output power.

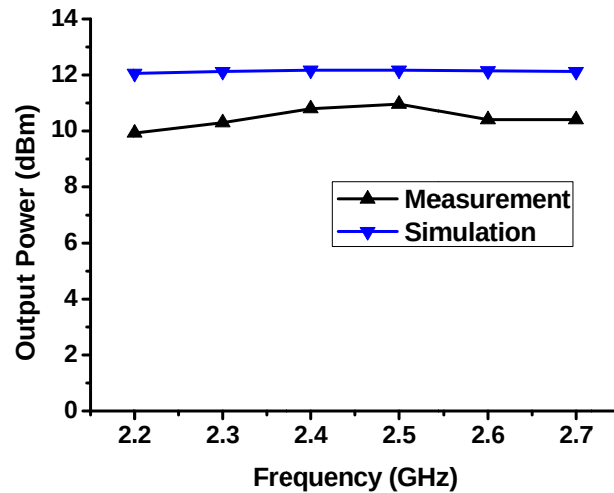


Figure 79: PA saturated power output versus frequency for Vbias= 0.5V and VDD=1.2V

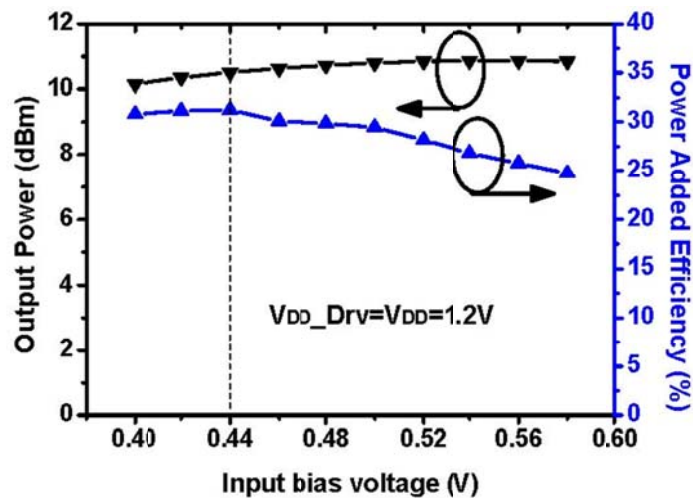


Figure 80: PA saturated output power and PAE for different input bias with VDD=1.2V

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