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Three main challenges to applying an all-electric architecture to smaller, quarter-scale prototype Navy vessels are pursued along with several related topics that have arisen over the course of the project as manpower became available as the initial tasks were completed. The three main challenges are: 1) Faster and more effective charging system for charging the main batteries in a quarter scale prototype destroyer, increasing the capacity eightfold within the same charging time, 2) Redesign of an uninterruptible power supply battery bank on the quarter scale prototype destroyer and charging system for fourfold greater service, and 3) Mitigation system for voltage sags experiences on the LSV2 prototype submarine. Additional problems addressed by the project team include: a) Feasibility study and design study for the addition of fuel cell energy storage to the prototype destroyer to either to replace or supplement existing battery based system, b) Design of data acquisition system for the prototype destroyer with emphasis on monitoring electrical system performance and battery condition, c) Battery charger control for the LSV2 prototype submarine, d) Analysis and design of a fast fault detection scheme for medium voltage direct current power systems, e) Evaluation and development of fault detection scheme for ungrounded and high resistance grounded medium voltage ac power distribution systems, f) Develop model of AESD electrical system in RTDS, and several other subprojects.

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## Technical Section

### *Technical Objectives*

Three main challenges to applying an all-electric architecture to smaller, quarter-scale prototype Navy vessels were defined in the initial proposal. The three main challenges are:

1) Faster and more effective charging system for charging the main batteries in the Advanced Electric Ship Demonstrator (AESD) quarter scale prototype destroyer, increasing the capacity eightfold within the same charging time,
2) Redesign of an uninterruptible power supply battery bank and charging system on the AESD for fourfold greater service, and
3) Mitigation system for voltage sags experienced on the LSV2 prototype submarine.

Several additional projects were defined in consultation with ARD-Bayview and other contacts at NSWC-CCD and our ONR project officers, with a few more added this year. These subprojects are:

a) Apply an alternate generation source such as a fuel cell to the prototype destroyer to either to replace or supplement existing battery based system,
b) Design of data acquisition system for the prototype destroyer with emphasis on monitoring electrical system performance and battery condition,
c) Battery charger control for the LSV2 prototype submarine,
d) Analysis and design of a fast fault detection scheme for medium voltage direct current power systems,
e) Evaluation and development of fault detection and prioritized tripped scheme simultaneous phase to ground faults in ungrounded and high resistance grounded medium voltage ac power distribution systems
f) Develop model of AESD electrical system in RTDS
g) Integration of the various UPS battery banks on the AESD into a DC microgrid. This microgrid could possibly be expanded to include the propulsion batteries.
h) Design of a graphical user interface to control the battery charging process on the LSV2 test platform at ARD Bayview.
i) Evaluation of trade-offs with maintaining high levels of power quality on the entire distribution system versus concentrating on point of use power management. Present systems seek to do both.
j) Development of subsynchronous oscillation development schemes

Solutions to each of the challenges are based on a system approach to the problems at hand.

This work is intended as part of a long-term effort to realize the vision for a power management research and teaching program for the Navy's base at Bayview, Idaho. The University of Idaho offers the academic talent, including research and teaching, from its growing electric power engineering program. The project is designed to attract the region's students, nearly all of which are U.S. citizens and enjoy what North Idaho has to offer, into the field of electric power engineering. This is the next step in an ongoing effort to build a resource that serves the entire Navy with electric power management expertise, based in north Idaho. The Navy as a whole faces a deficit of trained electric power engineers, so developing this vision opens a valuable source of trained people and technical expertise for the Navy and benefits the economy of the region and the State of Idaho.

### *Technical Approach*

The general approach for each of the subprojects described above has been to have teams of undergraduate and graduate students pursue each task. In every case the approach for each of the subprojects listed in the objectives started with a period of project learning, followed by development and implementation of a computer simulation model. Hardware prototypes were built and results were matched with the simulation models. The simulation model was then rescaled to present a design for the full scale system. The students presented their results in conference papers, with preliminary work presented in student poster competitions.

For challenge 2, and subprojects a) and c), we started with a senior design team sponsored on a small contract from ARD-Bayview to perform the initial project research and proof of concept design. A Master's student (or a senior entering their final semester) worked with the senior design team during the second semester and then continued the work to final completion and extend the project beyond the focused scope of the senior design project. This model was also used in subproject b), where the senior design project was sponsored by the main DEPSCoR grant to improve data available to implement solutions for challenges 1 and 2.

Subprojects d) and e) are being performed by students who had other support but were interested in working on projects related to shipboard power systems. The student who started subproject d) works on system protection and control studies for a consulting firm in the region. He was an instruction for the Navy in South Carolina prior to starting his current job. He brings his work experience to this project, including his knowledge of current protection practices for terrestrial power systems, especially working with wind farm collector systems. Two students worked on different aspects of subproject e). One was a part time Master's student who pursued his degree through distance education and now is working on a Ph.D. This student is an engineer working at a naval shipyard in Mississippi and was interested in pursuing a topic that solved a problem that was not directly related to his job. The second student is a full time graduate student on campus. Subproject f) is being done by a full time Masters student. Subprojects g) and h) started as a senior design project and was completed by a Masters student. Subprojects i) and j) were started by Ph.D. students who have not completed their degrees at the time of this report. They are both working full time in industry and completing their dissertations on a part time basis.

The remainder is this report is compiled from student reports, theses and technical papers. As a result the writing style and figure numbering style will change from section to section.

***Final Status***

## *Challenge 1: Faster and more effective charging system for charging the main batteries in the Advanced Electric Ship Demonstrator (AESD) quarter scale prototype destroyer*

This topic was the focus of a Master's thesis, titled "Harmonic Distortion Mitigation for Electric Vehicle Recharging System," completed early June 2009 by John Finley. The thesis has been forwarded to ARD Bayview.

The current harmonics produced from the operation of the battery chargers produce system conditions that cause the control circuitry of the battery chargers to malfunction. The AESD has 12 battery strings, each with sixty 12V cells. There are 12 commercial battery chargers, each of which consists of two individual charger units connected in parallel on the ac side and in series on the dc side in order to achieve the maximum voltage needed. At the time they were manufactured, there were two variants of the battery charger, each of which the user's manuals describe as power factor corrected to minimize harmonic distortion. One variant was designed to operate from a 208V three phase supply, and the other from a 480V three phase supply. The chargers used on the AESD are designed to operate from a 480V supply, which can either come through a shore power connection or from an onboard diesel generator for charging between test runs. Figure 1 shows the converter layout. The buck converter maintains the input voltage to the inverter at a fixed level. The 208V version has a boost converter in place of the buck converter, which should provide very good harmonic power factor correction.

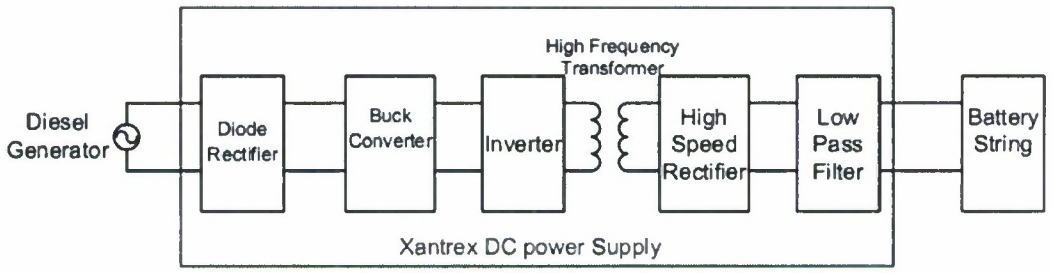


Figure 1: Battery Charger Block Diagram

The buck converter does not provide any assistance in correction of the current harmonics drawn from the rectifier. The inverter appears to be controlled to provide some degree of power factor correction, but the harmonic distortion is still significant. Figures 2 and 3 show one phase of the input current waveform when the voltage applied to the batteries is low (150V) and relatively high (400V) measured on experimental tests on one of the battery charger units in our lab. These values are chosen because they are typical values for the two units. The lower of the two units in each pair is operated at constant 400V output and the top unit varies its voltage during charging.

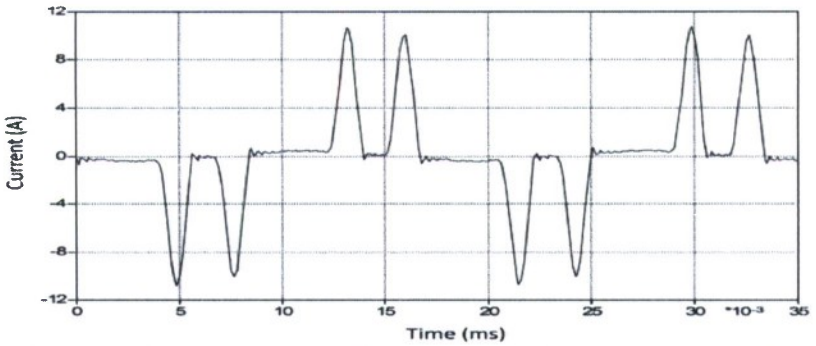

Figure 2: AC current waveform for 150V dc output operation

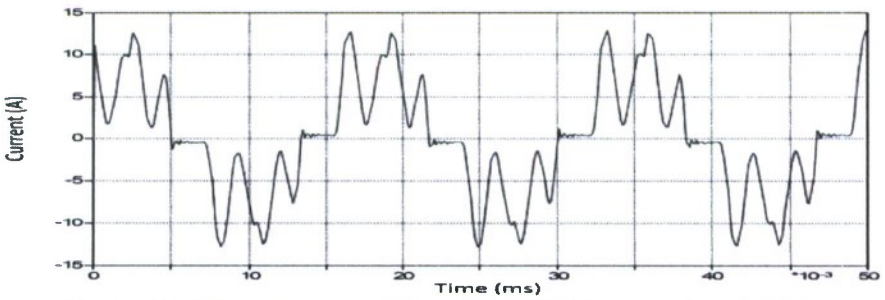

Figure 3: AC current waveform for 400V dc output operation

One can observe from Figure 3 that there is some wave shaping taking place in the battery charger, but the voltage distortion is still significant. The net current when these are added in parallel is dominated by the waveform in Figure 3. When this current passes through source impedance, the voltage applied at the rectifiers is distorted by the harmonic voltage drip. The source impedance when charging from shore power is lower enough that the voltage distortion tends not to limit charging. However, the effective impedance of the onboard generator is much higher, and the voltage distortion is severe enough that the chargers shut down if all of the chargers are operated at the same time. Figure 4 shows the voltage at the generator terminals with half of the chargers operating. The system cannot operate from the generator with more chargers operating, significantly increasing the time to recharge the propulsion batteries.

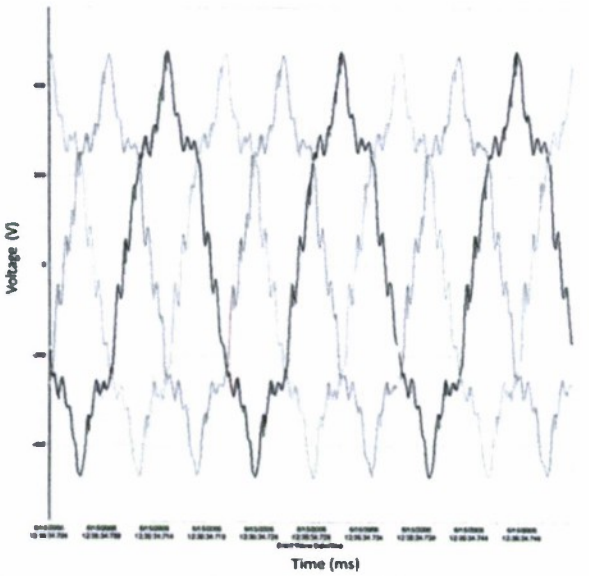

Figure 4: Generator terminal voltage with six chargers operating

Extensive research was conducted to properly characterize the battery charger to design appropriate solutions for harmonic mitigation. Three harmonic mitigation techniques are presented to reduce the harmonic emission of a diode bridge rectifier used to recharge the main propulsion batteries of an electric vehicle. Research was conducted to properly characterize the battery charger to design appropriate solutions for harmonic mitigation. The solutions presented are described below.

a. Better utilization of the internal harmonic mitigation inherent to the battery chargers
   The harmonic mitigation in the power supply improved as the voltage was increased. One strategy explored is to increase the output voltage of the lower charger in each part to its maximum output voltage of 600V. This is still below the minimum allowed discharge level of the battery banks. Figure 5 shows the resulting current waveform, compared to an ideal sine wave.

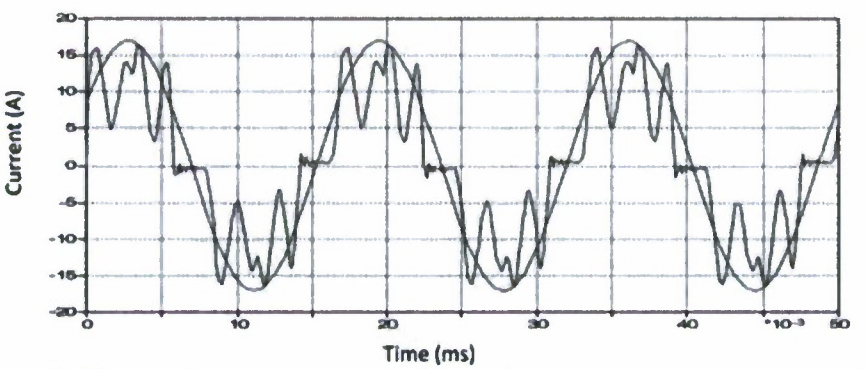

Figure 5: Charger input current waveform when output voltage is 600V dc.

While this approach does improve the total harmonic distortion of the current drawn by the rectifiers over the range of charging operation, it is not sufficient to allow all 12 chargers pairs to operate simultaneously from the generator.

b. Increasing the effective pulse number of the diode bridge
The second option explored was connecting the chargers in either a 12 pulse or a 24 pulse configuration by adding an input transformer. The 12 pulse converter connection is shown in Figure 6. The key to this configuration is having half of the load supplied through a wye-wye connected transformer and the other half through a wye-delta connected transformer. The thirty degree shift will result in cancellation of harmonics on the order of odd multiples of 6 plus/minus 1. So for example, the $5^{th}$ and $7^{th}$ harmonics are eliminated through cancellation, while the $11^{th}$ and $13^{th}$ add to the same value they would have without this connection. The main benefit of this configuration is the cancellation of the $5^{th}$ and $7^{th}$ current harmonics, which are the largest drawn by the chargers.

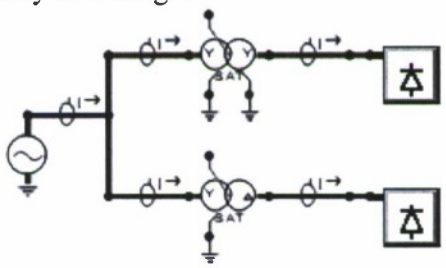

Figure 6: 12 pulse connection of battery charger rectifiers

The rectifier symbols in Figure 6 each represent six battery charger sets connected in parallel. An additional transformer needs to be added to the AESD in order to implement this solution. There is a suitable space available on board for this transformer. Figure 7 shows simulation results with the current battery charger operating modes and 12 pulse operation. Note that the current is still fairly distorted, but will most likely allow all 12 chargers to operate simultaneously, although we were unable to verify experimentally with only one charger.

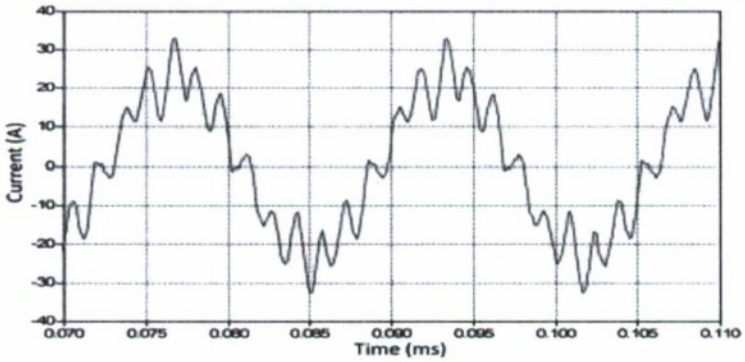


Figure 7: Input current waveform for 12 pulse operation

Another option is to create a 24 pulse rectifier. In this case, the voltage waveforms applied to the rectifiers are offset from each other in 15 degree increments. This results in the lowest current harmonics supplied by the being either the $23^{rd}$ and $25^{th}$, and then the $47^{th}$ and $49^{th}$ harmonics, and so on. Transformers to create this phase shift usually require a zig-zag transformer in addition to the wye and delta shifts, as shown in Figure 8. Figure 9 shows the resulting current waveforms supplied by the generator.

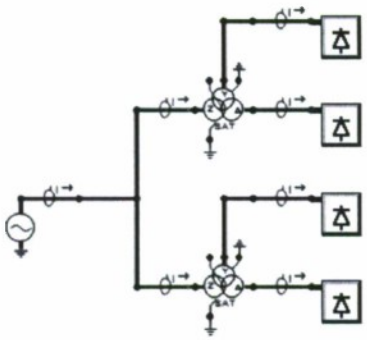

Figure 8: Twenty four pulse rectifier connection

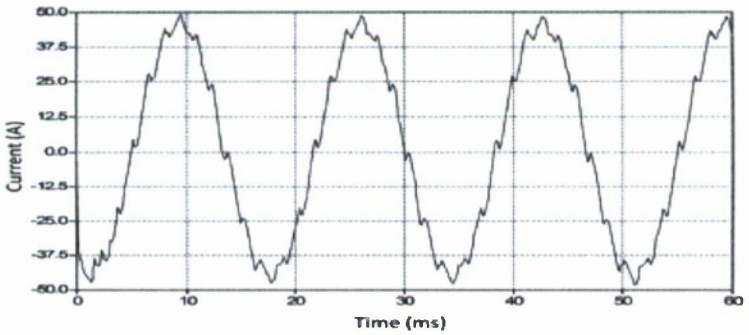


Figure 9: Generator currents under 24 pulse operation.

This transformer will generally take more space. However, one is already available on the AESD in the form of the transit transformer. This is used to run the propulsion motors from the generator when moving the shift from the dock to the test range. Study of the transit transformer shows that there is a place to wire in the rectifiers. Contactors would need to be added to allow the diesel generator to either supply the chargers or the propulsion drive. Figure 10 shows the general layout, with lines leaving the transit transformer to go both to the switch gear for the motor drives and to the battery chargers.

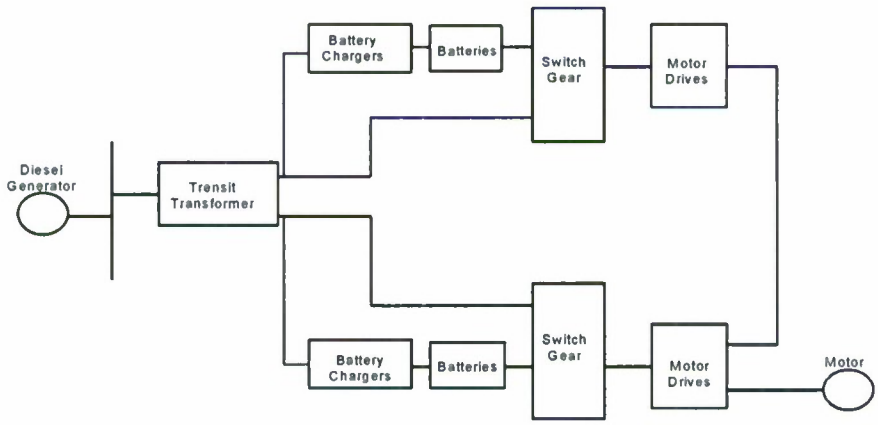


Figure 10: Twenty four pulse rectifier operation with transit transformer

c. Adding harmonic filters

The final approach studied in depth is to add harmonic filters. Harmonic filters can take the form of either passive filters or active filters. To get effective filtering in this case the bandpass LC filters would need to be applied to the largest harmonic frequencies. These are connected in parallel with the distribution system and need to provide a much lower impedance path for the harmonic currents than the path through the source. This is difficult to do in the space available. In addition, the filters would need to have very high quality factors in order to filter an acceptable percentage of each harmonic.

Active filters use a power electronic converter in a current regulated PWM control mode controlled to draw the harmonic currents measured on the distribution lines to the converter. A single filter can remove a wide range of harmonic frequencies. This will involve a higher upfront cost, and increase losses. But it will take less space. Figure 11 shows a simulation using a simple active harmonic filter turned on part way into a simulation run. The current harmonic THD is reduced from approximately 60% to 2.5%.

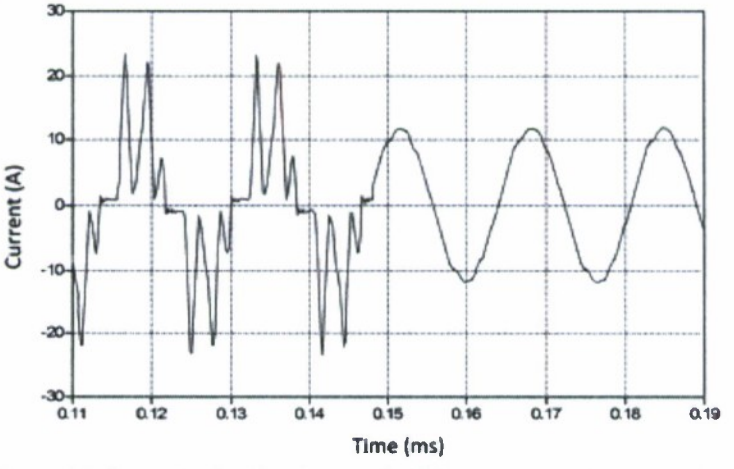


Figure 11: Impact of active harmonic filter on generator current

The key to application of any of these solutions is how the terminal voltage waveform at the generator is improved. Figure 12 shows the simplified circuit representation of the generator. Note that the voltage drop across the generator impedance is a function of frequency. The inductive reactance increases as the harmonic order increases. So even though the harmonic currents are small compared to the fundamental, they are dropped across a larger impedance. The generator reactance is based on the sub-transient inductance for the harmonic terms since the non-60 Hz currents will couple to the damper bars.

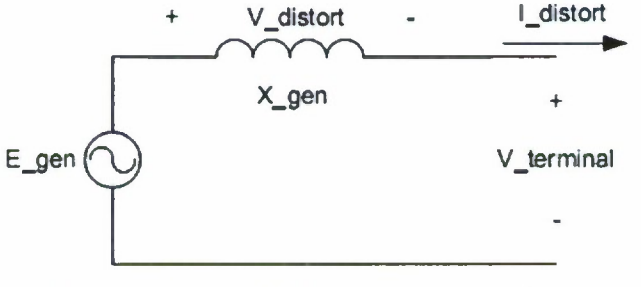


Figure 12: Simplified generator equivalent

Figures 13-16 show the voltage waveforms for the different cases. Figure 13 shows the present situation with six chargers. This is a good match for Figure 4. Figure 14 shows the results for a voltage adjustment (option "a" above) with six chargers. The waveform is definitely improved, allowing at least a few more chargers to run. But as shown in Figure 15, the waveform is still severely distorted and will probably exceed the threshold for tripping the rectifiers. Figure 16 shows simulation results with the voltage with a 24 pulse rectifier connection used. No obvious distortion is visible in the waveform. The results are the same with the active filter present.

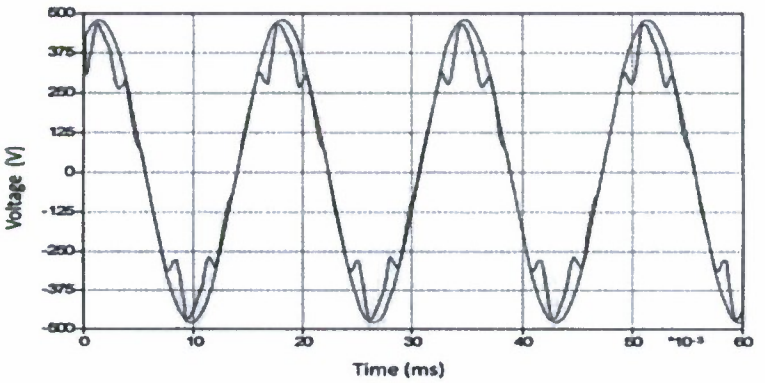


Figure 13: Phase A voltage (with clean reference) with 6 chargers and present control and configuration

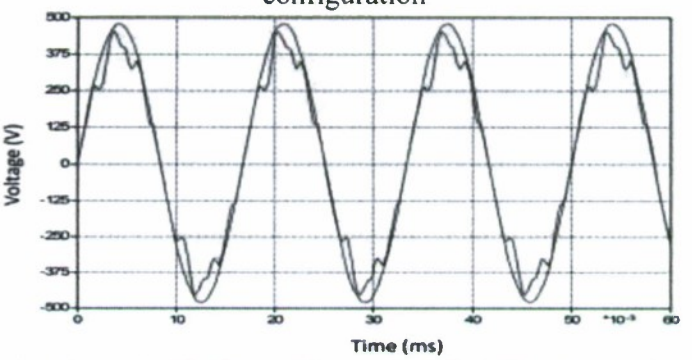


Figure 14: Phase A voltage (with clean reference) with 6 chargers and voltage adjustment solution applied

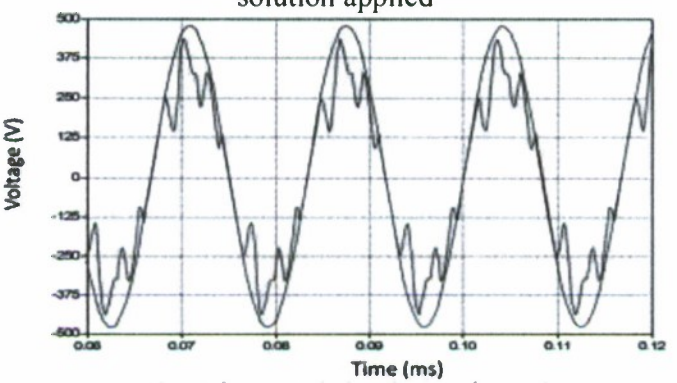


Figure 15: Phase A voltage (with clean reference) with 12 chargers and voltage adjustment solution applied

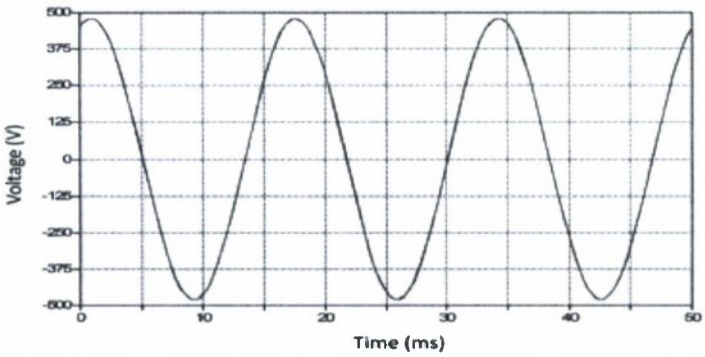

Figure 16: Phase A voltage (with clean reference) with 12 chargers and 24 pulse rectifier configuration applied

This project task is completed. A paper from this task was published in the proceedings of the 2011 North American Power Symposium.

## *Challenge 2: Redesign of an uninterruptible power supply battery bank and charging system on the AESD for greater service*

Uninterrupted Power Supplies (UPS) are currently used to power monitoring and control equipment on the AESD during test runs. The test runs cover a period of approximately 10-12 hours. After each test run the generator is switched on for short 15-30 minute periods as the data is compiled. This charging time is not sufficient to fully recharge the UPS batteries. Eventually the batteries are largely depleted, and approximately half way through the testing day the batteries the batteries are charged by the generator for a 2 hour period. Of the four UPS packs on the ship, number 3 is the first to deplete initiating the 2 hour recharge period. The focus of this project is improving the performance of UPS-3 and improving the charging time.

This project challenge has been broken down in several parts, each of which has been addressed by a different group of students.

Task 1: Develop fast charging algorithm

Several charging algorithms have been reviewed. The current charging algorithm used by the UPS requires 2 hours to deliver 90% state of charge. An algorithm has been found that can restore this amount of energy within 30 minutes (See Figure 17). An obstacle to implementing this algorithm is the high current requirements needed. Research is being made to implement a similar algorithm with lower current demands, but still improved recharge times over the existing system. Ultracapacitors have also been considered for use as additional storage. As the batteries reach higher states of charge, they accept less and less current. During the recharge process the current is dropped in steps as higher states of charge are reached, and the unused energy could be routed to the ultracapacitors.

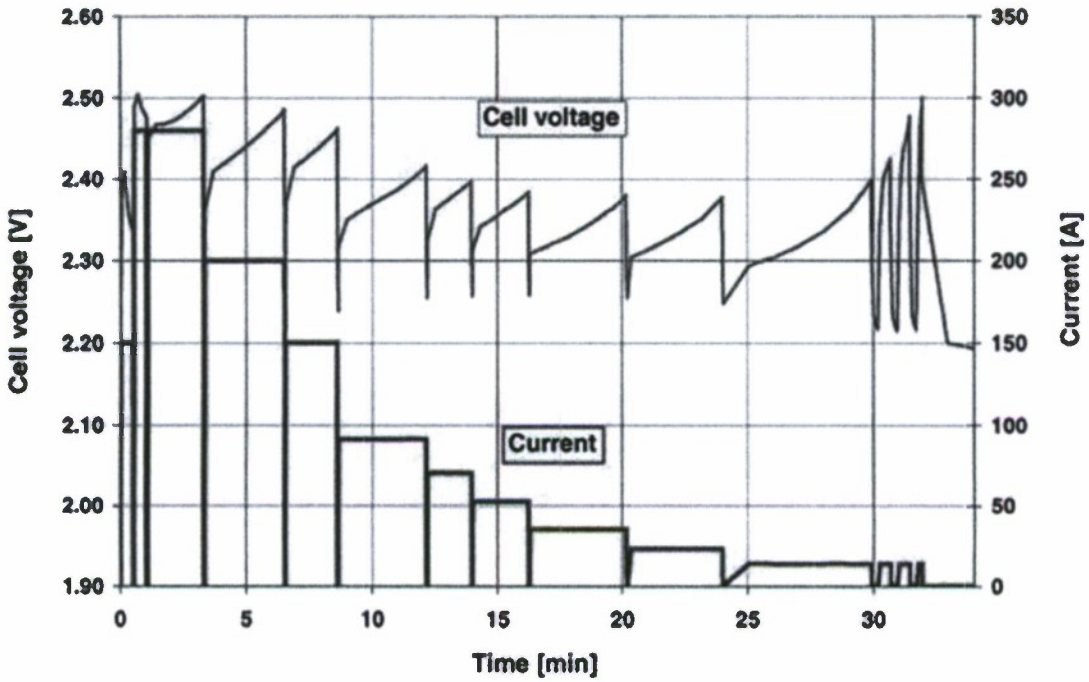


Figure 17: Current step-down fast charging procedure.

Another benefit of this fast charging algorithm is the life span of the batteries is extended. Please refer to figure 18. Previous experimentation in published papers has shown a 40% longer cycle life for batteries with fast charging.

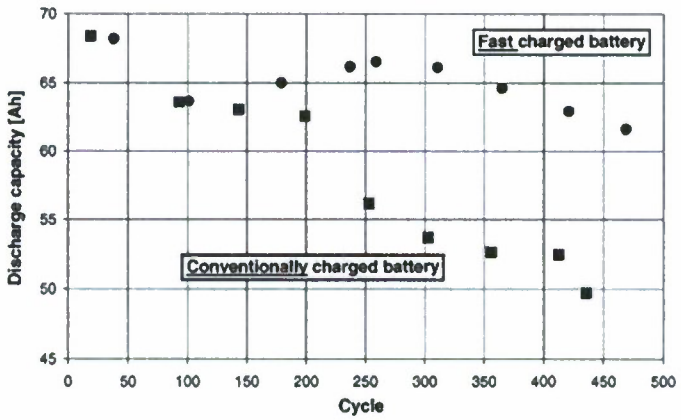


Figure 18: C/5 capacity measured during the regular capacity check-ups carried out each 50 cycles for conventional and fast charged batteries.

A proposed solution is to add an additional charger and 10 33Ah batteries as an additional source to UPS#3 (Figure 19). The fast charger will be able to supply the needed currents and the batteries are already available. This reduces the cost of installing the new system and a less expensive power supply can be used.

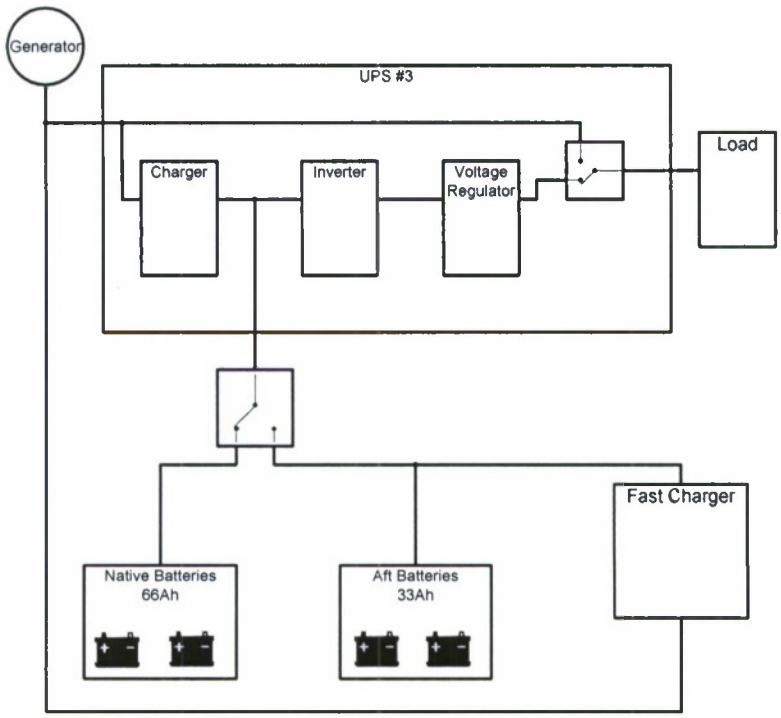


Figure 19: Integration of fast charging with the current system.

Task 2: Improve Battery Performance through Charge Equalization

This topic applies to both the propulsion batteries and the UPS batteries.

The graduate student working on this has explored research ideas and created a research path for myself. This has included reading technical papers on topics of batteries, battery charging, battery charge equalization, and electric circuit based modeling of batteries. Two papers were selected to follow up on in battery charge equalization. They are entitled Switched Capacitor System for Automatic Series Battery Equalization (Pascual and Krein) and Balance Charging Circuit for Charge Equalization (Hsieh,Moo,Tsai).

From the papers two computer models were created to simulate the charging and equalization of the AESD batteries. The first model is referred to as "SwitchedCap" because it is a switching capacitor was created in LTSpice IV. It originally had 6 batteries to equalize but to allow it to run a bit quicker in simulation it was pared down to just 3 batteries. The idea behind the model is that a capacitor is switched in and out across the battery terminals. If the capacitor has a higher voltage than the battery then it drops charge onto the battery. If it has a lower voltage then the capacitor is charged and drops charge onto the next battery in the string. It is an automated self leveling system.

The second model for equalization is a Buck-Boost converter model. The basic idea is that an individual battery voltage is compared to the average voltage of all batteries. If the voltage is higher than the average, the Buck-Boost converter is turned on and routes charge around the

battery where it is deposited onto a battery below the average value. A Matlab model was created to simulate its operation. Checking for proper operation can be done by a simple plot of controller on/off switching and voltage of the battery at the time of switching. For the actual implementation on the boat we expect a microcontroller will be used to handle decision making and switching. For both models the switches chosen are MOSFETS because they have no moving parts and are highly reliable. The student is now to the stage where he is ordering hardware to attach to the batteries and collect initial data to show the concepts work.

Finally, the student has created an economic model to show the value of charge equalization. The model showed how much equalization would be needed in order to pay for the hardware and installation. The model is implemented as a spreadsheet.

Task 3: Develop DC-DC Converter with Large Step-Down Voltage Ratio for Electric Vehicle Applications

In electric vehicles, there is a significant requirement for stepping down battery voltages to power convenience loads and emergency loads. There are many resources regarding stepping down battery voltages. Conventional methods put two buck converters in series as shown in Figure 20. However, in order to make the output as small as possible, those schemes select a really small duty cycle. This sets a high requirement for filtering circuits.


Figure 20. Conventional method to step down battery voltage

The large step-down DC-DC converter here focuses on a very small output/input ratio with midrange duty cycles. Application involves boosting to batteries for emergency back-up power. Also, in the oil well industry, 240V is standard for piston in communications and 5V is common for powering digital instruments.

DESIGN

The specifications of the converter are as follows:

- 240 volts input
- Duty cycle: <85% buck side, >15% on the boost side.
- 10-20 volts output;
- Output ripple less than 7%

Figure 21 shows the scheme of the design.

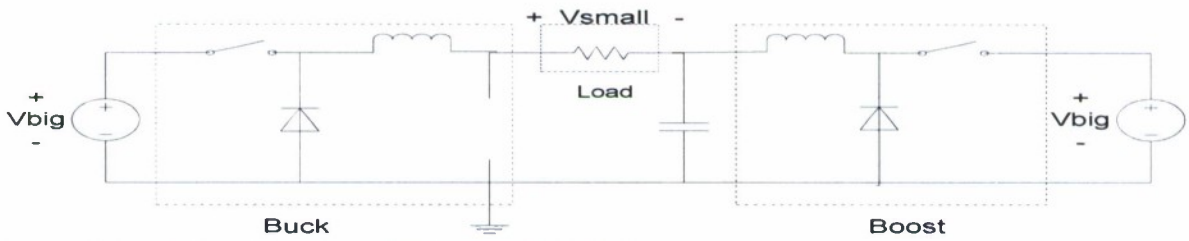


Figure 21. Basic Model for Large Step-Down DC-DC Converter

In this configuration, a buck converter with a 240V DC input is placed in series with a boost converter with a 240V output. A low-voltage load is placed in series with a boost converter, floating between the buck and boost converters. Since the output is the difference between the buck output and boost input, the duty cycles for both converters don't have reach extreme. Because a midrange duty cycle is used, filtering requirements are much less than for the conventional method of putting two buck converters in series. The same source as the input is placed at the end of the boost converter. Therefore, some of the power flows back to the same source, which raises the efficiency significantly.

## SIMULATION AND FREQUENCY ANALYSIS

Simulation was used to acquire much of the information describing the output behavior of the DC-DC converter. Although the input voltage of the converter can be within a wide range, 240 volts is used in the simulation because it is standard in many applications, for example, the piston voltage in the oil well industry. The pulse voltage controls the MOSFETs to function as switches. The output loads can be simplified as a 20 ohms resistance. Figure 22 show the schematic of the converter using LTSpice.

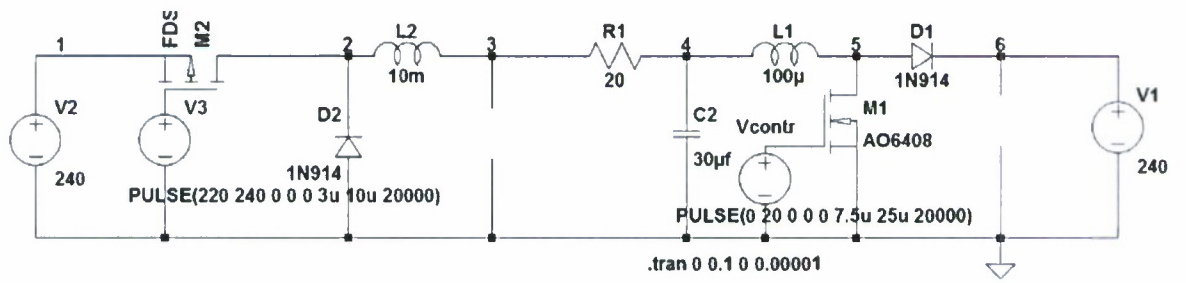


Figure 22. Large Step Down DC-DC Converter Schematic

Figure 23 shows the simulation result with 80% of duty cycle, 100 kHz frequency on the buck side and 30% duty cycle and 40 kHz on the boost side.

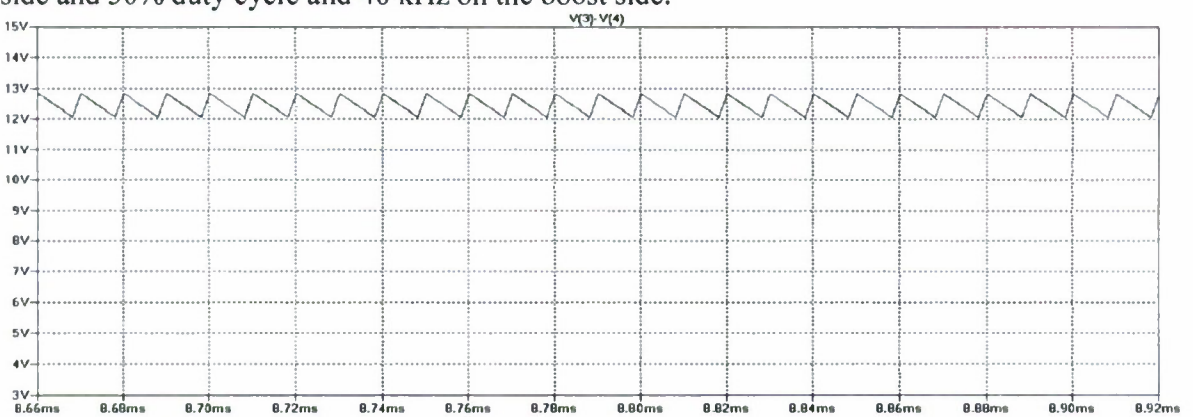


Figure 23. Simulation of the Converter's Output Performance using LTSpice

The output voltage and the voltage ripple are influenced by many parameters in the converters.

a) A bigger duty cycle on the buck side and a smaller duty cycle on the boost side can achieve a smaller output voltage, as shown in Figure 24.

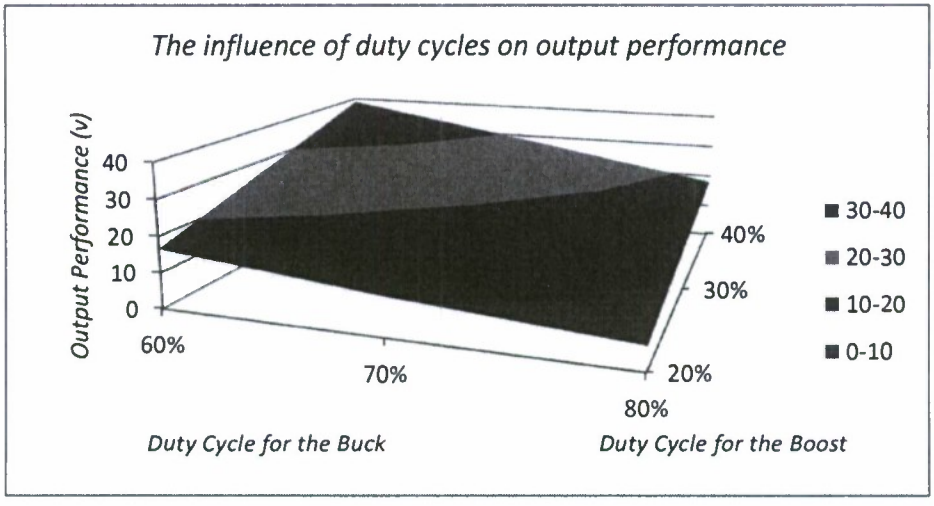


Figure 24. The Influence of Duty Cycles on Output Performance

b) The switching frequency on both side of the converters also have impact on output performance. A bigger frequency on the buck side reduces the voltage ripple significantly. On the other hand, a bigger frequency on the boost side lowers the output average but adds more ripple to the simulation. Figure 25 shows the performance.

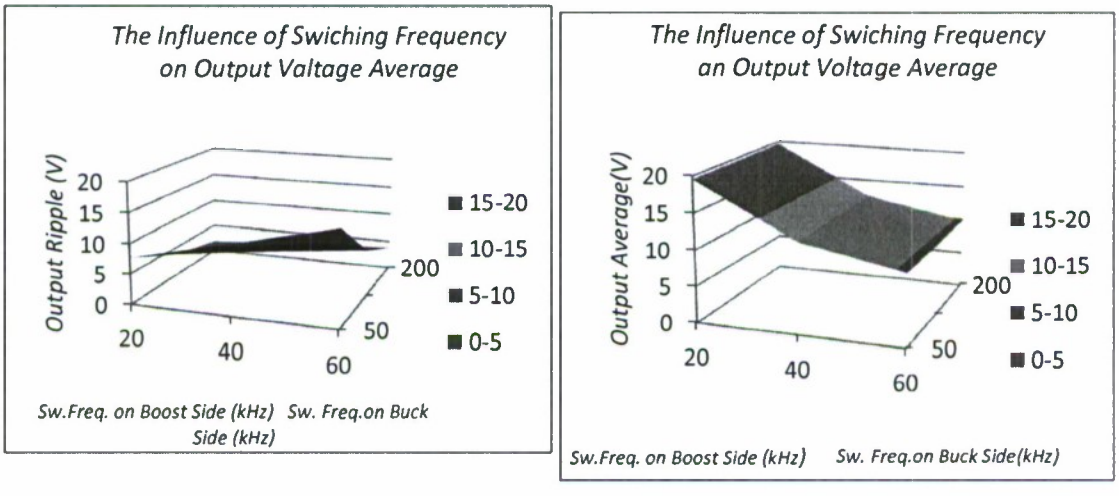


Figure 25. The Influence of Switching Frequency on Output Voltage Average and Ripple

c) The increase of the boost side of the inductor (L1) can shift the output down. Therefore, a smaller voltage can be achieved with a bigger L1 by sacrificing voltage ripple. On the other hand, the increase of the buck side of the inductor (L2) does not have much effect on the output average, but reduce the voltage ripple significantly. Figure 26 shows the performance.

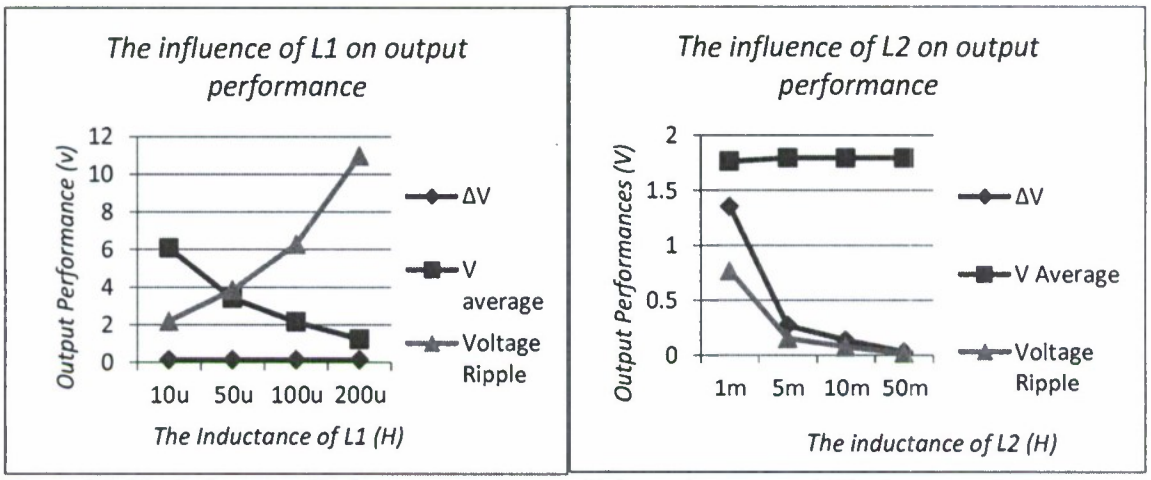


Figure 26. The Influence of Inductances on Output Voltage Average and Ripple

d) The capacitor at the end of the buck converter can be got rid of to reduce cost. However, it can reduce the output voltage ripple significantly and can be used if the output ripple is highly emphasized in the application.

Frequency Analysis

System Stability needs to be considered in the real applications. The system frequency analysis model is extracted as shown in Figure 27.

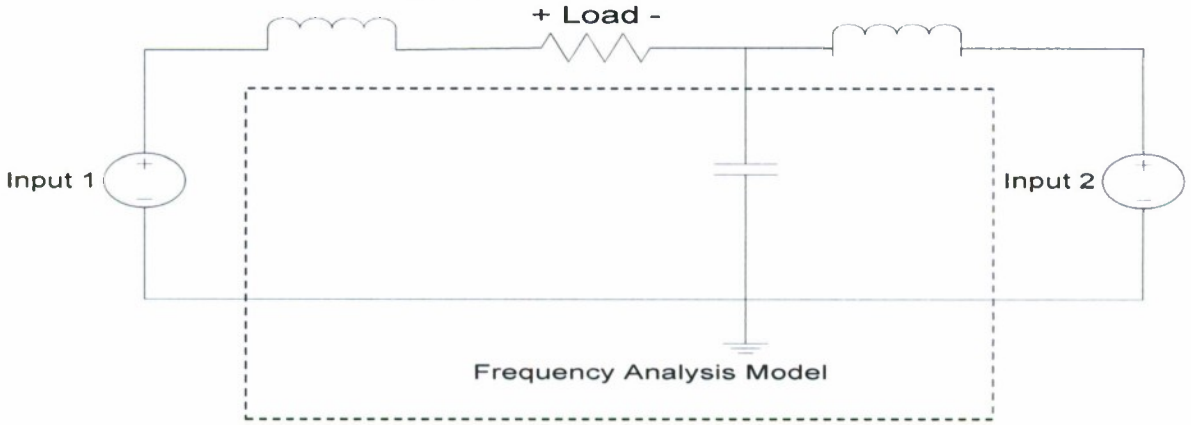


Figure 27. Frequency Analysis Model for Large Step Down DC-DC Converter

The state-space representation was used to set up the model for the system. MathCAD® and MATLAB® were involved in order to achieve system transfer function for both inputs. Equations (1) shows the system transfer functions.

$$tf_1(s) := \frac{1000 \cdot s^2 + 2.631 \cdot 10^{11}}{s^3 + 2 \cdot 10^4 \cdot s^2 + 2.964 \cdot 10^8 \cdot s + 5.261 \cdot 10^{12}} \qquad tf_2(s) := \frac{-2.631 \cdot 10^{11}}{s^3 + 2 \cdot 10^4 \cdot s^2 + 2.964 \cdot 10^8 \cdot s + 5.261 \cdot 10^{12}}$$

Since both the power supply and the switching frequency are independent on the output voltage, the system is an open loop passive circuit. The dc gain is -26dB for both inputs as shown in Figure 28, therefore even if a feedback loop is closed in the system, the gain is small enough and unlikely to cause problem.

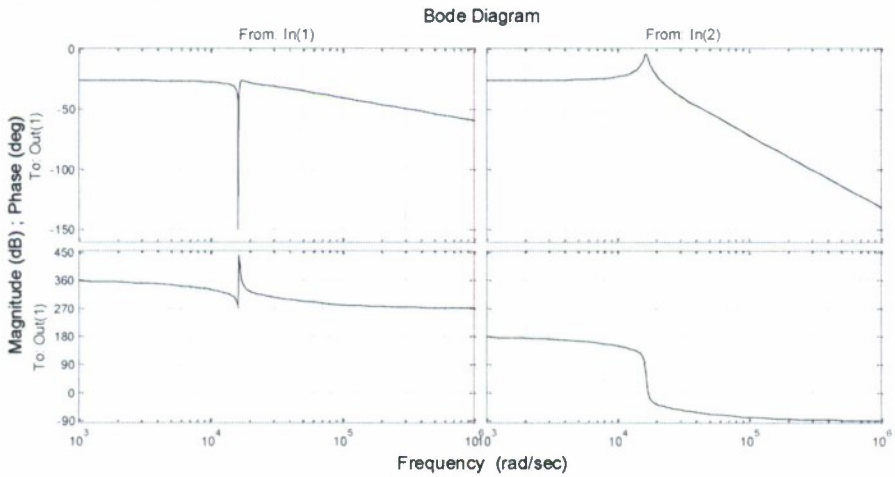


Figure 28. Bode Diagram of the system frequency analysis model

HARDWARE IMPLEMENTATION

The converter algorithm has been theoretically developed and successfully simulated using LTSpice®. To further verify the theoretical development and test of the output performance in a real-world application environment, the converter was implemented in the converter testbed. The hardware test was under 10 volts input, a reduced scale initial prototype. As is shown in the simulation, the average output is about 420mV with 6%-7% ripple. The output/input ratio (0.42/10) goes align with the simulation (12.4/240) and the frequency response (-26dB). The output ripple (0.025/0.42) also goes align with the simulation (0.8/12.4).

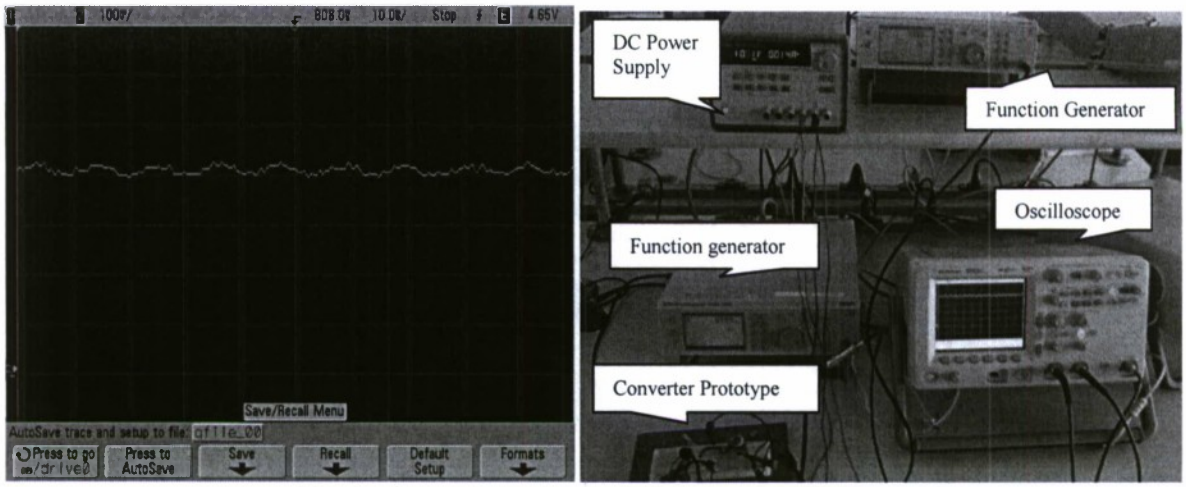

Figure 29. Hardware test of the converter and testbed overview

As a follow-on project, ARD-Bayview sponsored a senior design project to look at integrating the various UPS battery banks on the AESD into a DC microgrid, which is described below under subproject g).

## *Challenge 3: Mitigation system for voltage sags experienced on the LSV2 prototype submarine*

This topic was first addressed by a senior design team, and then became the focus of a Master's thesis, titled "Voltage Sag Mitigation Technique for a Large Electric Vehicle Propulsion System," completed the summer of 2008 by James Klein. The thesis has been forwarded to ARD Bayview and several conference papers have been published from the work.

The objective of this work was developing a solution to overcome the limitation the LSV2's electric vehicle (EV) energy storage system. This EV is utilized primarily for acoustic research and is powered by valve-regulated lead acid (VRLA) battery modules. The acoustic data is gathered during test sequences where the vehicle operates autonomously. Each test sequence contains individual runs that discharge the propulsion battery, consuming a certain amount of its stored energy. During the high speed portion of the run, a large amount of current is drawn from the propulsion battery, which creates voltage sag at the load of the propulsion system. If this voltage sag reduces the voltage at the load beyond a certain low-voltage threshold, the protection circuitry within the electric vehicle automatically stops the run and the data gathered during this partial run becomes invalid. The electric vehicle must then be recharged by an external power source, a process that takes over six hours to complete, before further testing can take place. Therefore, the objective of is to detail a solution that provides the propulsion power system with supplemental energy at the appropriate time, thereby holding the load voltage above the low-voltage threshold and allowing the completion of the test run. An excerpt from the text from one of the papers written from this work follows.

The electric vehicle (EV) discussed in this paper is a very unique EV. Its energy storage system, which consists of valve-regulated lead acid (VRLA) battery modules, is capable of

sourcing 900V at more than 2500A. The vehicle is used primarily to gather acoustic data during test sequences where the vehicle operates fully autonomously. Each test sequence contains individual runs that discharge the propulsion battery, consuming a certain amount of its stored energy. During the high speed portion of the run, a large amount of current is drawn from the propulsion battery, which creates a voltage sag at the load of the propulsion system. If this voltage sag reduces the voltage at the load beyond a low-voltage threshold of 742V, as shown in Fig. 30, the protection circuitry within the electric vehicle automatically stops the run and the data gathered during this partial run becomes invalid. The EV must then be recharged by an external power source, a process that takes a considerable amount of time, before further testing can take place. Therefore, a solution is desired that provides the power system with supplemental energy at the appropriate time, thereby holding the load voltage above the low-voltage threshold and allowing the completion of the final test run.

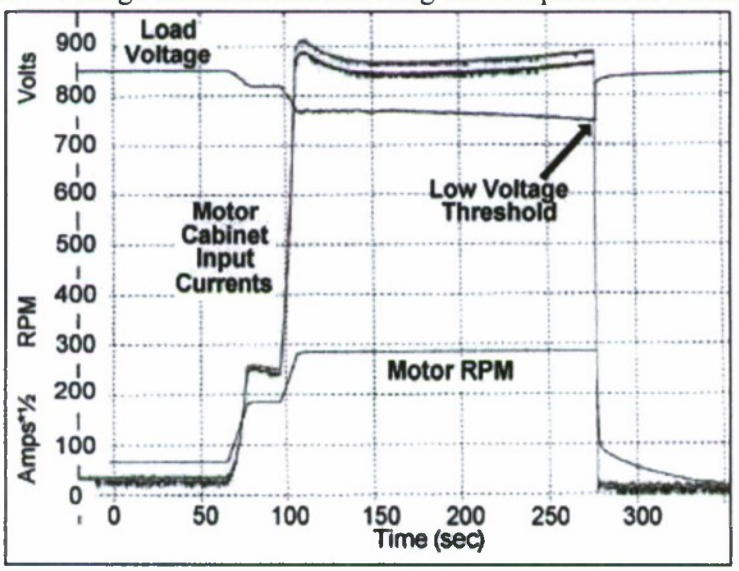


Figure 30: Data from EV's power system during a faulted test run

## II. DESIGN CONSTRAINTS

The solution to this voltage sag problem must be capable of providing a minimum of 10V at a system current level of 1300A for a period of 25 seconds. Properly utilizing this stored energy to mitigate the steady voltage sag shown in Fig. 30 is the primary objective for this project. However, a secondary objective is that the solution also be capable of providing pulsed power support during times of hard acceleration. In order to actually be implemented within the EV's existing power system, the solution must also meet the following design constraints:

1) The solution is not allowed to modify the existing architecture of the propulsion power system.
2) The solution is not allowed to alter the existing control scheme of the EV.
3) A modular design is necessary to properly fit within the existing space inside the EV.
4) The solution must operate autonomously.
5) The solution must not endanger the survivability of the EV.

These design constraints each carry a high level of importance, as a successful solution design must be able to satisfy all of them simultaneously. If the design meets the energy

and functionality requirements, but cannot physically be housed within the EV, it is not a practical solution. Likewise, if there is any possibility that the voltage sag solution might cause an unsafe operating condition, it is not a practical solution. It is vital to keep in mind that this project seeks to increase the functionality of an existing, fully operational, autonomous, EV. The newly created voltage sag solution must maintain the high degree of reliability that has previously been designed into this unique vehicle.

## III. DESIGN CONSIDERATIONS

This project began as a senior design research project at the University of Idaho in the fall of 2006. The solution created by the senior design team [1] provided the foundation for the redesigned solution presented in [2]. The following paragraphs layout the initial design process that was undertaken by the senior design team and points out recent design changes that have occurred and the reasoning behind each change. The three main areas of this design process are configuration options, interface options, and reserve energy storage device.

### A. Configuration Options

The configuration of the solution deals with the relationship between the main propulsion battery and the proposed reserve energy source. The two basic configuration options for this application are parallel and series. An example of a parallel configuration is shown in Fig. 31. This type of configuration has been studied extensively in the area of EV drive systems and is commonly referred to as power sharing [3] [4].

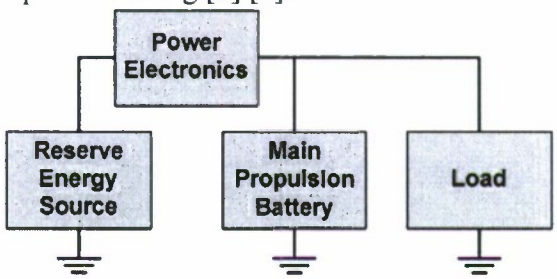


Fig. 31 – An example of a parallel configuration

The main benefit of power sharing is the ability to reduce the peak current sourced by the main propulsion battery. Power sharing is not necessarily intended to be used as a voltage sag mitigation technique. However, by properly utilizing the reserve energy source to provide the demanded peak current, the overall power system would increase in efficiency, the main propulsion battery would not degrade as quickly, and the vehicle would therefore be able to operate longer before the low-voltage threshold is reached.

The main drawback to this power sharing approach is the requirement to match the voltage level of the reserve energy source with the voltage level of the main propulsion battery. Due to the high power operation of our EV and the limited space available to house the voltage sag solution, a parallel configuration quickly becomes unreasonable.

An example of a series configuration is shown in Fig. 32. This type of configuration is similar to the dynamic voltage restorers (DVR) used for utility applications [5] [6].

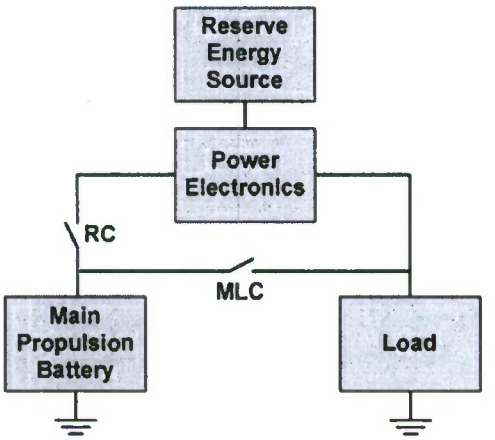


Fig. 32 – An example of a series configuration

The main benefit of this configuration is the ability to size the reserve energy source directly to the amount of voltage sag measured at the load. Therefore, a reserve energy source slightly greater than 10V could be used to mitigate a 10V sag while the parallel configuration option would require an equivalent reserve energy source of 752V. The main drawback to the series configuration is the need for some type of switching scheme to place the reserve energy source in series with the main propulsion battery. It was originally determined that electromechanical contactors could be utilized to safely control the flow of current throughout the power system during voltage sag mitigation. However, opening and closing the contactors during a test run presents reliability concerns and creates significant acoustic noise. Therefore, a second design option has been developed that utilizes a single power diode in place of the main line contactor (MLC). These two design options will be analyzed further throughout this paper.

Due to the inherent ability of the series configuration to mitigate voltage sags within a high power system, this configuration was originally chosen by the senior design team. This design decision has been upheld throughout the lifetime of the project and has been proven effective through simulation and lab model testing, as presented in Sections IV and V, respectively.

B. Interface Options

Fig. 33 shows a power electronics interface between the reserve energy source and the main propulsion battery. However, a direct interface could also be implemented that would allow the reserve energy source to naturally discharge into the existing power system. This direct connection interface, as shown in Fig. 4, was the initial design choice for this project.

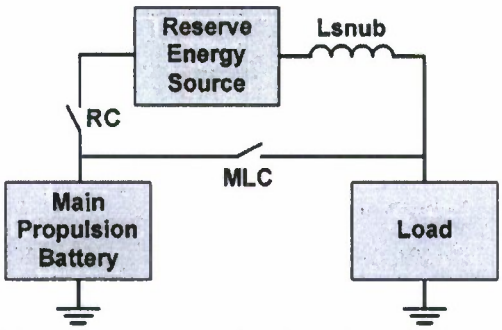

Fig. 33 – Direct connection interface design option

The snubber inductor is needed to limit the inrush of current created by closing the reserve contactor (RC) and essentially shorting the reserve energy source through the MLC. A current transducer could then be used to open the MLC near its zero current crossing and allow the reserve energy source to be placed in series with the main propulsion battery and the load of the power system. The voltage level at the load would then increase sharply followed by a natural decay corresponding to the discharge of the reserve energy source. This discharge would be irreversible and uncontrollable and the power system would not be capable of returning to normal operation once the voltage sag mitigation was completed.

This direct interface option was originally chosen due to its ease of implementation. However, it is only capable of satisfying the primary objective of this project. The direct interface option would not be suitable for mitigating voltage sags caused by pulsed power operations, such as hard acceleration. Therefore, a power electronics interface has been created that builds off of the knowledge gained by the direct interface solution. Fig. 34 shows that this design utilizes a buck converter interface between the reserve energy source and the existing power system. An on-board microcontroller is used to properly open and close the contactors as well as vary the duty cycle of the switching device. This allows the reserve energy source to be utilized efficiently and provides the ability to mitigate both temporary and prolonged voltage sags within a single test run.

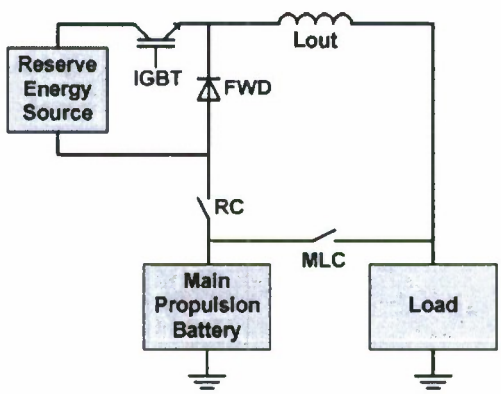

Fig. 34 – Buck converter interface design option

C. Reserve Energy Storage Device

With the configuration and interface of the voltage sag solution determined, the next step is to choose a suitable energy storage device to be used as the reserve energy source. The initial solution created by the senior design team selected a bank of ultracapacitors to be implemented as the reserve energy source. This decision was made mainly due to the low

equivalent series resistance of the ultracapacitor and its documented ability to contribute voltage to a power system nearly instantaneously.

During the redesign phase of this project, it was found that the ultracapacitor may not be the most beneficial energy storage device for this application. The VRLA battery used for the main propulsion battery possesses internal resistance and dynamic response characteristics that are more than sufficient for the demands of the reserve energy source. The main benefit of the VRLA battery that makes it stand out against the ultracapacitor bank is its energy density. Rough calculations show that the VRLA battery bank would possess an energy density greater than ten times that of the ultracapacitor bank. Therefore, by utilizing the VRLA battery as the reserve energy source, the voltage sag solution will be able to mitigate a low-voltage condition for a longer period of time than an equivalently sized ultracapacitor bank.

## IV. PSPICE SIMULATION RESULTS

To verify the overall operation of the voltage sag solution before, during, and after a low-voltage condition, PSpice circuit simulation software was used. A programmable current source was used to create a similar load profile as seen during a single test run of the EV. The current demand was accentuated in order to create both a temporary voltage sag and a prolonged low-voltage condition during the high speed portion of the run. An actual test run is approximately 325 seconds long, but since an average model of the buck converter circuitry was not implemented, the time-scale of the simulation has been manipulated such that a simulated test run only lasts 325ms.

A simplified, equivalent circuit for the existing power system and the voltage sag solution with the main line contactor is shown in Fig. 35.

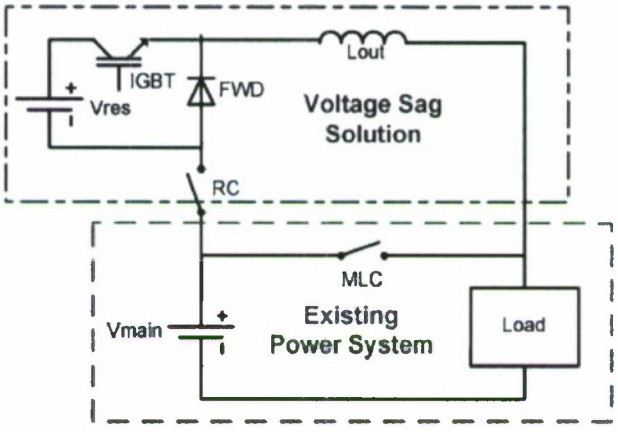


Fig. 35 – Voltage sag solution with the main line contactor design

Running a simulated test run with the voltage sag solution programmed to ignore any low-voltage conditions produces the plots shown in Fig. 36. As expected, all of the current flows through the MLC and the load voltage sags well below 742V during both the hard acceleration and the prolonged high speed operation.

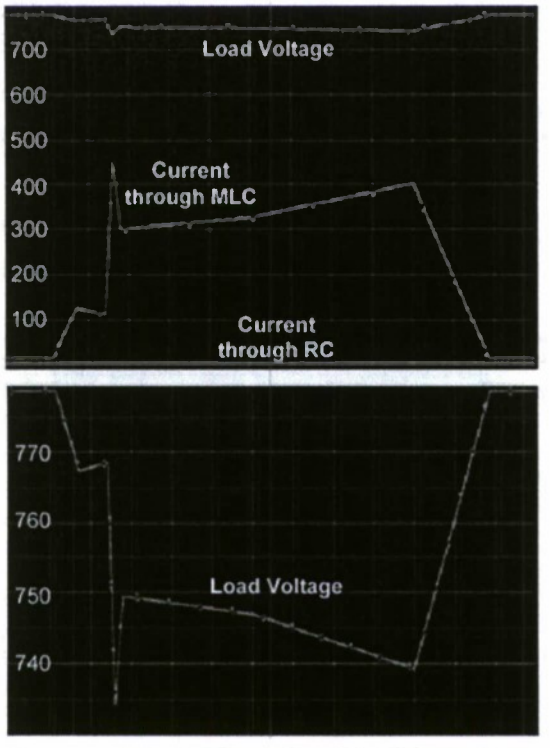


Fig. 36 – System response without the aid of the voltage sag solution

By programming the solution to mitigate any voltage sags that occur below 745V and running the same load profile as before, the results shown in Fig. 37 are obtained.

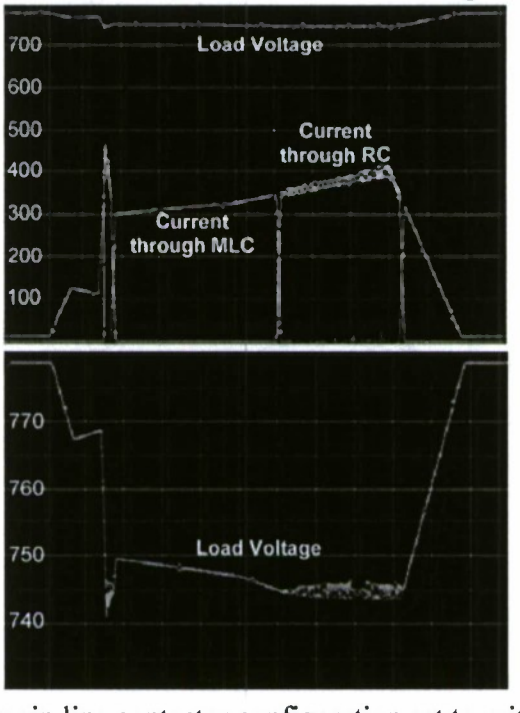


Fig. 37– Results for the main line contactor configuration set to mitigate sags below 745V

To compare the operation of the main line diode configuration and the main line contactor configuration, the circuit shown in Fig. 38 was implemented within PSpice Again, the solution was programmed to mitigate sags below 745V and the same load profile was used. The simulation results for the main line diode configuration are shown in Fig 39.

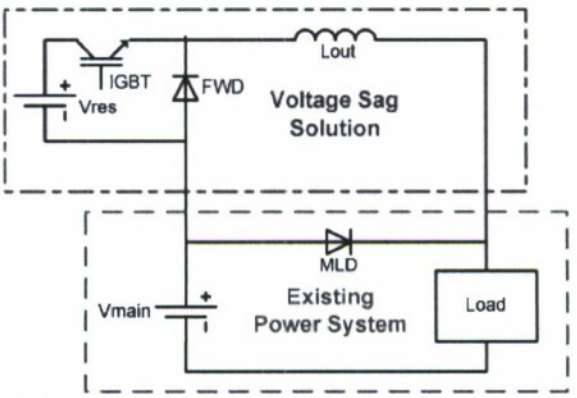


Fig. 38 – Voltage sag solution with the main line diode design

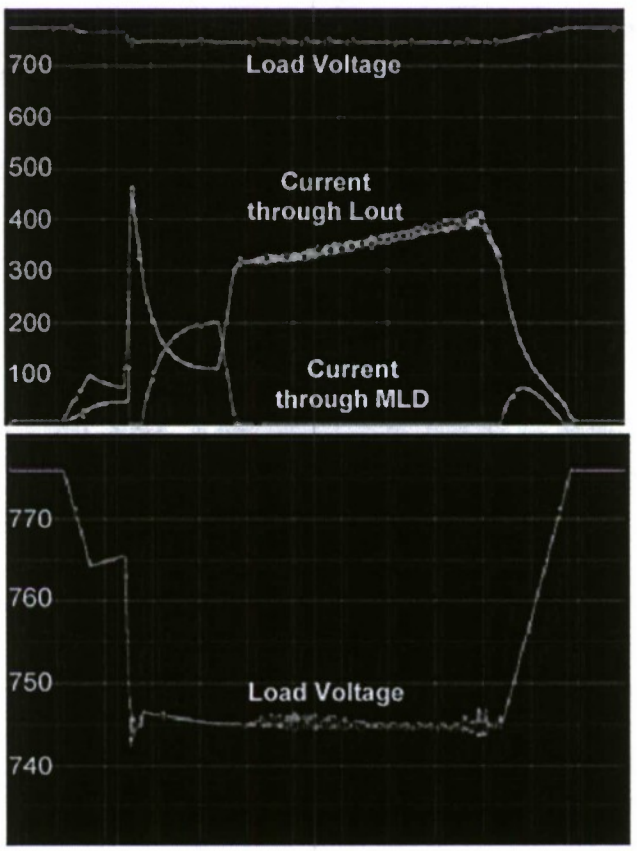


Fig. 39 – Results for the main line diode configuration set to mitigate sags below 745V

Although the operation of the main line contactor and main line diode configurations is not exactly the same, the load voltage waveforms of Fig. 37 and Fig. 39 demonstrate that both are clearly capable of mitigating a low-voltage condition.

## V. LAB MODEL RESULTS

To demonstrate the real-world functionality of the main line contactor and main line diode configurations, scaled lab models were constructed. Voltage sag was created by reducing the resistance of the rheostat by hand. By programming the voltage sag solution to mitigate voltage sags below 14.8V and then applying the same load profile, the results verified that the voltage sag solution worked as designed. It was also verified that the voltage sag solution switched out of the system during the short period between the temporary voltage sag and the extended voltage sag. After obtaining the results from the main line contactor configuration, the lab model was redesigned to utilize a motor generator set as the load. The reserve contactor was removed and the main line contactor was replaced by a power diode. Again, the set up performed as expected.

## VI. DESIGN COMPARISON

The simulation and lab model results verify that both the main line contactor (MLC) and main line diode (MLD) configurations are effective methods of mitigating voltage sags. Therefore, other characteristics of these two configurations must be considered in order to decide which solution is better suited for operation within the actual vehicle. Electric vehicles have always suffered from one fatal flaw, a limited operational range due to insufficient stored energy. Therefore, efficiency is often the first and foremost consideration for any new drive system component. If this were the only consideration for this project, then the MLC solution would be the clear winner. A power diode device possesses a forward voltage drop of greater than 2V anytime current is flowing through it. Additionally, a resistive voltage drop is present that directly corresponds to the amount of current flowing through the diode. The combination of the forward voltage drop and the resistive voltage drop makes the MLD solution much less efficient than the MLC solution. It is also important to note that the MLD configuration requires the power diode to always be in the power system, regardless of the load voltage level. Therefore, the efficiency of the power system during normal operation will be reduced if the MLD solution is implemented whereas implementation of the MLC solution would not change the efficiency during normal operation.

A second characteristic to consider is the performance of the two configurations. As mentioned previously, the main purpose of this electric vehicle is to gather acoustic data during high speed test runs. The electromechanical contactors rated for operation within the vehicle create significant acoustic noise when they are opened or closed. Since the voltage sag solution is most likely to operate during the high speed portion of the run, the MLC configuration may create acoustic noise that deteriorates the quality of data gathered during the run. Conversely, the MLD configuration contains no mechanical components and operates relatively silently.

Finally, the reliability of each configuration must be considered. The survivability of the vehicle is by far the most important aspect of any test run. No amount of efficiency or performance increase would be acceptable if it were to come at the cost of reliability. Aside from the obvious reliability concern of actually opening and closing contactors during high speed operation, the control needed to properly manipulate the contactors is not a simple task. The voltage sag solution controller must monitor the current flowing through the MLC while it is closed and monitor the voltage level on either side of it while it is open. For the MLD configuration, the voltage sag solution controller does not need to concern itself with

anything other than the load voltage. This simplification creates a much more reliable and robust solution.

Like so many problems, the best solution is not always obvious. It is possible that neither the MLC or MLD configuration is the best solution for this case, but rather the best solution may be a combination of the two. Fig. 40 shows a possible hybrid solution that benefits from the efficiency of the MLC configuration while also utilizing some of the reliability of the MLD configuration. Further study is needed to determine which design configuration should be implemented within the existing EV power system.

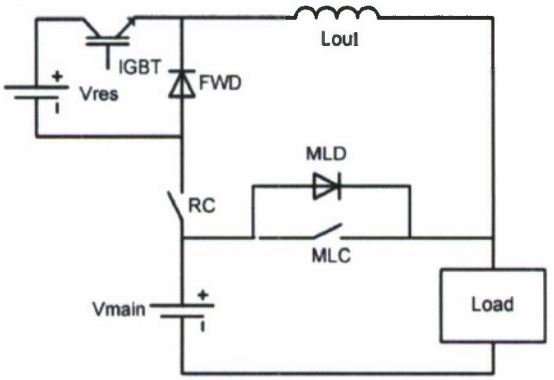


Fig. 40 – Hybrid MLD and MLC configuration

## VII. CONCLUSION

The design process of a voltage sag solution for a unique, high power electric vehicle has been presented. The final solution is based on the principles of a dynamic voltage restorer. A reserve energy source, consisting of VRLA batteries, is switched into a series configuration with the main propulsion battery and controlled through a buck converter interface. The effectiveness of the solution has been proven through PSpice simulation and lab model testing. Multiple design options exist and each has its own set of benefits and drawbacks. Therefore, further study is needed to determine the optimal configuration of the voltage sag solution for this application. Once implemented within the existing power system, the voltage sag solution will allow the electric vehicle to accelerate at a higher rate and complete test runs that otherwise would have been aborted.

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## *Subproject a) Apply an alternate generation source such as a fuel cell to the prototype destroyer to either to replace or supplement existing battery based system*

This project started as a senior design project funded directly by Bayview. A Master's student followed up on this work and looked at several options integrating battery energy storage with the fuel cell system. This work was completed with a MS thesis in December 2009. Three conference papers have been published out of this work. Key points from the thesis follow:

### *Current Power System*

AESD is powered through both a diesel generator and batteries. Propulsion power comes from a single 250 kW diesel generator through a transit transformer during transit to the test array on the lake. A power flow diagram for the AESD for the transit to the test array is given in Figure 1.1. The red line in Figure 1.1describes the power flow during transit of AESD to test array. Once the AESD is in the test array on the lake, propulsion power is taken from 12 strings of batteries which together provide up to 650 kW of power. The power flow diagram for the testing is given in Figure 1.2. The red line in Figure 1.2 describes the power flow during test runs.

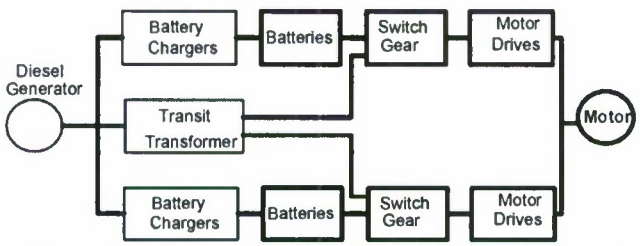



**Figure 1.1 - Power flow of AESD during transit to test area**

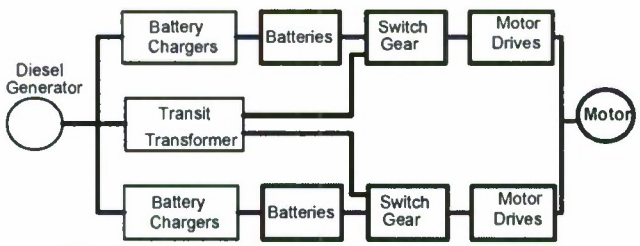



**Figure 1.2 - Power flow of AESD during testing**

### *Limitations of the Current System*

AESD's current power system has some limitations, which result in the reduction of the overall operational efficiency of the ship. As mentioned, propulsion power of the ship comes from both diesel generator and batteries. Diesel generators produce electricity through combustion of fuel. The diesel generator has the problems of limited power production and sensitivity to harmonic current draw. The diesel generator produces noise and exhaust that could be objectionable. The batteries also have disadvantages. They have a long recharge time of approximately 14 hours and a limited runtime of only 3 hours. Furthermore, the battery charging system introduces harmonic distortion to the AC side of the power system. The impedance of the diesel generator combined with the non-sinusoidal current feedback from the battery chargers produces voltage distortion that limits the functionality of the power system. The battery charging system is also current-limited and it requires a substantial amount of space.

### *Thesis Objective*

The primary aim of this project is to recommend a method of AESD propulsion power that is cleaner and more efficient than the current propulsion power sources. Fuel cells are known to be good options for propulsion because of their high efficiency and low emission. Different fuel cell technologies were examined to recommend the best fuel cell technology for AESD. Proton Exchange Membrane Fuel Cell (PEMFC) was found to be the best candidate fuel cell type for AESD application. This thesis discusses whether to replace 3 out of 12 battery strings, to replace all 12 battery strings, or to replace the entire AESD power system with fuel cells. One of the other objectives of this thesis is to recommend a power conditioning system consisting of filters and isolated dc-dc converters for the fuel cells to achieve comparable power requirements for the system. Fuel cells have slow response to sudden load changes. A secondary energy source consisting of lead-acid batteries is recommended to assist the fuel cell during load changes. This thesis explains PEMFC modeling for both steady state and transient studies. This thesis also outlines the interconnection of fuel cell with secondary energy source and the bi-directional dc-dc converter. The control system for fuel cell hybrid system is also studied in this thesis.
The current power system specifications of AESD dictate the basic requirements for fuel cell integration; these are summarized in Table 3.1.

| Parameters | Specifications |
|---|---|
| Output Voltage | 714 ± 5% DC |
| Current | Greater than 75 A per string |
| Power | Greater than 50 kW per string |
| Energy | Greater than 77.760 MJ |
| Dimensions | 570 $ft^3$ (Volume of battery racks) |
| Fuel Storage | Comply with NAVSEA and State of Idaho's requirements for waste streams |
| User Interface | Remote means to control and shutdown |

**Table 3.1 - Design Specification of AESD**

### *Fuel Cell Integration Options*

US Navy personnel at Lake Pend Oreille stated three primary options for the integration of fuel cells into the AESD.

## Option 1 – Replace 3 of 12 battery strings with fuel cell strings

This option involves replacing the 3 strings of batteries with fuel cells. Each string will be required to match existing battery strings to within +/- 5% for voltage and current. Output power/string is 50 kW with

total output power of 150 kW. In this option, any fuel cell problem will also make battery propulsion inoperable. The primary benefit of Option 1 is less reliance on the fuel cell's power conditioning system. Each battery string that is replaced by a fuel cell module has to match the existing battery string in AESD for voltage and current during all operations. This option employs fuel cells in parallel with batteries in a fashion that can't be easily optimized for hybrid operation, resulting in power supplies with different time responses. Fuel cell's output current is not directly controlled, and there is a mismatch between fuel cell and battery impedances. This makes it difficult to implement Option 1 (power systems that have fuel cells in parallel with batteries). Each battery string in the AESD currently provides 720 ± 5% V. The selected fuel cell module's voltage varies from 440V- 800V, depending on the load condition. Monitoring the fuel cell module voltage to match the battery voltages requires a complex control system. Another disadvantage of this option is that the space made available by removal of the 3 battery strings is not sufficient to house the fuel cell modules and the power conditioning system. An output power of 50 kW is required for each fuel cell string. The efficiency of the power system in Option 1 is low and the emission is high because the diesel generator is still in the system. This option does not provide solutions to the problems of transients and noise introduced by the diesel generator. This option does not resolve the harmonic distortion problems of battery charging system and the limited run time of batteries. A power flow diagram for Option 1 is given in Figure 3.3.

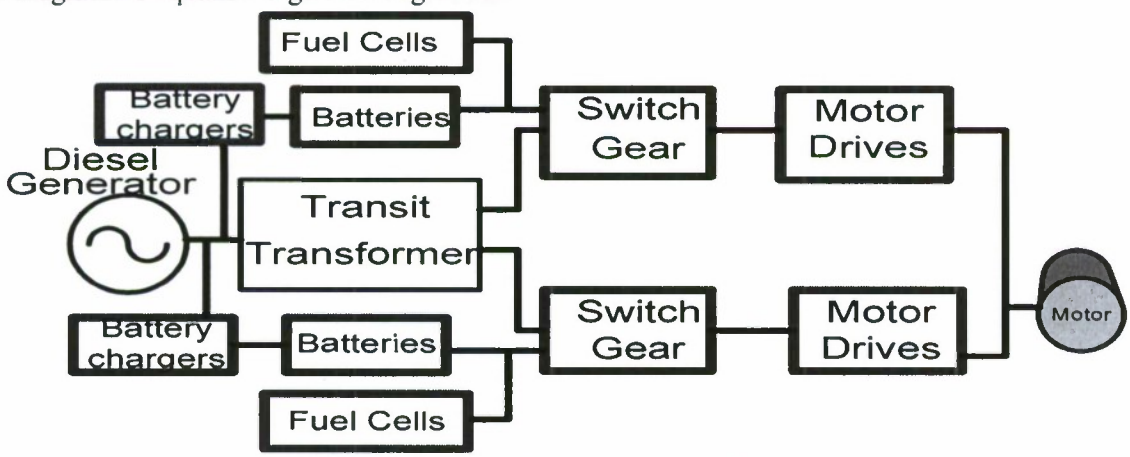



**Figure 3.3 - Power flow diagram for Option 1**

## Option 2 – Replace all 12 battery strings with fuel cells

Option 2 is about replacing 12 battery strings with fuel cells while keeping diesel generator in the system. Battery strings are considered for replacement because battery charging is the cause of most of the limitations of the current system. This option allows for complete removal of the batteries and the DC charging system. In this option, the motor drive is fully dependent on fuel cells. Propulsion power is supplied by the diesel generator to the transit of the ship to the test array on the lake. Once the ship is on the test array, fuel cells provide power for the system. The primary benefit of this option is using fuel cells in place of batteries and thus avoiding the issue of long charging time and limited run time of the batteries. The problem of harmonic distortion introduced by battery charging system is avoided. The other benefit is that we are increasing the power density of the system since fuel cells have better power density than batteries.

However, this option has some drawbacks; the space created by removal of the battery strings cannot accommodate the fuel cell modules, fuel storage system, and the power conditioning system. This option does not resolve the problem of transients because transients are produced by diesel generator and diesel generator is included in the power system. The overall efficiency of the power system is low because of the presence of diesel generator in the power system of option 2. For this option, emissions are relatively

high because the diesel generator is still part of the system. The power flow diagram of Option 2 is given in Figure 3.4.

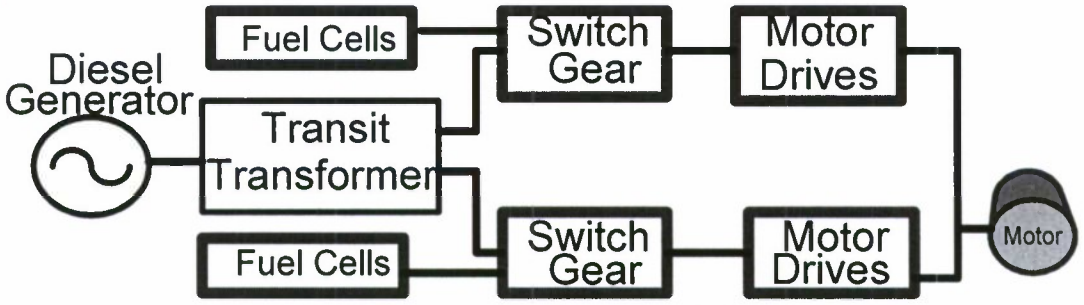



**Figure 3.4 - Power flow diagram for Option 2**

## Option 3 – Replace entire power system with fuel cells

This option requires the complete replacement of power system with fuel cells. Here, matching to battery strings is not an issue and makes it ideal for any likely drive application. This option allows the entire power system to be operated with fuel cells exclusively. The main advantages of this option are having a power system which is fully operated by a renewable energy source. This option makes the power system highly reliable. The operating temperature of the power system is less than 80 $^{0}$C. Battery strings have to be replaced by fuel cell modules and dc-dc converter, which has to be able to provide electrical isolation. Option 3 results in a power system that is highly efficient with low emissions as it is fully dependent on fuel cells. By implementing option 3, the problems of audio transients introduced by diesel generator and the problem of harmonic distortion introduced by battery charging system can be avoided. There are some technical challenges in implementing this option, first of all fuel cell modules have to be operated in parallel to meet the power requirement of the system. When fuel cells are connected to a bus in parallel there is a higher possibility of circulating current to inject back to the fuel cell modules. This can reduce the efficiency and service life of the fuel cell modules therefore the circulating current must be blocked from entering in to the fuel cell modules [ ***10*** ]. For the purpose of simplifying the analysis fuel cell modules are assumed to have matched characteristics, such as equal impedances, equal load sharing and equal response time. However, because of impedance mismatching, in practice some modules could supply more current to the bus than others. The control system to be built has to address this problem. The power flow diagram for Option 3 is given in Figure 3.3.

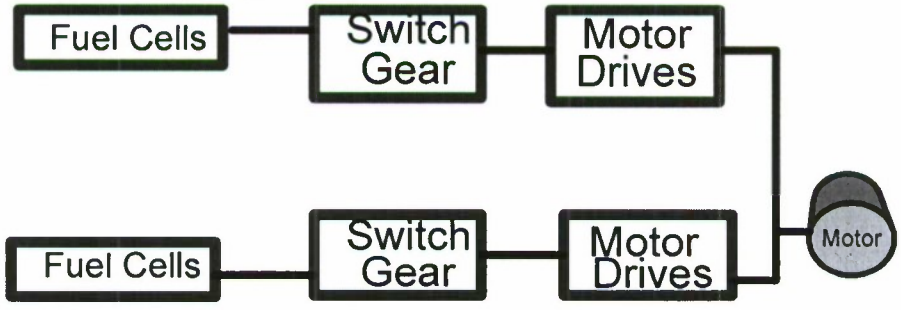



**Figure 3.3 - Power flow diagram for Option 3**

### *Selected Fuel Cell Integration Option*

The three options were compared to find which one would be the best option for AESD's operation. Parameters of comparison include advantages and disadvantages of each option. Complexity of the

control system to implement options, efficiency and emission level of each option was also compared. Comparison of three fuel cell integration options is given in Table 3.2.

| | Option 1 | Option 2 | Option 3 |
|---|---|---|---|
| Advantages | Less reliance on fuel cells | No batteries and battery charging system | Power system fully operated on renewable energy. |
| Disadvantages | Fuel cells in parallel with batteries. Diesel generator is still in the system. | Diesel generator is still on the system | Requires 5 fuel cell modules and 12 DC-DC converters |
| Control system complexity | High | Low | Low |
| Space | Adequate | Adequate | Adequate |
| Efficiency | Low | Low | High |
| Emission | High | Medium | Low |
| Transients | High | High | Low |
| Harmonic Distortion | High | Low | Low |

**Table 3.2 - Comparison of fuel cell integration options**

A comparison of the three options reveals that Option 3 is the most advantageous. Option 3 requires complete replacement of the current power system in the AESD with a new power system which is fully dependent on fuel cells. The total power required is 650 kW. The Ballard HD 6 fuel cell module only produces 130 kW of power. Therefore, five of the HD6 modules will be required to operate in parallel to meet AESD power requirements. Currently, there 12 battery strings on AESD. Each battery string replacement candidate has to meet the same voltage, current, and power rating (714 ± 5% V, 75 A, 50 kW) requirements. In order to implement Option 3 and meet these specifications, five HD 6 modules will need to be connected to the input of a DC bus and 12 DC-DC converters are needed as the output of the DC bus to power the motor drives. A robust control system must be built to monitor the parallel operation of the fuel cells.

Caution must be employed when paralleling fuel cells [***11***]. A diode or other protection scheme must be inserted in series with the fuel cell modules to block any circulating current between fuel cell modules. Inserting diodes add losses to the system. In order to implement option 3, the power system has to be sited in the available space (570 $ft^3$).

Based on the recent research, the weight of the reformer for a 25 kW fuel cell output is 75 kg, and the volume is 2.58 $ft^3$ [***12***]. AESD's operation requires 650 kW of power therefore the reformer will have a minimum weight of 1950 kg and a volume of 67.08 $ft^3$. Energy density of methanol by volume is 15.912 MJ/L. It was calculated that 77.6 MJ of energy is required for 6 high speed runs (18 minutes) of the AESD. By assuming 85% efficiency of the methanol reformer it is calculated that 5.75 L of methanol is needed for six high speed runs. The Steam Reforming of Methanol (SRM) fuel processor coupled with PEM fuel cells can achieve about 50% overall efficiency [***4***]. Power conditioning system requires 50 $ft^3$ of volume. The total volume required for five HD6 modules is 98.2 $ft^3$. Therefore the total volume required is 215.28 $ft^3$ for implementing option 3.

The fuel cell integration bus for option 3 is given in Figure 3.4. Five Ballard HD 6 fuel cell modules are the input of the dc bus. The input power of the dc bus is 625 kW, and the input voltage varies from 440 to 800 V. Twelve full-bridge dc-dc converters (FBDC-DC) are the output of the dc bus. Each dc-dc converter's output voltage is more than 714 V and output current is more than 75 A.

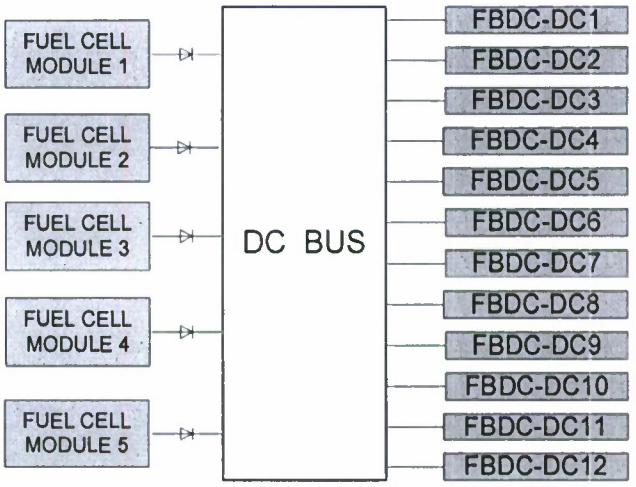



**Figure 3.4 - Fuel cell integration bus for Option 3**

### *Power Electronics Interface*

The output voltages of fuel cells may vary with age and load current [***2***]. For AESD application, the regulation of the voltage is important. Therefore, the integration of fuel cells to AESD requires a power electronic interface. Fuel cells respond slowly to sudden load changes due to their slow internal electrochemical and thermodynamic responses. Fast dynamic load demands cause significant voltage drop. Fuel cells have no overload capabilities, and cannot accept reverse current [***2***]. The current ripple caused by the dc-dc converters and inverters can reflect back to the fuel cell stack [***10***]. Fuel cells are more vulnerable to low frequency ripple caused by the inverters because fuel cells cannot regulate the pressure level fast enough to react to the current variation. The efficiency of a fuel cell is reduced with output ripple current [***2***].

The power conditioning system should control the fuel cell output voltage, convert the fuel cell output to the appropriate type and magnitude, provide little to no harmonics on output side of fuel cell, operate efficiently under all conditions and add little to the cost of the overall power system [***2***]. Due to the fuel cell's slow response, secondary energy sources should be used to maintain bus voltage during start-up and fast power ramping transients. Batteries and ultracapacitors are suitable choices for these secondary energy sources. They can be interfaced to the system using bi-directional dc-dc converters [***13***]. A description illustrating the integration of a secondary energy source to the fuel cell source is as given in Figure 3.5.

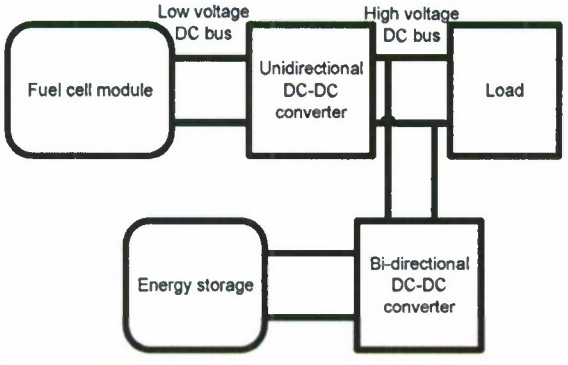



**Figure 3.5 - Integration of the secondary energy source to the system**

The application of a bi-directional dc-dc converter yields the advantage of a faster, more stable response. The dc–dc converter is needed to draw power from the secondary energy source to boost the high-voltage bus during AESD starting. Until the fuel cell voltage rises to a level high enough to hold the high-voltage bus, the secondary energy source provides the energy through the dc-dc converter. During load decrease energy can also be fed back and stored in the secondary energy source using the bi-directional dc–dc converter.
Electrical isolation between the low voltage output of the fuel cell and high voltage dc output is required to protect the fuel cell and the motor load. Any reverse current to the fuel cell can be blocked by a diode inserted in series with the fuel cell. This blocks circulating current between fuel cell modules and current ripple under low power operation. Current ripple can be filtered by implementing a capacitor to absorb the ripple. The diode brings additional losses to the power system and thus reduces the efficiency. The addition of the filter capacitor adds to the cost, size and reliability of the converter. The output voltage applied to the load by the fuel cell can be kept constant through the use of a dc-dc converter.

### *DC-DC Converters*

The fuel cell dynamic response defines the control structure of the power conditioning system. The dc-dc converter to be designed must not react to load steps faster than the fuel cell. The dc-dc converter has to control and condition output power of the fuel cell and its electric characteristics have to match with that provided by the fuel cell and demanded by the load. In order to reduce the effects of current and voltage ripple on the fuel cell, the input current and voltage ripple of the dc-dc converter must be small . To ensure the highly efficient and reliable operation of the fuel cell, the dc-dc converter has to apply a suitable strategy to adjust the output power of the fuel cell when it works under load current variations. The dc-dc converter must fit in to the requirements of high step-up conversion ratio, high stability of the output voltage during variations of the output current and input voltage, and high efficiency. As mentioned earlier, the fuel cell must be electrically isolated from the load. The dc-dc converter is a good candidate to provide this isolation.
The aforementioned requirements exclude all dc-dc converters without transformers and converters for which stable output cannot be produced for varying input voltages. Maintaining high efficiency in the dc-dc converter mainly depends on low current and voltage stresses on power transistors, utilization of the B-H characteristic of the transformer in all quadrants, low input current ripple, low number of components, and simple design of the transformer. The options for the dc-dc converters are narrowed down to full-bridge, half-bridge, flyback, and push-pull topologies.
The recommended dc-dc converter topology for AESD is a full-bridge. The full-bridge dc-dc converter is highly efficient, stable, and it can provide isolation via a high-frequency transformer. The input and output current and voltage ripple of a full-bridge converter are small, and will ensure the safe operation of the fuel cell module and the power transistors used for switching. The power transistors' current and voltage stress are low in full-bridge topology. The flyback converter provides electrical isolation and voltage step up capability but has a relatively low operating efficiency and a low power-handling capability. The push-pull converter is highly efficient; however, the push-pull converter's transient response is poor. For the push-pull topology the transformer has an input and output center tap. The center tap transformers are more complicated to design and build than conventional transformers, and the cost of the transformer is higher. Center tap topology also requires larger windings on the primary side and thus results in bigger physical size and higher weight. The half-bridge topology was not selected because of its lower efficiency compared to the full-bridge, plus it is very difficult to keep a circuit symmetric with the half-bridge. This topology is required to have a more complex control circuit accommodate any rapid change in input voltage.
The schematic of the unidirectional full-bridge dc-dc converter is given in Figure 3.6. The approximate turns ratio of the transformer will be 1:2.

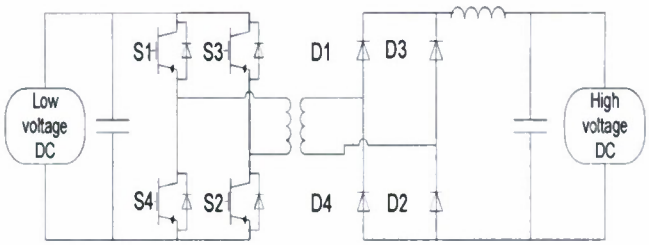



**Figure 3.6 - Unidirectional dc-dc converter for AESD**

## Bi-directional dc-dc converter for energy storage device

A bi-directional dc-dc converter allows both directional power flows for energy storage discharge and recharge. Its response needs to be fast enough to compensate for the slow dynamics of the fuel cell during start-up or sudden load changes. Either a push pull topology or full bridge topology can be employed in boost voltage mode. In buck mode, converters employ full bridge, half bridge, or forward converter topology. Full bridge type bi-directional dc-dc converter has discharging efficiency of 94% and charging efficiency of 95%. Therefore a full bridge bi-directional dc-dc converter is recommended for AESD operation. The schematic of the full-bridge bi-directional dc-dc converter is given in Figure 3.7.

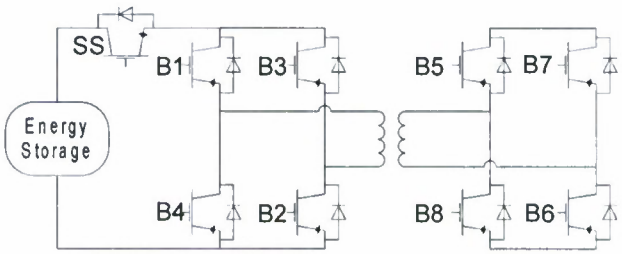



**Figure 3.7 - Bi-directional dc-dc converter for AESD**

### *PEMFC dynamic model using in PSCAD*

A PEM fuel cell consists of a cathode and an anode electrode with a proton conducting membrane separating the electrodes. In this section, a mathematical approach is proposed for building a PEM fuel cell dynamic model based on certain assumptions,

- one-dimensional treatment
- ideal and uniformly distributed gases
- constant pressure in the fuel-cell gas flow channels
- the fuel cell works under 100 $^0$C and the reaction product is in liquid phase
- the fuel is humidified $H_2$
- the oxidant is humidified air
- thermodynamic properties are evaluated at the average stack temperature by neglecting temperature variations across the stack
- parameters for individual cells can be lumped together to represent a fuel cell stack

A block diagram for building an electric circuit model for PEMFC is given in Figure 4.1. The C in the block diagram represents the capacitance of the double layer charge effect.

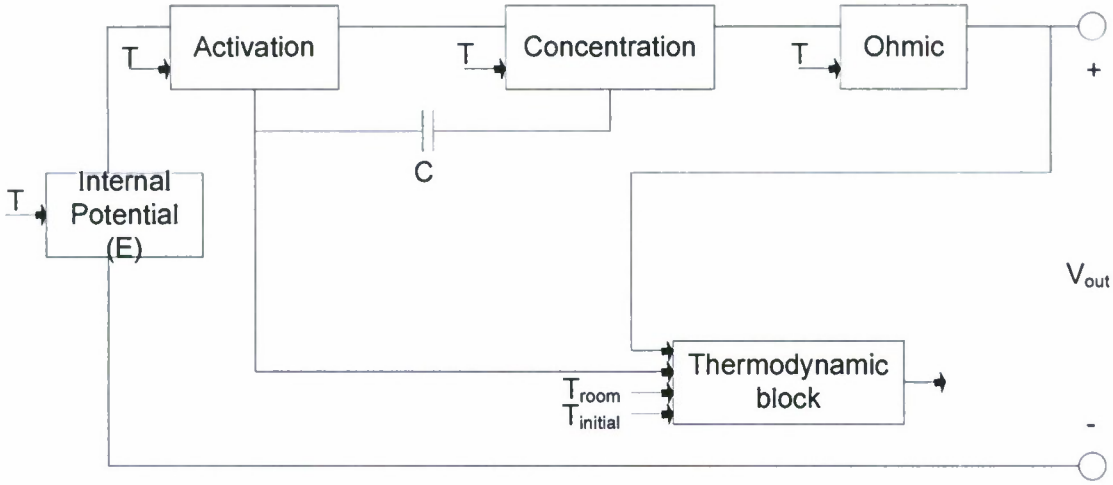



**Figure 4.1 - Block diagram for building an electrical circuit model for PEMFC**

## Equivalent circuit for internal potential (E)

The fuel cell internal potential is a function of load current and temperature. An equivalent electrical circuit for the internal potential is given in Figure 4.2. The input $E_0^0$ is the standard reference potential at standard state ($T$=298 K and $P$=1 atm) and the output of the equivalent circuit is the PEMFC stack internal potential, $E$. The current and temperature controlled voltage source, $f_1(I,T)$ represents the current and temperature dependent part of Nernst Equation (an equation which can be used to determine the equilibrium. The current controlled voltage source, $f_2(I)$ represents the overall effect of the fuel and oxidant delays for the total number of cells in series in fuel cell stack.

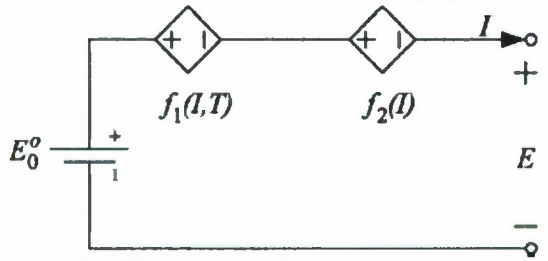



**Figure 4.2 - Electrical circuit for internal potential (E)**

An electrical circuit for the internal potential E was built in PSCAD/EMTDC and is shown in Figure 4.3. $I$ is the load current and *Tout* is the temperature of PEMFC stack. Neither of these quantities is constant. *Panode* and *Pcathode* are constants, *Panode* has a value of 1.5 atm and *Pcathode* has value of 1 atm.

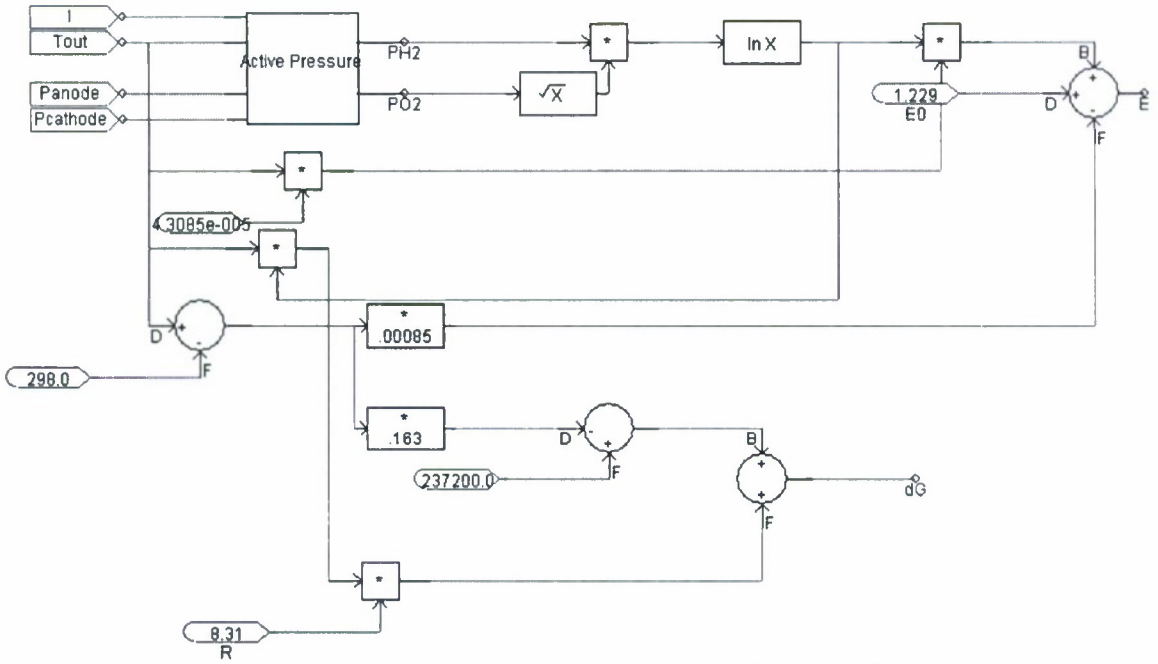



**Figure 4.3 - PSCAD sub module for internal potential E**

The internal potential module has a sub block called the Active Pressure module and the inner components of the block are given in Figure 4.4. This block is used to calculate the effective partial pressures of both hydrogen and oxygen. The effective pressures are used in the Nernst equation to find PEMFC output voltage.

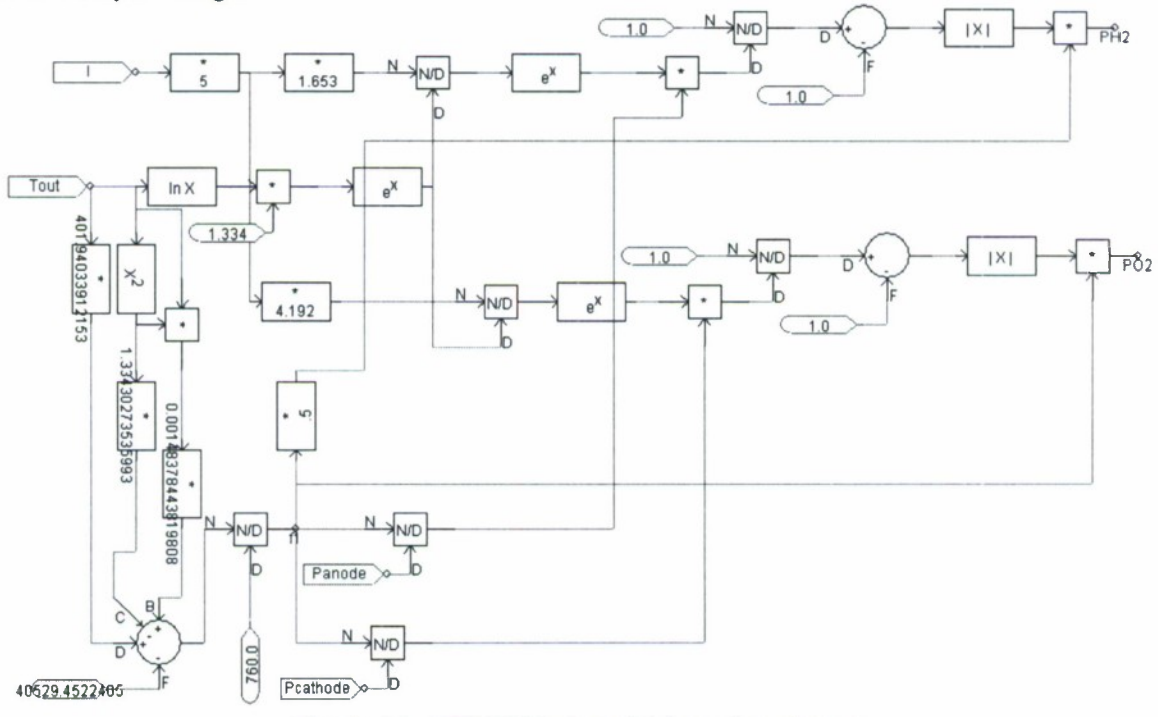



**Figure 4.4 - PSCAD block model for active pressure**

## Equivalent circuit for the activation loss

Activation polarization results from the relatively slow speed of the reactions occurring within the cell. It depends on the nature of the electrode, ionic interactions, ion-solvent interactions, and the electrode-electrolyte interface. The loss due to activation polarization can be reduced by increasing cell temperature. The activation voltage drop is mainly divided into two parts, $V_{act1}$ and $V_{act2}$. $V_{act1}$ is the voltage drop affected only by the fuel cell internal temperature and it is modeled by a constant voltage source in series with a temperature-controlled voltage source. However, $V_{act2}$ is both current and temperature dependent and it can be modeled by the voltage drop across a temperature and current dependent resistor $R_{act}$. The resistor $R_{act}$ consists of a fixed resistor ($R_{act0}$), a current-dependent resistor ($R_{act1}(I)$) and current- and temperature-dependent resistor ($R_{act2}(I,T)$). An electric circuit model representing activation loss in the PEMFC is given in Figure 4.5.

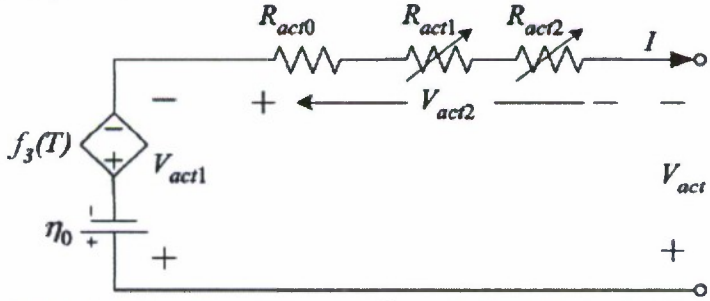



**Figure 4.5 - Electric circuit model for activation loss in PEMFC**

The PSCAD block for $V_{act1}$ is given in Figure 4.6 and the PSCAD block for $V_{act2}$ is given in Figure 4.7.

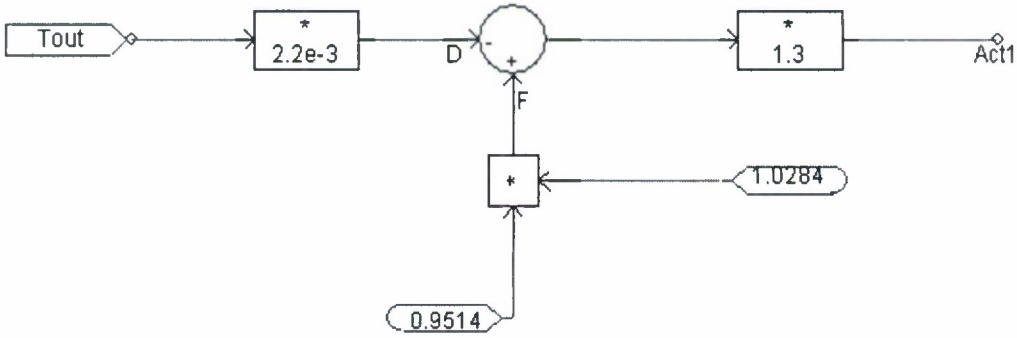



**Figure 4.6 - PSCAD block for Vact1**

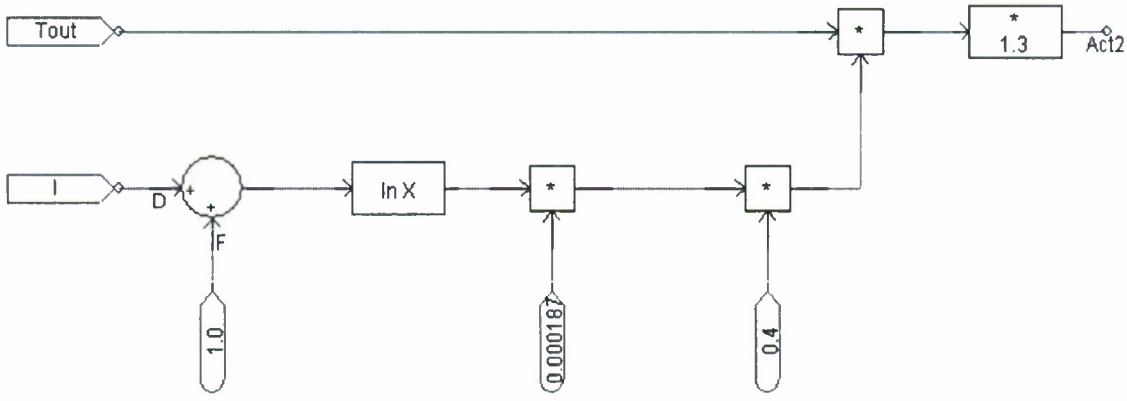



**Figure 4.7 - PSCAD block for Vact2**

## Equivalent circuit for ohmic voltage drop

Ohmic polarization results due to the resistance of the polymer membrane to the transfer of protons, and the resistance of the electrode and collector plate to the transfer of electrons. Therefore ohmic resistance of PEMFC consists of the resistance of the polymer membrane, the conducting resistance between the membrane and electrodes, and the resistances of electrodes. Ohmic voltage drop can be modeled by a current-and temperature-dependent resistor $R_{ohm}$. $R_{ohm}$ is composed of a constant part $R_{ohm0}$, a current dependent part $R_{ohm1}$, and a temperature-dependent part $R_{ohm2}$. Equivalent circuit model for ohmic voltage drop in PEMFC is given in Figure 4.8.

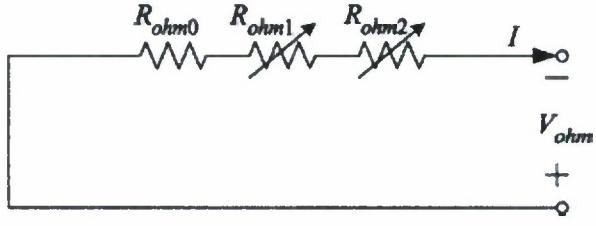



**Figure 4.8 - Equivalent circuit model for ohmic voltage drop in PEMFC**

A PSCAD model of the ohmic voltage drop in PEMFC is given in Figure 4.9. *Tout* is the stack temperature of PEMFC and *I* is the load current. Both them are variables. The numerical constants in the block are from the equations given in [***16***].

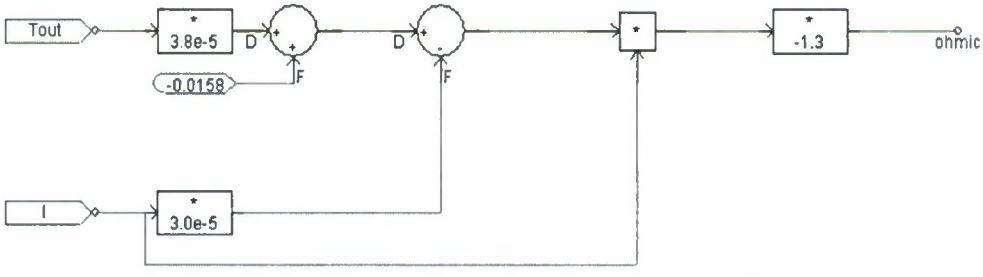



**Figure 4.9 - PSCAD model for ohmic voltage drop in PEMFC**

## Equivalent circuit for concentration voltage drop

Concentration polarization is due to gas concentration changes at the surface of the electrodes [***18***]. During the reaction process, concentration gradients can be formed due to mass diffusions from the gas flow channels to the reaction sites. At high current densities, slow transportation of reactants to the reaction sites is the main reason for the concentration voltage drop [***20***]. Concentration voltage drop can be modeled by a current-and temperature-dependent resistor $R_{conc}$. $R_{conc}$ is composed of a constant part $R_{conc0}$, a current dependent part $R_{conc1}$, and a temperature-dependent part $R_{conc2}$. Equivalent circuit model for concentration voltage drop in PEMFC is given in Figure 4.10 [***16***].

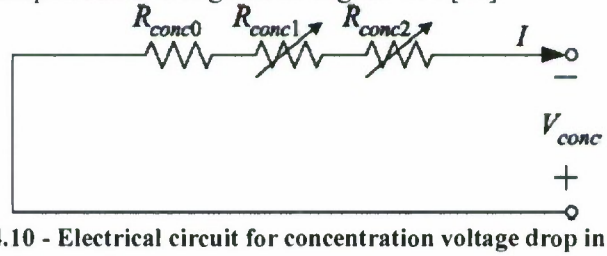



**Figure 4.10 - Electrical circuit for concentration voltage drop in PEMFC**

A PSCAD model for concentration voltage drop in PEMFC is given in Figure 4.11.

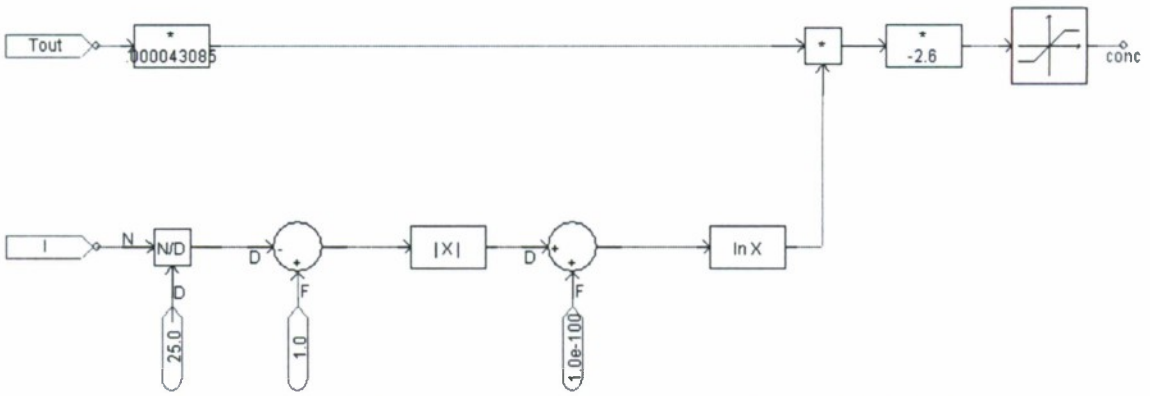



**Figure 4.11 - PSCAD model for concentration voltage drop in PEMFC**

## Equivalent circuit model for capacitance of double-charge effect

Fuel cells also exhibit a fast dynamic behavior known as the "charge double-layer" phenomenon. The "charge double-layer" stores electrical charge and thus energy. The collection of charges by the layer generates an electrical voltage that corresponds to the combination of activation polarization and concentration polarization. Whenever the current suddenly changes, it takes some time before the activation polarization and concentration polarization follow the change in the current [***21***]. The layers can store electrical energy and behave like a ultracapacitor [***16***]. The capacitance can be calculated through measurement of the dynamic response of a real fuel cell stack in a very short time range (millisecond) [***22***]. [Figure 4.12 illustrates how charge double-layer effect together with the activation, concentration, and ohmic resistances model the fuel cell dynamic response [***18***].

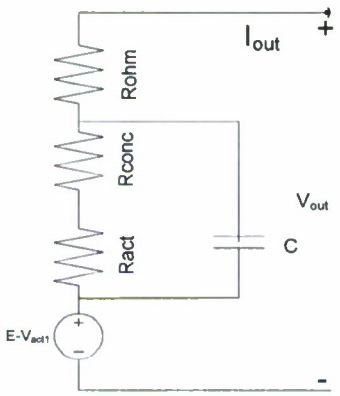



**Figure 4.12 - Equivalent circuit of the double charge-layer effect inside PEMFC**

A PSCAD block modeling the charge double-layer effect is given in Figure 4.13. The gain of the block transfer function is 1 and time constant is 40s.

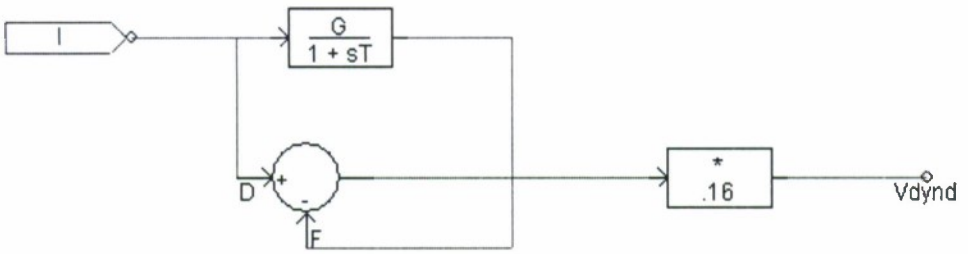


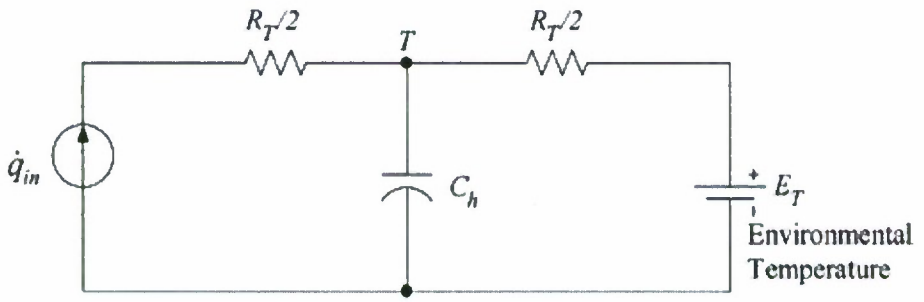

**Figure 4.13 - PSCAD block for charge double-layer effect**

## Circuit model for thermodynamic block

There are some analogies between the thermodynamic quantities and electrical quantities. These analogies enable us to develop an electrical circuit model for the thermodynamic block. The analogies between thermodynamic and electrical quantities are given in Table 4.1. The thermodynamic property inside the fuel cell is described in [***16***]. The equations described in [***16***] can be simulated by the *R-C* circuit given in Figure 4.14 [***19***].

| Electrical potential: $U$(V) | Temperature: $T$(K) |
|---|---|
| Electrical current: $I$(A) | Heat flow rate: $P_h$(W) |
| Electrical resistance: $R$(Ω) | Thermal resistance: $\theta$ (K/W) |
| Electrical capacitance: $C$(F) | Heat capacity: $C_h$ (J/K) |
| $R * I = \mathrm{U}$ | $\theta * P_h = T$ |
| $I = C * \frac{du}{dt}$ | $P_h = C_h * \frac{dT}{dt}$ |

**Table 4.1 - Analogies between thermodynamic and electrical quantities**




$R_T$ = Thermal Resistance
$C_h$ = Heat Capacity

**Figure 4.14 - Equivalent circuit for the thermodynamic property inside the PEMFC**

The power consumed by the activation, ohmic, concentration losses is regarded as a heat source which results in a temperature rise in the fuel cell. The rate of change of heat source is given by:

$$q_{in} = (E - V_{out}) * I \tag{4.1}$$

Where $R_T$ is the thermal resistance due to air convection in the fuel cell, which can be written as:

$$R_T = \frac{1}{A_{cell} * N_{cell} * h_{cell}} \tag{4.2}$$

Where $h_{cell}$ is the convective heat transfer coefficient (W/(m$^2$K)), $N_{cell}$ is the number of cells in series in the fuel cell stack, $A_{cell}$ is the area of individual cell [***16***].

The PSCAD block representing the thermodynamic propertues of PEMFC is given in Figure 4.15. The input parameters of the block are load current (*ISS*), room temperature (*Troom*), and temperature of PEMFC stack (*Tout*). The only constant parameter to the thermodynamic block is room temperature (307.7 K); both load current and temperature of PEMFC stack are not constant. A detailed description on the equations used for the modeling of the thermodynamic block is given in [***16***].

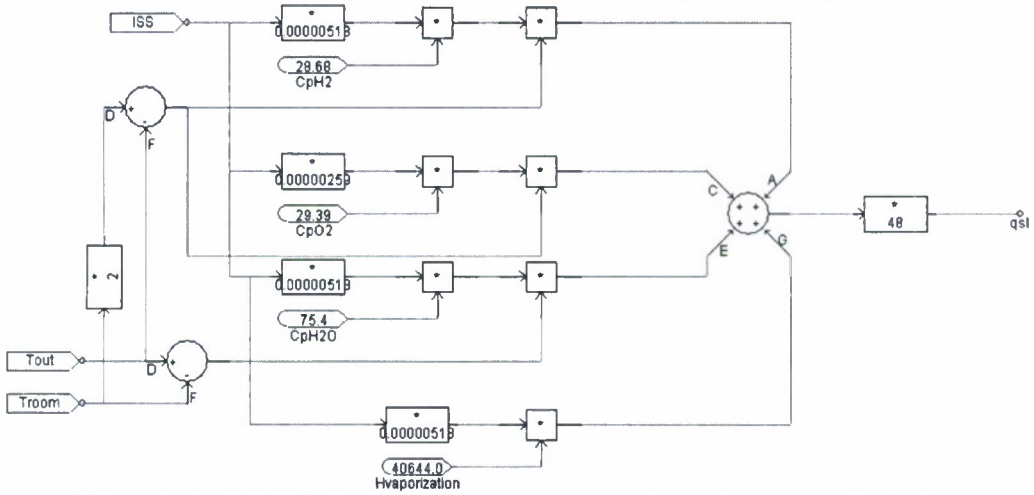



**Figure 4.15 - PSCAD block representing the thermodynamic property of PEMFC**

### *PSCAD model structure of PEMFC*

The previous section has introduced all the chemical, electrical and thermodynamic properties of PEMFC. All of the appropriate and significant PEMFC properties are modeled using electrical equivalent circuits. The full PSCAD model of PEMFC is a combination of the above mentioned individual blocks. The outer block of PSCAD modeling PEMFC is given in 4.16. The input parameters of the PEMFC block are load current (fed back from the external electric power circuit) (*I*), anode pressure (*Panode*), cathode pressure (*Pcathode*), room temperature (*Troom*), initial temperature (*Tinitial*). The output parameters of the PEMFC block are output voltage (*Vout*) and stack temperature (*Tout*). The circuit model in PSCAD representing PEMFC is given in Figure 4.17. Inner block combines the terminal voltage and thermodynamic block of PEMFC. This block also represents the number of cells in series in the stack. In this case there are 48 cells in series as seen near the bottom of Figure 4.17. Output temperature is controlled through a saturation block. The lower limit of the saturation block is 273 and the upper limit of the saturation block is 373.

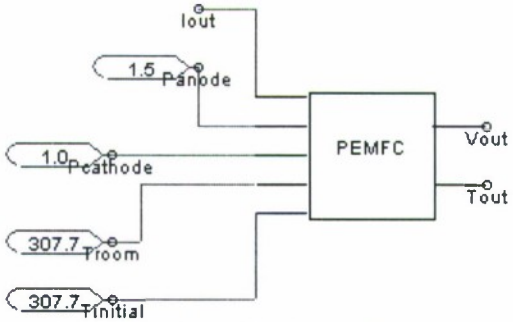



**Figure 4.16 - PSCAD outerblock representing PEMFC**

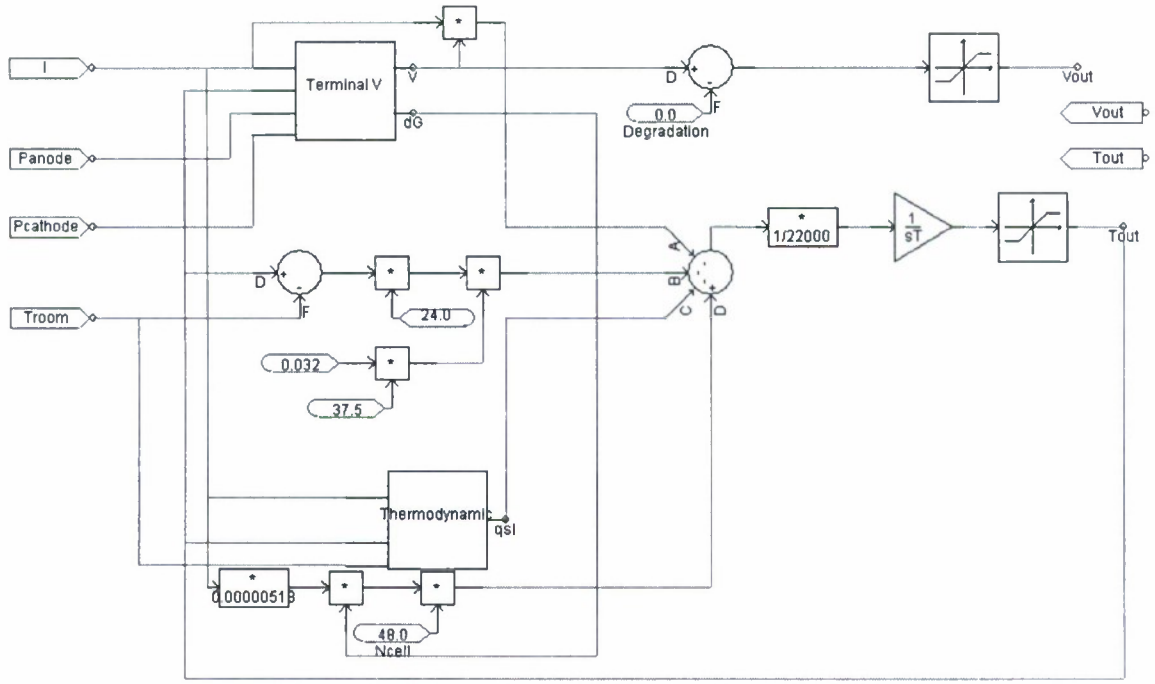



**Figure 4.17 - Inner block of PSCAD model of PEMFC**

The thermodynamic block was explained in earlier. The terminal voltage block shown in the PSCAD model of Figure 4.17 is shown in Figure 4.18. The figure consists of block models of activation, concentration and ohmic polarizations of PEMFC, internal voltage of PEMFC, and a delay block that imitates the charge double-layer effect of PEMFC [***17***].

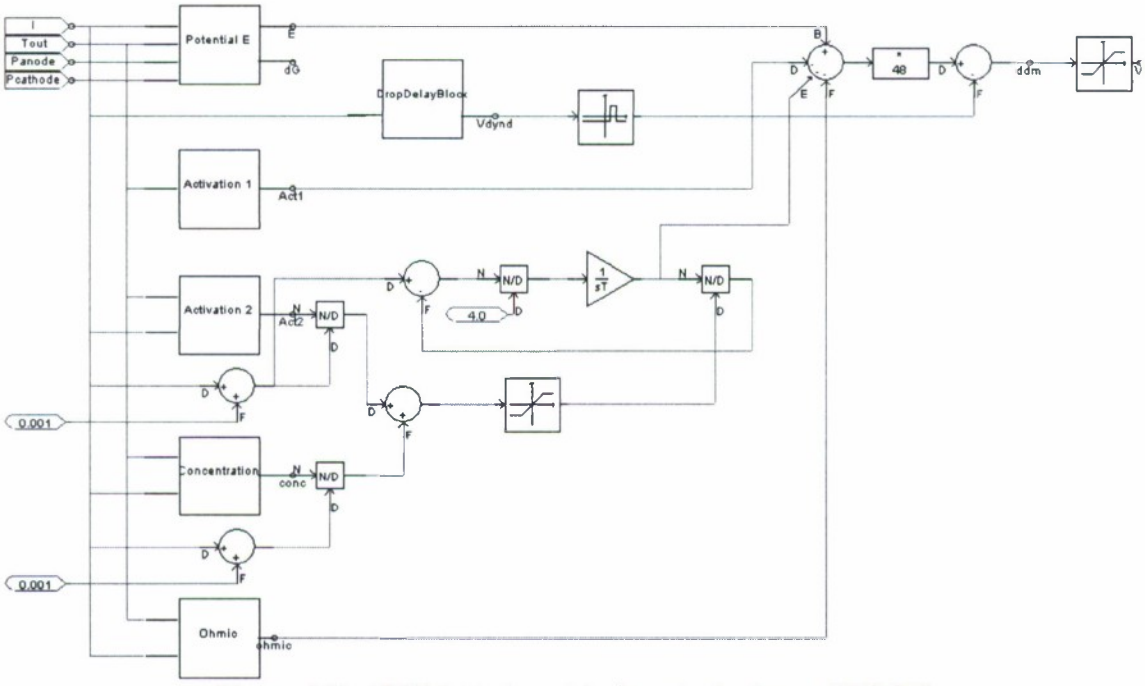



**Figure 4.18 - PSCAD block model of terminal voltage of PEMFC**

### *PEMFC model validation*

The data used in this chapter were obtained from a 500 W SR-12 PEMFC stack manufactured by Avista Labs (currently RelioOn, Inc.). The specifications of this fuel cell stack are given in Table 4.2 [***16***] .

| Description | Value |
|---|---|
| Capacity | 500 W |
| Number of cells | 48 |
| Operating environmental temperature | 5-35 $^0$C |
| Operating pressures | Panode=1.5 atm, Pcathode=1.0atm |
| Unit dimensions (W*D*H) | 56.5 cm*61.5 cm*34.5 cm |
| Weight | 44 kg |

**Table 4.2 - Specifications of SR-12 500 W PEMFC Stack**

### *Integration of Fuel Cell and Battery*

The integrated system of fuel cells and batteries to a high voltage DC bus through dc-dc converters is illustrated in Figure 6.6. Fuel cell is connected to high voltage DC bus using uni-directional dc-dc converter, and batteries are connected to high voltage DC bus using bi-directional dc-dc converter. The dc-dc converter power flows during battery discharge are given in Figure 6.7. During battery discharging mode, static stitch (SS) of the bi-directional converter is gated on to let the battery assist the fuel cell. Power flows of the dc-dc converter during battery charging are given in Figure 6.8. During battery charge mode, the static switch (SS) of the bi-directional converter is gated off, the excess energy in the high voltage DC bus flows through the freewheeling diodes of SS and the bi-directional dc-dc converter and charges the battery [***14*** ].

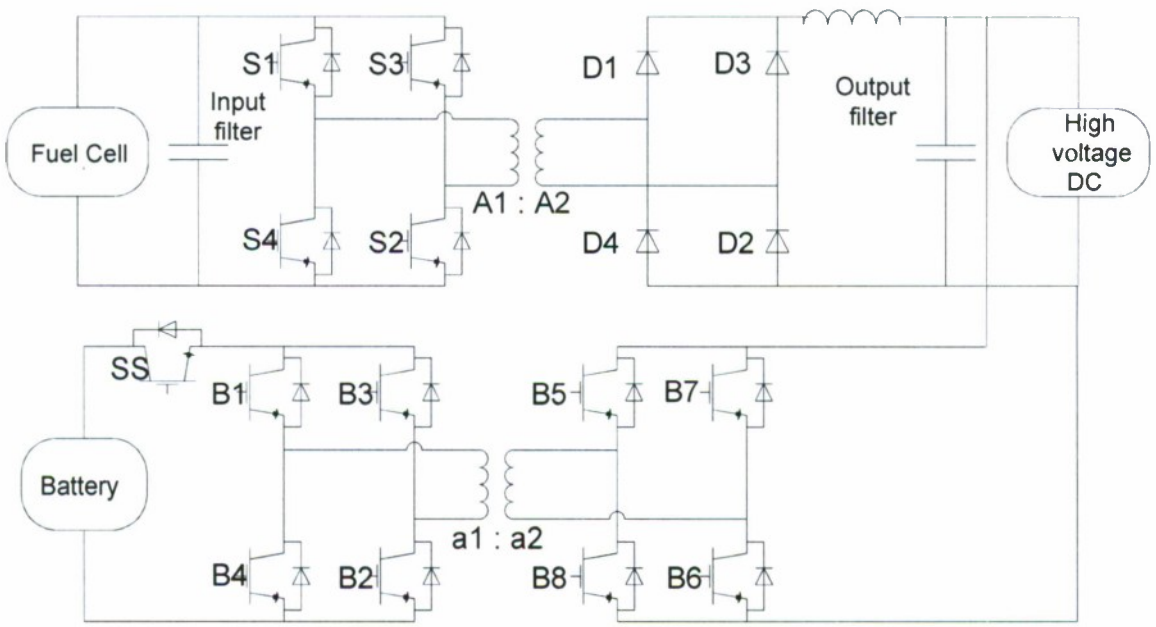



**Figure 6.6 - Integration of fuel cell and battery**

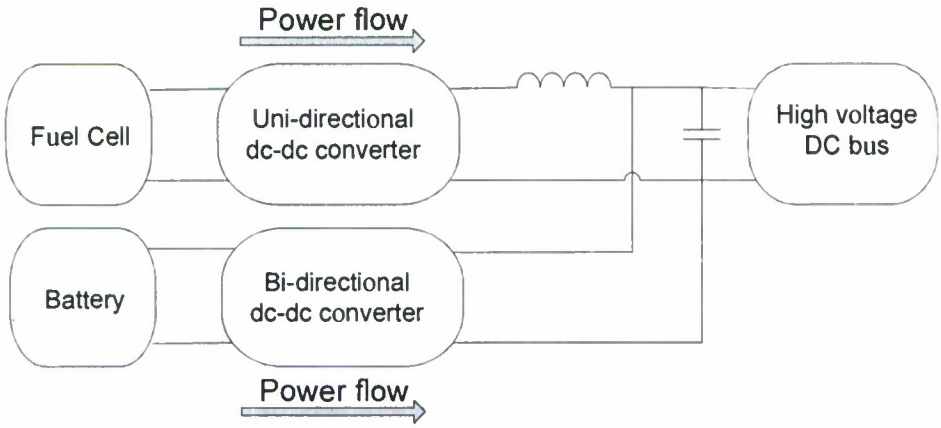



**Figure 6.7 - Power flows of dc-dc converter during battery discharging**

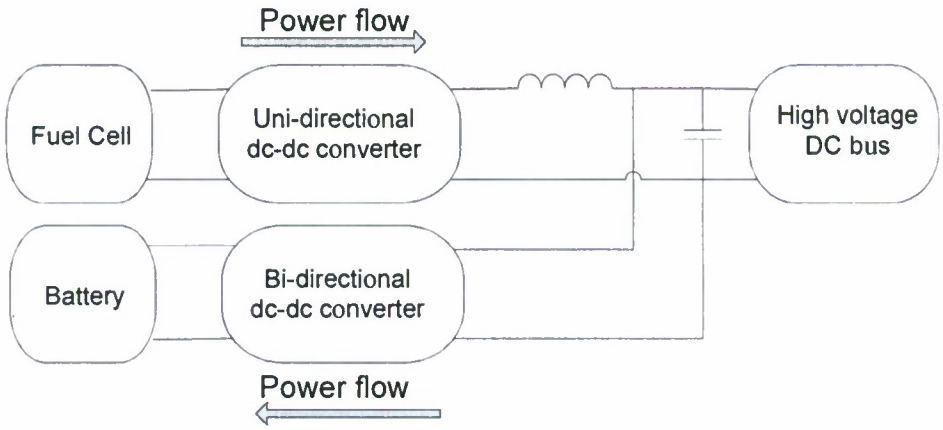



**Figure 6.8 - Power flows of dc-dc converters during battery charging**

The complete integrated system for AESD is given in 6.9. Five fuel cell modules are inputs for the dc bus. Fuel cell modules are connected to the dc-bus using diodes to block any circulating current between fuel cells. Twelve full-bridge dc-dc converters are the output of the integration bus. The secondary energy storage is connected to an individual high voltage dc bus for each of the 12 load input points in parallel with the full bridge dc-dc converter using the bi-directional dc-dc converter. The voltage at input side varies from 440 V- 800 V. However, output of the 12 high voltage buses maintains 720 ± 5% V.

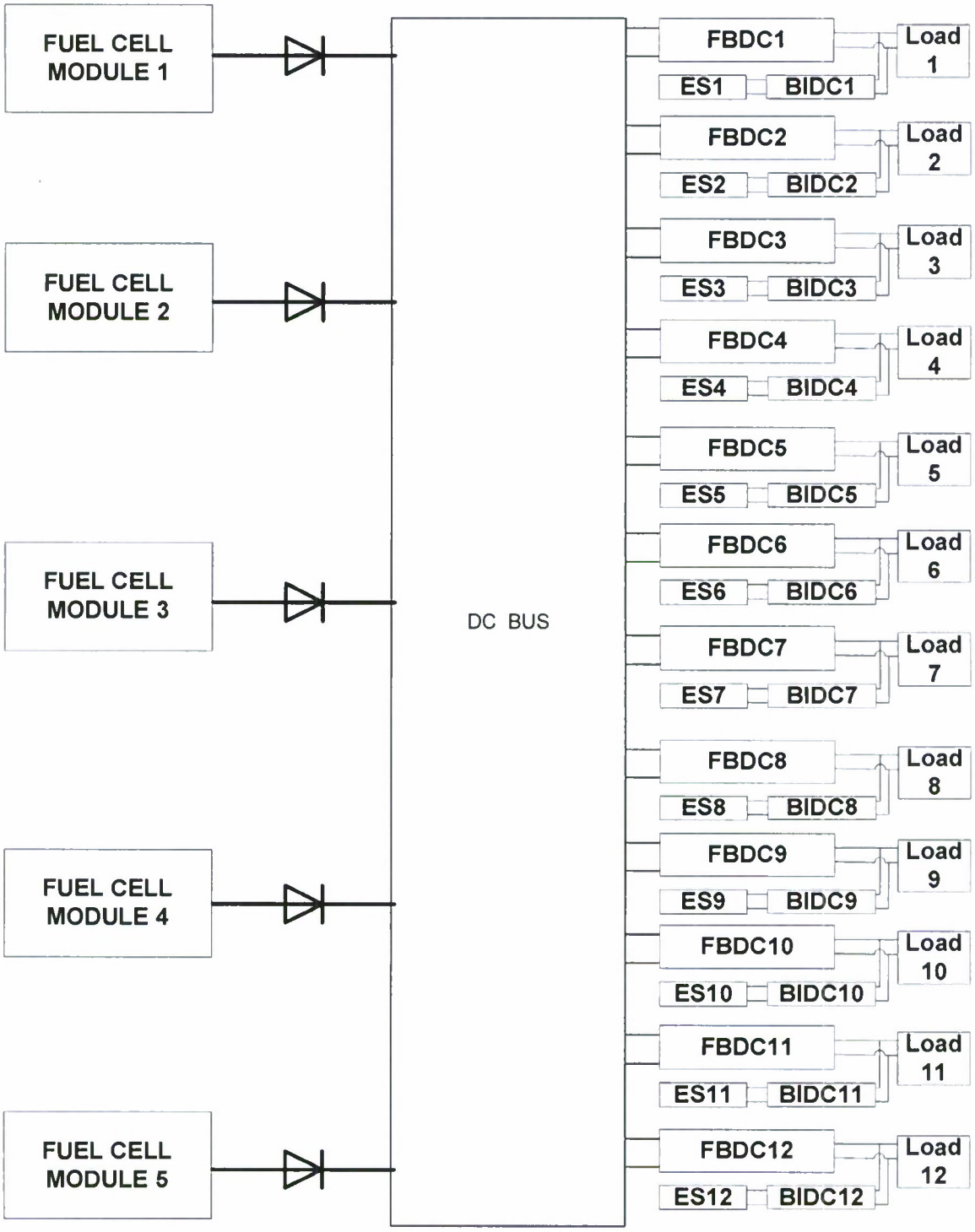



**Figure 6.9 - Fuel cell integration bus for AESD**

### *Lead-Acid Battery Model*

A simplified circuit model of a lead-acid battery is used for the PSCAD simulation [***16***]. The PSCAD model of the lead-acid battery is given in Figure 7.4. The values of capacitances and resistances are calculated on a 360 V and 82 kWh model. The assumption here is that model is that the battery model will remain within the range of interest (100 ± 5%), and that the difference between charge and discharge resistances is negligible [***27***].

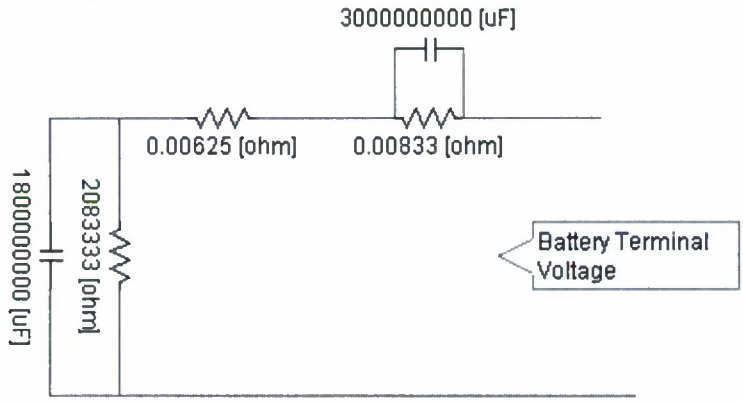



**Figure 7.4 - PSCAD model of lead-acid batteries**

### *Bi-directional dc-dc converter*

A bi-directional converter enables the power flow to and from the batteries. A PSCAD model of the bi-directional converter is given in Figure 7.5. The switches used for simulation study are non-ideal. Each of the switches has an on resistance of .01 Ω (typical value of PSCAD/EMTDC switch model). The high frequency transformer's turns ratio is 1:2. The batteries' voltage at the terminal is 360 V and the voltage required at the high voltage side bus is 720 V. This is the reason for selecting the above mentioned turns ratio.

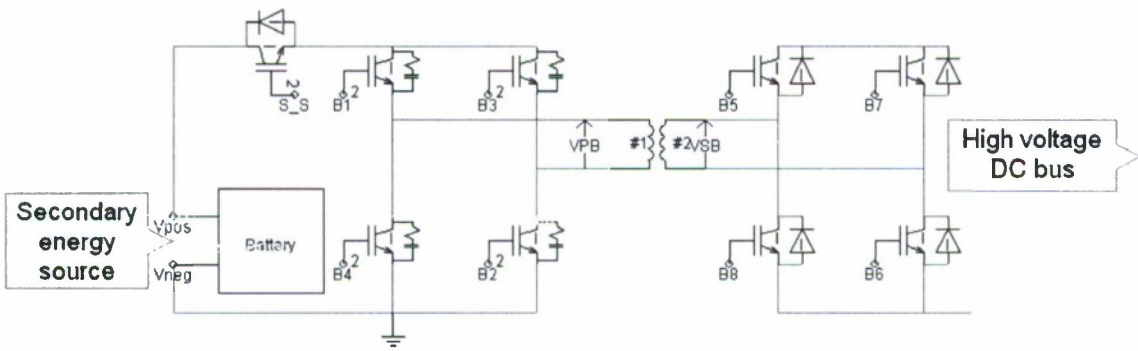



**Figure 7.5 - PSCAD model of bi-directional dc-dc converter**

## Control of bi-directional converter

The bi-directional flow of the dc-dc converter is controlled by turning switch S_S on and off. During the battery discharging mode, switch S_S is turned on, and during battery charging mode the switch is turned off; power can flow from the high voltage dc bus to the battery terminal through the anti-parallel diode of the switch S_S during battery charging mode. The switch S_S is voltage controlled. The dc voltage at the high voltage side of the converter is compared to a threshold (675 V), and whenever the voltage goes below the threshold the switch S_S is turned on to let the battery to deliver power. Whenever the high

voltage bus dc voltage is greater than or equal to the threshold, the switch S_S is turned off. The PSCAD voltage comparison block for the switch S_S is given in Figure 7.6.

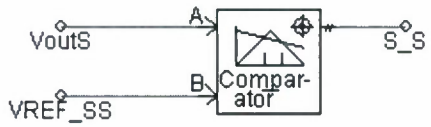



**Figure 7.6 - PSCAD block of voltage comparator**

### *PSCAD Model of the entire system*

PSCAD model of the entire system is given in Figure 7.7. The output voltage of the PSCAD block is divided by 1000 and multiplied by 20; this is to imitate the series combination of 20 fuel cells and to normalize the voltage from kilovolts to Volts. The output current is varied between 40 A and 80A. The control circuit for the system is given in Figure 7.8. The system models only the battery discharging mode (start up and load increase) therefore the switches on the secondary side of the battery transformer (B5 to B8) are turned off.

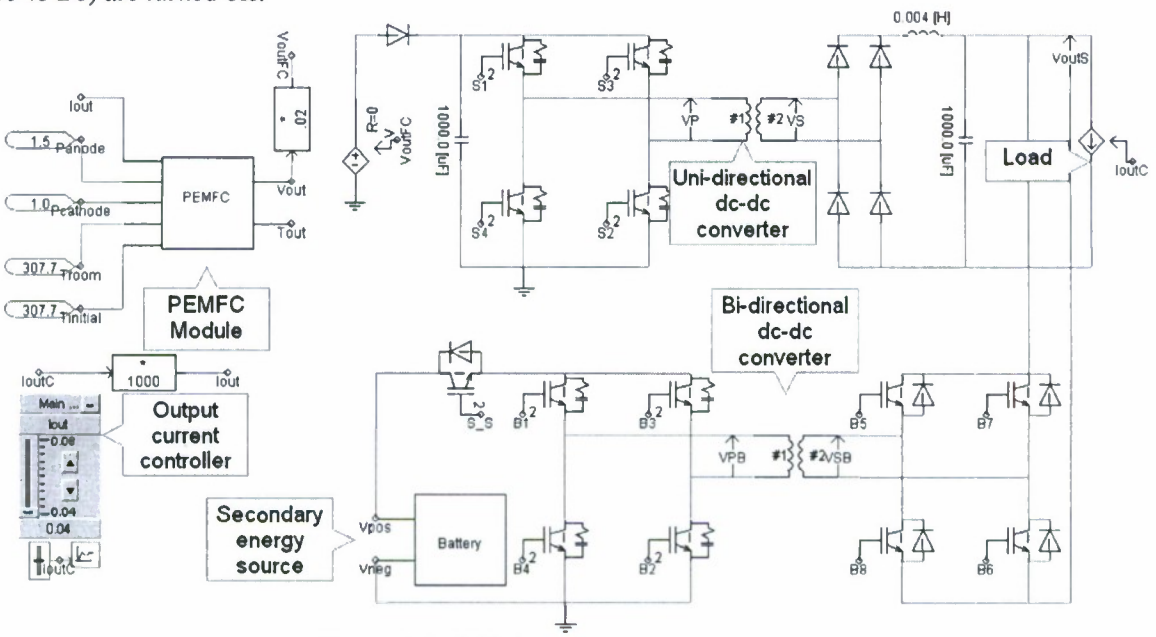



**Figure 7.7 - PSCAD model of the entire system**

## Dynamic response of the system

In the previous section, steady-state response of the system is analyzed. In this section, the dynamic response of the system is examined. The Load current is varied from minimum to maximum in step increments. The responses of both the fuel cell stack and secondary energy storage are evaluated. The Load current profile of the dynamic test is given in Figure 7.17. The Output voltages of fuel cell stack and high voltage dc bus are given in Figure 7.18. As the load current increases, the output voltage of the fuel cell stack decreases due to polarization voltage drops. The duty cycle for the dc-dc converters is given in Figure 7.19. For low load current, the controller employs a minimum duty cycle. As the load current increases duty cycle also increases and reaches its maximum value (.475) at maximum load current. Gating signals for the switch that connects secondary energy source to the high voltage dc bus are given in Figure 7.20. During the start up secondary energy source is connected to the dc bus to assist the fuel cell to meet the change in load current. Once the fuel cell picks up the load secondary energy source

is disconnected. At maximum load current secondary energy source is connected to the high voltage dc bus. The Temperature profile of the fuel cell stack is given in Figure 7.21.

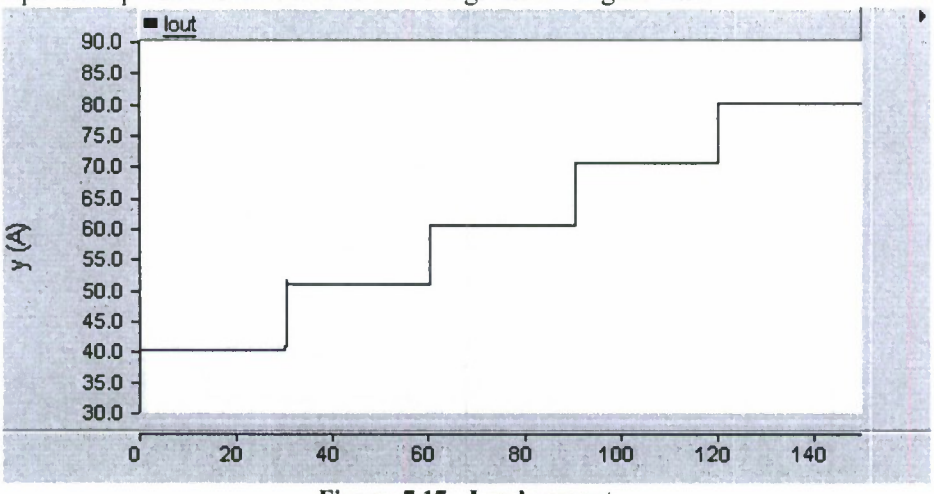



**Figure 7.17 - Load current**

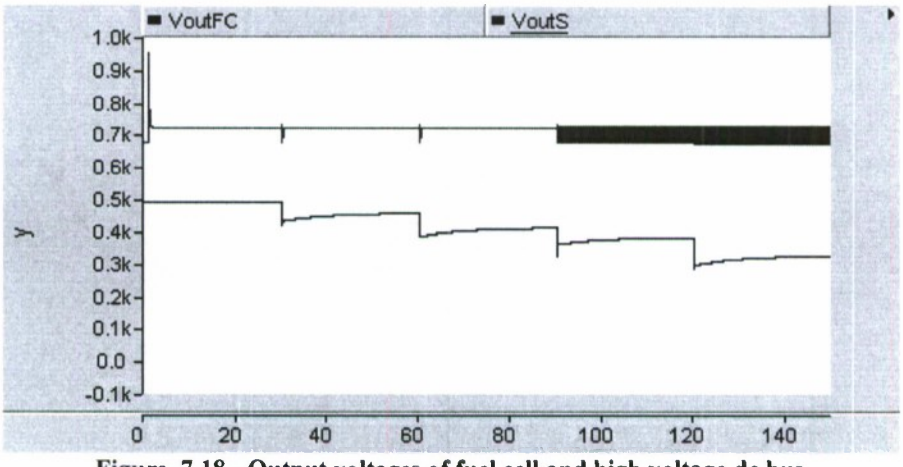



**Figure 7.18 - Output voltages of fuel cell and high voltage dc bus**

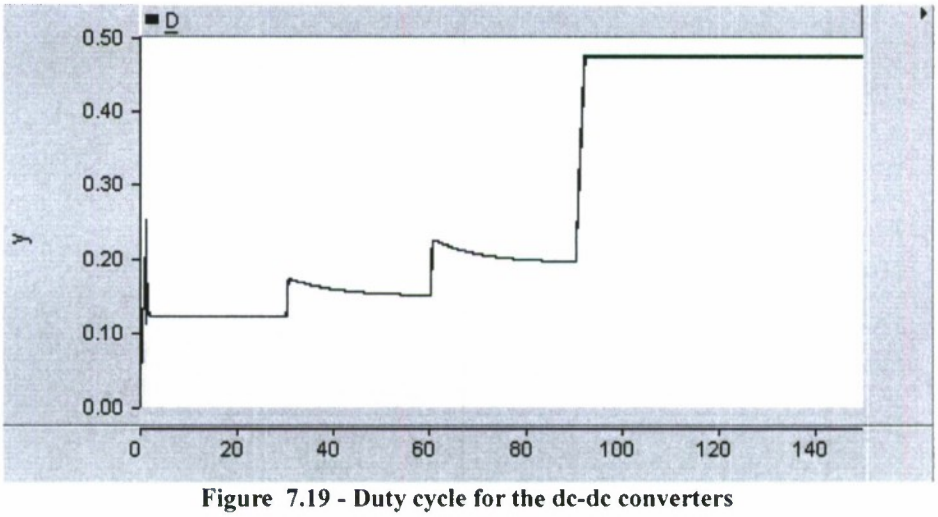



**Figure 7.19 - Duty cycle for the dc-dc converters**

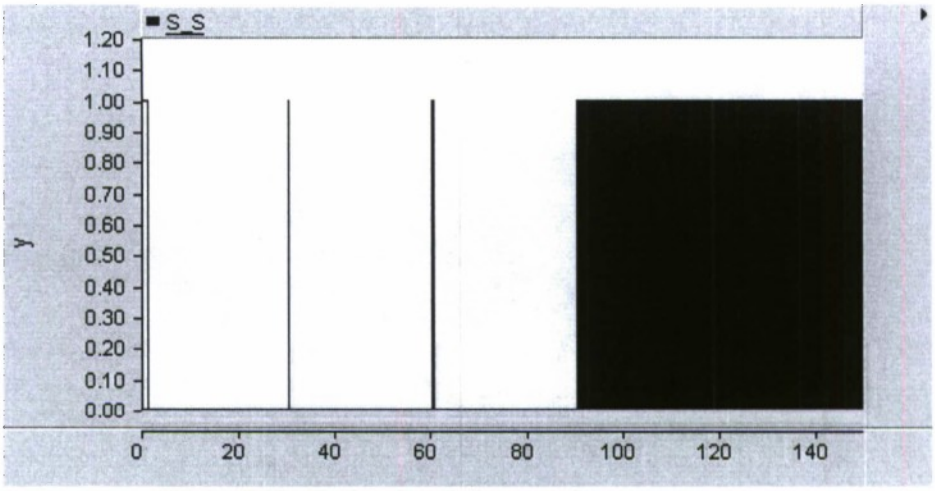



**Figure 7.20 - Gating signals for secondary energy source**

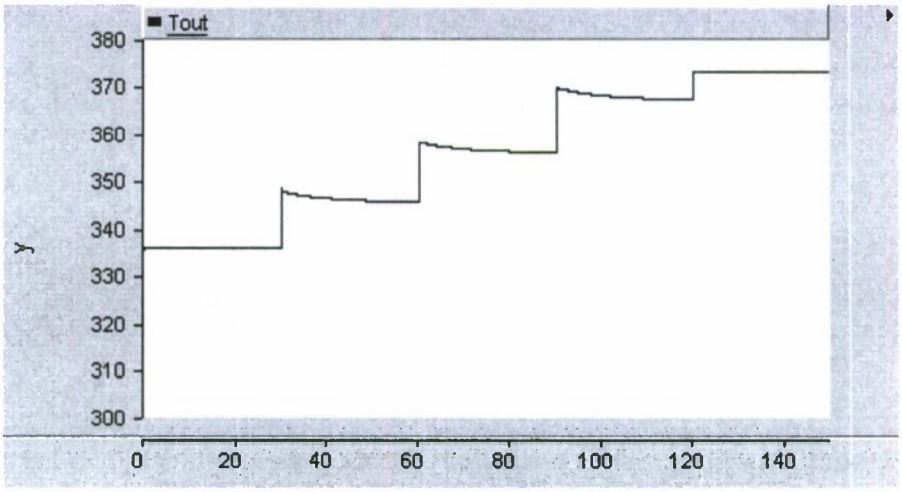



**Figure 7.21 - Temperature profile for fuel cell stack**

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## *Subproject b) Design of data acquisition system for the prototype destroyer with emphasis on monitoring electrical system performance and battery condition*

The Acoustic Research Detachment (ARD) of the Naval Surface Warfare Center, Carderock Division (NSWCCD) is located at the southern end of Lake Pend Oreille, in Bayview, Idaho. The ARD tests the acoustic characteristics of quarter scale models of ships in order to develop technology used in electric ships. The Advanced Electric Ship Demonstrator (AESD) is a quarter scale model of a destroyer built to demonstrate advanced electric ship and propulsion technologies. The AESD is currently being used to test various electrical systems on ship under different conditions.

### Problem

Data from the AESD's electric propulsion system is essential to the understanding and development of the electric ship technology. This performance data is not readily available for analysis either in real-time or post experimental. Due to the rarity and high cost of the test runs, the accuracy and availability of the data is exceedingly important. A Data Acquisition System (DAQ) is required to gather, manage and store this information for easy viewing and analysis.

### Existing System

The AESD currently has a data recording and storage system on board that collects and stores voltage, current and temperature data from the propulsion system batteries. This battery data is correlated with the time and location information from the Global Positioning System (GPS) receiver. The data monitoring and storage system is also being used for monitoring and controlling systems other than the propulsion batteries. This data collection system gives only real-time display of the information being gathered. Data collected by the existing system can be viewed while it is taken or after it has been downloaded in a spreadsheet format to an external system. It is difficult to organize and use this data for post-experimental analysis due to the large number of data points obtained from over 2000 channels.

## Objective

The objective of our project is to design and build a stand-alone prototype of a data acquisition and storage system that will interface with the existing systems on the AESD. We are narrowing the scope of our project to focus on acquiring voltage, current and temperature data from the propulsion systems batteries and the uninterruptable power supply (UPS) batteries. This data acquisition system will be designed to interface with other systems on board the ship to enable future expansion of the system.

The DAQ will manage and display data from existing and newly designed sensors. Battery voltage, current and temperature data will be taken and correlated with time and position information acquired from use of an existing GPS receiver on board the ship. We are designing a real-time graphical representation method of the collected data which will allow for easy viewing and data analysis during the experiments. The collected data will be downloadable to allow for post-experimental analysis and storage.

## Design Methodology

A data acquisition system was designed with the ability to collect, display, and store data collected on the AESD. The block diagram for the proposed data acquisition system is shown in Figure 41. The voltage, current and temperature data from the batteries will be displayed graphically in real-time. The data will also be written to an external hard drive for storage and post-experimental analysis. The data acquisition hardware used in our system was purchased from National Instruments. Our system utilizes LabVIEW™ tool kit to manage the data acquisition system.

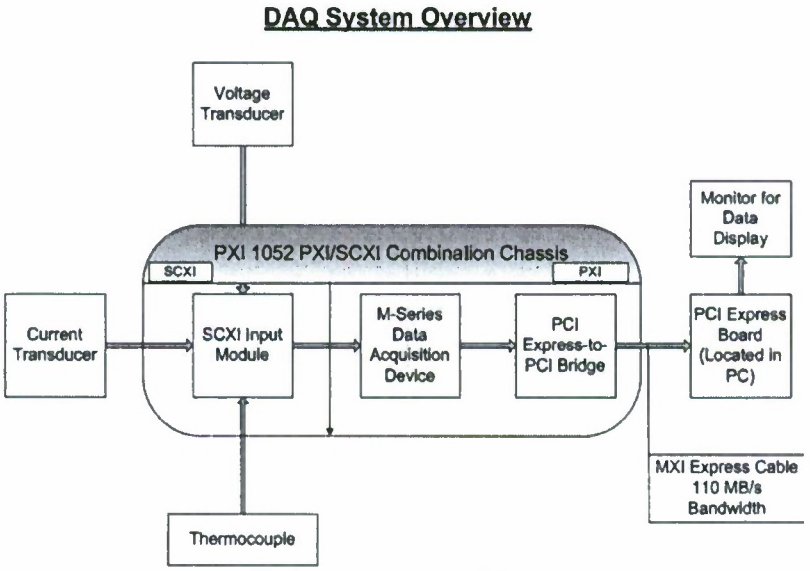



*Figure 41: Proposed block diagram of Data Acquisition System*

## System Specifications

The DAQ is to be designed according to the following specifications:

- **Ungrounded system** – As the DAQ will be on board the AESD, the DAQ needs to be ungrounded and all sensors need to be designed without a ground reference.

- **Minimum 12 hours of data storage** – This is required in order to store all the data that is obtained from a test run.
- **Space efficient and rack mountable** – The system must fit in one 6 ft tallx19-inch wide equipment rack
- **Ability to integrate with the existing data system on the ship** – The system will help manage the data that is obtained from existing data acquisition hardware on board the AESD.
- **120 VAC and 25 Amps of available power** – The power budget for a complete systems is a max of 3000 Watts

## DAQ hardware

The DAQ hardware shown in Figure 42 was purchased from National Instruments (NI). We decided to purchase the NI DAQ hardware after research into the capabilities of similar systems offered by major competitors. The LabVIEW™ toolkit, also developed by NI, allows graphical programming of the DAQ hardware. This level of integration allows a more rapid development time of more complex data acquisition and control software.

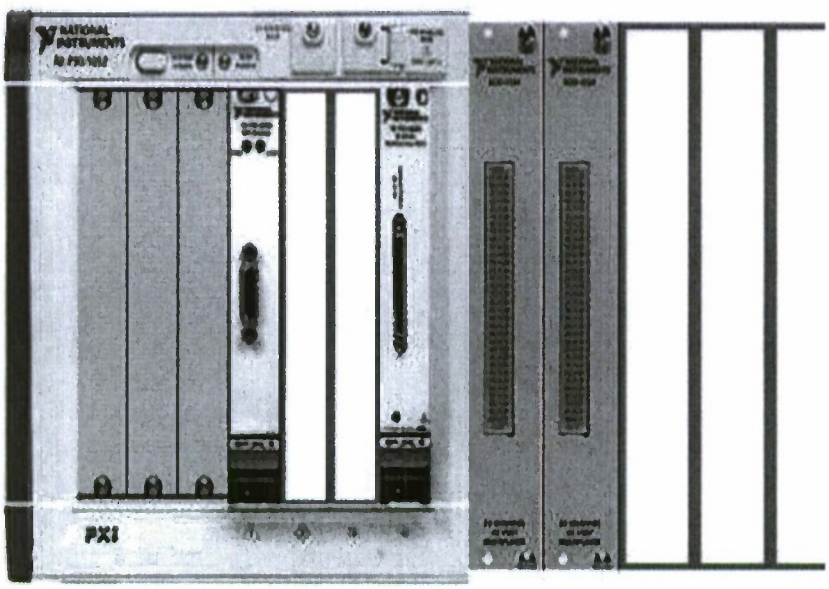



*Figure 42: National Instruments Data Acquisition System*

## LabVIEW™ Program

LabVIEW™ provides a graphical tool with built-in Virtual Instruments (VIs) that help in easier programming and acquiring data. LabVIEW™ programming is done on the *Block Diagram*. The user interface is called the *Front Panel*.

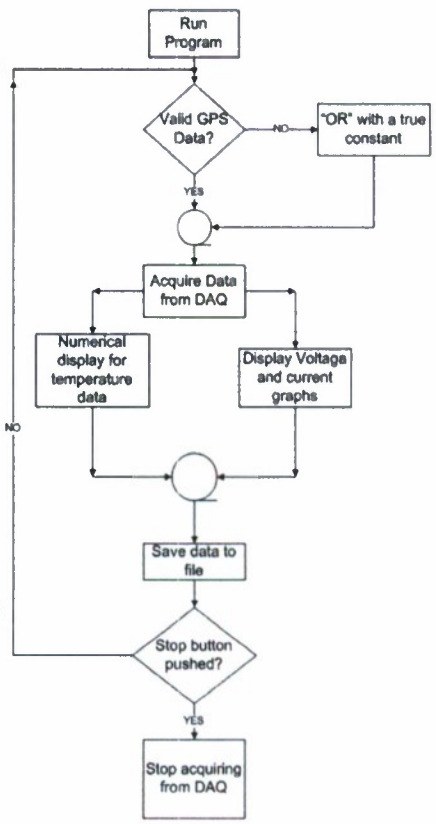



*Figure 43: Flow diagram of the Program*

The program for the NI DAQ was written in order to provide a user control and display. The program provides for a real-time display of all the measurements that are being made from the DAQ along with saving this data to a specified file. This file can be opened with analysis tools for post processing the data. The location and the file name can be changed from within the code.

A flow diagram for the program is given in Figure 43. This is the flow of what the block diagram does once the user starts running the program.

In order to start acquiring data, the user has to start the program once, and the data will be acquired till a stop condition is met. The code checks for a valid GPS signal available. If this happens, then the system starts acquiring data, displaying the voltage and current data in graphical form while displaying the temperature data in a numerical form.
The voltage, current and temperature data along with the GPS data is combined and is saved to file. At this point, the program checks for a stop condition. If a stop condition is present, then data acquisition stops otherwise the program continues to run and acquire data.

## Features of the Control Program

- **Front panel**: The front panel provides the user interface from which the program can be controlled. The control/Indicator tab of the front panel is shown in Figure 44.


*Figure 44: Front Panel Control/Indicator Tab*

The front panel has been divided into different tabs:

- **Instructions:** Provides the user with instructions on how to control the program and how to read the different LEDs that are on the Control/Indicator tab. It also provides instructions on simple navigation from the Front Panel to the Block Diagram if any changes are required in the program.
- **Control/Indicator:** Displays the different LEDs that indicate how different parts of the program are performing. It also has a time indicator which displays how long the data acquiring has been going on for.
- **Error:** Displays the different errors (if any).
- **Voltage Graphs:** Displays the different voltage graphs from the opto-coupler and ABB voltage sensor channels.
- **Current Graph:** Displays the current graph
- **Temperature Readings:** Provides the temperature readings in a numerical form.

- **GPS:** Provides the specified GPS data.

- **Data acquiring and displaying**: Acquires the Voltage (V), Current (A), and Temperature (°F) from the battery bank and is displayed on the front panel graphs. Figure 45 gives an example of this display.

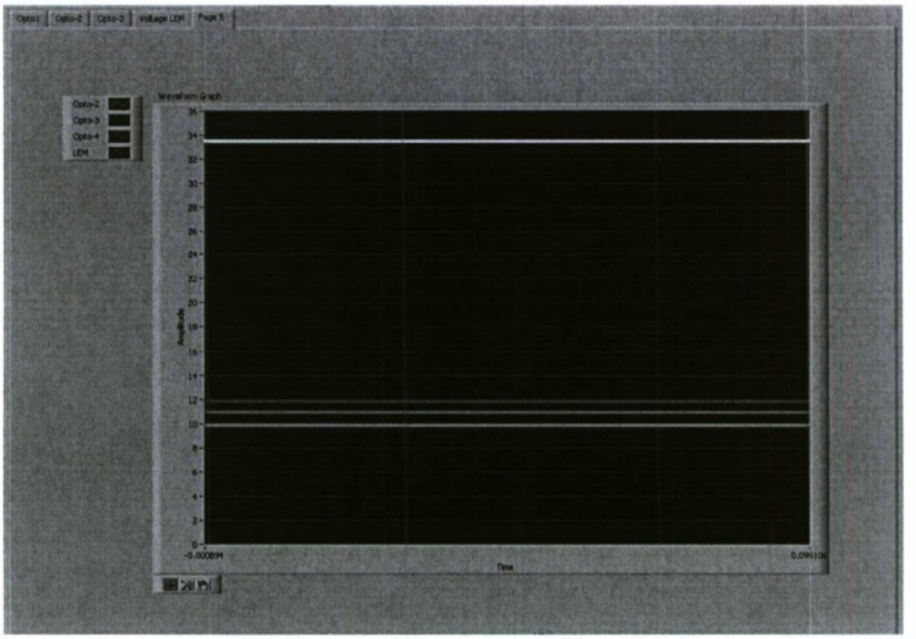


*Figure 45: Output voltage real-time display*

- **File saving**: The acquired data is saved to a specified file. This file name and location can be changed according to the user's needs. The data is saved in a LabVIEW™ Measurement File (.lvm) format which allows the user to open this file with different analysis tools. The data is also saved to a backup file in case the main file is corrupted.

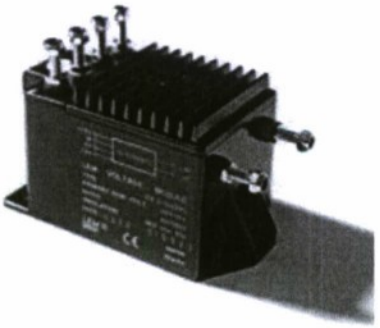
- **Time/Location stamping**: The saved data to the file is time and location stamped. This data is obtained from the serial communication with the GPS.

- **Error logging**: If an error is observed on the system, it is documented along with a time and location stamp in a text file called 'Error Log'.

## Sensors

Sensors were an integral part of designing a robust data acquisition system. Sensors need to be accurate in a wide range of operating conditions and just as importantly, they need to consume as little power as possible. While there are a lot of plug and play sensors available that would fit our needs, cost was also a factor in determining which sensors we would use in our lab setup and which ones we would recommend for our final configuration. Extensive research was done to find sensors that could be used in our system for both proof of concept as well as in the final configuration. Below is a brief summary of the sensors we used. This includes sensors for voltage, temperature and current measurements as well as a GPS receiver that was used to provide time and location stamping.

## ABB Voltage Sensor



### Features

- Closed Loop Hall Effect Voltage Transducer
- Measuring Range: 0 to 500 V
- Output Voltage: 0 to 10 V (Max)
- Supply Voltage: ± 15 VDC
- ± 0.2% Accuracy at 25 °C

*Figure 46: ABB Voltage Sensor*

## LEM Current Transducer

### Features

- DC Current Transducer
- 3 Jumper Adjustable Ranges: 5, 10, 20 Amp Max
- Supply Voltage: 20-50 VDC
- ±1% Accuracy at 25 °C

*Figure 47: LEM Current Transducer*

## Type K Thermocouples

### Features

- Temperature range: -452.2°F to 1562°F
- SCXI Modules designed for Thermocouple inputs with integrated Cold Junction Compensation ICs
- Cost is approximately $1.00/ft for shielded thermocouple wire

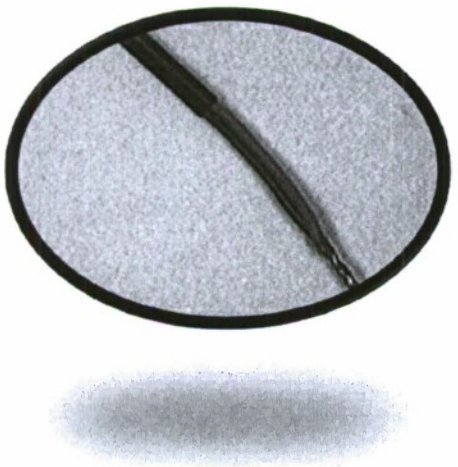


*Figure 48: Type K Thermocouple*

## Optocoupler Type Sensors

The ABB Voltage Sensors shown in Figure 46 are perfect for the battery voltage measurement due to the capability of handling very high voltages, but they were too expensive considering we need nearly 800 of them for the final configuration. This led to the need to design our own voltage sensors that would be capable of handling high voltages present on the battery bank and isolate the voltages from the DAQ. Shown below in Figure 49 is the voltage sensor we designed using linear optocouplers. Figures 50 and 51 show the simulation results and experimental results, respectively.

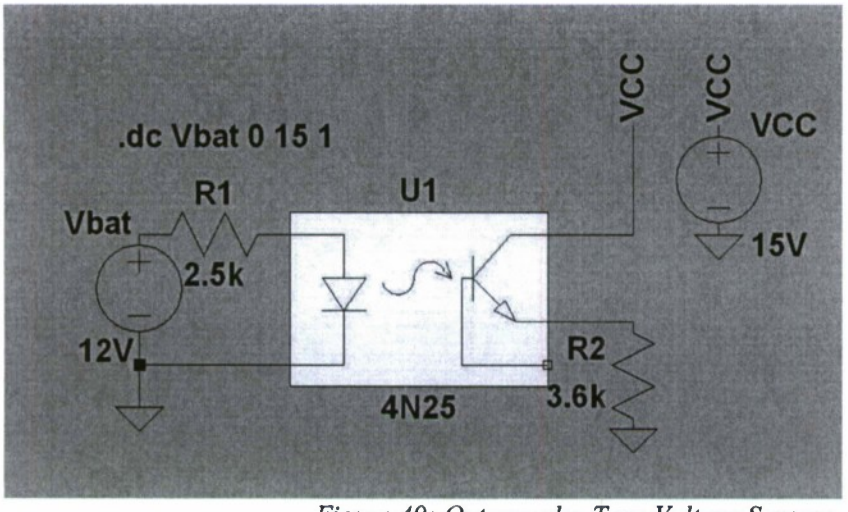



*Figure 49: Optocoupler Type Voltage Sensors*

## Features

- Low power consumption
- Only one voltage reference or ground reference
- Simple design
- Linear input to output

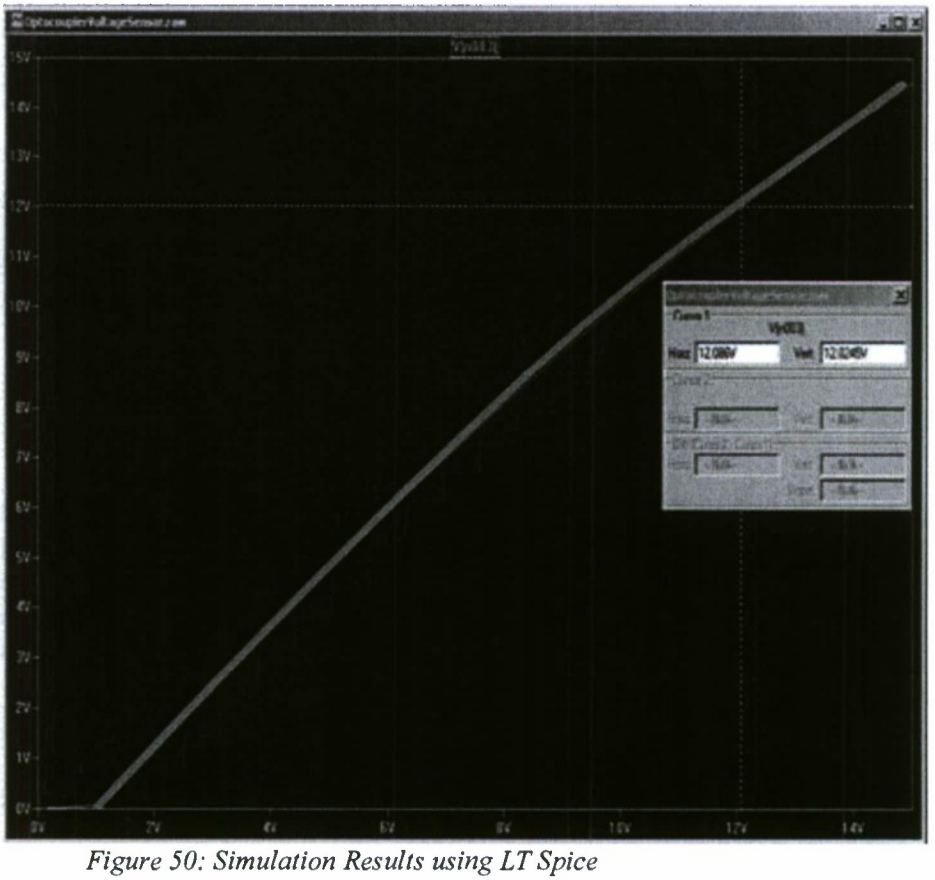


*Figure 50: Simulation Results using LT Spice*

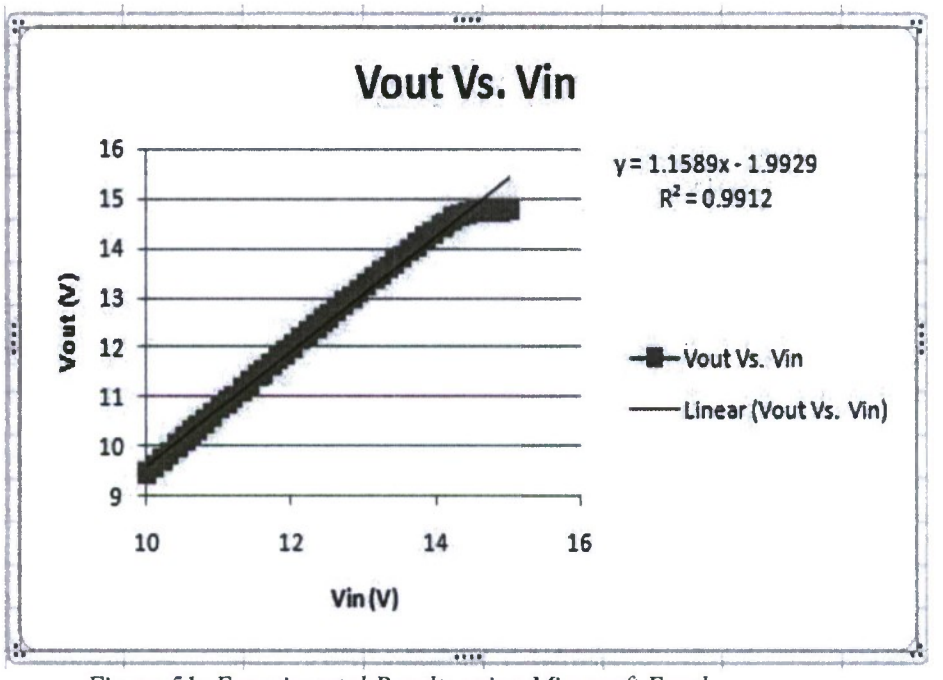



*Figure 51: Experimental Results using Microsoft Excel*

## GPS Receiver

As part of our project deliverables, we needed to be able to acquire GPS data for time and location stamping to accompany the data from the batteries. This data is transferred from the GPS unit shown figure 52, to the PC via a serial cable in National Marine Electronics Association (NMEA) format. This data was then read into LabVIEW™ and merged with the battery data. This was done for proof of concept to show that time and location stamping can be done if GPS is available.


*Figure 52: Garmin GPS Receiver*

## Testing

The lab model was setup following the system architecture. The actual lab setup which includes the ABB Voltage sensors, the Current LEM Sensor, the designed Voltage Sensors and the K-type thermocouple sensors. The lab model is shown in figure 53.

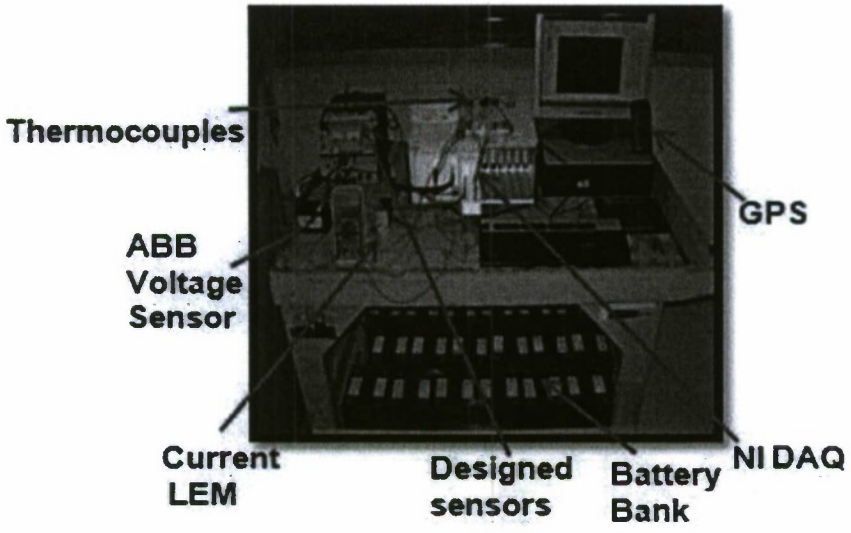



*Figure 53: Lab model*

Tests were run on the whole system shown above for a period of 2 hours where different measurements were taken. Measurements were taken on 9 different channels which included:

- ABB Voltage Sensor: *1 channel*
- Current LEM Sensor: *1 channel*
- Optocoupler Voltage Sensors: *3 channels*
- K-type Thermocouple Sensors: *4 channels*

GPS data was simultaneously recorded for this test run. The measurements taken from these channels, along with the GPS string, were written to a LabVIEW™ Measurement File (LVM). An error log was also kept for this test run and no errors were recorded.

Figure 54 shows the saved data file from the test run. It only shows the first couple of sets of data points along with the file headers. The LVM file in this case has been opened with Microsoft Excel™.

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Multi_Headings | No | | | | | | | | | | | | | | |
| X_Columns | One | | | | | | | | | | | | | | |
| Time_Pref | Absolute | | | | | | | | | | | | | | |
| Operator | Administrator | | | | | | | | | | | | | | |
| Date | 12/2/2008 | | | | | | | | | | | | | | |
| Time | 54:21.3 | | | | | | | | | | | | | | |
| ***End_of_Header*** | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | |
| Notes | | | | | | | | | | | | | | | |
| Channels | 14 | | | | | | | | | | | | | | |
| Samples | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | 1 | 1 | 1 | |
| Date | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | 12/2/2008 | |
| Time | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | 54:21.5 | |
| Y_Unit_Label | | | Volts | Volts | Volts | Volts | Volts | Volts | Volts | | | | | | |
| X_Dimension | Time | Time | Time | Time | Time | Time | Time | Time | Time | Time | Time | Time | Time | Time | |
| X0 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | |
| Delta_X | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | 1 | 1 | 1 | 1 | 1 | |
| ***End_of_Header*** | | | | | | | | | | | | | | | |
| Time | Voltage | Current | Opto 1 | Opto 2 | Opto 3 | thermo0 | thermo 1 | thermo 2 | thermo3 | Latitude | Longitude | Speed(knots) | Untitled 3 | Untitled 4 | Comment |
| 0 | 33.405331 | -0.003163 | 11.84453 | 9.905565 | 11.037454 | 0.703502 | 0.663948 | 0.703982 | 0.722095 | 0 | 0 | 16.5 | 0 | 0 | |
| 0.1 | 33.587856 | -0.003163 | 11.846141 | 9.903555 | 11.032622 | 0.706079 | 0.663787 | 0.703177 | 0.72274 | | | | | | |

*Figure 54: Example of saved datafile format*

This data being saved was also displayed on the Front Panel of the LabVIEW™ program in real time. The numerical display for the temperature readings is shown in Figure 55.

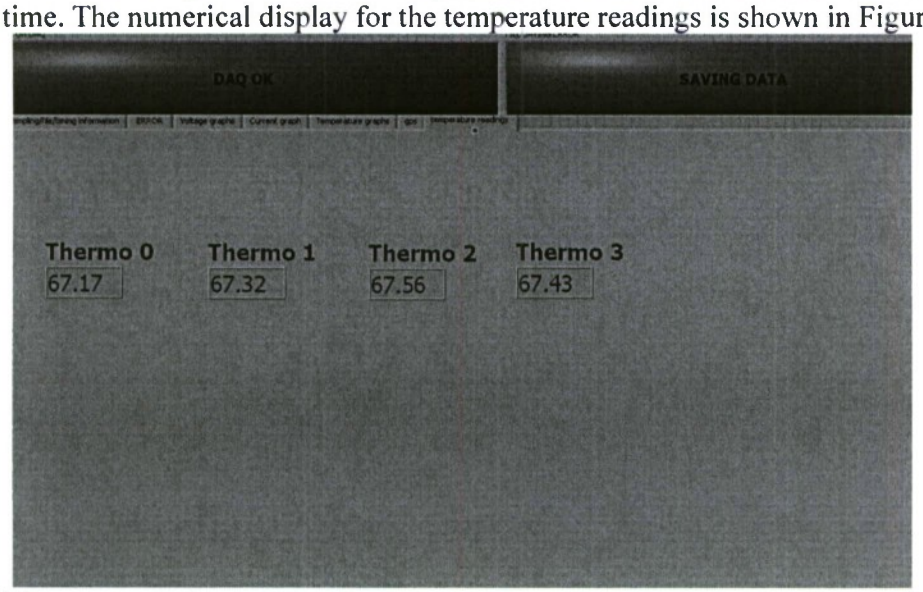



*Figure 55: Temperature display.*

Figure 56 shows the display for the current data that is being taken by the LEM Current Sensor. The current was being drawn by a variable resistive load bank.

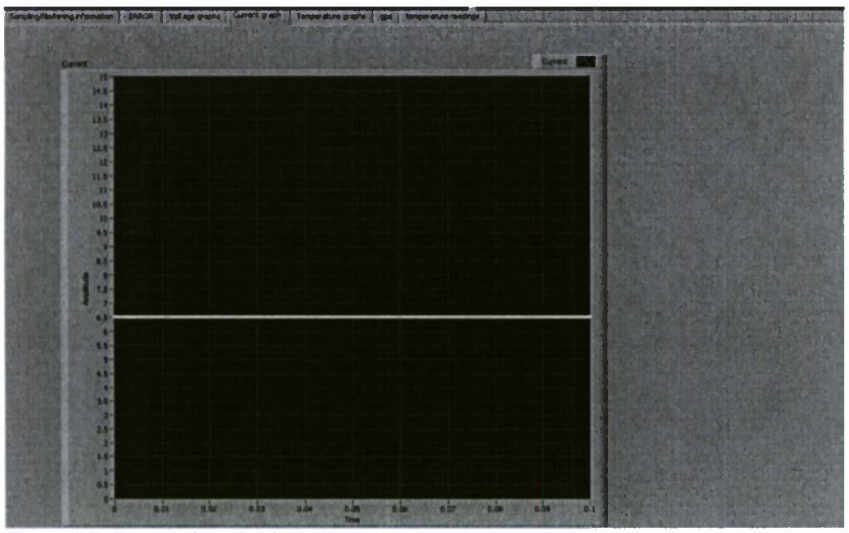


*Figure 56: Current data display*

Figure 57 shows the display for the voltage data measured from the optocoupler sensors and the ABB Voltage Sensor. The white plot indicates the measurement for the ABB Voltage Sensor and the red, green and blue indicate the optocoupler sensor measurements. The ABB Voltage sensor was measuring across all 18 batteries in the bank to get a total measurement and the optocoupler sensors were across 6 of the 2V batteries to test in the 12 V range.

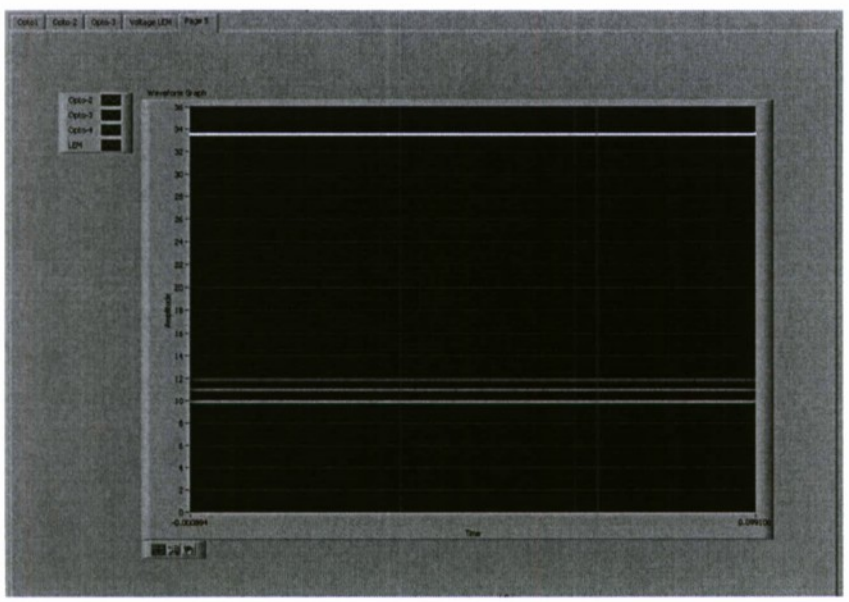


*Figure 57: Voltage data display*

## Calculations

In order to define some specifications, calculations were done for the complete system. The ARD required that latency be less than 6 seconds from measurement to display and storage, and that the power consumption be less than 3000 Watts.

## Latency

The latency for this system is defined the time that a change on one of the sensors is acknowledged and observed on the display. The latency is dependent on the sampling frequency. With a higher sampling frequency, the changes were transferred faster.
In order to observe a change on the Current display, a load bank was used. The latency for the system was observed to be approximately 1 second. This is the latency when the GPS is included in the system. Without the GPS in the system, the latency is less than a 100 ms (0.1 seconds) as the LabVIEW™ program does not have to wait for the GPS string to arrive.

## Power Consumption

A total power consumption analysis was also done for the complete lab model. This included the power from the different sensors, the PC and the DAQ. The total power was calculated to be 510 Watts.

## Final Design

The final configuration of the Data Acquisition System is a large scale National Instruments system based on the prototype Lab model used for experimentation. The system was designed to measure and store voltage, current, and temperature data from the propulsion system batteries as well as the Uninterruptable Power Supply (UPS) batteries. This system requires over 800 channels of voltage and temperature measurements and 15 channels of current measurements. Extensive coding was completed using LabVIEW™ to acquire, display and manage the data which can easily be implemented to accommodate a large number of channels required by the Navy onboard the AESD. All sensors required for the large scale system have also been designed and tested in the lab for a complete and operable system. This includes a GPS system for time and location stamping with the battery data.

## Hardware

As mentioned above, the final hardware configuration is a large scale of the lab model designed to accommodate the data acquisition onboard the AESD. This system is a combination of SCXI Chassis' for the input modules and a PXI chassis for the control and power supply modules. The system will include 5 SCXI chassis' for the 52 input modules required to handle the large channel count. These chassis' will be connected in a star configuration to the PXI chassis which will contain all of the data acquisition cards for each SCXI chassis and a triple output power supply for sensor power and control. Included in this PXI Chassis is the MXI Express controller which is used to communicate and send data to the controlling PC. This whole system including the controlling PC and an external 250 GB hard drive can be mounted in a single 6 ft x 19 in rack onboard the AESD. All data sheets provided by National Instruments. System flow diagram and main components are shown below.

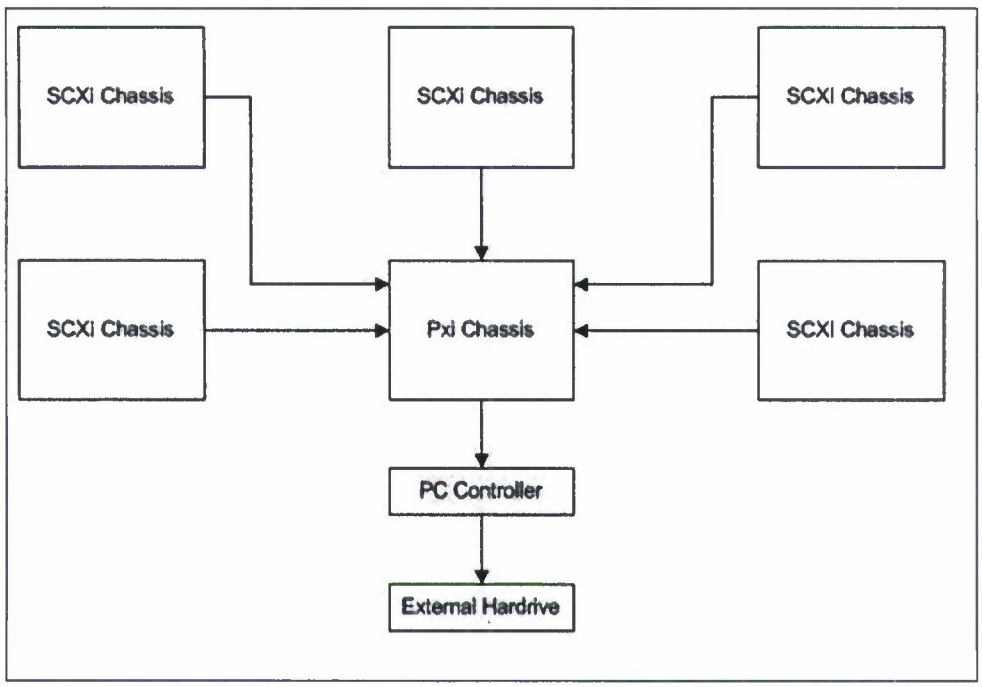



*Figure 58: Flow Diagram for Complete System*

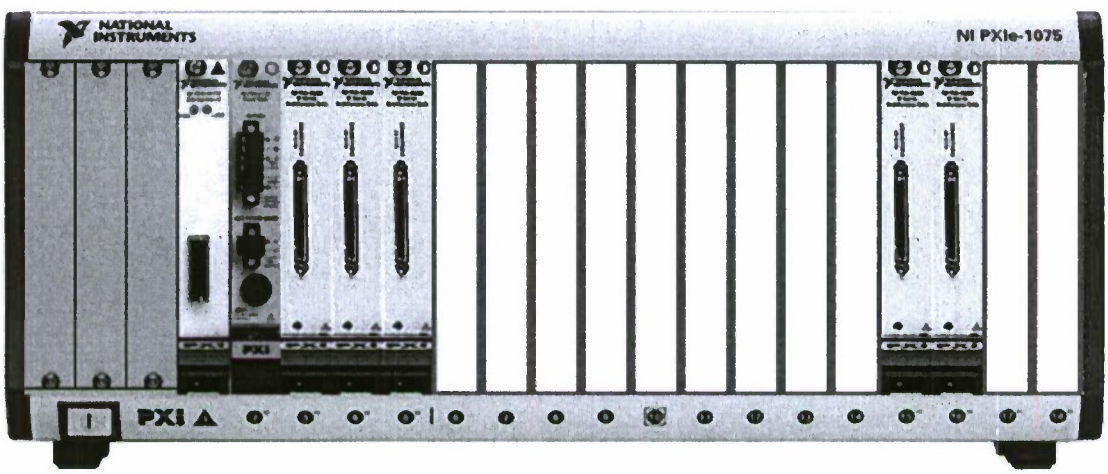



*Figure 59: National Instruments PXI Chassis*

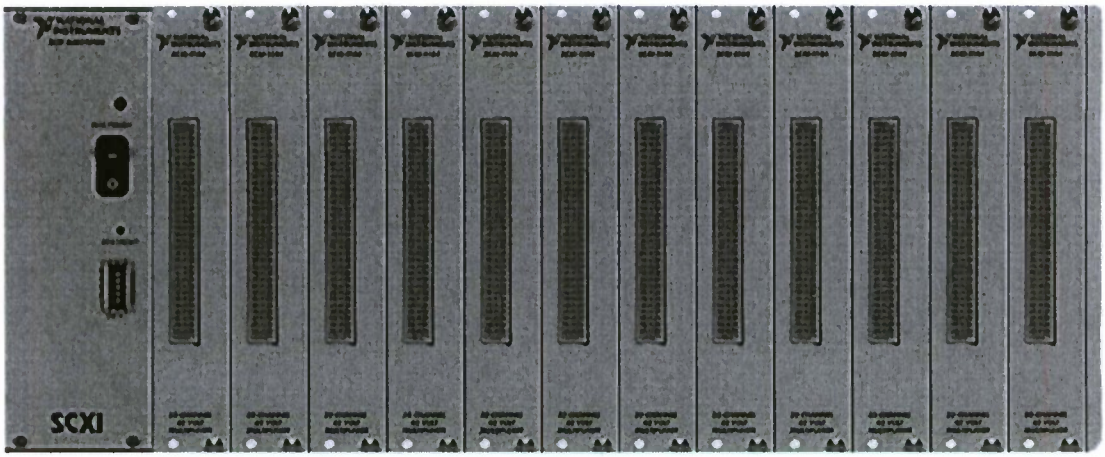



*Figure 60: National Instruments SCXI Chassis*

*Figure 61: National Instruments Rack Mount PC*

## Cost Analysis

| Part # | Item | Cost | QTY | Total Cost |
|---|---|---|---|---|
| SCXI-1001 | 12-Slot Chassis | $1,849.00 | 5 | $9,245.00 |
| SCXI-1346 | Multi-Chassis Adapter | $199.00 | 5 | $995.00 |
| SCXI-1361 | Real Filler Panel | $19.00 | 51 | $969.00 |
| SCXI-1102C | 32 Ch Thermocouple Card | $1,499.00 | 26 | $38,974.00 |
| SH68-68-EP | Multi-Chasses Connector Cable | $99.00 | 5 | $495.00 |
| SCXI-1303 | Thermocouple Connector Block | $329.00 | 26 | $8,554.00 |
| SCXI-1300 | Voltage Connector Block | $219.00 | 26 | $5,694.00 |
| SCXI-1104C | 32 Ch Voltage Card | $1,499.00 | 26 | $38,974.00 |
| PXIe-1062Q | 18-Slot Chassis | $6,199.00 | 1 | $6,199.00 |
| PXIe-PCIe8372 | MXI Express Terminal | $2,099.00 | 1 | $2,099.00 |
| NI 8353 | Rack Mount PC Controller | $5,098.00 | 1 | $5,098.00 |
| PXI-6251 | Data Acquisition Card | $1,199.00 | 5 | $5,995.00 |
| PXI-4130 | Triple Output Power Supply | $2,649.00 | 1 | $2,649.00 |
| SCB-68 | I/O Connector Block | $299.00 | 5 | $1,495.00 |
| 4N-25 | Optocoupler Voltage Sensor | $0.50 | 1030 | $515.00 |
| Type K | Thermocouple Wire (per ft) | $0.76 | 2000 | $1,520.00 |
| DK-20-C10 | Current Transducer | $417.25 | 15 | $6,258.75 |
| Software | LabVIEW™ | $4,699.00 | 1 | $4,699.00 |
| | | Total | | $140,427.75 |

The cost per channel of the recommended system is $87.17. This is a complete price included all the items mentioned above. If more channels are required to interface with this system, another SCXI chassis would be required along with the necessary input modules. The additional cost per channel was estimated to be $68 per channel for additional channels.

## POWER CONSUMPTION

As mentioned above in our system specifications, we had a power budget of 3000 Watts. We were able to design a complete system that would only use 1350 Watts. This includes all the National Instruments Hardware and the controlling PC, as well as all the power required by the sensors and the power that would be drawn from the batteries when measurements are being taken. This is a major accomplishment of our project, being that the power budget was very important and we were able to reduce it to less than 50%.

## Future Work

In this section, further work that can be done on the project is defined. There are different sections that can be worked on. Ideas to reduce power consumption and give more functionality to the system are given.

The sensors on the batteries draw a small amount of power but adding all of them up for the complete system will draw enough power that it would be more efficient to turn these sensors off when they are not being used. The complete system has a total of 768 batteries. To accomplish this, a power supply can be used which is being employed in powering the sensors up. The do this a power supply can be added to the system that would be needed anyway to power the sensors. If this power supply was connected to the system it could be turned on or off determined by the run button in LabVIEW™. This would be relatively easy to program in and then the only issue is how well the sensors respond to being powered on and off as far as calibration goes. This could be tested once the sensors have been fabricated and 1% resistors are used to get the most accurate results.

Another approach that can be used to reduce power consumption is to switch off the voltage inputs to the sensors when not in use. Without any power to the sensors, the input has resistance on them which gives rise to a current draw. If these inputs could be disconnected when they are not in use, then there would be no current draw on the batteries unless the data is being read. This can be done with an opto-relay that has a high isolation voltage rating. The input must be large enough to handle the common mode voltage that can reach up to 700 Volts. For the project, a package from Clare™ was researched but due to time restrictions, this feature was not added to the final design. This could be added easily to the sensors and once completed; a two layer board could be laid out for the parts to be soldered to. These sensors would have more functionality than the purchased sensors, can be integrated with LabVIEW™, and they are also much cheaper. The extra functionality would add to the cost of the sensor, but the safety of the NI equipment must be taken into consideration. Since this equipment is very expensive it would make sense to design safety features in to save the system from possible damage.

The Garmin GPS being used, outputs a sentence every second. The GPS onboard the ship might have different specification compared with the Garmin GPS being used. This is something that needs to be checked in order to integrate the project with the existing system on the ship. The data structure and how the data is sent on the Bayview ship is something to look at. The one that is used in the prototype is a standard one however it could be different aboard the ship. Right now LabVIEW™ is taking the data from a serial connection from the GPS on our prototype. This is not the only way to get the GPS time and location stamp into the data set.

In the final design, the temperature sensors (thermocouples) will be run into a thermocouple card in the DAQ chassis. This will allow for direct temperature readings from the sensors into LabVIEW™. It should be quite easy to set up the scaling in LabVIEW™ and read temperature. The temperature could be monitored so that if the temperature of the batteries went above a

certain threshold, a warning could be displayed. This would be helpful to those conducting the test so that equipment does not get damaged. This can also be done for voltages and currents. If the DAQ system reads that there is a problem and say the voltage is rising the system can be programmed to disconnect the voltage input from the batteries if a certain threshold is exceeded. Implementing this system into the AESD will also allow for real time monitoring of charging the batteries. The discharge is not the only thing that can be monitored. If the behavior of this large battery bank can be captured then means of improving the life and charging ability can be implemented. For charging there could be a completely new scheme developed such as a higher sampling rate to be able to see harmonic problems in LabVIEW™ using the same setup. Also the GPS data is not as important when the ship is not moving; therefore, the data can be taken without the GPS. This will save time and hopefully the resolution can be obtained without taking out sections of the battery bank inputs to the DAQ system.

We extended this subproject when a summer student expressed interest in data acquisition. In this case, we applied our expertise to building an automatic cycling unit for the batteries that both vehicles use. The unit had been started by a senior design project group. The summer student completed the project: he strongly solidified the hardware and developed a much more stable and reliable software. As a junior in electrical engineering, he then published his work at a leading conference in India. We should remember that Indian universities and industry are quite good at this subject. The standards for acceptance were quite high and me met them. His work is briefly described below:

We have created a novel design of an Automated Cycler Unit (ACU) for VRLA batteries. LabVIEW handles all the decision making for the system. It communicates with DAQ system to interact with the Switching panel (to switch between charging and discharging circuits), to control the Power Supply and monitor the voltage and current levels in the system. SOC accurately monitors the conditions of the battery. The system utilizes a novel approach for real-time SOC assessment and performs accordingly. Due to its versatile features like SOC based Charging, Dynamic Internal Impedance feature and Periodic Standby, the algorithm offers a configurable framework for the cycler. The data-logging block of the cycler records data as a spread-sheet and offers convenient post-operation analysis of the battery. This system is an up-gradation for a previous design synthesized for cycling batteries for Large Scale Vehicles.

## *Subproject c) Battery charger control for the LSV2 prototype submarine*

This project was initially funded as senior design project by ARD Bayview, so it is not directly funded by the DEPSCoR grant. The senior design project was completed in May 2009. An undergraduate student funded through this grant finished this project in the summer of 2010.

### 1. Introduction

VRLA (Valve Regulated Lead Acid) Batteries are Unique Low-maintenance rechargeable batteries. Their construction liberates them from the need of adding water continuously. These are also termed as Recombinant Batteries. This is because, the Oxygen evolved during the process at the positive plates, recombines largely with the Hydrogen at the negative plate, thus producing water and hence preventing any Water Loss.

## 2. Cycler Algorithm

The Main VI consists of a number of smaller VI(s) (or SUB VIs as they are referred to). The ACU typically performs the co-ordination of all these tasks in a desired manner as planned, while the SUB Vis perform their specific tasks. This will facilitate easy debugging for the Application in event of any faults. Also, if there are any desirable modifications or improvisations in the Charging or Discharging Algorithms, it could be done very easily without influencing the entire system. For an optimum performance, following method was chosen for the Battery to charge it optimally.

1. Charge the Battery at a Constant Current Rate at C/4 (50 Amps in this case) until the SOC reaches to around 80%.
2. Switch to Constant Voltage rate where the Battery will be maintained at a constant voltage depending on the Spec sheet, till the SOC rises to 115%)
3. Switch to "Trickle Charge Mode". Under these conditions, only the current required to supplement for self-discharging of the battery is supplied. This trickle takes place at a Constant current of C/600 to C/300 (330mA to 667mA approximately).
4. While discharging, the batteries should not be discharged to a SOC less than 50%. Observing that the State of Charge of the battery is extremely pivotal for an Optimum Battery life, SOC was chosen as the base parameter for all the switching and stepping in the Cycler.

### 2.1 Why State of Charge???

VRLA batteries should be always prevented from Overcharging or Undercharging. Overcharging (SOC > 115%) of these batteries is highly undesirable as it leads to production of more Hydrogen than which can combine with the O2. The Excess H2 then escapes through the valves, therefore practically; we spilled some of our electrolyte. Continued Gassing will lead to a lot of Electrolyte loss, and hence the batteries will not last long. Similarly, If the batteries are under-charged (SOC < 107%), all of the Lead Sulphate (PbSO4) is not utilized. Therefore, some of it remains on the Positive and negative plate, which eventually hardens to form a thicker layer. This depletes the electrolyte Specific gravity and the battery life degrades. Also, as the Battery accumulates charge, its capacity to accept more charge reduces. Continuously charging the battery with a High Magnitude Current will lead to Gassing of the battery, whereas using very low current will practically take FOREVER, for the battery to get fully charged.

### 2.2 State of Charge : Assessment

#### 2.2.1 Initial Research:

The State of Charge is defined as the available capacity expressed as a percentage of some reference, more likely its current. Hence, its current Ah content with reference to its total capacity is an indicator of its SOC. SOC cannot usually be determined directly. In general there are four methods to determine SOC indirectly:

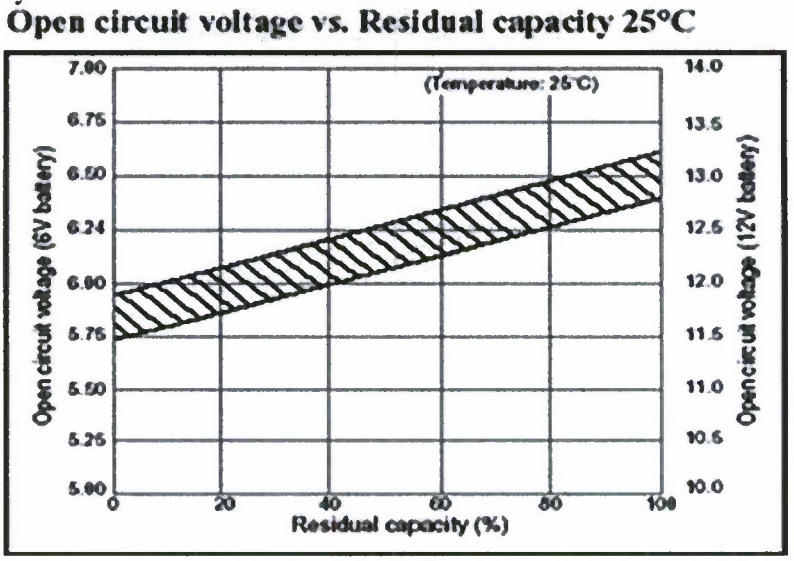
1. Specific Gravity Measurement :
2. Terminal Voltage
3. Coulomb Counting
4. Internal Impedance

### 2.2.2 Methods of Determining the State of Charge

Numerous methods can be employed to estimate the State of Charge of a battery. Some are specific to particular cell chemistries. However, most depend on measuring some convenient parameter which varies with the state of charge.

#### 2.2.2.1 Voltage Based SOC Estimation

This uses the voltage of the battery cell as the basis for calculating SOC or the remaining capacity. Results can vary widely depending on actual voltage level, temperature, discharge rate and the age of the cell and compensation for these factors must be provided to achieve a reasonable accuracy. The following graph shows the relationship between the Open Circuit Voltage and the Remaining Capacity at constant temperature and discharge rate for a high capacity Lead Acid cell. Note that the cell voltage diminishes in direct proportion to the remaining capacity.




Lead Acid Battery

#### 2.2.2.2 Direct Measurement

This would be easy if the battery could be discharged at a constant rate. The charge in a battery is equal to the current multiplied by the time for which it flowed. Unfortunately there are two problems with this. In all practical batteries, the discharge current is not constant but diminishes as the battery becomes discharged, usually in a non-linear way. Any measurement device must therefore be able to integrate current over time. Secondly, this method depends on discharging the battery to know how much charge it contained. In most applications except perhaps in qualification testing, the user (or the system) needs to know how much charge is in the cell without discharging it. It is not possible either to measure directly the effective charge in a battery by monitoring the actual charge put into it during charging. This is because of the Columbic efficiency of the battery. Losses in the battery during the charge - discharge cycle mean that the battery will deliver less charge during discharge than was put into it during charging.

#### 2.2.2.3 SOC from Specific Gravity (SG) Measurements

This is the customary way of determining the charge condition of lead acid batteries. It depends on measuring changes in the weight of the active chemicals. As the battery discharges the active electrolyte, sulphuric acid, is consumed and the concentration of the sulphuric acid in water is reduced. This in turn reduces the specific gravity of the solution in direct proportion to the state of charge. The actual SG of the electrolyte can therefore be used as an indication of the state of charge of the battery. This technique of determining the SOC is not normally suitable for other cell chemistries.

#### 2.2.2.4 Current Based SOC Estimation - (Coulomb Counting)

The energy contained in an electric charge is measured in Coulombs and is equal to the integral over time of the current which delivered the charge. The remaining capacity in a cell can be calculated by measuring the current entering (charging) or leaving (discharging) the cells and integrating (accumulating) this over time. In other words the charge transferred in or out of the cell is obtained by accumulating the current drain over time. The calibration reference point is a fully charged cell, not an empty cell, and the SOC is obtained by subtracting the net charge flow from the charge in a fully charged cell. This method, known as Coulomb counting, provides higher accuracy than most other SOC measurements since it measures the charge flow directly. However it still needs compensation to allow for the operating conditions as with the voltage based method. Three current sensing methods may be used.

- Current Shunt The simplest method of determining the current is by measuring the voltage drop across a low ohmic value, high precision, series, sense resistor between the battery and the load known as a current shunt. This method of measuring current causes a slight power loss in the current path and also heats up the battery and is inaccurate for low currents.
- Hall Effect transducers avoid this problem but they are more expensive. Unfortunately they cannot tolerate high currents and are susceptible to noise.
- GMR magneto-resistive sensors are even more expensive but they have higher sensitivity and provide a higher signal level. They also have better high temperature stability than Hall Effect devices.

Coulomb counting depends on the current flowing from the battery into external circuits and does not take account of self-discharge currents or the Columbic efficiency of the battery. In some applications such as automotive batteries, the "continuous" battery current is not monitored. Instead the current is sampled and the continuous current is reconstructed from the samples. In such cases the sampling rate must be fast enough to capture the current peaks and troughs associated with the acceleration and regenerative braking corresponding to the user's driving style.

#### 2.2.2.5 Internal Impedance

During the cell charge - discharge cycles the composition of the active chemicals in the cell changes as the chemicals are converted between the charged and discharged states and this will be reflected in changes to the cell impedance. Thus measurements of cell internal impedance can also be used to determine SOC however these are not widely used due to difficulties in measuring the impedance while the cell is active as well as difficulties in interpreting the data since the impedance is also temperature dependent. Fuzzy Logic and other similar models have been used to overcome these problems and ASICs have been developed for this purpose.

### 2.2.2.6 Other State of Charge Measures

This method depends on maintaining a constant driving pattern and major inaccuracies will be introduced if the driving pattern changes. It can also not be applied when intermittent charging is involved as with HEVs. While the measure may not be suitable as a basis for BMS in automotive use, it could still provide a verification check of the BMS model predictions for safety purposes.

### 3. The Preferred Algorithm

Terminal Voltage based SOC estimation was selected for the present application. The major advantages with this method was that (a). Terminal Voltage was always precisely available from the DAQ. Therefore, calculating SOC would be easily possible in real time or during post-process analysis. (b). The Trend of SOC with respect to Terminal Voltage was linear. Therefore, by precise calculation of Terminal Voltage vs. SOC at any two points, SOC could suitably be estimated at other points on the graph, with suitable accuracy.

### 3.1 Associated Problems

The above algorithm was fairly accurate for OCV vs. SOC estimation. Open Terminal Circuit Voltage has been defined as the Terminal Voltage across the battery under Open Circuit conditions after it has rested for approximately 4-5 hours. This is an extremely accurate measure for SOC. However, the motive here was to assess the SOC in real-time, i.e. when it was undergoing charging/discharging. Leaving the battery on a standby for even one hour was definitely not practical.

### 1. Differences in the OCV and Terminal Voltage:

The Battery Voltage or the OCV, expectedly, is lower than the previously measured Terminal Voltages (in case of Charging Cycles) and higher (in case of Discharging Cycles) as follows from the Kirchhoff's Voltage Law.

During Charging,
Vbattery = VTerminal – IString*RBattery (since Battery is acting as the LOAD)

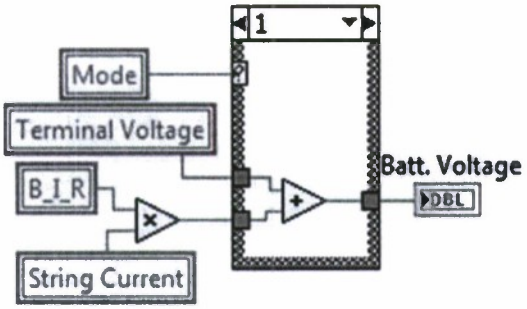
During Discharging,
Vbattery = VTerminal + IString*RBattery (since Battery is acting as the Source)

### 2. Dynamic Internal Impedance:

Battery's internal Impedance has a standard value provided by the manufacturer. However, while charging or discharging, there are a lot of chemical reactions involved inside. Depending on the acid concentration, present state of charge and the current flowing through its terminals, the Internal Impedance of the battery exhibits a dynamic nature. It can be said that IR of the battery is slightly different under Load and No-Load conditions. Therefore, the offset from the OCV is also dynamic.

### 3.2 Solution Adopted

1. As for the first associated problem, the system can incorporate an offset value at all times, calculated using the Measured String Current and Internal Impedance (DIR) of the Battery. This will reduce the deviation to a considerable extent.




2. Periodic Stand-By Mode will be used. This involves switching the battery to Open Circuit conditions every 30 minutes, for a period of 3 minutes. This has a lot of benefits which have been explained in greater detail in the final report.

3. During Periodic Stand-by Mode, DIR is calculated to update the current value. These measures reduce the offset from the actual OCV value considerably. Moreover, since the algorithm is not very rigid about the value of SOC, a slight deviation from the actual calculated value (2-7%) hardly is of any significance. In fact, the system has been designed to ignore slight dip in SOC at the critical SOC values, where transitions between Charging/Discharging Steps occur.

## *Subproject d): Analysis and design of a fast fault detection scheme for medium voltage direct current power systems,*

This project will be performed by a part-time Master of Science student working for a local power engineering consulting firm. He also has prior experience as an instructor for the Navy in Charleston South Carolina. Project scope has been defined in consultation with Nathan Spivey of NSWCCD Philadelphia. Work will continue on this project in the coming year.

The introduction to the thesis is included below.

### *1.1 Introduction*

The United States Navy is exploring medium-voltage direct current (MVDC) as an option for future shipboard electrical distribution systems. Perceived advantages of MVDC distribution over AC include converter optimized AC generators, smaller transformers, reduced cable weight, improved acoustics, and rapid detection and control of fault currents [1]. Timing of fault detection and fault clearing in AC systems is limited to about 1 cycle of a 60 Hz waveform, constrained by the ability of protection systems to recognize fault conditions in an already time varying signal. The United States Navy is considering use of MVDC to reduce fault detection and mitigation time to less than 5 μs [2]. The purpose of this thesis project is to evaluate the feasibility of using existing MVDC technology to achieve such a rapid DC fault detection and response without sacrificing security for demanding operating conditions. The study included simulation using the Real Time Digital Simulator (RTDS®) platform at the University of Idaho's power research laboratory [3]. Voltage source converter (VSC) technology was selected for AC

to DC conversion due to its ability to provide rapid and independent control of real and reactive power while maintaining unidirectional voltage polarity, all of which are desirable for a reconfigurable distribution system.
The next two sections provide information about the system topology and simulation platform. VSC design and DC-side protection schemes are covered in Chapter 2. The third chapter contains simulation results for steady-state and transient operating conditions with single and dual VSC topologies. Normally, multiple converters would be required for redundancy and operational flexibility. However, the single converter case is a useful simplification and is representative of a situation following loss of the redundant converter(s). A shipboard MVDC system can have more than two source converter terminals, but a dual VSC bi-directional power flow system was sufficient for this study. Simulator optimization also imposed restrictions on the number of converters that could be modeled in detail.
Chapter 4 presents analysis and simulation results for DC bus faults and fault recovery. Conclusions and a summary of future work are included in Chapter 5.

### *1.2 System Topology*

The U.S. Navy is exploring an all-electric ship with integrated propulsion as an option to meet the operational and fiscal requirements of the future naval fleet. Figure 1 is a high level illustration of the basic electric plant for the all-electric ship as described in the Navy's Next Generation Integrated Power System (NGIPS) roadmap [1]. Power conversion modules (PCM) convert AC power from the generators to DC which is distributed through the ship over cables between power distribution modules (PDM). The PDMs consist of switchgear and controls for routing and interrupting flow of power in the MVDC network. Loads (not shown) are served from the PDMs.

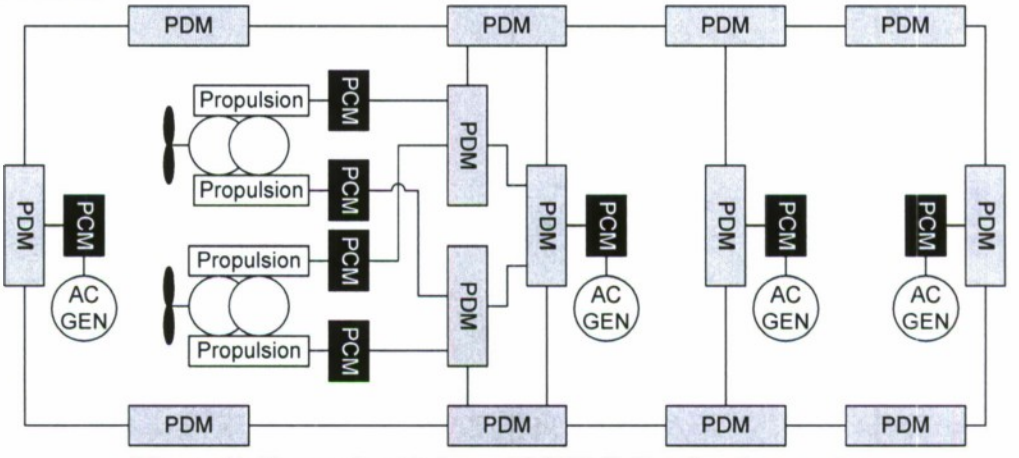



**Figure 5: Example shipboard MVDC distribution system**

Because of simulator limitations, the topology was simplified for this study to that shown in Figure 2. Here, the PDMs are DC circuit breakers, PCMs are the voltage source converters and loads are actively controlled DC loads. Despite the simplification, the model retains essential characteristics necessary for productive fault study. These characteristics include 1) detailed modeling of VSC passive and active components with associated controls, 2) control interaction between more than one VSC terminal, and 3) multiple protection zones for study of fault detection and response. Both pole-to-pole and pole-to-ground loads were considered. The

dashed box in Figure 2 shows the portions considered in the study cases with a single converter terminal.

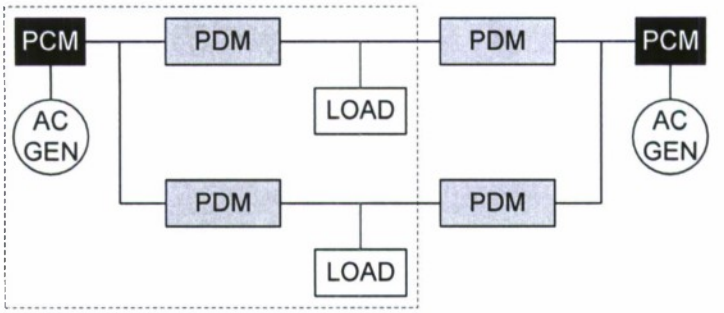



**Figure 6: Simplified MVDC network for simulation**

### *1.3 Simulation Platform*

A number of platforms were considered for simulating the shipboard MVDC system. Among these were the Alternative Transients Program (ATP-EMTP), PSCAD/EMTDC®, and RTDS®. The RTDS was chosen because it provided the fastest means of development, troubleshooting, and production of results. Also, its real-time capability helps improve understanding of system behavior by allowing users to directly interface with the continuously operating model. ATP-EMTP was used as necessary for verification of RTDS results. This section provides basic information about the RTDS including limitations imposed by real-time simulation.

The RTDS is a digital electromagnetic transient simulator capable of solving power system and control networks in real-time [3]. In other words, it can solve power system equations fast enough to generate and continuously update voltages, currents, and control signals with accurate timing. Such real-time simulation used to require a transient network analyzer. The RTDS includes input/output modules for closed loop control studies involving interface with external equipment such as protective relays. Interface with external equipment was not used in this thesis project. User interface with the RTDS is via a software package called RSCAD which contains an extensive library of power system and control components. RSCAD also has a module called Runtime in which users develop control panels for interacting with the model being solved in real-time.

The RTDS performs calculations on RISC based processors which have deterministic processing intervals. Normal power system networks and their controls are solved by the RTDS with a 50 μs time step. However, VSC simulation requires better time resolution for stable and accurate network solutions due to high frequency pulse width modulation (PWM) and switching of semiconductor valves. To support this, RTDS developed small time-step VSC subnetworks which solve VSC components with time-steps between about 2-4 μs. The small time-step solutions can be interfaced with the large time-step network. The interface between a small time-step subnetwork and the large time step system requires use of a special interface transformer. Additionally, an interface between separate small time-step subnetworks requires a special cable component. Both these interface components are based on a travelling wave model of a transmission line. A minimum travel time of one large time-step governs the inductive and capacitive properties of the components. However, cable distances on shipboard distribution systems are relatively small and unrealistically large travel times could interfere with performance of multi-terminal VSC control simulation. Therefore, the entire model was implemented in a single small-time step subnetwork. RSCAD allows the user to view a

processor map which shows the time intervals required to solve each model component. An example is included in Appendix A. The map illustrates a tradeoff between the number and complexity of components and the ability of the RTDS to perform calculations in real-time. If too many components are used, the processing burden can be too much for a real-time solution. Limiting the number of detailed VSC bridge circuits in this study to 2 ensured that solution time-steps remained below the recommended 4 μs.

Processing of the the electrical network solution, PWM triangle wave, and IGBT gating signals is performed by the RTDS with the small time-step. However, the controls processor is still limited to 50 μs. Voltages and currents from the small time-step solution are sampled once each large time-step for use by the controls processor. This imposes some inaccuracy, but early investigations showed that RTDS performance was sufficient for the electrical system and control time constants expected. The limitations on processing speed added an additional element of realism since sampling rates for protection equipment can be a significant factor in the speed of response.

Semiconductor valves such as insulated gate bipolar transistors (IGBTs) are modeled in the RTDS as quasi-ideal switches having a small on-resistance and a large off-resistance. The model includes snubber series capacitance and resistance. Where important, information about RTDS modeling of other components is discussed in context in the report.

The goal of this thesis project was to evaluate the feasibility of achieving MVDC fault detection and response times within 5 μs. The feasibility analysis accounted for protection limitations imposed by operational transients. The study included development of mathematical models of the VSC controls and the passive fault response. Methods for speeding up fault detection and control response were evaluated and tradeoffs identified. RTDS simulations verified the models and provided means of performing sensitivity studies and identifying operational constraints on protection settings. The general conclusion from these studies is that a 5 μs response time is not likely to be feasible for the VSC system and protection schemes analyzed. Limiting factors are primarily the tradeoffs associated with switching frequencies and passive elements such as the AC-side inductors, DC-side shunt capacitors, and DC-side cable inductance. Figure 83 summarizes the data obtained via simulation and analytical methods.

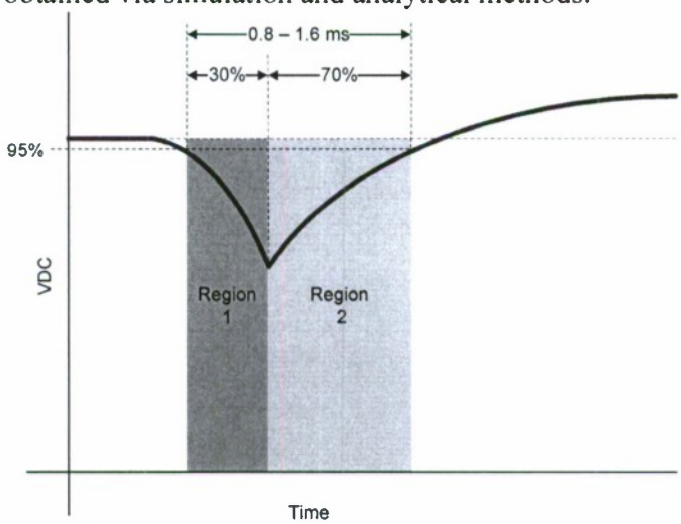



**Figure 7: DC fault response summary**

The total time the DC bus voltage dropped below 95% varied between about 0.8 and 1.6 ms. Region 1, from fault inception up to breaker operation, accounts for about 30% of this time and the remaining time is due to control response in Region 2. Tables 6 and 7 summarize the factors causing delay in these two regions. Means for improving the delay and tradeoffs are also listed.

**Table 2: Region 1 – fault detection and clearing delay considerations**

| Cause of Delay | Means for Reducing Delay | Tradeoff/Limitation |
|---|---|---|
| Desensitization of protection settings due to operational transients | Use current differential protection and/or install distributed voltage measurements as practical to reduce inductance between possible points of fault and voltage measurement locations | Complicates and adds cost to protection scheme |
| Non-instantaneous decay of DC bus voltage due to VSC shunt capacitance, cable inductance, and cable resistance | Minimize cable lengths and reduce the VSC shunt capacitor | Cable sizes will be driven by ampacity and ship layout. Reducing the size of the shunt capacitor results in an increased voltage ripple on the DC bus. |
| Sampling rate of protective equipment | Significant advance in protective device processing speeds | Time and research and development cost. Little need for this in commercial systems. |

**Table 3: Region 2 – recovery delay considerations**

| Factor | Means for Reducing Delay | Tradeoff/Limitation |
|---|---|---|
| Control system time constants limited by switching frequency | Increase the switching frequency | Increased switching losses and more complicated controls |

Even though the study indicates that a 5 μs DC fault detection and response time is unlikely for the VSC system studied, the results also show that such a rapid response may not be necessary for satisfactory performance. If fault duration can be limited to about 100 μs, the impact on the DC bus voltage was shown to be minimal. Additionally, performance could be managed by designing loads to handle voltage excursions like those in simulated results.

## *Subproject e) Evaluation and development of fault detection and prioritized tripped scheme simultaneous phase to ground faults in ungrounded and high resistance grounded medium voltage ac power distribution systems.*

Many existing shipboard power systems are ungrounded or high resistance grounded systems. Cables are used to connect the power apparatus. System that is ungrounded has some inherent advantages. Eighty percent and above of the faults in power systems are single line to ground fault. However, in ungrounded systems, the system can operate intact as long as the loads are connected line to line. The phase to phase and phase to ground capacitance, and the high grounding impedance determine the magnitude of the fault current, which is small and in the range of milliamps to several amps. Because of this limited ground fault current, ungrounded systems have well-known advantages such as low thermal stress, better personnel safety and more reliable load service [1]. Figure 1 shows a typical ungrounded distribution feeder. Moreover, as the impedance of the cables used on ships are relatively small, it is hard to implement distance protection elements.

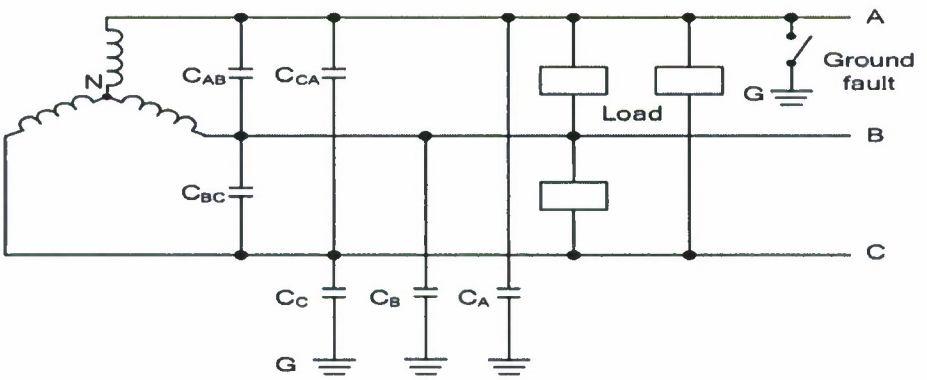



Fig.1. Ungrounded power system

Because the line to line voltages is intact and the loads can still work after the first single line to ground fault happens, generally we do not want the relay to trip but to give some warning signal. Figure 2 shows how the voltages will change before and after the fault in an ungrounded system.

However, for the unfaulted phases, we will see overvoltage on them [1]. Under certain conditions, we might see abnormal overvoltage also [2]. Thus, it is quite possible that another line to ground fault caused by insulation failure will happen if the first fault have not been cleared yet. These will effectively combine to cause a double line to ground fault and large amount of fault current will flow in the system. Under these circumstances, the line differential current elements of the relays will assert and trip the breakers.

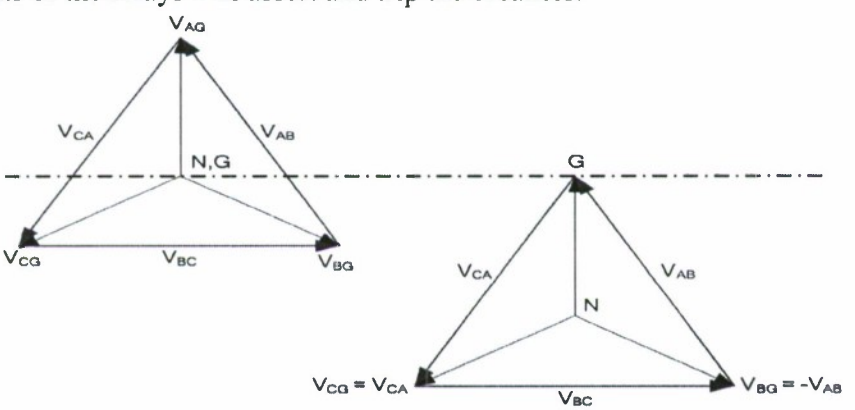



Fig.2. Voltage relationship before and after a ground fault in an ungrounded system

Dusang developed a technique to trip only one of the faulted lines, allowing critical loads to remain online and minimizing breaker trips [3]. He performed the Mathcad simulation of the protection scheme. In this paper, the protection scheme is improved to be comprehensive to all kinds of possible situations. The protection algorithm implementing the improved scheme is implemented in RSCAD environment and the hardware in the loop test is done utilizing existing SEL 311 relays..

## Protection scheme

The protection scheme introduced here capitalizes on the current differential and ground differential elements of the relays, namely, SEL 311 relays, to detect the location of the simultaneous faults and selectively isolate one of them, continuing providing power to crucial loads. Figure 3 shows a notional shipboard power system schematic representation.

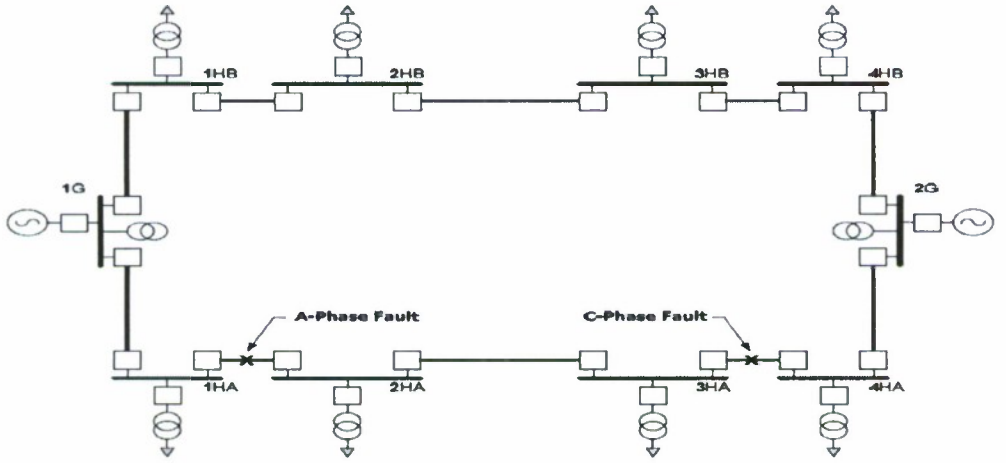



Fig. 3. A notional shipboard power system schematic representation

As said before, the first single line to ground fault on phase A will not affect the running of the power system and we do not want to trip the breakers. However, we do send an alarm to announce the fault and allow for graceful shutdown. It is the same if a C to ground fault happens on its own. But if the C phase fault happens when the A phase fault is not cleared, effectively a line-line to ground fault forms and the relays associated with the cable between 1HA and 2HA and the cable between 3HA and 4HA will trip because of the large fault current. As a consequence, the transformers on Bus 2HA and 3HA will lose power. Same thing happen if we have a single phase to ground fault happening on line 1 and another line to line fault happens on line 2. Based on where we have the simultaneous faults, a larger area may lose power and islanding may also be evolved.

However, if we establish communication among the relays, we can make a decision based on information from a wider area and minimize the number of trips, remaining the crucial loads online. Figure 4 shows the flowchart of the proposed protection scheme.

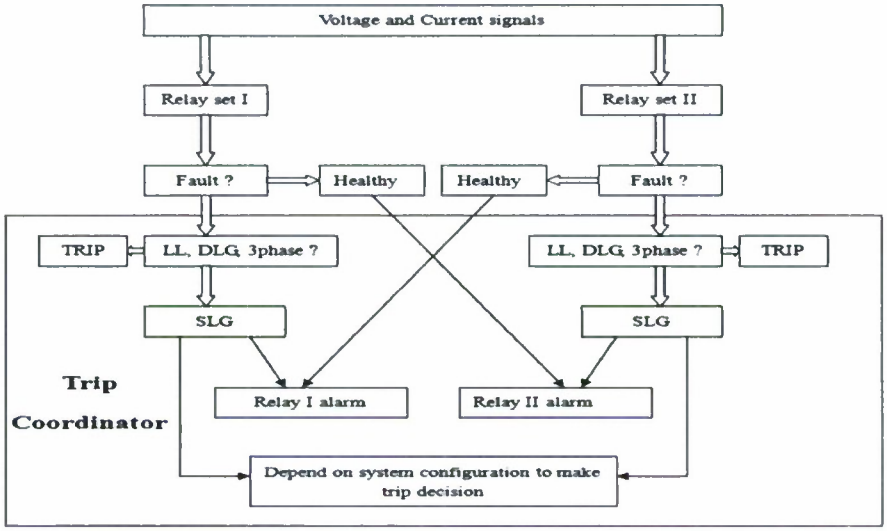



Fig. 4. Flowchart of the integrated protection scheme

Based on wide area data, we are able to make a decision that can minimize the number of trips and also from the point of view of overall system stability requirement. However, communication latencies among the relays are ignored here.

## Hardware in the loop test

A simple study system was constructed to do the hardware in the loop test here. There is a solidly grounded generator and two high resistance grounded transformers. The line models are built based on the real cables that are used in shipboard power systems (model of the cable). The faults can happen in multiple locations. For each fault can be single line to ground fault, line to line fault, double line to ground fault or three phase fault. There is one set of relays on each of the line. A one-line diagram of the system drawn using the ATPDraw graphical user interface for ATP is shown in Fig. 5.

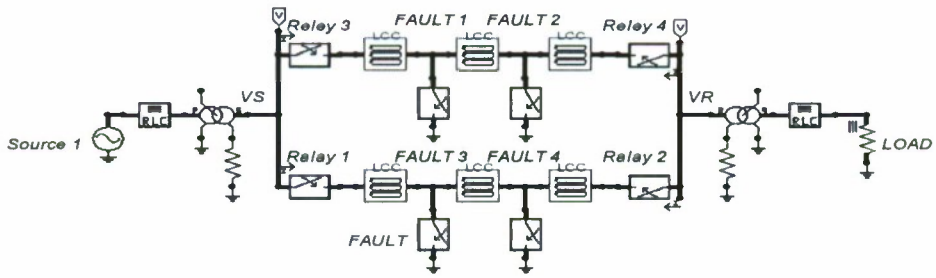



Fig. 5. A notional shipboard power system being tested on

The line voltage and current signal data is sent to the low voltage test interface of the relays. Utilizing local information, the relays will make fault decisions and send the fault decisions back to the RTDS. The trip coordinator executing the proposed protection algorithm will use the output signals from the two sets of relays and make the final decision and trip the desired breakers in the power system. The simulations will continue running with the breakers in their new states. Figure 4 shows the infrastructure of how the simulated power system, the trip

coordinator, the two sets of hardware relays and the RTDS are related to each other. The idea here is to use hardware relays to utilize local information and detect fault location and send the information to the trip coordinator and process the large area information,

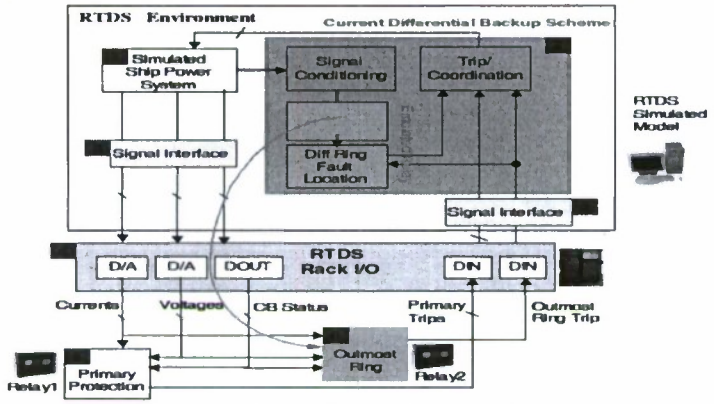



Fig. 6. Hardware in the loop test layout

Figure 7 shows the how the RTDS and the hardware are actually interfaced with each other.

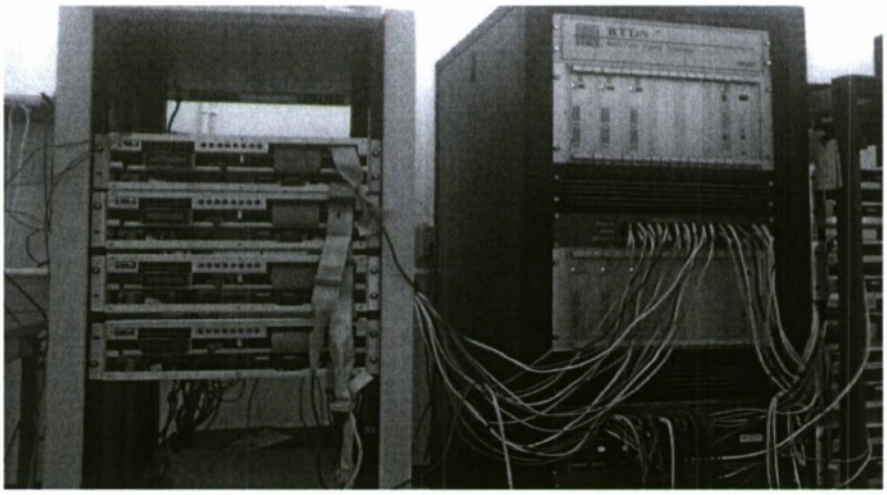


Fig. 7. Picture of apparatus of the hardware in the loop test(Notations need to be added)

## Hardware implementation

After doing hardware in the loop test and confirming that this protection scheme is effective in protecting crucial loads and minimizing the number of trips, the algorithm is implemented with hardwares. Figure 8 shows the layout of the apparatus. However, current and voltage signals still come out from the RTDS.

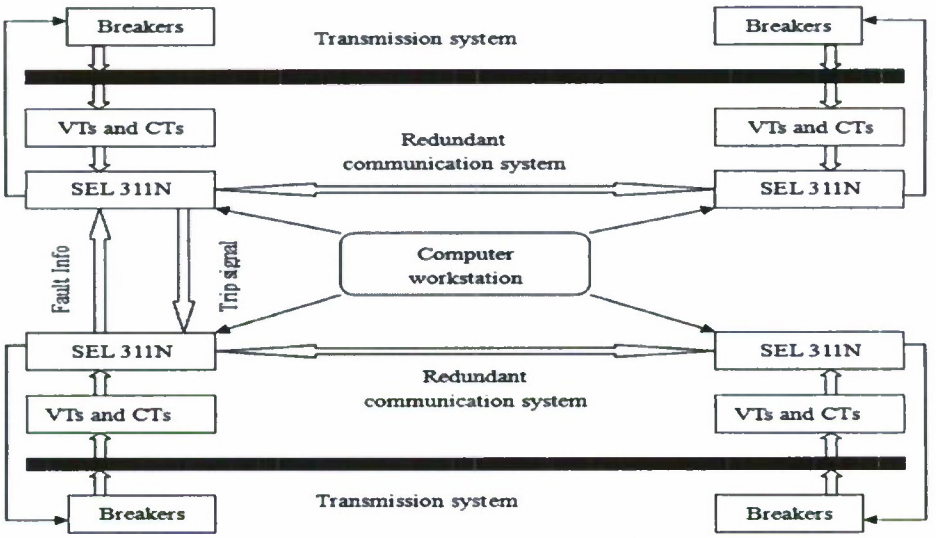



Fig. 8. Layout of the hardware implementation

Figure 9 shows the hardware implementation of the proposed integrated protection scheme. The voltage source here is used to help transmit the fault information among the relays.

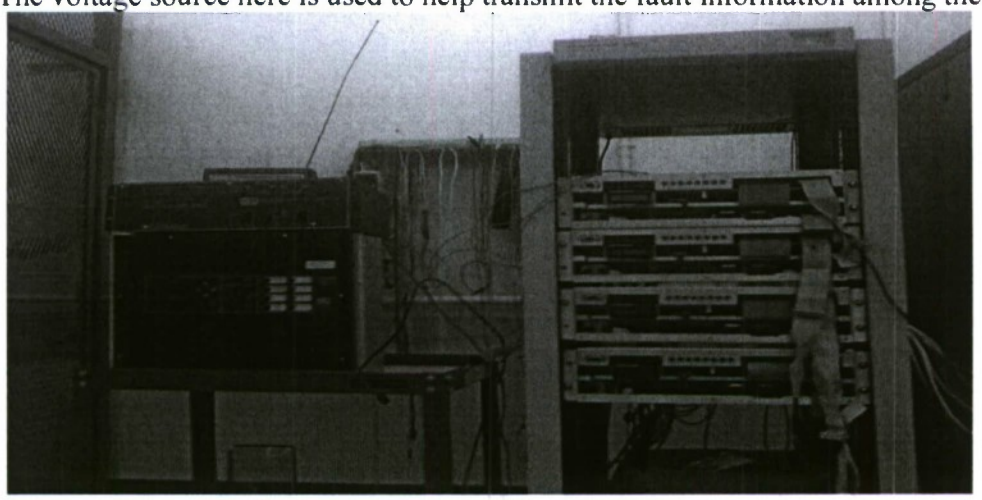


Fig. 9. Picture of the hardware implementation

## Test results and comparison

A set of tests has been done to test the effectiveness of this integrated protection scheme in a hardware in the loop manner. The same battery of test was also done to test the hardware implementation.

1. SLG fault at location 1

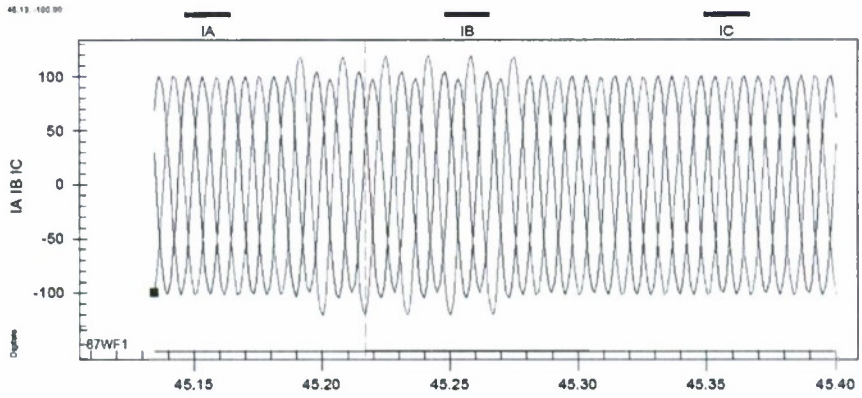


Fig. 10. Hardware relay performance for a SLG fault

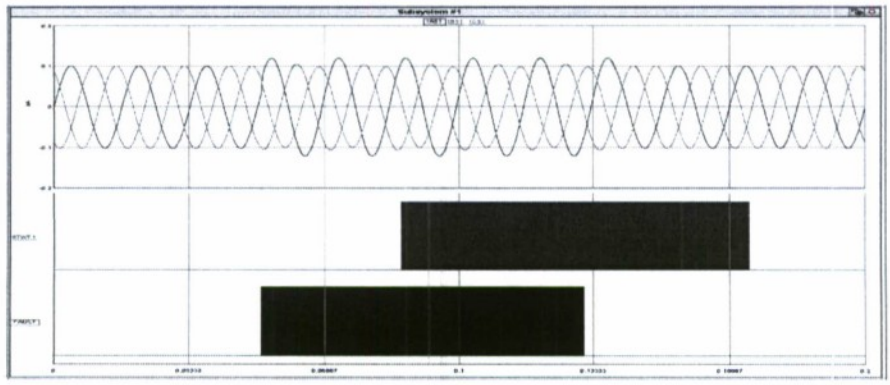


Fig. 11. RTDS performance for a SLG fault

As we can see here, after the single line to ground fault is initiated, there was small amount of fault current flowing in the system. And there are be overvoltages on the two unfaulted phases all over the system, which makes fault detection pretty hard. To find out where the fault is, the line crews need to open circuit the power system section by section until the zero sequence voltage is gone. The set of relays used here utilize core flux summing CTs to get the actual residual current and detect the ground fault. Because the magnitude of the fault current is pretty small, the resolution of A/D converter is higher than the converters for phase currents. And this is also the reason why the relays do not use the phase currents to compute the residual current in this kind of application. In this way, we can know exactly which is the faulted line.

After the single line to ground fault happens, it takes the relay less than two cycles to detect the fault and send out the warn signal saying there is a line to ground fault on line 1. Due to the fact that the output contacts of the relay need some time to operate and the RTDS digital input module needs time to detect the status change of the outputs contacts, the RTDS takes more than two cycles to get the warning signal.

2. DLG fault at location 3

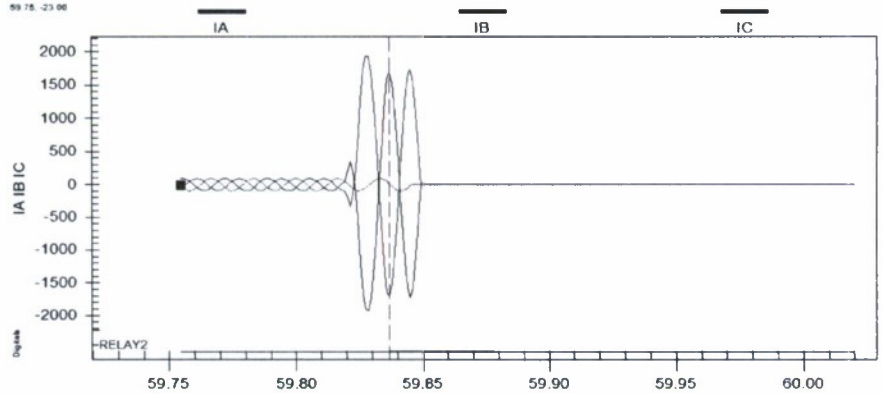



Fig. 12. Hardware relay performance for LL fault

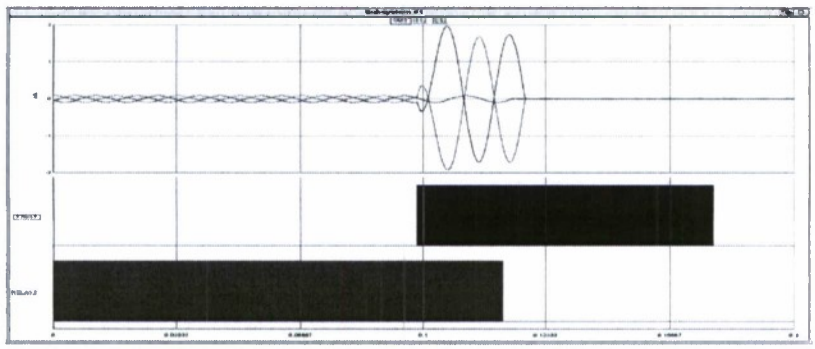


Fig. 13. RTDS performance for LL fault

According to the protection algorithm, if there is a line to line fault on any of the line, the corresponding relay will trip the line. The relay takes about one cycle to detect the fault and the breakers open at natural current zero. The breakers were set to be closed at one and open at zero. This is why we got the RTDS performance as above.

3. First SLG fault (phase A) at location 1, second SLG (phase B) fault at location 3

If we have a fault at location 1, and 0.02 second later, another fault happens at location 3, the following graphs give the corresponding performance of the proposed algorithm.

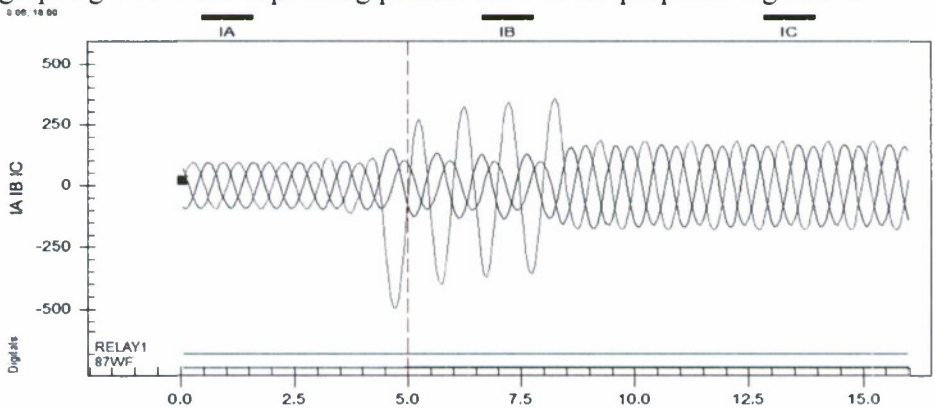



Fig. 14. Hardware relay performance for simultaneous fault (Relay set 1)

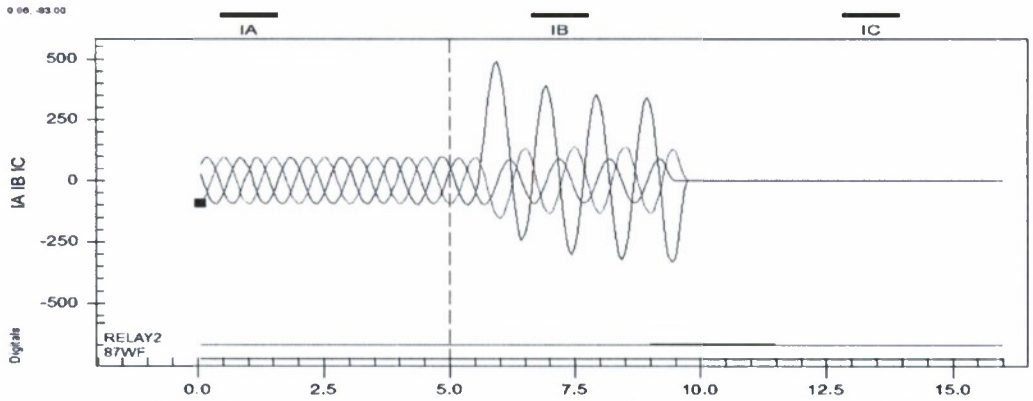


Fig. 15. Hardware relay performance for simultaneous fault (Relay set 2)

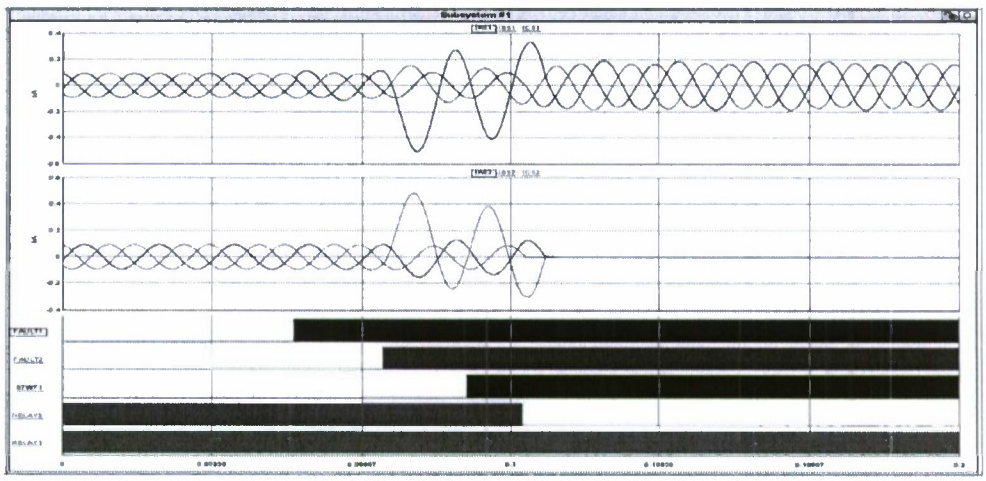


Fig. 16. RTDS performance for simutaneous fault

We can see here that the proposed algorithm works as proposed and protects crucial loads effectively. The power is continuously supplied to the loads after the faults happen. After the second fault is cleared, the warming signal is still on. This provides us some time to find out where the fault is and clear the fault before another fault happens.

The time consuming difference between hardware in the loop test and the hardware implementation is about 2 cycles. The reason is that the RTDS takes really short time to process the fault information from the local relays (in the order of micro seconds). However, the actual hardware implementation utilizes output and input contacts to transmit the trip signal, which is a lot slower.

If we do not have coordination among the relays, we can see the corresponding relay response is as follows:

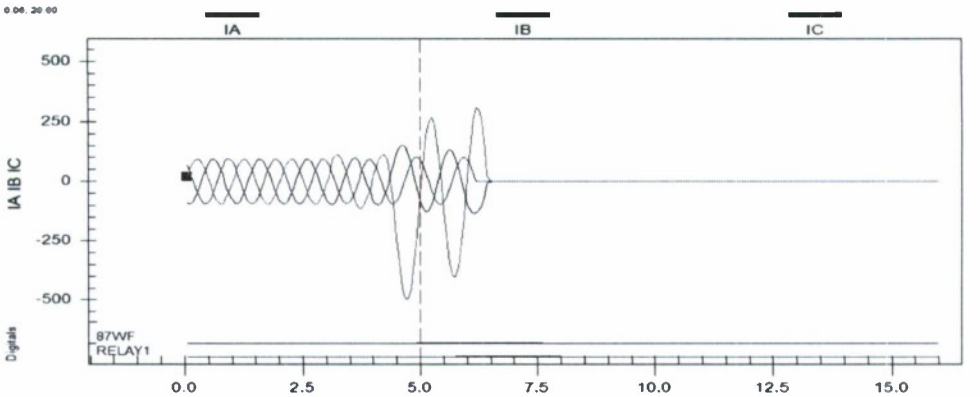



Fig. 17. Relay 1 response to simultaneous fault without communication among the relays (SLG on Line1 and SLG on Line2)

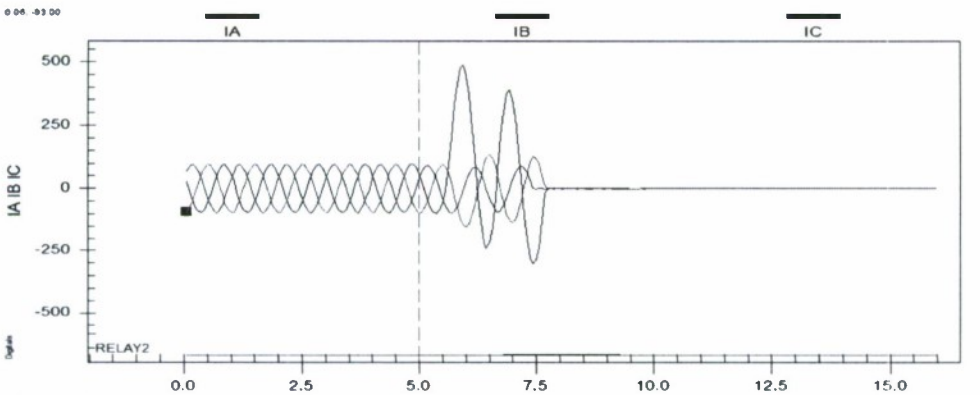



Fig. 18. Relay 2 response to simultaneous fault without communication among the relays(SLG on Line1 and SLG on Line2)

The line differential elements of the relays will pick up the fault and open the breakers on both of the lines. Therefore, the crucial loads will be out of power, which will expose the submarines and ships under extreme danger. This is especially a problem for the next generation all-electric ships.

4. First SLG (phase A) fault at location 2, second DLG (phase B&C) fault at location 4

If we have a fault (phase A to ground) at location 1, and 0.02 second later, another fault (phases B and C to ground) happens at location 3, the following graphs give the corresponding performance of the proposed algorithm.

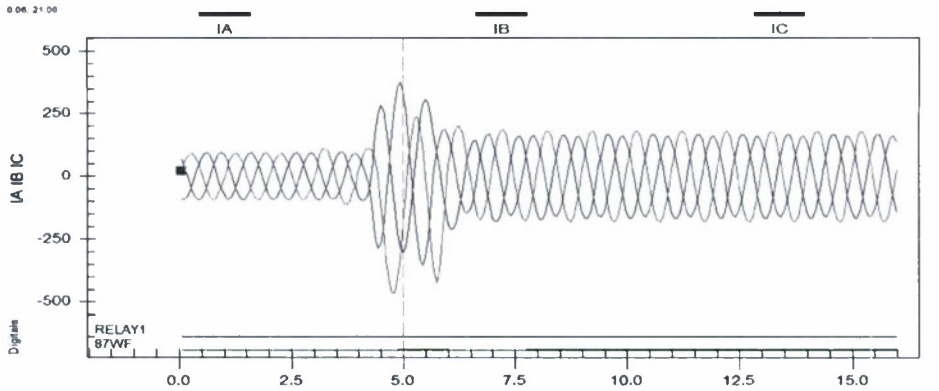



Fig. 19. Relay 1 response to simultaneous fault with communication among the relays (SLG on Line1 and DLG on Line2)

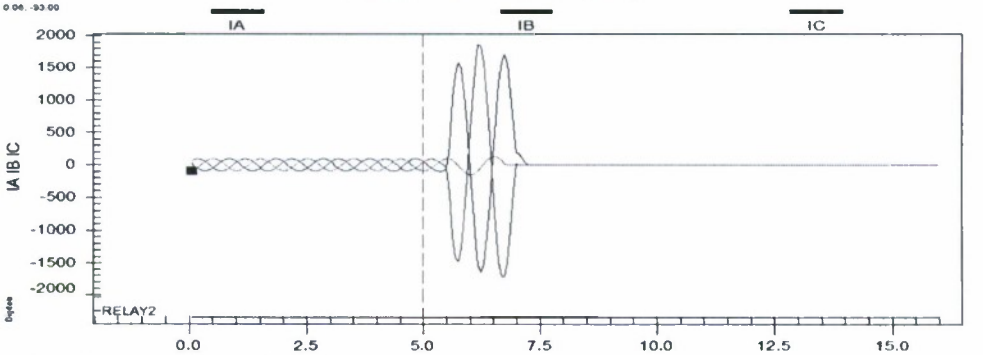



Fig. 20. Relay 2 response to simultaneous fault with communication among the relays (SLG on Line1 and DLG on Line2)

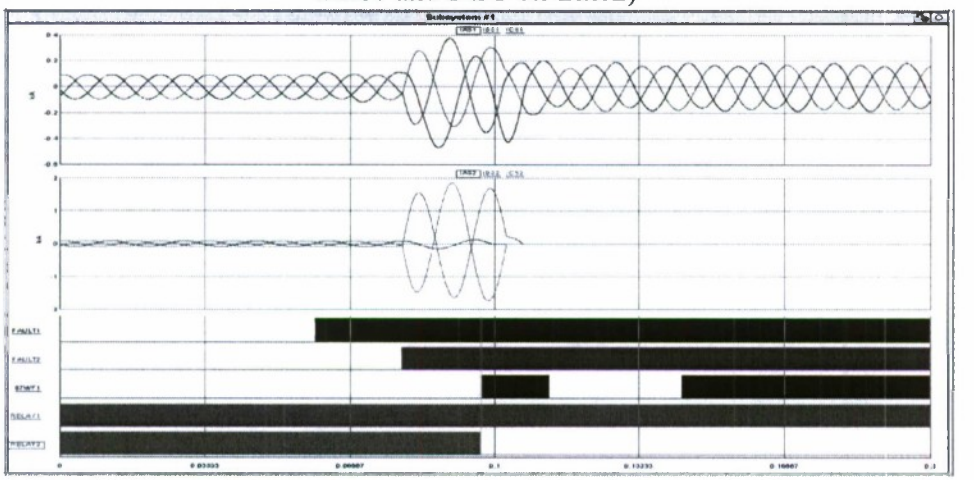


Fig. 21. RTDS performance for simultaneous fault (SLG on Line1 and DLG on Line2)

The proposed algorithm cleared the double line to ground fault and continuously supplies power to the crucial loads. The ground differential element de-asserts for a short period of time and then asserts again after the second fault is cleared, warning that there is still a ground fault on line 1.

The following graphs show what happens in this situation if we do not have communication among the relays.

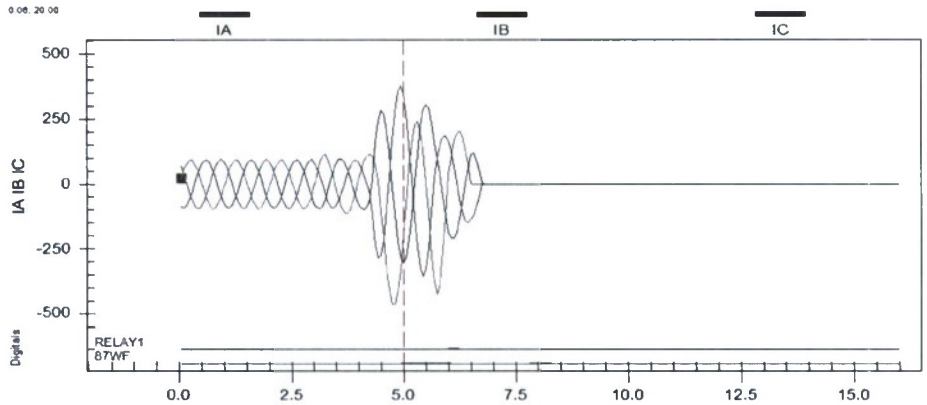


Fig. 22. Relay 1 response to simultaneous fault without communication among the relays (SLG on Line1 and DLG on Line2)

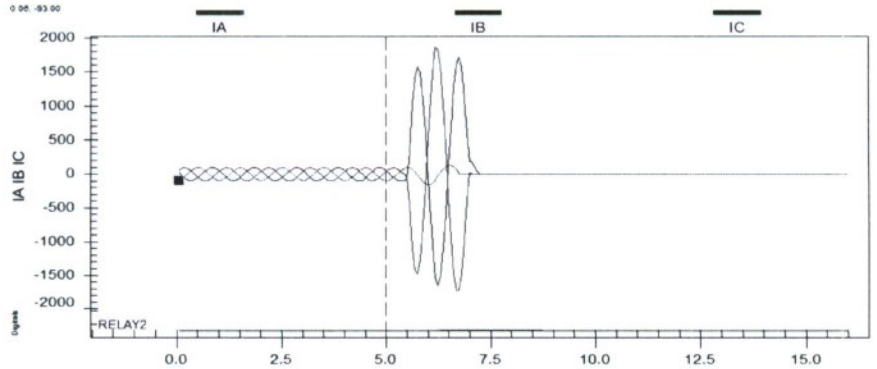


Fig. 23. Relay 2 response to simultaneous fault without communication among the relays (SLG on Line1 and DLG on Line2)

As what happened in case 3, both lines will trip and the loads will be out of power.

## *Subproject f) Develop model of AESD electrical system in RTDS*

This is a MS thesis project that started in January 2010. The graduate student developed a model of permanent magnet synchronous machine and associated drive system. The manufacturer of this same system in AESD was not willing to provide sufficient data to validate the model. A description of the PSCAD/EMTDC model is given below. As an alternative, the student then developed a model of an induction generator that would be appropriate to replace the AESD's synchronous machine model. The student presented his work in a conference paper in May 2011. The final thesis was published in August 2011. A synopsis of this thesis is given below.

This thesis has provided an approach to modeling the VSD and attached PMSM for a large electric vehicle with limited information given on the VSD and PMSM. Additionally details regarding the development of a modified VBR model of an induction machine and a field oriented controller compatible with this topology have been presented. Due to technical limitations encountered during modeling in the RSCAD/RTDS environment concessions had to be made during modeling and these and the reasons behind them are detailed by this thesis. With

completion of the research for this thesis the sponsor has a RSCAD/RTDS and PSCAD/EMTDC model capable of modeling the full inverter with basic control as requested; additionally the sponsor has the ability to use the induction machine model in PSCAD/EMTDC to determine how an induction machine would operate in place of their current PMSM.

RSCAD/RTDS has proven challenging but ultimately rewarding to work with. For modeling traditional power system situations that mostly involve frequencies around 50 to 60Hz and single digit multiples thereof, RSCAD/RTDS provides an excellent simulation option. Operations can be carried out in real-time without the need to carry out multiple lengthy simulations to determine response to parameter changes. However for simulation involving high frequencies (>10 kHz) or requiring custom small time-step module components RSCAD/RTDS provides significant drawbacks, from distortion of signals, to steep requirements on custom user content. It is the author's opinion that the sponsor should continue to rely on traditional electromagnetic transient programs to simulate this system until the RSCAD/RTDS small time-step VSC module offers better support for custom components and higher frequencies, and less dependence on large-time step signals for VSC module operation.

While the PSCAD/EMTDC model was originally only a stepping stone to modeling on the RSCAD/RTDS platform, the modeling ended up being very productive and further provided an environment in which to test out the addition of an induction machine. The induction machine model, while not being a true VBR model (due to solution delay) features the connectivity and visual advantages of a VBR method model and should provide the sponsor and future users with an easy to manipulate model with better transient support and potential configurability than the built-in PSCAD model. Building a custom model in PSCAD/EMTDC is fairly straight-forward, and access to PSCAD's full model library is available for all custom models. The lack of time-step restriction also frees the user from having to worry about coding efficiency. From the PSCAD/EMTDC results it appears as though an induction machine would work correctly with the sponsor's system, though it is impossible to know for sure with only limited data available from the project sponsor.

## *Subproject g) Integration of the various UPS battery banks on the AESD into a DC microgrid. This microgrid could possibly be expanded to include the propulsion batteries.*

In a related project, ARD-Bayview sponsored a senior design project to look at integrating the various UPS battery banks on the AESD into a DC microgrid. This microgrid could possibly be expanded to include the propulsion batteries. This project was completed in summer 2011. A summary of the work is given below.

### *Background on DC Microgrids*

The US navy is implementing the DC Zonal Electrical Distribution Systems (DC ZEDS) for the next generation warships [10]. The combat systems, propulsion and fire-fighting resources on the warships need a redundant supply of power during fault conditions. Also, replacing AC radial system on present ships would have significant gains in terms of improving compartment arrangement, reducing weight, increasing survivability, reducing ship motion, improving fuel efficiency, damage control and environmental impacts.

## Protective system design in SPS

One strategy being employed in the architecture of Ship Board Power Systems is to use the Zonal distribution instead of radial which was used earlier. The author in reference [11] gives the advantage of zonal distribution over radial. The architecture in figure 1 is employed for Zonal distribution in DC Zonal Electrical Distribution System (DC ZEDS). This type of zonal design ensures power continuity during a fault and also isolates a fault with minimal impact to un-faulted portions of the system.

Reference [12] describes a simulation model for protecting DC ZEDS utilising the power electronic devices inherent in the DC system along with electro-mechanical isolating switches. Figure 2 shows the DC ZED with each zone fed by a Phase Controlled Rectifier(PCR). AC bus provides the input power to PCR and it feds the DC ZEDS with rectified DC. The output of each PCR is controlled by a central processor unit through which the PCR can communicate with all other DC components. In the event of loss of power from any AC bus, the PCR limits its output preventing overloading on the system.The author explains how the coordination of fault response of power electronics with static or isolating switches can implement a very effective DC distribution system with this architecture .

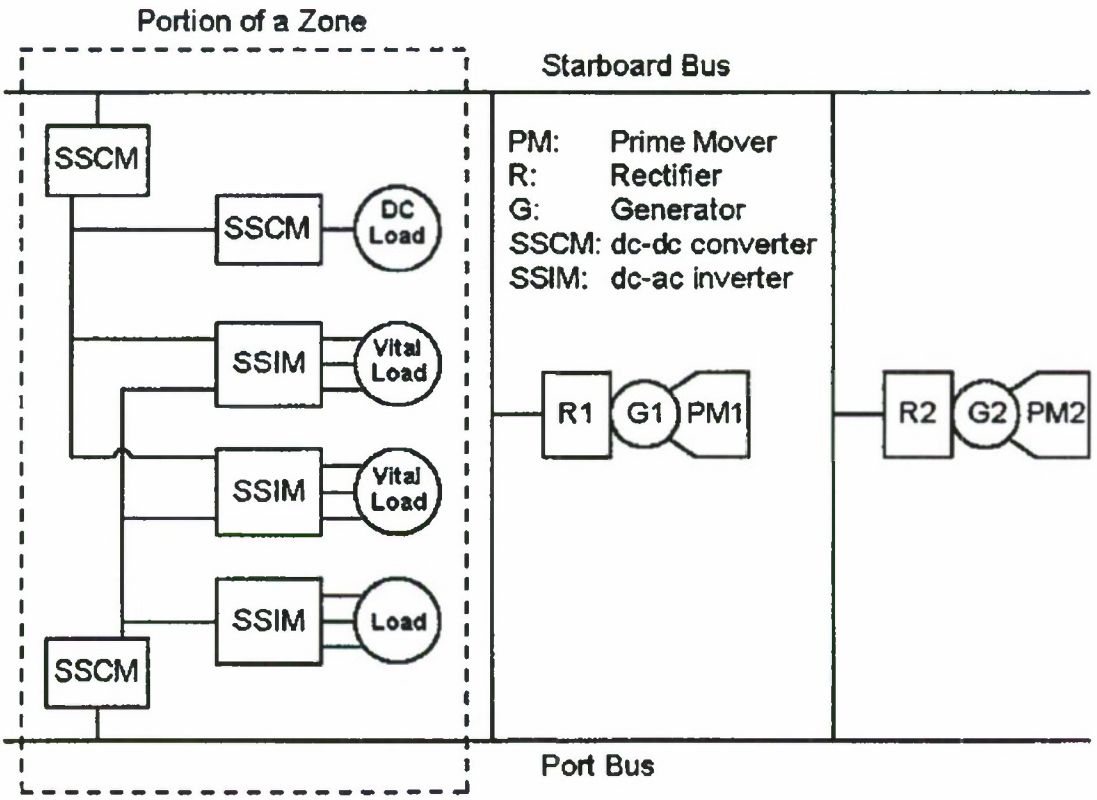



**Figure 1: DC Zonal Architecture [11]**

Reference [13], presents an integrated approach to design and simulation of the protection management system for a Medium Voltage DC System (MVDC). The author finds a method for fast detection and isolation of the fault using modern DC circuit breakers and coordinating with relays. A rapid communication between sensing, control, and power devices is realized. A new model based approach is described here in which communication, control and power systems are integratedly modeled. The power system is designed on virtual test bed VTBPro which generates C code. This code is imported into

Simulink which models the controls. This Simulink model execution is integrated in the event-based OpNet simulator creating a periodic event.

Reference [14], gives another example for combining the modeling and simulation of power systems and control systems. The author uses RTDS to model the overcurrent relay model and for performing closed loop coordination testing of relays. Two SEL 351 relays are modeled in RSCAD (graphical interface to RTDS) to achieve relay coordination.

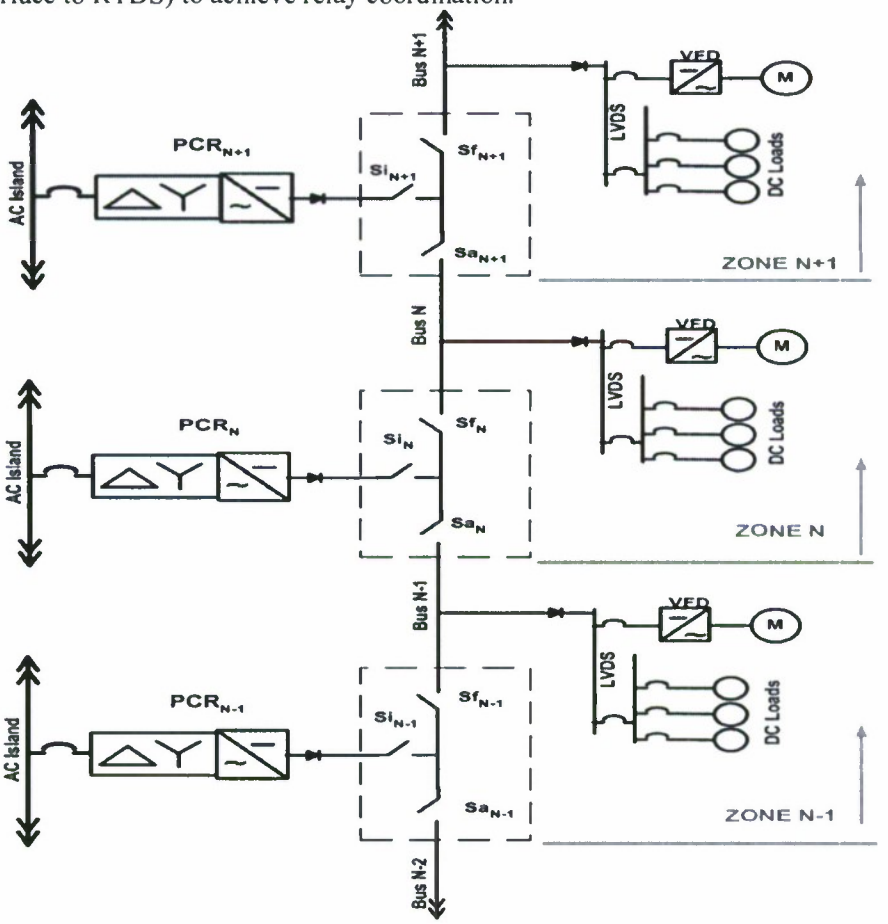



**Figure 2 : DC ZEDS [12]**

On the other hand, Ring bus configuration based IPS architecture is used in [15], with four generators, two main and two auxiliary, two propulsion load and the ship service load. The one-line diagram of such a type of system is as shown in figure 3. High current superconducting fault current limiters (HTS-FCL's) are considered by the author as a way to limit fault currents. The system is modeled in Matlab simulink blockset and the details of the model are presented.

The SPS protective system design is thus a zonal distribution architecture with high degree of reconfiguration and redundancy. Though the high degree of detailed modeling may not be required for terrestrial power systems but the SPS still provides a good reference for the protective system design of DC microgrids.

## Fault detection in SPS

Am approach to protect a DC system is addressed in reference [18]. The dynamic performance of the AC side of the ship board power system is analyzed for understanding and detecting a fault or an arcing phenomenon on the DC side of the system. A 12-pulse converter is modeled with an output of 5000V and 2000 amps DC from 13.8kV line-line RMS AC source. The instability caused in the 12-pulse converter system by the DC fault is explored in this reference to detect and isolate the fault. An algorithm is developed based on the zero crossing technique where the faulted waveform is compared to the non faulted one and when the comparison doesn't match a signal is sent to converter. During a fault, the faulted waveform shows transients which helps in detecting fault. This reference makes idealized assumptions in setting the firing angle of the thyristors to 100deg and reversing the converter mode upon the occurrence of the fault. This is theoretically possible but may not work on practical system. Also, the actual method to detect DC fault cannot rely on this comparison algorithm due to delay factors and non-synchronized signals.

AC side fault interruption based protection system based on DC side over current sensing is proposed in reference [19]. The converter is used as a crow bar which shuts down upon the occurrence of a fault on the DC side. Overcurrent based fault isolation using solid state circuit breaker (SSCBs) is also discussed in this reference. The system considered here is a VSC which converts 4160V AC to 7kV DC. The SSCBs can interrupt a fault current about 3 times rated current in this case. The DC capacitor overcharging is prevented by turning of the converter and thus preventing capacitor discharge.

Adaptive and state estimation based protection schemes are explored by the authors in [20] and [21]. An adaptive protection system verifies the system topology and if there is a change in the topology due to some disturbance it updates the relays with new calculated settings. State estimation technique detects the fault based on high speed state estimation calculations. These techniques are dependent on high computational speeds on compact systems and hence may not be useful for the terrestrial power systems.

### DC Microgrid Protection

While the SPS systems provide a good reference for DC Micro-grid modeling and protection, the terrestrial and SPS systems differ in many aspects. Redundancy in each aspect of system design is expected in SPS. Transmission line dynamics, grounding, system reconfiguration, loading are different in the SPS than that of terrestrial systems.

The terrestrial DC micro-grid has higher power rating compared to SPS and hence the protection system design should account for high fault current interruption and fault isolation. Thus, there are challenges which are unique to terrestrial system that are needed to be addressed while modeling and conducting protection studies.

The protective strategies at normal micro-grid ratings are not yet studied for a DC system. The key requirement for any protective system is safety, the standards and guidelines are yet to be addressed for DC protective system safety. Safe protection strategies include protecting electrical equipment from faults and also appropriate grounding practices.

Key design criteria for any protective system are [1]:

- *Reliability*—Predictability of the protective system response to faults and dependability to not trip spuriously on transients or noise
- *Speed*—Fault is removed from the system and normal operating voltages is rapidly restored
- *Performance*—Continuity of service to the loads; where a lower performing system loses a significant portion of its loads when a fault occurs
- *Economics*—Installation and recurring costs; generally in opposition to performance, i.e. a good performing system generally costs more.

- *Simplicity*—Quantity of parts, zones of protection, level control de-centralization needed to ensure its reliability

The degree to which these requirements are met depends on the protective system design, grounding, fault detection, switchgear and current sensing technologies. The following sections address some of these issues.

### *DC Current Sensing Techniques*

Current sensing plays a vital role in sensing the change in current. Conventional AC power systems utilize Current Transformers (CT) to measure the current flowing in a line. Current transformers can be thought as normal transformers with turns ratio in a range 300:1 to 500:1. Thus they have a huge number of primary windings than on secondary which divides the current in the same ratio. Generally the output of CTs is around 5A AC which is sufficient to operate a relay. During fault conditions the output across CT changes which is sensed by the relays and circuit breakers are acted thereupon.

CTs are not used to measure the DC current. They usually saturate and tend to behave as non linear component in saturation. Saturation makes the CT give incorrect output which may mislead the circuit breaker operation. A number of preventive measures are taken in AC systems to prevent saturation of a CT by DC offset during transients.

Various methods available to sense the DC current are briefed as follows [22].

#### Hall Effect Transformer

When a current is flowing through a conductor (or semiconductor), voltage is developed across its sides if a magnetic field is applied to the material perpendicular to the plane of the conductor. This is Hall Effect. The Hall sensor measures this voltage.

The Hall Effect transformer consists of torodial magnetic core with a gap where the hall sensor is placed. These hall elements detect the magnetic flux due to the magnetic field around the conductor. The most accurate measurement is obtained when a number of Hall elements are placed in gaps along the torodial core, the output of which is fed to an amplifier and the amplified currents pass through the torodial core nullifying the magnetic field. The sum of all currents is proportional to primary current.

#### Flux Gate Transformer

This principle works on detecting the saturation state of magnetic circuit. The magnetic core has a similar structure as that of Hall torodial core. The core is made of material with high magnetic permeability and immersed in the magnetic field which is to be measured.

A signal is fed to the core which leads the material to symmetric saturation in the absence of external field. When the magnetic field being measured is applied the symmetry is lost. Current is injected in a way that the lost symmetry is restored. This current is proportional to current being measured.

#### Flux-Gate Transducers

The Flux-Gate transducers work on the same principle of flux gate transformers. Here the magnetic field generated by the current is detected by means of a sensor as in Hall effect transformer. The standard flux gate transducers use a torodial magnetic circuit with an air gap where the sensor is placed with a

secondary winding. The non standard flux gate transducer uses the torodial core itself as measuring sensor, thus without including the air gap. This is as shown in figure 4.

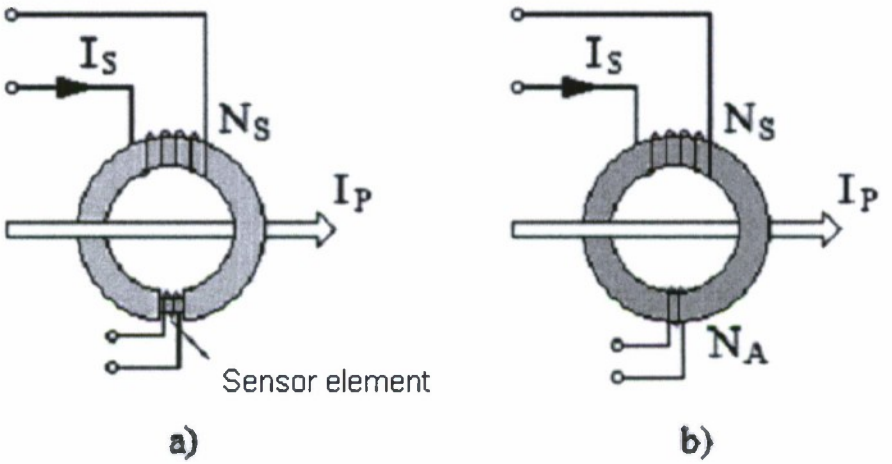



**Figure 4: Structure of a Flux-gate transducer: a) standard and b) without gap in the magnetic path [22]**

Reference [22] gives a comparison of all the above principles in measuring DC current and a detailed description on using Flux gate transducers for measuring DC current.

## Optical Current Sensors

Optical current sensors are based on the principle of Faraday Effect in the optical fiber. Faraday Effect is the phenomenon where in if a magnetic field is applied along the propagation direction, right and left circularly polarized light waves travel at different speeds as in figure 5. Thus the waves accumulate a path difference or proportional phase difference which is related to current flowing through conductor.

In this type of sensor a simple loop of optical fiber is placed around the current carrying conductor. The sensor integrates the magnetic field along a closed path of the optical fiber. This eliminates the torodial core and also eliminates the dependence on sensor position in the core.

ABB manufactured the ABB FOCS (Fiber Optic Current Sensor), in which three different output signal formats are available: a digital output with 24 bit resolution, analog voltage output (0.2-1V) and analog current output (4-20mA) [31]

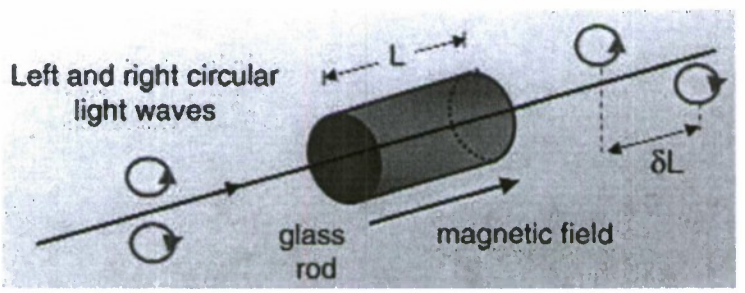


**Figure 5: Faraday effect [31]**

## Rogowski Coil

Rogowski coil works on the principle of Faraday's law that states "the total electromotive force induced in a closed circuit is proportional to the time rate of change of the total magnetic flux linking the circuit". The circuit is shown in figure 6.

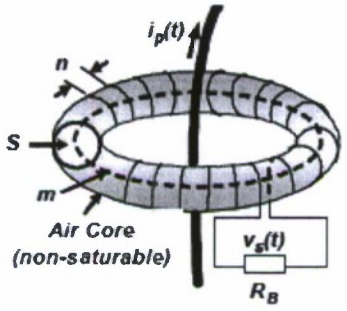



**Figure 6: Rogowski Coil [23]**

Voltage can be induced in the conductor either by moving the conductor through the magnetic field or by placing the wire loop in a time varying field.

Rogowski coil can be primarily used to measure high AC currents as the coil is free from saturation. If the coil can be moved in the magnetic field then DC currents can be measured.
Electrochemical processing plants use Rogowski coils to measure the DC bus currents .The measurement head is moved through the magnetic field, creating a flux coupling change, and the dc current level can be measured. Figure 7 shows one of such instruments used to measure DC current [30].

**Figure 7: Segmented coil [30]**

An experiment was performed with the rogowski coils available in UI power lab to test the DC current sensing. The experimental setup consists of an oscilloscope connected to the output leads of the rogowski coil and the rogowski coil is wrapped across a DC current flow. The coil didn't sense any current as there was no change in field. If the coil is moved vigorously it showed some disturbance on the CRO screen.

All the current sensing techniques mentioned above are used to measure DC current at industrial level where the currents are low. These techniques are not explored for the distribution systems yet.

### *DC Protective Devices*

Reference [1] gives a review of the viable protective devices and new circuit breaker technologies which is briefed in the following section.

In AC systems, the circuit breakers isolate the faults, with an arc, opening the current flow path upon an over-current condition. Current is forced to zero by extinguishing the arc. Now the voltage from power source is applied across the circuit breaker. The circuit breakers are designed optimizing the fact that there happens natural current zero in AC systems. This is not the case in DC systems.

Fuses, Circuit Breakers are the commercially viable devices that are used for the protection of low rated DC systems. The protective device used must be able to dissipate the energy during interruption. Solid-State Circuit Breakers (SSCBs) are being considered for the fault interruption in Ship Board Power Systems. SSCBs can interrupt over-currents much faster by setting the threshold fault current to a lower value.

Low voltage DC power supplies as in traction, mining, battery protection etc use fuses for protection. Fuses are the ideal protective devices for systems where there is high di/dt rise, which makes the fuse reach its melting point. Fuses may not be considered as a reliable protection device for DC micro-grid as they are only suitable for small lengths of cables.

Conventional Circuit Breakers are also being considered for protection in DC systems. But, the CBs are designed optimizing the fact that there exists a natural current zero in power transmission, which is not the case in DC system. Capacitive discharge from the output filters of power converters as discussed in the previous section aggravates the limitation. Circuit breaker time trip coordination is difficult to achieve and also the speed of isolating fault and recovery is limited in case of DC Circuit Breakers.

Solid State switches can be considered to interrupt high DC current. Reference [24] gives the application of solid state switches to the DC industrial power system. The author initially discusses two methods one of which uses the thermal effect of high temperature superconductor to limit the fault current. The other method is to integrate pulse-by-pulse current limiting technique into the control of solid state switch. The switch is closed by operating a gate signal using pulse-by-pulse current limiting technique. It should be noted that the switch used to isolate the fault should dissipate stored energy during interruption. Hence the solid state switch should carry with it sufficient current limiting inductance and voltage clamping circuitry.

There is continuous energy dissipation in SSCBs due to their addition in circuit. They are not a perfect replace for electro-mechanical CBs currently used in AC systems. Proper switch gear technology for isolating DC faults is still under study.

### *Issues in Dealing with the DC Protective Devices*

DC over-current protection is not similar to AC protection. In AC systems Circuit Breakers are designed such that they open the current flow path when an over-current is detected with an arc. The arc dissipates the energy and as the arc extinguishes current is forced to zero. This is aided by the natural current zero in AC system.

Three significant issues have been identified as a result of developing a DC distribution system for a shipboard power system [25]

- Capacitive discharge of upstream power converters into sudden short circuit faults leading to loss of coordination between upstream and downstream circuit breakers and potential circuit breaker damage

- Difficulty in coordinating upstream and downstream circuit breakers fed by current limiting DC power converters
- Necessity of adding redundant circuit breaker poles in order to mitigate the loss of circuit breaker clearing capability when multiple ground faults short out circuit breaker poles

The peak of the current surge is limited at the load, closest to fault, by the impedance between the power converter and the fault. The current at the circuit breaker closest to the fault is limited by the impedance between the upstream and downstream circuit breakers and the current at the upstream circuit breaker is limited by the impedance between the power converter and the upstream circuit breaker.

This results the coordination of upstream and downstream circuit breakers highly impossible assuming the breakers trip. This also results in incomplete clearing of fault considering Molded Case Circuit Breakers (MCCBs) as protective devices. The testing procedure and the other two issues that limit the use of conventional circuit breakers can be referred from [25]

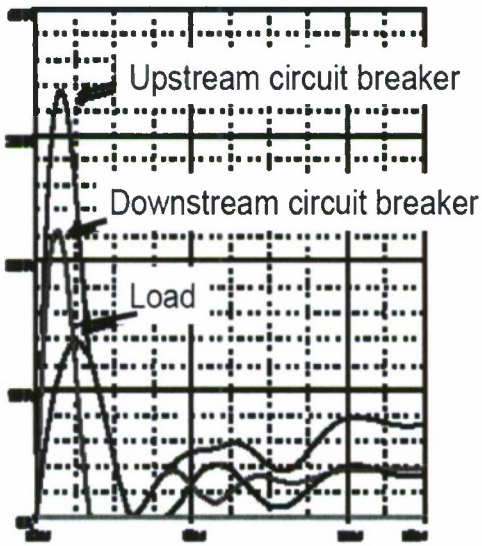



**Figure 8: Capacitive discharge current due to a sudden fault [25]**

### *Protective System Design*

The author in reference [1] suggests the following fundamental requirements for the safe, reliable and well performing DC micro-grid.

1. No single point of failure
2. Redundantly fed electrical zones or buses that can be rapidly separated from the bulk power system
3. Ability to rapidly re-configure the system, island the system and re-direct power away from a fault while minimizing interruption of power to non-faulted portions of the system
4. Ability to locate and isolate faults without the need for inter-component communications
5. Ability to recover from a fault to a reliable configuration and mode of operation
6. Load prioritization into sensitive vs. non-sensitive
7. Minimize the effect of a faulted load on other loads

8. Redundant feeds to sensitive loads
9. Ability to quickly shed non-sensitive loads
10. Load and power flow management from a centralized control
11. Transient operational capability in degraded modes, such as loss cooling and loss of power flow management
12. Condition-based maintenance

1.

The author further gives the examples of DCZED in SPS and MTDC systems where DC distribution is implemented and further evaluates the systems based on the aforementioned fundamental requirements concluding that each of those system architectures can meet the 1 to 5 numbered requirements. These systems are reviewed in the earlier sections of the report.

### *Fault Detection Techniques*

The fault detection techniques that can be investigated for the future DC micro-grid depends on the system topology and the type of converters (VSC or CSC) that are employed. Various fault identification techniques implemented in SPS and MTDC systems are briefed in earlier sections. While the AC side faults can be determined and isolated by the standard techniques being employed in AC micro-grids, the DC side fault characteristics are yet to be studied. System configuration and grounding methods are important aspects which need to be studied before selecting the protection schemes.

Standard overcurrent technique cannot be relied on as the VSC IGBTs restrict the fault current flow. Reference [26] details many issues that make the overcurrent coordination difficult at the distribution level with increased distributed generation. Relying on the fault studies for the proposed system the overcurrent protection can be set as back-up scheme.

Line Current differential scheme is an attractive option with increased reliability on communication networks and the advent of digital relays. While arguments based on cost and the reliability of the communication network are evident, with proper coordination and disturbance tolerance, line current differential scheme can be employed as primary fault detection on the DC systems. Reference [16] and [6] explains the current differential scheme employed in SPS and HVDC systems respectively.

Other schemes presently employed in DC systems include rate of change of current and rate of change of voltage or undervolatge schemes. These schemes are dependent on the type of converter (CSC or VSC) employed. Change of voltage schemes can only be employed for CSC based schemes [5]

New innovations in fault detection schemes include the wavelet based mechanism [9], state estimation based detection schemes [21] presently being investigated for MTDC and SPS systems respectively. The conventional current differential and overcurrent protection are the methods still that can be relied on. Use of converters for fault identification can also be explored.

## *Project Results*

The Advanced Electric Ship Demonstrator (AESD) is a large scale model electric vehicle. It supports an onboard generator, propulsion batteries and an auxiliary power system for instrumentation. Currently, the only active model resides in Bayview, Idaho at the Bayview NAVSEA base. The model is ¼ scale of the actual prototype and is available for instrumentation and acoustic testing.

The AESD is also referred as the Sea Jet since it is comparable to the Navy destroyers of that class. It has a length of more than 133 feet and a full load displacement of 120 tons (239,000 pounds) [1]. The Sea Jet uses Lake Pend Oreille as its primary testing zone because the

lake is very deep and fairly isolated. The majority of the acoustic testing is done during the night when there will be few civilian boats on the water. During the colder months, tests can begin earlier in the day. Civilian boats are rarely seen on Lake Pend Oreille from November to February. With no boats to disturb the water, there is little acoustic contamination and is an excellent area to perform acoustic tests.

While the Sea Jet is docked, the propulsion batteries are charged and the Uninterruptible Power Supply (UPS) are also charged. They are charged by a standard power source on land. Once the Sea Jet leaves land, it is dependent on the UPS, propulsion batteries and a generator. There is a diesel generator on board that can charge the batteries and UPS while out on the lake. The generator is loud and can only be used between tests. The actual testing occurs when the AESD reaches a checkpoint in the lake and from then on the generator is turned off and the AESD is only running on battery power. These tests periods are referred to as quiet mode runs.

The majority of data received is from quiet mode runs. To gather more effective data the quiet mode runs need to create less acoustic noise. While there are a few problems that need to be looked at more closely, the biggest problem is caused by the UPS.

X.2 Problem

The main limiting factor in the platform's operational effectiveness is the auxiliary power system. Currently, the auxiliary loads are powered by four independent UPSs during quiet mode (battery) operations. The UPS loading and battery issues prevent the AESD from supporting the desired test plan. Age and frequent use has reduced the ability of the UPSs batteries to hold a charge. Additionally, operational efficiency of the AESD decreases due to the limited internal charging rate of each UPS that extends the downtime between quiet mode runs. Furthermore, the quality of AESD acoustic data is being impacted by significant acoustics of the UPS units.

Ideally the quick solution would be to remove the UPS and the problem would be solved. But the UPS provide an integral role in the auxiliary system, by providing backup power in case of a primary power failure, and must be replaced by a similar component. The UPS hums constantly and causes definite acoustic contamination. If the UPS are taken out, a new auxiliary system will need to be developed that will still allow all the vital loads to constantly have power.

X.3 Objectives

The objective of this project will be to perform a feasibility study to find a better design to power the auxiliary power system. This includes: replacing the four UPSs and creating a longer quiet mode run time followed by a shorter charge time of the battery banks. The current UPS design has many deficiencies and a new auxiliary design is needed. The goals are to provide uninterrupted power flow to every load, increase the duration of battery usage, decrease charge time for batteries, and decrease acoustic contamination.

X.4.1 Design 1

Specifications

The first proposed design outlines a DC system made up of twenty four lead acid batteries that are used for the propulsion system currently on the ship. The batteries are arranged into 3 strands of eight series batteries resulting in 96 volts as the output voltage. They cannot be arranged in parallel yet because if one strand discharges faster than the others they will not be at the same voltage, so they are sent through individual DC/DC converters with voltage regulation that keep them at a constant 120V dc. The value in the three strands that is if one of the strands

goes down, the remaining two can supply the necessary amount of power to the loads. The single common bus removes any isolation factors as they all draw from the same source, but it also allows the use of one inverter which is better than the previous four and the new inverters are a lot quieter than the built in UPS inverter's. Also, a switch will be provided to switch to the generator power or to silent mode for testing. 24 batteries is the minimum amount of batteries needed to sustain a quiet mode run in this design, more batteries can be added to increase the run time.

The UPS's were not designed to be run on the internal batteries for extended periods of time; they only kicked in for a little when the main source went down. Due to this, the batteries in the UPSs are likely nearing end of life. They also are not meant or designed to be quiet. This design provides a solution for all of the problems, and using this idea, actual components in the market can be found that will be rated for the load. A diagram of design one is represented in figure 17.

With the batteries assumed to be drained only 60%, the run time was approximately 43 minutes. This run time can be increased with more batteries. 43 minutes is comparable to the previous design run time and it will have less acoustics. The cost for design 1 was estimated at $6700.00, the majority of the cost was due to the 24 lead-acid batteries.

**Design Schematic 1**

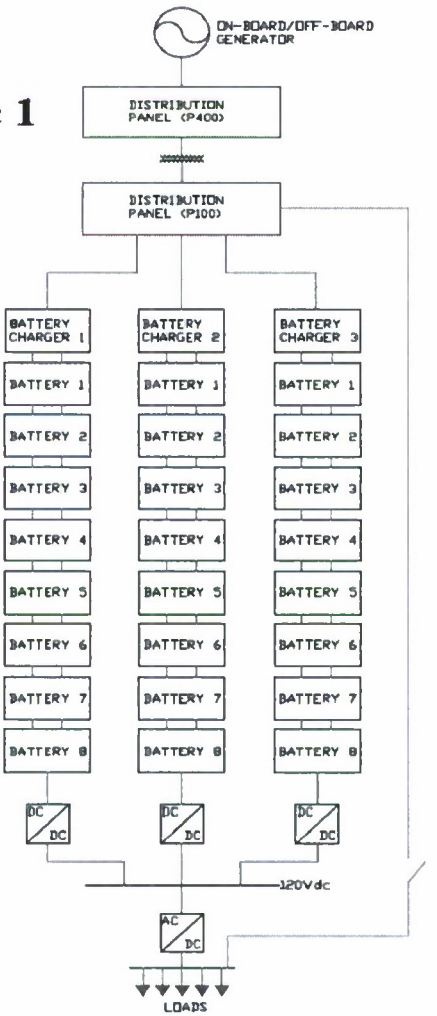



Figure 17. One-Line Diagram

X.4.2 Design 2

Specifications

Design option two connects the auxiliary power system into the propulsion system. The auxiliary loads consume only 6.36 kW, while the current propulsion system consumes 600 kW. An addition of 6.36 kW to 600 kW is small enough to not make a difference on the amount of batteries needed. Unfortunately, the propulsion battery system is split into twelve different strings of lines. We will only be able to connect to one of the battery strings. A schematic of design two is represented in figure18.

The main advantage of this design is it would tie the auxiliary system into the existing propulsion system. Also, the design will provide constant power to the auxiliary loads. The four UPSs from the original auxiliary system design would be eliminated which should decrease the acoustics. A DC/DC converter and an inverter would still be needed to provide the correct voltage to the loads.

With the batteries assumed to be drained only 60%, the run time was 107 minutes with just the auxiliary power system running. With the propulsion system running at the same time as the auxiliary system the run time falls to only 12.2 minutes. This is compared to a run time without the UPS system added of 13.7 mins. So, we lose approximately 10% of the potential run time. It is worth noting that Bayview considers a single run a 10 min period. A few other disadvantages of this design would be the added acoustics compared to design one and the implementation of the digital switch between the propulsion batteries and the reserve batteries.

Furthermore, there is a possibility that the line may fail and the auxiliary system would be without power. A possibility would be to use the battery bank from design option one which would work as a failsafe if there was a failure to the main power supply. If there was a need for a different source of power for the auxiliary system, a digital switch would change to the reserve battery bank. The reserve battery bank would consist of 24 batteries, 3 parallel strings of 8 batteries in series. This would provide an ample supply of power for a short term fix if the main power supply fails. The cost for design 2 was estimated at $1400.00

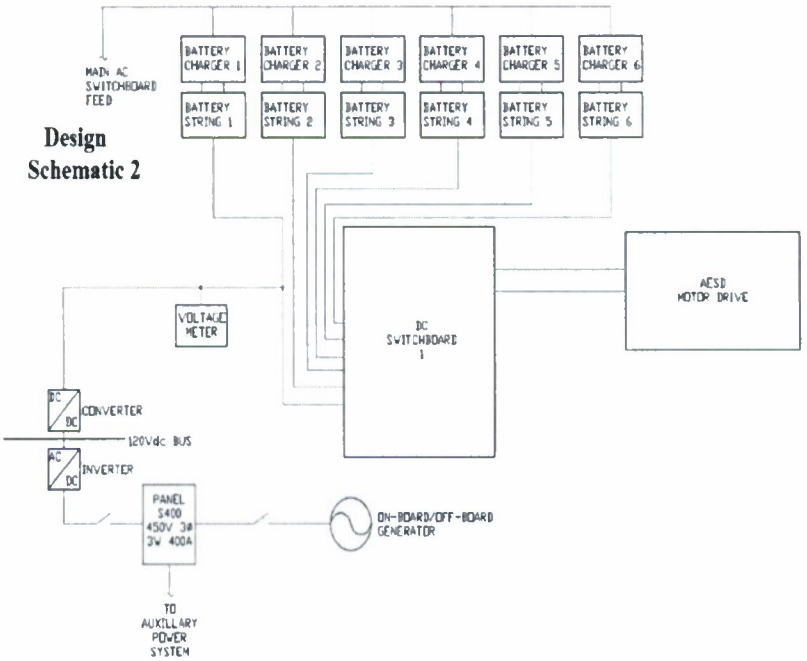



Figure 18. One-Line Diagram

X.4.3 Design 3

Specifications

Design option three connects the auxiliary power system into all twelve battery strings in the propulsion system by means of a DC switchboard. The DC switchboard will allow all the strings to be drawn on by the auxiliary system. As previously mentioned, the auxiliary loads consume only 6.36 kW, while the current propulsion system consumes 600 kW. An addition of 6.36 kW to 600 kW is small enough to not make a difference on the number of batteries needed. When a line of the propulsion system reaches a critical voltage point the ships operator will be able to manually switch the auxiliary power system onto a new string from the propulsion system. A diagram of design three is represented in figure 19.

Again the auxiliary system must have power at all time, which means a backup system may be needed. The battery bank from design option one would work as a failsafe if there was a failure to the main power supply. If there was a need for a different source of power for the auxiliary system, a digital switch would change to the reserve battery bank. The reserve battery bank would consist of 24 batteries, 3 parallel strings of 8 batteries in series. This would provide an ample supply of power for a short term fix if the main power supply fails.

The main advantage of this design is it would tie the auxiliary system into the existing propulsion system and all of its battery strings. Also, the design will provide constant power to the auxiliary loads for a greater period of time and allow the ship operator to monitor the voltage on each line of the propulsion system closer. The four UPSs from the original auxiliary system design would be eliminated which should decrease the acoustics. A DC/DC converter and an

inverter would still be needed to provide the correct voltage to the loads. So there still will be some acoustic contamination.

With the batteries assumed to be drained only 60%, the run time was 21.4 hours with just the auxiliary power system running. With the propulsion system running at the same time as the auxiliary system the run time falls to only 13.7 minutes. A few other disadvantages of this design would be the added acoustics compared to design one and the implementation of the digital switch between the propulsion batteries and the reserve batteries. Design 3 is also more costly than design 2 because of the DC switchboard. The cost for design 2 was estimated at $4400.00.

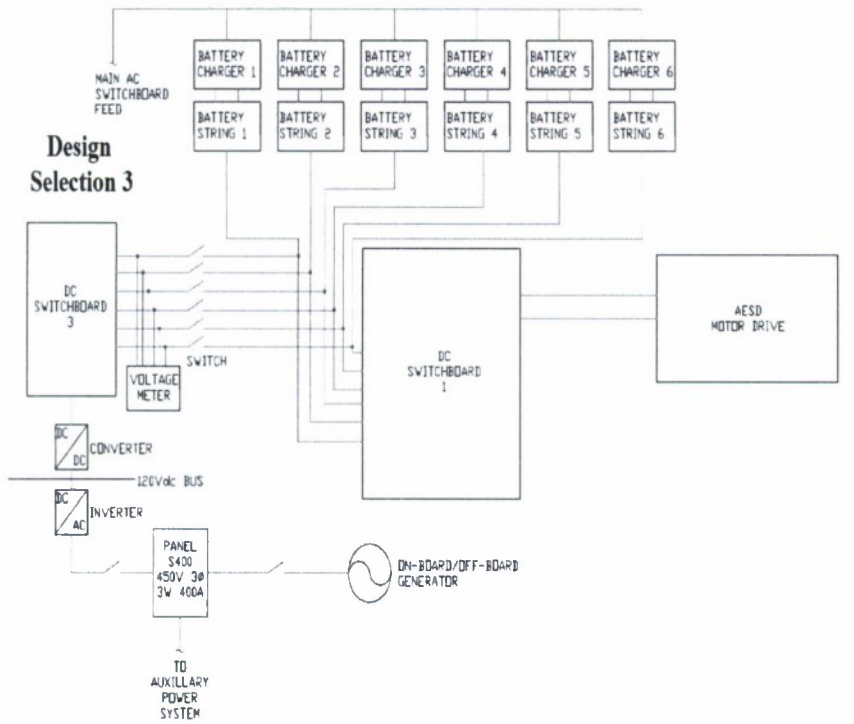



Figure 19. One-Line Diagram

X.5 Conclusion

Currently, Design 2 is considered the most promising. The reason for this is it will provide the run times that were desired. Along with the run times Design 2 will provide less hardware installation; including but not limited to one inverter, one DC to DC converter, and wiring to connect the devices into the existing propulsion system. Design 2 will also be the least expensive system to implement, with less hardware and ultimately less installation time Design 2 will meet all of the requirements of the project without sacrificing the current performance of the Sea Jet.

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## *Subproject h) Design of a graphical user interface to control the battery charging process on the LSV2 platform at ARD Bayview.*

One of the projects to address this issue considered a Graphical User Interface to control the charging process in a convenient fashion. Excerpts from a conference paper describing this work are given below.

Proposed system

The proposed system allows the technician to monitor directly the charge via the computer workstation. The technician then commands adjustments, again from a computer workstation, without rising from the chair. Due to government contract restrictions, the proposed changes to the system must be add-ons for the current chargers, making no physical changes to units themselves. This adjustment interface contains an eight-port serial communications card with a custom (student-designed) graphical user interface (GUI) that controls the charging process of the seven propulsion chargers and the single auxiliary system charger. This addition of computer control of the chargers from the technician's office streamlines the charging process, increases productivity, and allows for improved implementation of the charging algorithm with almost instantaneous command response from the charger outputs.

Problem definition[1]

The charging profiles require several adjustments to both the voltage and current levels applied during a charging cycle. These charging profiles maximize the life of the lead acid batteries used on board the USS Cutthroat. Eight charging stations are connected to eight strings of batteries. The battery bank is separated into propulsion and auxiliary to facilitate servicing the power requirement of each system. The propulsion system battery bank is comprised of 1680, two-volt, valve regulated lead acid (VRLA) batteries connected in four parallel strings. The auxiliary battery bank, powering the test equipment and supporting apparatus, consists of 186, two-volt, VRLA batteries connected in a single string. After each LSV2 underway (operation), both the propulsion and auxiliary batteries require recharging. Throughout the charging process, voltage and current transitions are manually controlled on eight separate battery chargers by a battery-charging technician. A typical battery charge lasts between approximately eight and sixteen hours under expected load. The process requires close monitoring to maintain the appropriate current and voltage levels applied to the batteries. This process introduces human error to the charging algorithm for the LSV2's battery bank. Once implemented, the proposed design will reduce the variations encountered using the present method. This will help to extend the lifecycle of the VRLA batteries used in the LSV2 as well as provide the maximum amount of stored charge for the performance of each test run.

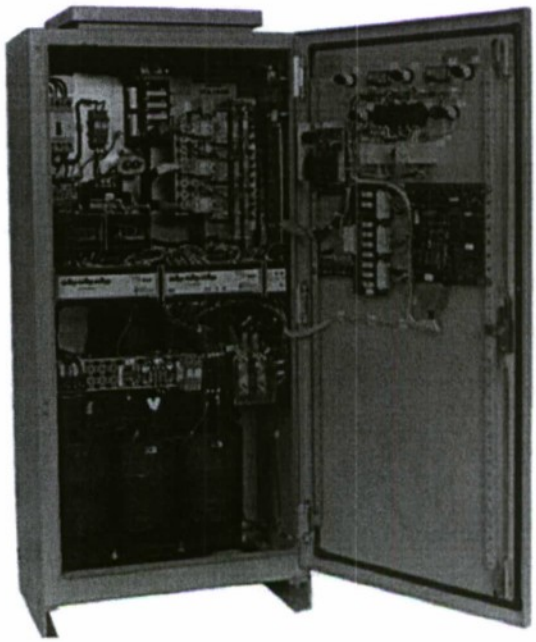


Figure 9. Interior of Charging Unit

Criteria for successful completion[1]

The team's objective is to investigate and design a remote control for the LSV2 charging system. The Navy research team requires that the current charging system remain unaltered because it works. It has also passed the lengthy technical approval process as agreed between the builder and the Navy. The Navy desires only an improvement shell, not a redesign or modification of the incumbent system.

Our improved design adds to the current system to accomplish our specific goals. The control system must have the ability to adjust the level of current and voltage supplied to the battery banks. Additionally, the control system must be able to display the front panel indicators of each of the eight charging units including: unit power, over voltage, over current, fan loss, over temperature, ground fault, and the current/voltage magnitudes. The controls on the front panel include adjustment knobs for voltage and current, and buttons for stop, start, and fault reset. The goal is to achieve remote manipulation of all of these controls.

Specifications

The primary goal of the research team is remote monitoring and control of all eight of the chargers. The charging units, manufactured by PTCI, have a remote/local stitch on the front panel connected to an ICS Electronics Corporation Model 2361 serial interface circuit board (Figure 9)[2]. The desired method of interaction with the chargers is to use this card, attaching external control to the serial interface circuitry installed via the J4 jack, 0.001-inch center pin connector. The interface card is mounted on the interior of the front panel and is easily accessible for the installation of the connecting cables. The ICS interface card is version 5 and has modifications that allow it to be powered through the main connection header (J2). The required power for the card is +12V (volts) unregulated at J2 on pins 17, 39, and 60 with ground connected to pins 16, 38, and 59. These power connections are already made in the charging unit. The J2 header is wired to control the charging unit and is connected per the manufacturer's design.

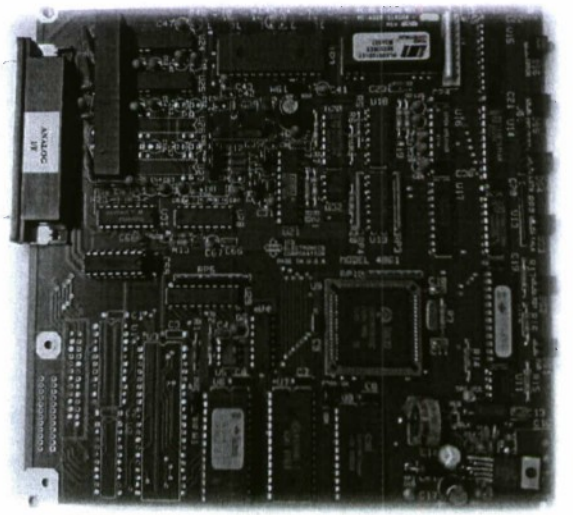


Figure 10. ICS 2361 Serial Interface Board

A graphical user interface (GUI, pronounced "gooey") is the chosen method for the battery technician to control the system. A GUI will enable the technician to communicate with the ICS board by entering desired values into preprogrammed fields, making it unnecessary for the technician to have programming knowledge. This will eliminate the need for additional training of the technician (e.g., to use a command line interface) as well as increase the speed of the commands as a program can communicate faster than human response times.

Front panel indications will be retrievable through the ICS card and displayed via the GUI. The primary use of the front panel indicators is to alert the battery technician of a fault condition. These indications must be checked and polled frequently, to assure their accuracy at the computer terminal display. The terminal emulation will send the check commands at regular

intervals, every five to thirty seconds, to check these fault indicators. These intervals will be kept as short as possible.

Design development restriction

The Navy requires the charging units remain unaltered from their original, functioning state. Any hardware necessary for the functionality of the design either must be already installed, or added in such a way that it does not interfere with the physical charging process itself. The statement of work from Navy reads: "Any additional hardware needed to accomplish autonomous charger control must be able to be installed, mounted, and operated in concert with the existing LSV2 battery chargers and must interface with the existing LSV2 support barge powering and cooling systems."

Additionally, the computer system used to control the chargers is a secure machine, isolated from outside data sources to protect the classified nature of the USS Cutthroat; because of this, there is no available Internet connection. Therefore, all software, for both the GUI and the hardware drivers, must be fully contained on a premade compact disc, which then installs and updates the system.

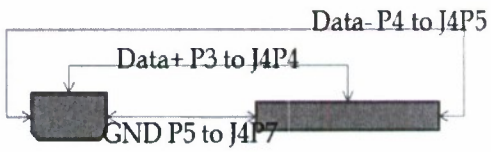



Figure 11. Wire Connections from Computer to ICS Board

Figure 12. MOXA CP-118EL, 8 Port Serial Communication Card

Hardware design: Connection to charger control cards

The ICS interface card has an RS-232/RS-485 connection at J4; connecting the following three wires achieves this connection: transmit data output (Tx), receive data input (Rx), and signal ground (GND). The ten-pin header located at J4 uses the following pin assignments for connecting these wires in a RS-232 configuration: Tx = pin 3, Rx = 2, and GND = pin 7 or pin 9. The signal ground is a very important component of serial communications as it is the baseline for all high and low determinations of signals. Therefore, it is necessary to take additional precautions to reduce the amount of electrically coupled noise by connecting wire shielding to a single ground point, eliminating ground-loop interference.

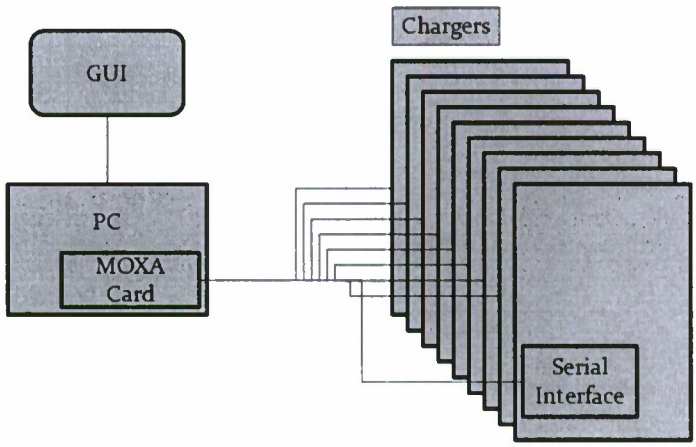



Figure 13. Wiring Diagram of System

Hardware design: Interconnecting Cables

The connection made between the computer workstation and the charger's interface

card raises specific concerns including shielding, cross talk, and length restrictions that need to be addressed. The communication cabling environment is electromagnetically noisy due to the magnetic flux generated by the chargers' large transformers. When these transformers step voltages to the appropriate levels during a charge cycle, they generate magnetic flux that can induce undesired voltages and currents. Magnetically coupled interference is very difficult to protect against; the proposed design uses twisted communication wiring to effectively cancel out electromagnetic interference (EMI) from external sources.[3]

The possible conflicts with the communications via electromagnetic wave interference imposes constraints on cable length. The length of the cable connecting the parts of the system begins to have a deleterious effect when it exceeds approximately 100 feet. The lengths required for this project range from 20 to 40ft, well within the length allowed. This restriction must be contained in all installation and maintenance instructions in order to avoid system failure due to this kind of electromagnetic interference (EMI) problem.

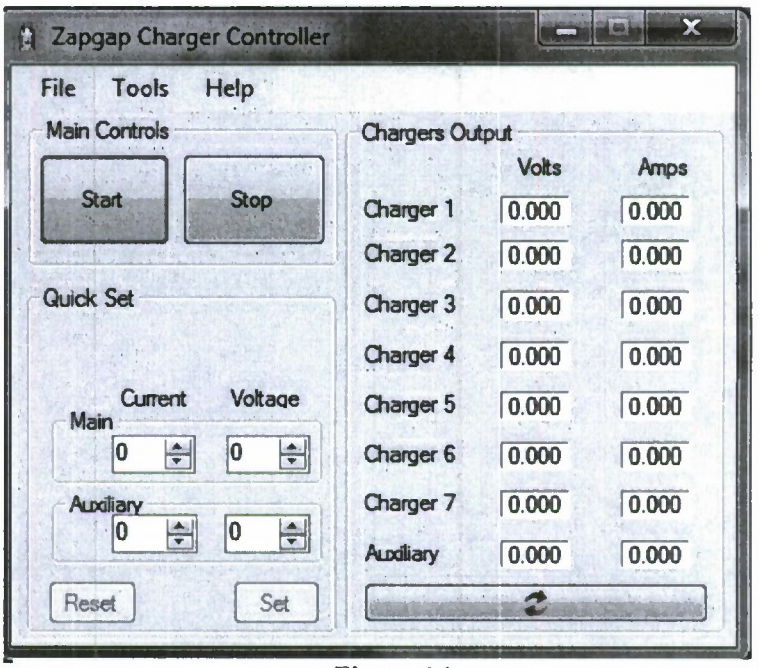



Figure 14:

GUI Simple Format

Software design

The graphical user interface (GUI) is a key part of this project because it is the point where the battery technician remotely interfaces with the chargers. There are two aspects necessary for this interface to be successful: ease of monitoring and ease of making adjustments. The chargers' front panel controls include three buttons (Start, Stop, and Fault Reset) and two knobs controlling voltage and current. An accompanying display shows a digital seven-segment LED readout. The design implemented these controls and display into the software for ease of use and familiarity for the technician. The GUI also provides fault.

Computer communications interface card

A MOXA CP-118EL card is the serial networking interface card is

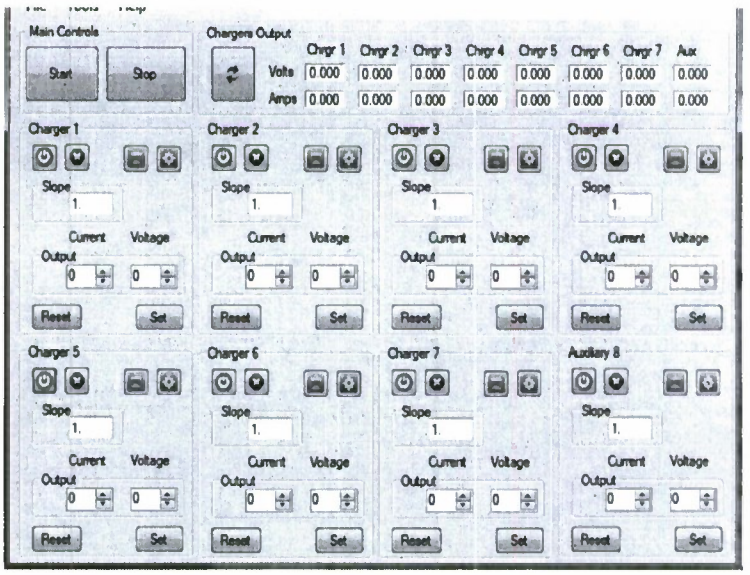


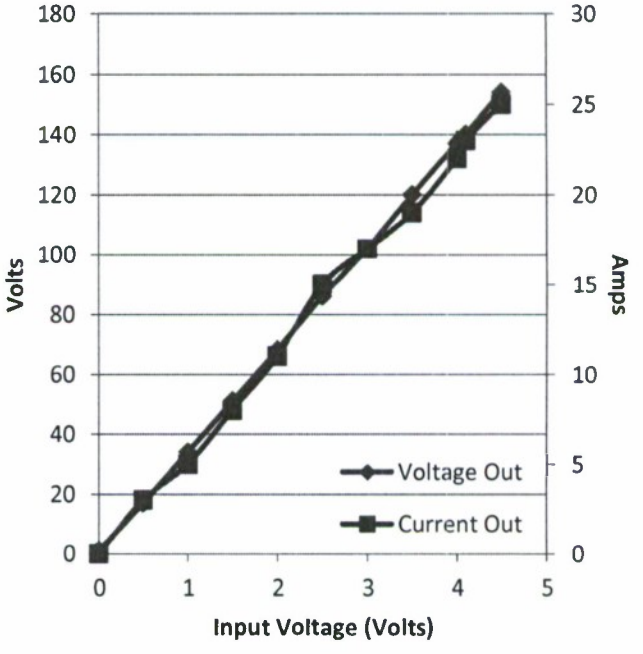

Figure 15:

GUI Advance Mode

installed in the PC to talk with the ICS cards. The product requires a computer workstation with an available PCI express slot on the motherboard for installation. Once connected, the switches must be set to select RS- 232. This changes the output pins and the output level range of the signal from the card. This product offers eight RS-232, optically isolated communication lines, allowing each individual charger to have its own COM port. The terminal emulation program, PComm Lite, included with the MOXA card, allowed us to interface with the serial connection to send preprogrammed SCPI commands to the ICS boards. MOXA PComm Lite provided an alternative to using Microsoft's more complex Win32 COMM API; this added flexibility when designing and interfacing the GUI with the system.

Wire and connectors

To ensure the highest quality signal was achieved during communication, a premade and shielded cable was used. Using standard DB-9 cable connectors allowed for an easy connection with the MOXA card that has eight DB-9 male headers corresponding to each of the available COM ports. It was then determined using an ohmmeter, which wires corresponded to the appropriate pins in the MOXA connection. A ten-pin header was then attached to the opposite end ensuring these individual wires were properly positioned to connect with the proper pins of the ICS board. Removing all unused wires from the ten-pin header was a precaution to reduce risk of noise. These extra wires were secured using heat shrink on the exterior of the cable. All cables were constructed fifty feet in length— omitting unnecessary connectors to prevent possible uneven



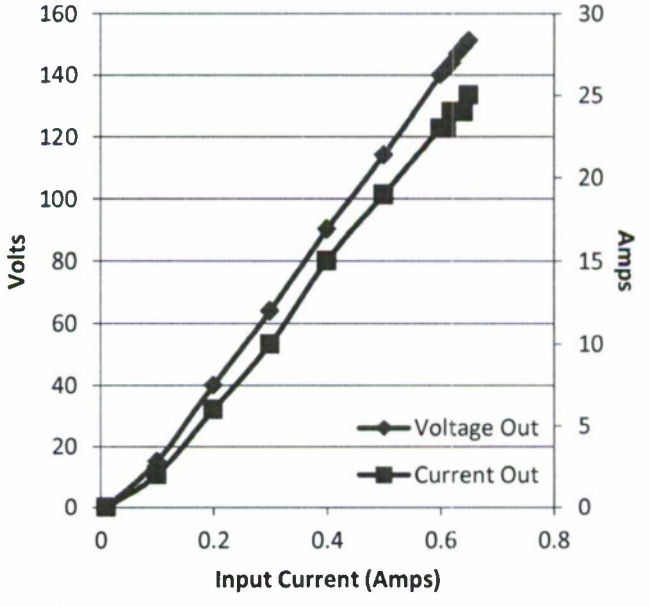




Figure 16. Calibration curves: Voltage and current response to respective voltage and current inputs

attenuation of the signal.

Graphical user interface (GUI)

The GUI has the human factors of a battery technician in mind. It incorporates the same terminology and control settings currently available on the front of the charging units. The GUI, implemented as a .exe file developed using Microsoft Visual Studios, allows the user to enter a desired value into a labeled block as a simple integer. The GUI then converts the desired inputs into Standard Commands for Programmable Instruments (SCPI), processed by the ICS cards inside of the chargers. The GUI makes it easier for users of all levels to control the chargers accurately. Its terminal mode, when open, allows the user to type in and send direct SCPI commands to the chargers. The standard mode, a programming interface, performs the same conversion for the user also. We designed the GUI for two different formats for entering commands: a simple format to send the same desired outputs to all chargers simultaneously (Figure 14), and an advanced format to make desired changes to a single charger at a time (Figure 15). The GUI contains all controls and indicators that are available on the front of all the chargers. The GUI allows for increased efficiency by sending out the required sequence of commands necessary to accomplish certain tasks in milliseconds instead of the order of seconds that humans can achieve.

Result of hardware testing

The hardware design and setup was tested using charger #1 as a base. These test results were then used to create the GUI, and provided a basis for the proper scaling of entries for mapping inputs to outputs. See Figure 16. This test, conducted on the Navy site at Bayview, Idaho, and following a specific test plan, verified that the ICS board connected to the MOXA card controlled the charger in response to the proper SCPI commands. The data obtained was the output voltage and current of the charger with respect to the input voltage and currents applied. These responses enabled computing a slope that could convert and calibrate the input integers to necessary SCPI values.

Software test, version 1.0

After the completion of the GUI, the software design was tested to verify correct operation and functionality between the GUI and the charging units. Once again, charger #1 performed the initial solo charger testing. This test was successful: the outputs entered into the GUI were correctly sent and implemented by the charger. However, these results could not be replicated on the other chargers, and it could not be determined if the GUI could accurately control multiple charges at once. While not able to set the outputs of chargers, other than Charger #1, the GUI was able to establish communications with all the chargers, and perform the basic start up and initialization procedure. After this initialization procedure, all commands to alter the outputs were received incorrectly by the chargers. The values entered into the GUI were not the values being sent to the chargers and use of the command prompt line showed the inaccuracies of what the GUI was showing and the values being read into the individual chargers.

Revisions to address the incomplete success of version 1.0

At the 2008 ASEE Annual Conference in Pittsburgh, we presented a successful model for organizing and teaching students using large, daunting projects like this.[5] This model again proved successful in enabling completion of this project on time and within budget. A team of

three undergraduates, under the supervision of a professor and one graduate student, designed the system during academic year 2009 - 2010. The graduate student mentored the undergraduates and then assumed responsibility for finishing the project. He solved the shortcomings of the project as described as follows.

An important discovery after the test was that a delay of 100ms between commands was not always long enough to allow the ICS board time to process a command before receiving a new one. The delay was set to 250ms to compensate for this. This delay change resolved the problem of commands not realizing on the charger.

Accuracy of data appeared to be a problem as well. Analog data was normalized to a 0-5V scale. Testing revealed an output reading from the charger by the ICS board could deviate by up to 0.2V. This large an error was not acceptable

In an attempt to overcome the error in reading the output, the GUI was modified to average five consecutive readings of the output for display. Though this reduced the error, it was still insufficiently accurate and unacceptably imprecise.

Output voltage readings of charger #1 were significantly more repeatable and more accurate than readings from the other seven chargers. Comparing the ICS board in charger #1 with charger #7 revealed that two capacitors, labeled C82 and C83 were missing on charger #7. These capacitors served as low pass filters on the plus and minus voltage lines that collected sensor data from the output of the charger. The resistor used was 1KΩ. The capacitors had a value of 0.022μF. The time constant of this circuit forms a cutoff frequency of 7.23MHz. This simple single pole filter eliminated the noise causing inaccurate voltage readings. Therefore, we added capacitors to the ICS board in charger #7 and accuracy improved to the level specified by the manufacturer. The rest of the chargers' boards were modified with the same capacitors.

Calibrate the chargers

We performed and recorded a manual calibration on chargers #1, #2, and #7. We calibrated the current first, by setting the voltage control to the maximum value of 5.0V, to avoid voltage limiting, and then step up the current control from 0-5V, in 0.25V increments. The process was repeated as the voltage stepped down, also in 0.25V increments. We repeated the process, this time setting the voltage control to its upper limit of 5V and stepping through the current, then decrementing the voltage control for the next sequence of current steps, etc. The data proved to be consistent and repeatable. From this data, we calculated appropriate calibration functions. The accuracy of the input to the output measured on the ICS board averaged 98.53% and 99.02% for the current and voltage respectively on charger #1; other chargers exhibited similar accuracy. The graduate student verified these results on site at the Navy base.

Educational aspects of this project

As mentioned earlier in this paper, we engaged the students using a previously successful model for organizing and teaching students using large, daunting projects. We presented the details of our model in our award-winning ASEE paper from 2008.[5] For this project, we again consider our method of teaching students to be successful for the following reasons:

- The project finished on time and under budget. Navy engineers and contractors who had attempted the same project in the past did not finish at all.
- Student anecdotal comments were strongly positive. All three students returned feedback that described their satisfaction with their learning. They encountered a wide

range of electrical engineering problems and solved each successfully to the satisfaction of the project's sponsor. The students identified and recognized this wide range of successful learning in their end-of-project comments.

- All three students graduated at the end of the semester that they completed the project. All three were offered employment with the project sponsor and all three accepted the offer. Often students who worked on Navy-sponsored projects since 2007 with our teaching model, nine accepted employment with the Navy
- The Navy sponsors returned strongly positive comments concerning the work and learning of the students. They applauded their organized approach, their problem-solving skills, their focused learning and performance, their meeting the deliverables on time and under budget, and their presentation skills.
- The Navy made bids with no less than $25,000 each of the next two semesters. Most senior design projects at our university draw less than $5000. The project officer made it clear that the success of students who completed this project had a lot to do with the Navy's returning with substantial money. We consider the project sponsor's hiring all of the students and then returning with substantial money for new projects for each semester since to be a strong indication of the success of our teaching methods.

Conclusions

This paper describes how a student design team, mentored by a graduate student, successfully automated data collection and command and control of a set of eight large battery chargers. They carefully established the specifications. They found that the chargers' interface board had multiple interface technologies, e.g., RS232, RS485, GPIB, etc. However, important components were missing from the boards and a means of multiplexing the signals from seven boards was lacking. They specified an appropriate interface and then bought the necessary parts, testing and proving the revised boards as capable of communicating through the available interfaces. Through and extensive search, they found a commercial board (MOXA CP-118EL) capable of interfacing that signals from the seven chargers with no translation or reformatting.

They then set about programming their tasks on the interface and multiplexer boards. They collected data and communicated it to a data file on the computer. They sent commands to the interface board in a manner that caused appropriate actions, e.g., start, check system for safe and defined initial condition, change parameters to conform to a desired state, engage charging mode, stop charging, set or change current level, etc. The students designed a graphical user interface to show the state of the system and to enable changes conveniently. When the design was finished, they demonstrated it in a laboratory on campus. Successful performance enabled them to travel to the Navy base and install their boards on the chargers. On their first trip, they identified several interface issues not readily apparent in the laboratory.

Version 1.0 performed within specifications on only one of the eight chargers. The graduate student then finished the project, using appropriate signal processing, such as filters and delays, bringing three chargers within specifications and proving that the remaining chargers could be likewise multiplexed within specifications. We provided a user manual for installation and operation of the system. This successful project again supports our methods of mentoring senior projects as presented in our 2008 ASEE paper.

We consider the projects sponsor's hiring all of the project's students (and nine of ten students since 2008 who performed their senior design work under our teaching model) to be a

strong endorsement of our teaching model. The project sponsor's returning with substantial money to fund more projects every semester since is also a strong indicator of the success of our teaching method.

## *Subproject i) Evaluation of trade-offs with maintaining high levels of power quality on the entire distribution system versus concentrating on point of use power management. Present systems seek to do both.*

The study will consist of an analysis of a shipboard MVDC power distribution network. Power quality, harmonic distortion, and transient analysis will be reviewed at the supply/generation side, transmission, and at the load side in an effort to determine an optimal configuration of filtering devices to improve power quality and reduce electrical noise.

The study will be conducted with computer simulation models under a variety of network topologies such as: varying the number and size of AC generators; varying the load types and sizes; and injecting electrical faults into the system. Load types will consist of at least the following types: LVDC loads; AC loads; and variable speed AC drive loads. Generation types will consist of: AC generators with an AC/DC rectifier; DC charge storage devices such as batteries, super-capacitors or fuel cells with a DC/DC converter; and a shore power connection with an AC/DC rectifier. The simulation environment will be the Matlab/Simulink software from Mathworks, along with the SimPowerSystems and Control toolbox.

## *Subproject j) Development of subsynchronous oscillation development schemes*

Some preliminary research has been done to study subsynchronous resonance (SSR) and phenomena are being found. SSR is becoming more and more of an issue these days and its effects are very complicated. SSR happens after disturbances happen in the system, which means the power system is dynamically changing during this process. With the benefits of synchrophasors, now it becomes possible to utilize wide area data and know the dynamic configuration of the power system. Based on the configuration of the dynamically changing system, we can identify the possible configurations that will potentially cause a SSR problem before we take any protection actions. It was found that the peak torque generated on the generator, which is the biggest concern of SSR, depends largely on the clearing time of the fault. A faster clearing time may cause a much larger torque. However, we need quicker relay response from the point of view of system stability. Research can be done to study what will be a good compromise between SSR protection and maintaining system stability.

What is more, SSR pose some filtering challenges for the digital filters. Full cycle cosine filters are used in the relays. This filter will not filter out the subsynchronous frequency components totally, which means frequencies in subsynchronous range will jeorpodize the measurements for fundamental frequency. Furthermore, magnitude and frequency information for the SSR component have to be obtained for SSR protection. However, because we do not know the exact value of this frequency, which vary from system to system and from time to time,

it is hard to extract the useful information quickly. Some good digital filtering algorithm needs to be used to extract the information in a quick and accurate fashion.

## *Journal Papers Published or Submitted:*

[1] B.K. Johnson, N. Fischer, and Y. Xia, "Impacts of Superconducting Cables on the Dynamic Response of Current Transformers and Protective Relaying Devices. *IEEE Transactions on Applied Superconductivity.* Vol. 21, No. 3, Part 2, pp. 2149-2152, June 2011.

## *Conference Papers Published or Submitted:*

1. J.M. Klein, H.L. Hess, and B.K. Johnson, "Cooperative Methodology for Successful Integration of Undergraduate and Graduate Research Projects," *Proceedings of the 2008 Annual Conference of the American society for Engineering Education*, Pittsburgh, Pennsylvania, 22-25 June 2008.
2. J.M. Klein, H.L. Hess, and B.K. Johnson, "Voltage Sag Mitigation Technique for an Electric Vehicle," *2008 International Symposium on Industrial Electronics (ISIE'08).* Cambridge, United Kingdom, June 30-July 2, 2008.
3. J. Klein, H.L. Hess, and B.K. Johnson, "Voltage Sag Mitigation Technique for an Electric Vehicle," *43rd Power Sources Conference*. Philadelphia, Pennsylvania, July 7-10, 2008.
4. J. Finley, D.I. Taylor, J.M. Klein, C. Byrne, H.L. Hess, B.K. Johnson, and J.D. Law, "Ultracapacitor Voltage Supplement for a Valve Regulated Lead-Acid-Battery Electric Vehicle," *43rd Power Sources Conference*. Philadelphia, Pennsylvania, July 7-10, 2008.
5. J. Klein, H. Hess, and B. Johnson, "Design Methodology of a Supplemental Energy Storage System for an Electric Vehicle," *Proceeding of the ASNE Electric Machines Technology Symposium*. Philadelphia, Pennsylvania, August 12-13, 2008.
6. L. Luckose, J. Finley, J. Klein, D. Pedersen, R. Britschgi, D. Lundgren, H. Hess, and B. Johnson, "Fuel Cell Power System for Naval Application," *Proceedings of the ASNE Electric Machines Technology Symposium*. Philadelphia, Pennsylvania, August 12-13, 2008.
7. E. William, B.K. Johnson, M. Manic, "Implementing an Intelligent Error Back Propagation (EPB) Relay in PSCAD/EMTDC 4.2.1," *2008 North American Power Symposium.* Calgary, Alberta, Canada, Sept. 28-30, 2008.
8. L.V. Dusang Jr. and B.K. Johnson, "Evaluation of Fault Protection Methods using ATP and MathCAD," *Electric Power & Energy Conference 2008.* Vancouver British Columbia, Canada, October 6-7. 2008.
9. L. Luckose, H.L. Hess, and B.K. Johnson, "Fuel Cell Propulsion System for Marine Applications," *Proceedings of the 2009 IEEE Electric Ship Technologies Symposium (ESTS)*, April 20-22, 2009, Baltimore, MD, pp. 574-580.
10. L. Luckose, H.L. Hess, and B.K. Johnson, "Power conditioning system for fuel cells for integration to ships," Accepted for the *2009 IEEE Vehicle Power and Propulsion Conference (VPPC)*, Dearborne, MI, 2009.

11. L. Luckose, H.L. Hess, and B.K. Johnson, "Power conditioning system for fuel cells for integration to ships," *Proceedings of the 2009 IEEE Vehicle Power and Propulsion Conference (VPPC)*, Dearborne, MI, 2009.
12. L. Luckose, H.L. Hess and B.K. Johnson, Paper presented at 2010 ASNE Electric Machinery Technology Symposium in Philadelphia
13. S. Page, H.L. Hess, "A Charge Equalizer for Improved Battery Life on an Electric Vehicle" Presentation at the 44th Power Sources Conference, June 2010, Las Vegas
14. N.J. Wiedeback, B.K. Johnson, J.D. Law, H.L. Hess, "A Customizable Voltage Behind Reactance Squirrel Cage Induction Machine Model for PSCAD/EMTDC," 2011 IEEE International Electric Machines and Drives Conference. May 15-18, 2011, Niagara Falls, Ont, pp. 1569-1574.
15. J. Byrne-Finley, B.K. Johnson, H.Hess, Y. Xia, "Harmonic Distortion Mitigation for Electric Vehicle Recharging Scheme," 2011 North American Symposium. August 4-6, 2011, Boston MA
16. B. Carpenter, M.W. Romine, M. Richardson, H. L. Hess, and B.K. Johnson, "Automated Battery Charger Instrumentation Interface for Multiple Interconnected Battery Strings as a Student Project," American Society for Engineering Education Annual Conference, June 26-29, 2011, Vancouver, BC.
17. L.Luckose, N.J.Urlaub, N.J.Wiedeback, H.L.Hess, B.K.Johnson, "Proton Exchange Membrane Fuel Cell (PEMFC) Modeling in PSCAD/EMTDC," IEEE Electrical Power and Energy Conference, October 3-5, 2011, Winnipeg, Manitoba, Canada.

## *Student Entries in Poster Contests*

- J. Finley "Ultracapacitor Voltage Supplement for a Valve Regulated Lead-Acid-Battery Electric Vehicle," Student Poster Contest at 2008 IEEE Transmission and Distribution Conference and Exposition, Chicago, Illinois, April 21-24, 2008. ** Placed 3rd in the competition.
- E.J. William "ANN Relays Used to Determine Fault Locations on Shipboard Electrical Systems," Student Poster Contest at 2008 IEEE Transmission and Distribution Conference and Exposition, Chicago, Illinois, April 21-24, 2008.
- M. Meena, Student Poster Contest at 2009 IEEE Power and Energy Society General Meeting, Calgary, Alberta, July 2009.

## *Master's Theses:*

1. James Klein "Design Methodology of a Supplemental Energy Storage System for an Electric Vehicle" Summer 2008.
2. Edward William "Fault Locating with an Error Back Propagation Algorithm for Shipboard Power Systems." Summer 2008.
3. Louis Dusang "Simultaneous Ground Fault Protection on Ungrounded Power Systems" Fall 2008.
4. John Finley "Harmonic Distortion Mitigation for Electronic Electric Vehicle Recharging Scheme" Summer 2009
5. Leo Luckose, "Fuel Cell Hybrid System for Shipboard Application", Graduated December 2009.

6. Jon Leman, "DC Fault Dynamics in a VSC Based MVDC Shipboard Distribution System" Master of Science Thesis, University of Idaho, December 2010.
7. Nathan Wiedeback, "Large Electric Vehicle Variable Speed Drive Simulation," Master of Science Thesis, University of Idaho, August 2011

## *Students associated with grant (either through senior design or funded graduate assistants) now working for the US Navy:*

1. James Klein, now working at ARD Bayview
2. Dirk Lundgren, now serving in active duty with the Navy. Attended the university of Idaho through the Seaman to Admiralty program.
3. Dave Petersen, now working at China Lake California as an electrical engineer.
4. Ryan Britschgi, now working Puget Sound Naval Shipyard as an electrical engineer
5. Wayne Romine, now serving in active duty with the Navy. Attended the university of Idaho through the Seaman to Admiralty program.
6. Branden Carpenter, now serving in active duty with the Navy. Attended the university of Idaho through the Seaman to Admiralty program
7. Margaret Richardson, now serving in active duty with the Navy.