Proceedings of the ASME 2011 International Mechanical Engineering Congress & Exposition
IMECE2011
November 11-17, 2011, Denver, Colorado, USA

IMECE2011-65562

THE IMPACT OF GaN/SUBSTRATE THERMAL BOUNDARY RESISTANCE ON A HEMT DEVICE

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ABSTRACT

The present work uses finite element thermal simulations of Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) to evaluate the impact of device design parameters on the junction temperature. In particular the effects of substrate thickness, substrate thermal conductivity, GaN thickness, and GaN-to-substrate thermal boundary resistance (TBR) on device temperature rise are quantified. In all cases examined, the TBR was a dominant factor in overall device temperature rise. It is shown that a TBR increase can offset any benefits offered through a more conductive substrate and that there exists a substrate thickness independent of TBR which results in a minimum junction temperature. Additionally, the decrease of GaN thickness only provides a thermal benefit at small TBRs. For TBRs on the order of 10^{-4} cm^2K/W or greater, decreasing the GaN thickness can actually increase the temperature as the heat from the highly localized source is not sufficiently spread out before crossing the GaN-substrate boundary. The tradeoff between GaN heat spreading, substrate heat spreading, and temperature rise across the TBR results in a GaN thickness with minimum total temperature rise. For the TBR values of 10^{-4} cm^2K/W and 10^{-3} cm^2K/W these GaN thicknesses are 0.8 μm and 9 μm respectively.

INTRODUCTION

The Department of Defense (DoD) is actively developing Monolithic Microwave Integrated Circuit (MMIC) technology to enable Radio Frequency (RF) systems with reduced component count and increased power density [1]. Recently, quality improvements in Gallium Nitride (GaN) electronic materials and the development of the High Electron Mobility Transistor (HEMT) device structure have allowed order-of-magnitude increases in both total power and power density over competing technologies [2]. However, the operating efficiency of these devices is highly dependent on their operating mode and frequency.

Consequently, even high efficiency Power Amplifiers (PAs) require significant cooling to maintain high electrical performance and reliability [3,4]. This is complicated by the unique structure of GaN devices which are fabricated on multi-material substrates optimized for electrical performance and not necessarily for heat transfer. Moreover, the HEMT structure creates highly localized hot spots in the active area of the device. As a result of these two conditions, the HEMT thermal stack is dominated by heat spreading and interface resistances, creating a challenging situation for thermal management.

There have been several past efforts at thermally modeling the GaN HEMT device. In the series of reports by Calame, *et al.*, the thermal performance of a GaN-HEMT package was evaluated in a number of material and package configurations, to examine the interaction of device- and package-level thermal effects [5-7]. Darwish, et al., have provided an analytical thermal resistance expression based on the solution of Laplace's equations in prolate steroidal coordinates and elliptical cylinder coordinates [8-9]. More recently, Douglas, *et al.*, modeled the effects of several HEMT design parameters including substrate thermal conductivity, the number of transistor gates, and die size [10]. These groups provided insights into device thermal behavior, but none addressed the issue of the inter-layer TBR present in the GaN HEMT material stack between the GaN and Substrate layers. The University of Bristol recently reported that this TBR in commercial devices on Silicon Carbide (SiC) substrates can reach levels greater than $6x10^{-4}$ cm^2K/W, which can increase the device's maximum temperature by up to 40%-50% [11,12].

The present study numerically examines the thermal characteristics of a GaN HEMT device and investigates the thermal impact of varying several device design parameters such as substrate thermal conductivity, substrate thickness, and GaN thickness. This investigation also includes the effect of the TBR, and shows that not only does ignoring this factor under-predict device temperature rise, but the interplay between TBR and heat spreading can lead to incorrect conclusions on how to improve HEMT thermal performance.

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
NOV 2011		**00-00-2011 to 00-00-2011**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
The Impact of GaN/Substrate Thermal Boundary Resistance on a HEMT Device	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **U.S. Army Research Laboratory,Adelphi,MD,20783**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

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15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT **unclassified**	b. ABSTRACT **unclassified**	c. THIS PAGE **unclassified**	**Same as Report (SAR)**	**9**	

NOMENCLATURE

GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
TBR	Thermal Boundary Resistance (cm²K/W)
MMIC	Monolithic Microwave Integrated Circuit
RF	Radio Frequency
PA	Power Amplifier
SiC	Silicon Carbide
FEA	Finite Element Analysis
h_{eff}	Effective Heat transfer Coefficient (W/m^{2}K)
AlGaN	Aluminum Gallium Nitride
AIN	Aluminum Nitride
DMM	Diffuse Mismatch Model
PAE	Power Added Efficiency
Θ	Temperature Rise (°C)
Θ_{Tot}	Maximum temperature Rise over ambient (°C)
T_{Max}	Maximum Temperature(°C)
T_{Amb}	Ambient Temperature (°C)
Θ_{AlG}	Temperature Rise due to AlGaN (°C)
Θ_{GaN}	Temperature Rise due to GaN (°C)
Θ_{TBR}	Temperature Rise due to TBR (°C)
Θ_{Conv}	Actual Convective Temperature Rise (°C)
Θ_{L}	Temperature Rise due to a Layer (°C)
Θ_{Lin}	Temperature Rise due to Linear Conduction (°C)
Θ_{Spr}	Temperature Rise due to Spreading Conduction (°C)
t	Layer Thickness (μm)
k	Thermal Conductivity (W/mK)
$l_{,}$	HEMT Device length (mm)
q_{Heat}	Heating (W/mm)
$\Theta_{Conv,Ana}$	Convective Temperature Rise due to perfectly spread heat source (°C)
$\Theta_{Conv,Cons}$	Convective Temperature Rise due to Constriction (°C)

BACKGROUND

HEMT devices are integrated into MMIC dies along with input and output circuits as shown by the example in Figure 1.

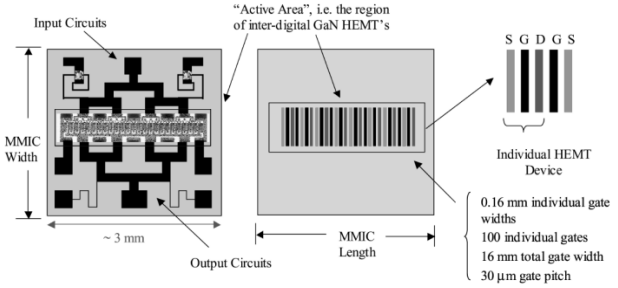

FIGURE 1: HEMT DEVICE ON MMIC DIE, FROM [5]

Within the active area, there are many individual transistor unit cells comprised of a single source, gate, and drain grouping. The present work studies the HEMT unit cell shown in Figure 2(a) with transistor geometry adopted from [4]. A heating zone of 0.5 μm by 0.03 μm was adopted from Sarua *et. al.*, who demonstrated close agreement between their 3-D finite difference model and micro-Raman and infrared thermography measurements [13]. This small heat zone length and orders of magnitude larger width allows the unit cell to be modeled in two dimensions as shown in Figure 2(b). To capture spreading effects from this unit cell, the substrate is extended to a total device length of 1 mm (not shown to scale in the figure).

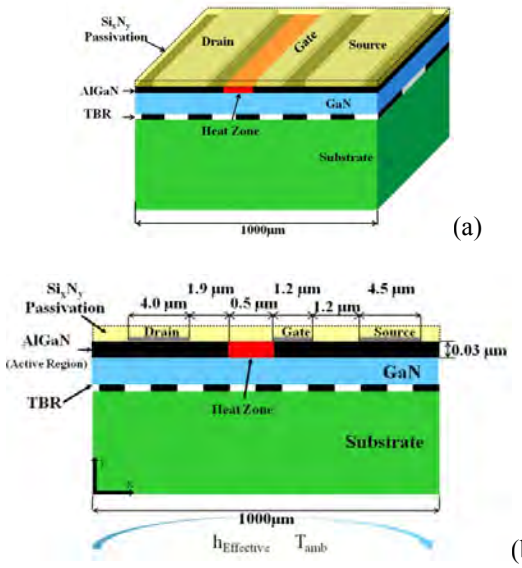

FIGURE 2: (a) GAN HEMT DEVICE (NOT TO SCALE) (b) SIMPLIFIED 2D GEOMETRY [13]

The active device is primarily comprised of a thin (tens of nm) Aluminum Gallium Nitride (AlGaN) layer grown on top of a thicker GaN film. The hot zones encountered in these devices have been previously modeled in the AlGaN layer [13] between the drain and gate. The metal gate, source, and drain electrodes define the component's electrical structure. The top surface is typically passivated with a thin Silicon Nitride (Si_xN_y) dielectric layer.

Due to the lack of available single crystal GaN substrates, the GaN layer in high performance devices is typically grown on a SiC substrate. However, the crystal mismatch between these materials requires Aluminum Nitride (AlN) and AlGaN buffer layers to reduce the number of lattice defects that would propagate up to the critical GaN layers. These buffer layers improve electrical performance at the top of the GaN layer. But, the low thermal conductivity buffer layer along with the "defective" transition layer and the lattice mismatch between the GaN and the substrate, create a TBR between the GaN and the substrate. Heat flowing into this substrate is then conducted to the "cooling solution," typically attached below the substrate and may include several thermal interface material layers, a heat spreader, and a cold plate. These components have been modeled in the present work by an effective heat transfer coefficient.

The TBR of an ideal GaN/SiC interface has been previously calculated, using the diffuse mismatch model (DMM), to be 10^{-5} cm²K/W [11,14]. This model only accounts for the acoustic

mismatch between the GaN and SiC layers and does not account for the additional TBR components. Consequently, this model under predicts recent experimental measurements by an order of magnitude [11,15].

Manoi *et al.* at the University of Bristol thermally benchmarked state-of-the-art HEMT TBRs from American, Japanese, and European manufactures that all used metal-organic chemical vapor deposition (MOCVD), but different buffer layer growth parameters [11]. Since the buffer layer is optimized for electrical and not thermal performance, a wide TBR range between $1x10^{-4}$ cm²/W and almost $7x10^{-4}$ cm²K/W was shown to exist because of microstructure defects [11,12]. These defects cause increased phonon scattering, which in turn reduce the effective conductivity of the buffer layers, increase the HEMT interlayer TBR, and consequently increase the maximum temperature rise by 10-40% when compared to a device with no TBR [11, 16,17]. Sommet, *et al.* inversely determined using FEA that the GaN/SiC TBR of their HEMT device was $2.2x10^{-4}$ cm²K/W which falls within the previously stated range [18].

Much effort has been put into reducing the temperature rise of HEMT devices. Some have looked at using different substrate materials like Douglas *et al.* [6], who recently modeled the thermal impact of using substrates with varied thermal conductivity. A sample of their results is shown in Table 1[10], where device temperature rise decreased by almost a factor of four as the substrate material switched from sapphire to silicon, and by another factor of two from silicon to SiC.

TABLE 1: SAMPLE RESULTS FROM DOUGLAS *ET AL.* FOR A TWO FINGER DEVICE AT 5 W/mm [10]

Substrate Material	*k* at 300K (W/mK)	$T_{Maximum}$-$T_{Ambient}$ (°C)
Sapphire	35	300
Silicon	148	80
SiC	400	40

Substrate materials with higher thermal conductivity than SiC, such as diamond, have also been studied. Jessen *et al.* first demonstrated chemical vapor deposition (CVD) diamond as a viable HEMT substrate material [19]. Since that time, it has been proven to provide temperature reductions when compared to comparable devices on SiC [4]. Chabak *et al.*, characterized AlGaN/GaN HEMTs on CVD diamond substrates [20]. Their process removes the original silicon substrate and replaces it with a 130 µm diamond substrate. This process contains an unspecified, proprietary GaN-Substrate interface with undetermined TBR values.

Device temperature rise can also be reduced by using thinner device layers. Perhaps for this reason, as well as application-driven thermal requirements, published HEMT substrate thicknesses have been reported as thin as 25 µm for CVD diamond, 100 µm for SiC, to even 1 mm for silicon [4,18,21]. Published material also has a wide range of GaN thicknesses for application-driven electrical, and perhaps thermal requirements, ranging from 0.47 µm to 3.8 µm and even up to 9 µm [21-23].

MODELING

The main methods discussed in the previous section to reduce device temperature rise are investigated using the FEA software ANSYS 12.0. The high order 2D thermal element, Plane77, is used and requires material properties and boundary conditions, as well as an appropriate mesh. Metrics are employed to clearly understand the tradeoffs underlying the observed trends with variable substrate thermal conductivity, substrate thickness, and GaN thickness for various TBRs.

Materials, Boundary Conditions, and Solution Space

The unit cell geometry shown in the Figure 2 (b) was modeled with the layer thicknesses and thermal conductivities shown in Table 2. For the purpose of this study, all thermal properties are assumed to be temperature independent and taken at their room temperature values. This assumption, allows the effects of multiple HEMT gates to be determined using superposition .

TABLE 2: HEMT LAYER THICKNESSES AND THERMAL CONDUCTIVITIES

	Thickness (µm)	*k* (W/mK)
SiC Substrate	300	400
GaN	1.1	130
AlGaN	0.03	30
Gold metal contacts	0.15	315
Si_xN_y Passivation	0.1	15

The external cooling portions of the package are assumed to be high performance components, such as a liquid-cooled cold plate, and are represented by an effective heat transfer coefficient of 100 kW/m²K applied to the bottom of the substrate.

It is worth mentioning that power levels for RF power amplifiers are typically described in units of Watts per millimeter of gate width (or gate periphery) in the direction perpendicular to the cross-section shown in Figure 2(b). The dissipated heat only equals the output RF power for a 50% Power Added Efficiency (PAE), which (for low input RF power) is defined as the ratio of RF output power to total power.

$$PAE = \frac{RF_{out}}{RF_{out} + P_{loss}} \quad (1)$$

High-performance power levels in recent years are on the order of 1-10 W/mm, with laboratory demonstrations in the range of 40 W/mm [24,25]. The present study normalizes all temperatures to an applied heat load of 1 W/mm, which translates into a heat flux of 67 GW/cm² for the 0.5 µm by 0.03 µm heating zone in the 2D model shown in Figure 2(b).

The solution space for this study is summarized in Table 3.

TABLE 3: SOLUTION SPACE

	Range
TBR	Zero to 10^{-2} cm²K/W
GaN/SiC TBR	10^{-4} to 10^{-3} cm²K/W
Substrate Thermal Conductivity	50 to 2000W/mK
Substrate Thickness	20 to 500 µm
GaN thickness	0.01 to 200 µm

It is seen that, to cover the full range of sensitivity, the TBR range is taken from zero to 10^{-2} cm²K/W. The substrate thermal conductivity is varied from 100 W/mK to 2000 W/mK to adequately represent the impact that Silicon, SiC, and Diamond substrates will have on the device temperature. The thermal conductivity of Sapphire (k_{th}~35 W/mK [10]) is not included in the range because it is seen as a less thermally viable substrate solution due to its reduced performance at higher cost relative to silicon [10,26].

The impact of layer thickness on temperature rise is studied by varying the substrate thickness from 20-500 µm. The upper range does not extend to 1 mm because substrate thickness's primary thermal impact was seen at values much smaller than 500 µm. Because GaN layer thicknesses are often determined based on electrical rather than thermal requirements, this study examined a wider range of GaN thicknesses than reported in the literature, taking values from almost zero to 200 µm.

It is important to note that the substrate thermal conductivity, substrate thickness, and GaN thickness were not varied simultaneously. Instead, a local sensitivity analysis was done for these device parameters, which requires the parameterization of each variable individually. Each variable however was run over the entire TBR range to fully determine its impact on the thermal performance of the HEMT device.

Mesh and Temperature Distribution

A mesh plot of the HEMT device with characteristics equal to those in Table 2 is shown in Figure 3.

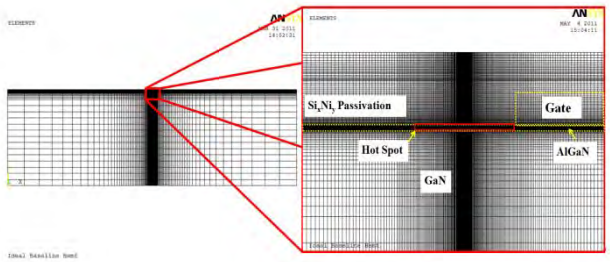

FIGURE 3: HEMT MESH PLOT WITH CLOSE UP VIEW OF HEATING REGION FOR NO TBR AND THE GEOMETRY LISTED IN TABLE 2

The figure to the right displays a magnified view of the hot spot which contains highly packed elements. This localized element density mirrors the local heat density in order to accurately capture the large temperature gradients.

Due to the nature of FEA, the results are inherently dependent on the mesh density and all meshes used are refined to eliminate mesh dependence. As shown in Figure 4, meshes with around 30,000 or higher high order Plane77 ANSYS 12.0 elements display element count independent temperature rise. The present work used meshes with element counts from ranging from 30,000 to 100,000 due to the wide range of geometries studied.

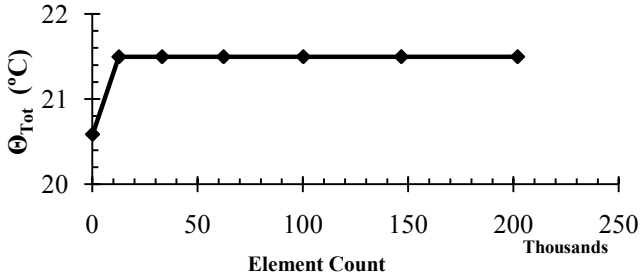

FIGURE 4: HEMT MESH CONVERGENCE FOR NO TBR AND THE GEOMETRY LISTED IN TABLE 2

The temperature distribution for the geometry detailed in Table 2 and 1 W/mm power dissipation is shown in Figure 5.

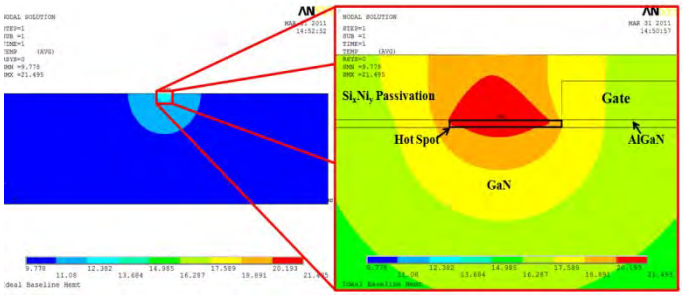

FIGURE 5: TEMPERATURE DISTRIBUTION WITH EXPLODED VIEW OF HEATING ZONE FOR NO TBR AND THE GEOMETRY LISTED IN TABLE 2

The smooth isothermal lines in the right figure provide confidence that the mesh refinement has accurately captured the temperature distribution at and around the heating zone. The non-symmetric temperature profile is due to its close proximity to the high thermally conductive metal gate.

Thermal Metrics

Determining the individual thermal impact of substrate thermal conductivity, substrate thickness, and GaN thickness requires the comparison of numerous metrics. They are formulated through analytical and numerical methods and are described by temperature rise. (Θ_{Tot}) for a unit power level of 1 W/mm.

Equation (2) defines Θ_{Tot} as the difference between the numerically determined maximum (T_{Max}), or junction, and ambient temperatures (T_{Amb}).

$$\Theta_{Tot} = T_{Max} - T_{Amb} \quad (2)$$

The maximum temperature rise is also equal to the summation of the individual layer temperature rises, the TBR temperature rise (Θ_{TBR}), and the effective convection temperature rise (Θ_{Conv}) as shown by equation (3).

$$\Theta_{Tot} = \Theta_{AlG} + \Theta_{GaN} + \Theta_{TBR} + \Theta_{Sub} + \Theta_{Conv} \quad (3)$$

The layer temperature rises (Θ_L) are defined as the difference between the numerically determined top and bottom maximum interface temperatures as shown by equation (4).

$$\Theta_L = T_{Top,Max} - T_{Bot,Max} \quad (4)$$

Slightly modifying the convention from [27], the temperature rise of each layer is also defined as the sum of the temperature rise due to linear conduction (Θ_{Lin}) and the temperature rise due to spreading conduction (Θ_{Spr}). This is given in equation (5).

$$\Theta_L = \Theta_{Lin} + \Theta_{Spr} \quad (5)$$

The linear component through each layer is the average temperature rise that would be present if the heat load was uniformly distributed over the entire cross sectional area. It is analytically calculated by equation (6) using the layer thickness (t), thermal conductivity (k), the 1 mm device length (l), and q'_{heat} of 1 W/mm.

$$\Theta_{Lin} = \frac{t}{k\,l} q'_{Heat} \quad (6)$$

Θ_{Spread} is simply calculated by subtracting Θ_{Lin} from Θ_L. The temperature rise associated with the TBR is calculated by determining the temperature jump at the GaN/Substrate interface.

The convective temperature rise from equation (3) is defined in equation (7) as the difference between the maximum back side temperature from the ambient temperature.

$$\Theta_{Conv} = T_{Back,Max} - T_{Amb} \quad (7)$$

In an effort to reduce the computational time, the length of the 2D geometry is set to 1000 µm which creates a slight heat constriction at the convective surface. Thus, the convective temperature rise is also equal to the summation of the temperature rise due to the constriction ($\Theta_{Conv\ Cons}$) and the temperature rise due to a perfectly spread heat source ($\Theta_{Conv\ Ana}$) shown by equation (8).

$$\Theta_{Conv} = \Theta_{Conv,Cons} + \Theta_{Conv\ Ana} \quad (8)$$

The convective temperature rise due to a perfectly spread heat source is analytically calculated by equation (9). Using q'_{heat} of 1 W/mm, effective heat transfer coefficient (h_{eff}) of 100 kW/m²K, and the length, l, of 1 mm, this calculation produces a 10°C average temperature rise.

$$\Theta_{Conv,Ana} = \frac{q'_{Heat}}{h_{eff}\,l} \quad (9)$$

$\Theta_{Conv\ Cons}$ is simply calculated by taking the difference between calculated values of $\Theta_{Conv\ Ana}$ and Θ_{Conv}.

RESULTS AND DISCUSSION

The model described in the previous section was studied by varying the TBR for different substrate thermal conductivities, substrate thicknesses, and GaN thicknesses in an effort to identify which parameters are significant in affecting the device temperature rise.

Substrate Thermal Conductivity Variation

Figure 6 details the substrate thermal conductivity parameterization for the range of TBR values. The substrate and GaN thickness are equal to those found in Table 2.

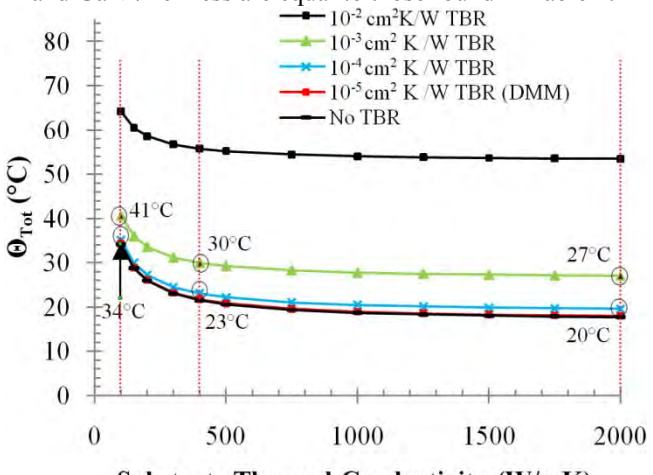

FIGURE 6: SUBSTRATE THERMAL CONDUCTIVITY SENSITIVITY ANALYSIS FOR 1.1 µm GAN THICKNESS, AND 300 µm SUBSTRATE

As expected, for all TBR cases tested, increasing the thermal conductivity decreased the maximum temperature rise. For the no TBR device, changing the substrate from Si (100 W/mK) to SiC (400 W/mK) provides around 11 ºC of temperature reduction. Moving to a diamond (2000 W/mK) substrate provides an additional 4 ºC improvement.

For a GaN/SiC device with an assumed substrate thermal conductivity of 400 W/mK, the maximum temperature rise will be between 23 ºC and 30 ºC for the GaN/SiC TBR range of 10^{-4} to 10^{-3} cm²K/W. Assuming no TBR changes associated with the high conductivity substrate, a 2000 W/mK substrate produces maximum temperature rises in-between 20 ºC and 27 ºC. This is a 3 ºC benefit over the entire range by switching the substrate material from SiC to a high quality diamond for the 1 W/mm heat dissipation case examined. It is expected that higher powers would multiply both the temperature rise and the benefit of increasing substrate conductivity.

Reference [20] describes the diamond substrate attachment process, but does not describe its associated TBR range. However, the TBR range in this study allows some conclusions to be drawn. For example, a diamond substrate (2000 W/mK) HEMT with a poor TBR (10^{-2} cm²K/W) can have a maximum temperature reduction of 55 ºC which is twice that of a SiC substrate HEMT with a 10^{-4} cm²K/W TBR. Thus, if the TBR increases due to substrate attachment process, the added benefit of the increased thermal conductivity can be offset by the increased TBR. Felbinger *et al.* performed an experimental comparison between a GaN-on-SiC device and a nearly equivalent device transferred to a diamond substrate. The fact that the device on diamond performed better thermally than the device on SiC at least suggests that the TBR can be maintained at acceptable levels during transfer [4].

Substrate Thickness

Figure 7 details the substrate thickness parameterization for the range of TBR values. The substrate thermal conductivity and GaN thickness are equal to those found in Table 2.

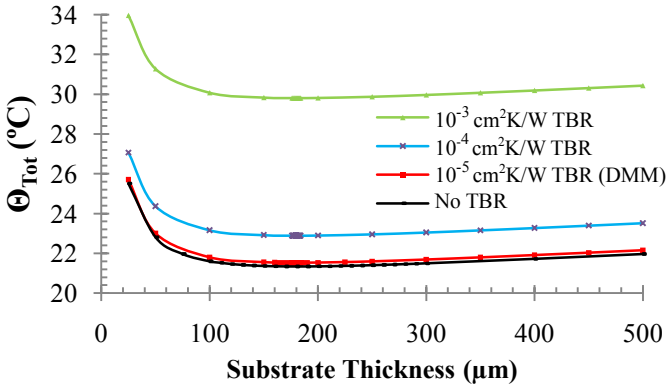

FIGURE 7: SUBSTRATE THICKNESS SENSITIVITY ANALYSIS FOR 1.1 µm GAN THICKNESS AND 400 W/mK SUBSTRATE CONDUCTIVITY

As the substrate thickness decreases, the temperature rise due to linear and spreading conductions decrease, with the spreading component decreasing more rapidly. This increases the heat constriction at the convective surface as represented by the bar graph in Figure 8.

These opposing effects are balanced at a certain substrate thickness. For the studied geometry and no TBR case, this minimum occurs at 182 µm. As shown by Figure 7, increasing the TBR increases the absolute values, but does not change the trend's shape. Thus, 182 µm thick substrates produce the minimum temperature for each configuration investigated (to within 2 µm). In addition, it is worth noting that the actual benefit of substrate thinning from 500 µm to 200 µm is minor.

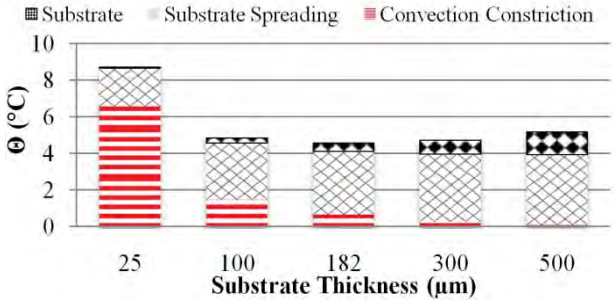

FIGURE 8: SUBSTRATE THICKNESS TEMPERAUTRE RISE TRADEOFF FOR 10^{-4} CM²K/W TBR, 1.1 µm GAN, AND 400 W/mK SUBSTRATE CONDUCTIVITY.

GaN Thickness Variation

Since the substrate is below the TBR, it is not surprising that the thermal conductivity and thickness results were relatively insensitive to TBR variation. However, the variation of GaN thickness demonstrates significant TBR dependence. In Figure 9, the maximum temperature rise is plotted as a function of GaN thickness for several TBRs. The substrate thickness and substrate thermal conductivity are equal to those found in Table 2.

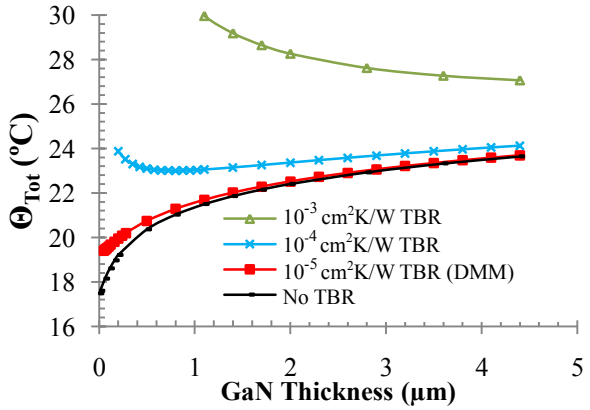

FIGURE 9: GAN THICKNESS AND TBR SENSITIVITY ANALYSIS FOR 300 µm SUBSTRATE, AND 400 W/mK SUBSTRATE CONDUCTIVITY.

For the no TBR case, varying the GaN layer thickness from 4.4 µm to 0.01 µm reduces the maximum temperature rise by about 6 ºC. If only the interfacial phonon scattering is included, (TBR=10^{-5} cm²K/W according to the DMM [11,14]), the temperature rise is largely unaffected until the thickness is below 1 µm. Thus, a GaN/SiC device with minimal or no TBR could see significant thermal benefits by employing a thin GaN layer. Their minimum values were not observed within the solution space studied

However, as mentioned previously, recent studies have indicated that actual devices contain higher TBR values. Figure 9 shows that this leads to a change in the GaN thickness trend. Within the GaN/SiC TBR range, 10^{-4} cm²K/W to 10^{-3} cm²K/W, and higher a decreasing GaN thickness does not always produce lower temperatures. As shown by Figure 10, a tradeoff between the temperature rises due to the GaN spreading

conduction, TBR, and to a lesser extent the substrate spreading conduction results in a minimum temperature with a corresponding GaN thickness. (Only the primary trade-off variables are shown in the figure).

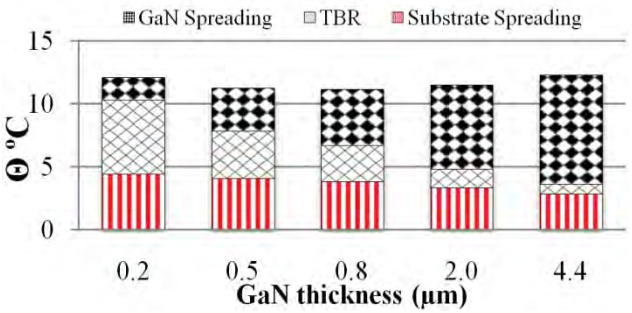

FIGURE 10: GAN THICKNESS TEMPERATURE RISE TRADEOFF FOR 10^{-4} CM^{2}K/W TBR, 300 µm SUBSTRATE, AND 400 W/mK SUBSTRATE CONDUCTIVITY.

The GaN temperature rise is large in devices with thick GaN layers because most of the heat spreading occurs in that layer before reaching the substrate interface. This places a much lower heat flux on the GaN/Substrate interface, which translates into a small temperature rise across the TBR. There is also little heat spreading through the substrate. However, thinner GaN layers spread minimally and consequently shift the heat spreading from the GaN to the substrate layer. This produces a substantial decrease in GaN spreading resistance and a slight increase in substrate spreading resistance. However, this also increases the temperature rise across the TBR because of the increased heat flux at the interface.

It is shown that for TBRs larger than 10^{-4} cm²K/W, the tradeoff between the components produces a TBR dependent minimum temperature as shown by Table 4. The minimum temperature and the associated thicknesses are listed in the second and third columns of the table. These can be contrasted to the maximum temperature rise of the 1.1 µm GaN thickness chosen as a baseline in this study.

TABLE 4: GAN THICKNESS SENSITIVITY ANALYSIS FOR 300 µm SUBSTRATE, AND 400W/MK SUBSTRATE CONDUCTIVITY

TBR (cm²K/W)	GaN thickness for Minimum Θ_{Tot} (µm)	Minimum Θ_{Tot} (°C)	Θ_{Tot} for 1.1 µm GaN (°C)
10^{-4}	0.8	23	23
10^{-3}	9	27	30
10^{-2}	78	31	56
10^{-1}	171	41	143

Smaller GaN layer thicknesses than those which produce the 'minimum temperature rise', as shown in Table 4, result in higher temperatures. In general, as the TBR is increased, the GaN thickness for minimum temperature increases due to the extra GaN spreading required to offset the higher restriction associated with larger TBRs. For completeness, Figure 11 shows the minimum temperatures for the 10^{-3} cm²K/W and 10^{-2} cm²K/W TBR devices, which are 9 µm and 78 µm, respectively. While the 78 µm case is unrealistic for practical GaN HEMT fabrication, high-voltage devices have been fabricated with GaN layer thicknesses up to 9 µm [23].

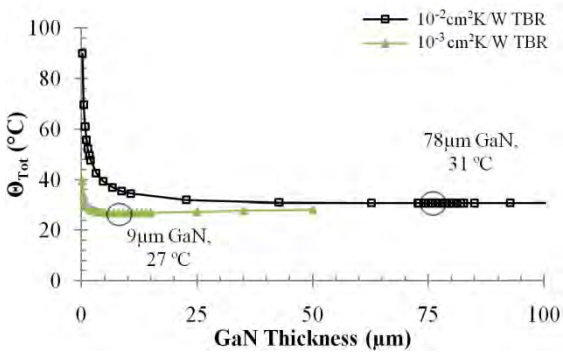

FIGURE 11: GAN THICKNESS AND TBR SENSITIVITY ANALYSIS FOR 300 µm SUBSTRATE, AND 400 W/mK SUBSTRATE CONDUCTIVITY.

CONCLUSION

By performing a parametric study of several GaN HEMT device parameters, trends related to thermal boundary layers and device thinning have been identified. In all cases examined GaN/substrate TBR was a dominant factor in device temperature rise. The substrate parameters examined, including thermal conductivity and thicknesses, showed temperature trends relatively independent of TBR. Increasing conductivity showed a significant initial benefit that starts diminishing after approximately 500 W/mK for the 1 W/mm case examined. Similarly, varying substrate thickness identified a minimum temperature value for all TBRs investigated, but the overall magnitude of this reduction for large changes in thickness is minor. Excessive thinning of the substrate appears to degrade the ability to adequately spread the heat before it is removed, increasing the maximum temperature rise.

Perhaps the most interesting results relate to the impact of GaN layer thickness on temperature rise. In the absence of any significant TBR, thinner GaN is always better as it more quickly moves heat into a higher conductivity substrate, where it spreads with less thermal penalty. However, this behavior changes dramatically in the presence of a significant TBR (showed to be around 10^{-4} cm²K/W or larger) where a trade-off between the temperature rise due to GaN spreading, TBR, and substrate spreading occurs. If the heat from the highly localized source is not sufficiently spread out before crossing the GaN/Substrate boundary, the TBR imposes a larger thermal penalty. This has the potential to offset any reduction in temperature rise from having a thinner GaN layer, and results in a minimum GaN thickness that is non-zero. Decreasing thickness below this amount will actually increase maximum temperature rise. Such a dramatic change in behavior due to the presence of the TBR demonstrates that any future efforts to better understand the thermal behavior of GaN HEMT devices or to improve their performance must take this factor into account.

DISCLAIMER

The views expressed are those of the authors and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

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