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14. ABSTRACT This project aims to design an amplifier that meets the specifications of the classic 741 operational amplifier. For this phase of the project, we focus on modeling transistors made of inorganic materials, particularly zinc tin oxide (ZTO), a solution processible semiconductor. Since n-type or NMOS transistors typically achieve higher mobilities (~5cm ² /Vs) than p-type or PMOS transistors, they were deemed to be better suited for our initial design. We have studied charge transport in ZTO transistors with zirconium oxide gate insulators and found that band transport is observed at high carrier concentrations. Ring oscillator circuits with frequency > 100 kHz have been demonstrated. Methods to improve the uniformity and yield of ZTO FETs have been worked out. Device models for ZTO FETs have been proposed and successfully tested on several circuits.					
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I. INTRODUCTION

Our goal is to create printable Op-Amp circuits with solution-based active materials. It was initially felt that the mobilities required would be $> 5 \text{ cm}^2/\text{V-s}$ and for this reason, we focused on amorphous oxide semiconductors. We demonstrated mobilities as high as $30 \text{ cm}^2/\text{V-s}$ in zinc tin oxide transistors, made from solution-based precursor chemicals. The gate insulator material was zirconium oxide, also deposited from solution.

AMORPHOUS oxide semiconductors (AOS) have been extensively studied for circuit applications, such as inverters [1, 2], ring oscillators [3, 4], transparent electronics, memory devices [5], and active-matrix backplanes [6]. Most of the AOS-based thin-film transistors (TFTs) used in circuit applications are processed with high-vacuum systems even though solution-based processes have the advantages of low fabrication cost and potential for large coverage area. This is because uniformity of device-to-device performance becomes a challenging issue when applying solution-processed AOS into more complex circuits [7]. It has been observed that the performance of solution-processed zinc-tin oxide (ZTO) devices drops as a patterned-gate structure is employed [8]. Patterned-gate structure introduces surface relief by means such as the step height of the gate electrode and spikes around the electrode edge caused by the lift-off process. Such surface relief disrupts the continuous growth of the ZTO precursor film, and thus affects device performance and uniformity.

The other issue often encountered in TFT-based circuits is the tight layout rule in mask aligning process. In most cases, the operating speed of a circuit is determined by the overlap capacitance between the gate and the source (S)/drain (D) electrodes. Thus, efforts have been devoted to reduce the overlap area and resulted in a tight alignment tolerance, usually less than $1 \text{ }\mu\text{m}$. This tight alignment tolerance makes the alignment process time consuming and can be problematic for circuits using printing process [9]. Different fabrication process and design have been studied such as using a self-aligned gate structure [3, 4].

In this report, we use a sol-gel based solution process to fabricate low voltage zinc-tin oxide (ZTO) circuits, including inverters and ring oscillators. An extended-gate design is employed to improve the gate-induced

surface relief by moving the spiky edge of the patterned gate away from the channel region. In addition, the nature of this gate design allows us to have larger alignment tolerance during fabrication.

II. EXPERIMENTAL

The ZTO TFTs used in our circuits have a bottom-gate and top-contact structure, as shown in Fig. 1 (a). Both the active layer (ZTO) and gate dielectric layer (ZrO_2) are deposited by a sol-gel method. An extended gate design, in which the interdigitated parts of the S/D electrodes are fully overlapped with the gate electrode, is employed to improve the performance uniformity of solution-processed films. Fig. 1 (b) illustrates the design of the extended-gate structure. The distance between the channel and the gate edge is kept at 10 μm or more. In this design, since the channel region of the TFTs is kept far away from the edge of the gate electrode, it mitigates the effect of gate patterning induced surface relief and allows a continuous growth of solution-processed ZTO film. In addition, this design does not require a tight alignment tolerance between the gate and the S/D electrodes, which increases the fabrication yield and makes the aligning process time efficient.

As shown in Fig. 1 (a), the substrate is glass and a recessed-gate configuration was fabricated by patterning and etching the substrate, and depositing 2.5-nm thick of Ti and 40-nm thick of AuPd as the gate electrode with an e-beam evaporator. Next, the precursor solution of ZrO_2 was spin-coated on the sample in a nitrogen environment, and followed by an annealing process in the ambient air at 500 $^{\circ}\text{C}$ for one hour. A dual layer gate dielectric is employed by repeating the deposition process once. A similar process was employed to deposit ZTO from ZTO precursor solution [10]. The resultant thicknesses of the ZrO_2 and ZTO films are 90 nm and 25 nm, respectively, and the gate capacitance is 240 nF/cm^2 . After ZTO deposition, vias were patterned and etched by reactive ion etching (RIE) to access the gate electrode and 90-nm thick silver was deposited as via plug with an e-beam evaporator. The ZTO active layer was patterned and etched by RIE to isolate individual devices. Finally, a 40-nm thick layer of aluminum was deposited as the S/D electrodes by thermal evaporation and followed by lift-off. Fig. 1 (c) shows a microscope image of circuits fabricated with the processes described above.

frequency is determined by the overlap capacitance between the gate and the S/D electrodes, or the area of the interdigitated fingers of the S/D electrodes. One easy approach to reduce the overlap capacitance and increase

the oscillation frequency is by reducing the width of the fingers. The width of the fingers in our current design is 10 μm , and can be significantly reduced to sub-micron scale by using techniques such as nano-imprint lithography. In addition, extended-gate design allows the use of relaxed layout rules (large alignment tolerance) for aligning the S/D, via and active layer masks to the gate pattern. This advantage is especially attractive for printing processes and device on flexible substrates, where fine alignment is hard to achieve.

III. DEVICE MODELLING

In low mobility devices (mobility $< 5 \text{ cm}^2/\text{V-s}$), band transport is not observed since the density of trap states is quite high and the Fermi level does not approach the band-edge, even at high gate biases. This is the case for all the devices employed in the circuits we have fabricated, which tended to possess lower mobilities than the unpatterned gate devices. In such devices, the multiple trap and release (MTR) model [11] works very well. According to the MTR model, the localized states within the bandgap may be described as an exponential density of states ($g(E)$) from the conduction band edge (E_c) [11].

$$g(E) = \frac{N_t}{kT_0} \exp\left(-\frac{E_c - E}{kT_0}\right) \quad (1)$$

N_t , T_0 , and k describe the total number of trap states, width of the exponential, and the Boltzmann constant, respectively. The number of filled trap states can be calculated using the Fermi-Dirac distribution, and integrating with respect to energy.

$$n_t = \int g(E)f(E)dE \quad (2)$$

The resulting integral can be simplified by assuming a slow-changing exponential near the Fermi energy. The Fermi-Dirac distribution can then be approximated using a delta function, and the integral simplifies to

$$n_t \approx \int_{-\infty}^{E_f} g(E)dE = N_t \exp\left(-\frac{E_c - E_f}{kT_0}\right) \quad (3)$$

Similarly, we assume that the number of carriers thermally excited to the conduction band edge can be described using the Boltzmann approximation.

$$n_c = N_c \exp\left(-\frac{E_c - E_f}{kT}\right) \quad (4)$$

Both of these assumptions break down when the Fermi level rises to within a few kT of the conduction band edge. However, for the devices described in this work, the relatively high trap densities and low effective mobilities support their use. This same reasoning leads us to assume that $n_t \gg n_c$. We can therefore approximate the total carrier concentration $n = n_t + n_c \approx n_t$.

Using equations (1) - (4), we end up with the following equation describing the effective mobility as a function of the electron Fermi level.

$$\mu = \mu_c \frac{N_c \exp\left(\frac{E_c - E_f}{kT}\right)}{N_t \exp\left(-\frac{E_c - E_f}{kT_0}\right)} \quad (5)$$

We can equate the total charge in the accumulation layer with the total charge induced by the applied gate voltage.

$$n = \frac{C(V_G - V_0)}{q} \quad (6)$$

Substituting this equation into Equation 5 gives us an expression for the Fermi level as a function of gate voltage, which is illustrated in Figure 1.

$$E_c - E_f = -kT_0 \ln\left(\frac{C(V_G - V_0)}{qN_t}\right) \quad (7)$$

Which, when substituted into equation 7 results in an expression for effective mobility as a function of gate voltage.

$$\mu = \mu_c \frac{N_c}{N_t} \left(\frac{C(V_G - V_0)}{qN_t}\right)^{\frac{T_0}{T} - 1} \quad (8)$$

This equation can be written in the form

$$\mu = \alpha \left(\frac{V_G - V_0}{V_{AA}}\right)^\gamma \quad (9)$$

With $\mu_c \frac{N_c}{N_t}$, $V_{AA} = \frac{qN_t}{C}$, and $\gamma = \frac{T_0}{T} - 1$

Equation (9) is the one used in commercially available amorphous Si FET models.

This suggests that amorphous silicon models can be used for the simulation of ZTO FETs. The main caveat is that the Fermi level must not be too close to the conduction band edge. This avoids complications of band

transport at high gate voltages. Commercially available a-Si device models were used to simulate ring oscillators and transistors successfully with the above approach and substitutions.

IV. CONCLUSIONS

We have demonstrated solution-processed low-voltage ZTO circuits, including inverters and ring oscillators, by using a high-k material, ZrO_2 , as the gate dielectric. In this study, employment of an extended-gate design ensures performance uniformity of the solution-processed films and allows larger alignment tolerance. Seven-stage ring oscillators with a propagation delay of $0.67 \mu\text{s}/\text{stage}$ at a supply voltage of 14 V were demonstrated. A device model for ZTO FETs suitable for use in circuit simulators has been derived. This model is based on the multiple trap and release transport model.

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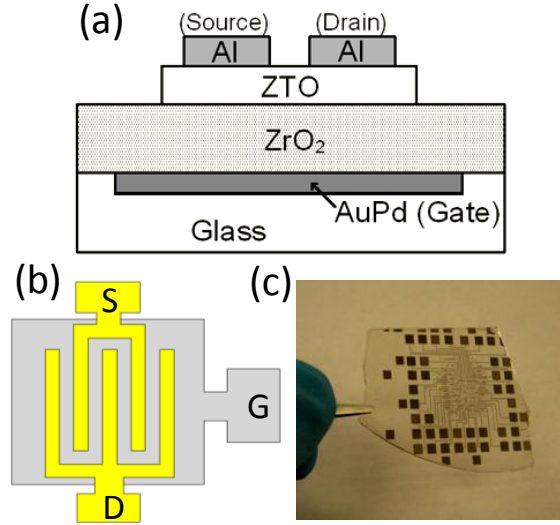


Fig. 1. (a) Device structure of a ZTO TFT with an extended-gate design. (b) Illustration of the transistor layout. (c) A photo image of the solution-processed ZTO TFTs and circuit on a glass substrate.

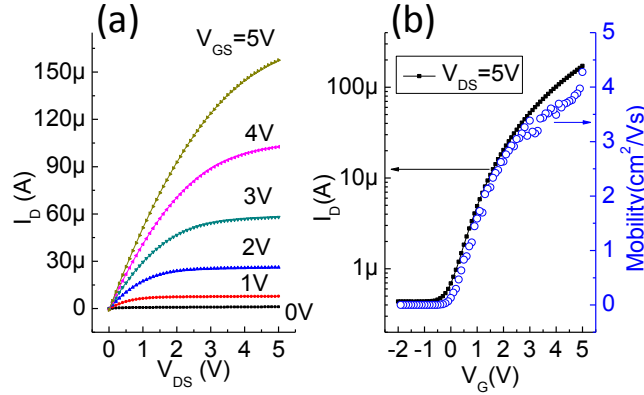


Fig. 2. DC characteristics of solution processed ZTO TFTs. (a) Output characteristics. (b) Transfer curves and saturation mobility as a function of gate voltage ($W/L = 80/4 \mu\text{m}$).

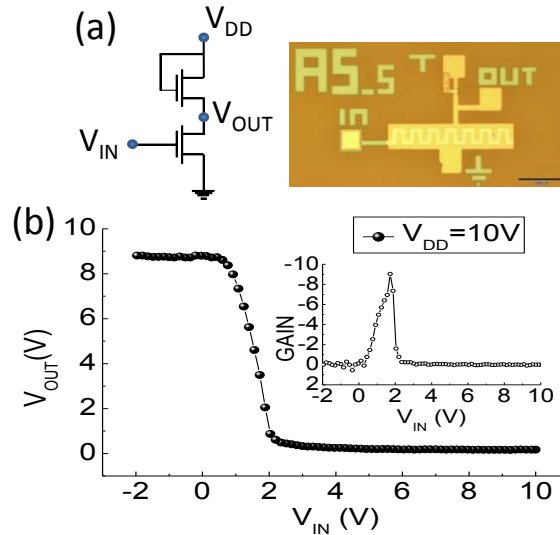


Fig. 3. Inverter circuit using all n-channel solution-processed ZTO TFTs. (a) Circuit diagram and a photo image of an enhancement-loaded inverter. (b) Voltage transfer curve ($W_{\text{Driver}}/L_{\text{Driver}} = 1000/18 \mu\text{m}$, $W_{\text{Load}}/L_{\text{Load}} = 20/12 \mu\text{m}$).

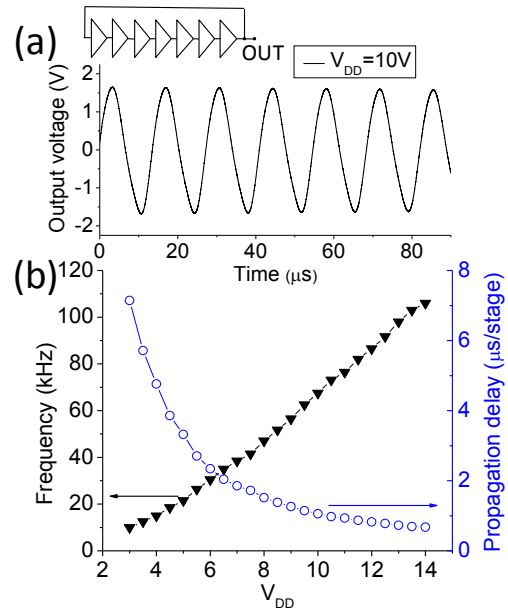


Fig. 4. Seven-stage ring oscillator circuit using all n-channel solution-processed ZTO TFTs. (a) Circuit diagram and ring oscillator voltage output operating at 76.5 kHz with a supply voltage of 10 V. (b) oscillation frequency and propagation delay as a function of the supply voltage (each inverter stage has $W_{\text{Driver}}/L_{\text{Driver}} = 600/4 \mu\text{m}$ and $W_{\text{Load}}/L_{\text{Load}} = 30/4 \mu\text{m}$).

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