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Statistical Memristor Modeling and Case Study in Neuromorphic Computing

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ABSTRACT

Memristor, the fourth passive circuit element, has attracted increased attention since it was rediscovered by HP Lab in 2008. Its distinctive characteristic to record the historic profile of the voltage/current creates a great potential for future neuromorphic computing system design. However, at the nano-scale, process variation control in the manufacturing of memristor devices is very difficult. The impact of process variations on a memristive system that relies on the continuous (analog) states of the memristors could be significant. We use TiO_2-based memristor as an example to analyze the impact of geometry variations on the electrical properties. A simple algorithm was proposed to generate a large volume of geometry variation-aware three-dimensional device structures for Monte-Carlo simulations. A neuromorphic computing system based on memristor-based bidirectional synapse design is proposed as case study. We analyze and evaluate the robustness of the proposed system in pattern recognition based on massive Monte-Carlo simulations, after considering input defects and process variations.

Categories and Subject Descriptors

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1. INTRODUCTION

In 1971, Professor Leon Chua predicted the existence of the memristor [1]. However, the first physical realization of memristors was first demonstrated in 2008 by HP Lab, in which the memristive effect was achieved by moving the doping front along a TiO_2 thin-film device [2]. Soon, memristive systems on spintronic devices were proposed [3].

The unique properties of memristors create great opportunities in future system design. For instance, the non-volatility and excellent scalability make it a promising candidate as the next-generation high-performance high-density storage technology [4]. More importantly, memristors have an intrinsic and remarkable feature called a "pinched hysteresis loop" in the $i - v$ plot, that is, memristors can "remember" the total electric charge flowing through them by changing their resistances (memristances) [5]. For example, the applications of this memristive behavior in electronic neural networks have been extensively studied [6][7].

As process technology shrinks down to decananometer (sub-50nm) scale, device parameter fluctuations incurred by process variations have become a critical issue affecting the electrical characteristics of devices [8]. The situation in a memristive system could be even worse when utilizing the analog states of the memristors in design: variations of device parameters, *e.g.*, the instantaneous memristance, can result in the shift of electrical responses, *e.g.*, current. The deviation of the electrical excitations will affect memristance because the total charge through a memristor indeed is the historic behavior of its current profile. In this work, we explore the implications of the device parameters of memristors to the circuit design by taking into account the impact of process variations.

The device geometry variations significantly influence the electrical properties of nano-devices [10]. For example, the random uncertainties in lithography and patterning processes lead to the random deviation of line edge print-images from their ideal pattern, which is called line edge roughness (LER) [11]. Thickness fluctuation (TF) is caused by deposition processes in which mounds of atoms form and coarsen over time. We propose an algorithm to generate a large volume of three-dimensional memristor structures to mimic the geometry variations for Monte-Carlo simulations. Here, we mainly focus on the impacts of geometry variations because previous experimental results showed that the geometry variations are the dominate fluctuation source as process technology further scales down [8].

Memristive function can be achieved by various materials and device structures. For its popularity, TiO_2-based memristor [3] is analyzed and evaluated in our work. However, our proposed modeling methodologies and design philosophies are not limited by the specific types of devices and can be easily extended to the other structures/materials with necessary modifications.

To demonstrate the impact of process variations on neuromorphic systems, we proposed a bidirectional synapse design and build a computing system using for pattern recognition. After embedding input defects and process variations, Monte-Carlo simulations were conducted to analyze and evaluate the system robustness. Interestingly, our experiments show that even if a large process variation exists in memristor devices, the performance of the memristor-based neuromorphic system is not affected much.

The organization of this paper is as follows: Section 2 introduces

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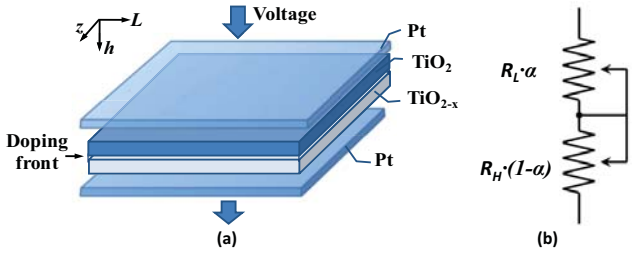

Figure 1: TiO_2 thin-film memristor. (a) structure, and (b) equivalent circuit.

the physical mechanisms of TiO_2 thin-film memristors; Section 3 analyzes the memristor model under process variations; Section 4 explains the three-dimensional memristor structure algorithm; Section 5 presents and analyzes the impact of geometry variation on the memristor electrical properties; Section 6 describe the neuromorphic system composed of bidirectional synapses and analyze its performance for pattern recognition; at last, Section 7 concludes our work.

2. TIO_2 THIN-FILM MEMRISTOR

In 2008, HP Lab demonstrated the first intentional memristive device by using a Pt/TiO_2/Pt thin-film structure [2]. The conceptual view is illustrated in Figure 1(a): two metal wires on Pt are used as the top and bottom electrodes, and a thick titanium dioxide film is sandwiched in between. The stoichiometric TiO_2 with an exact 2:1 ratio of oxygen to titanium has a natural state as an insulator. However, if the titanium dioxide is lacking a small amount of oxygen, its conductivity becomes relatively high like a semiconductor. We call it oxygen-deficient titanium dioxide (TiO_{2-x}) [9]. The memristive function can be achieved by moving the doping front: A positive voltage applied on the top electrode can drive the oxygen vacancies into the pure TiO_2 part and therefore lower the resistance continuously. On the other hand, a negative voltage applied on the top electrode can push the dopants back to the TiO_{2-x} part and hence increase the overall resistance. For a TiO_2-based memristor, R_L (R_H) is used to denote the lowest (highest) resistance of the structure.

Figure 1(b) illustrates a coupled variable resistor model for a TiO_2-based memristor, which is equivalent to two series-connected resistors. The overall resistance can be expressed as

$$M(\alpha) = R_L \cdot \alpha + R_H \cdot (1 - \alpha). \tag{1}$$

Here α ($0 \leq \alpha \leq 1$) is the relative doping front position, which is the ratio of doping front position over the total thickness of TiO_2 thin-film.

The velocity of doping front movement $v(t)$, which is driven by the voltage applied across the memristor $V(t)$ can be expressed as

$$\frac{v(t)}{h} = \frac{d\alpha}{dt} = \mu_v \cdot \frac{R_L}{h^2} \cdot \frac{V(t)}{M(\alpha)} \tag{2}$$

where, μ_v is the equivalent mobility of dopants, h is the total thickness of the TiO_2 thin-film; and $M(\alpha)$ is the total memristance when the relative doping front position is α.

Filamentary conduction has been observed in nano-scale semiconductors, such as TiO_2. It shows that the current travels through some high conducting filaments rather than passes the device evenly [16][17]. However, there is no device model based on filamentary conduction mechanism yet. Considering that the main focus of this work is the process variation analysis method of the memristor, which can be separated from the explicit physical model of memristor, the popular bulk model of TiO_2 is applied. Recent experiments showed that μ_v is not a constant but grows exponentially when the bias voltage goes beyond certain threshold voltage [18]. Nevertheless, the structure of TiO_2 memristor model, *i.e.*, Eq. (1), still remains valid.

Table 1: The device dimensions of TiO_2 memristor.

	Length(L)	Width(z)	Thickness(h)
Thin-film	50 nm	50 nm	10 nm

3. MATHEMATICAL ANALYSIS

The actual length (L) and width (z) of a memristor is affected by LER. The variation of thickness (h) of a thin film structure is usually described by TF. As a matter of convenience, we define that, the impact of process variations on any given variable can be expressed as a factor $\theta = \frac{\omega'}{\omega}$, where ω is its ideal value, and ω' is the actual value under process variations. The ideal geometry dimensions of the TiO_2 thin-film memristor used in this work are summarized in Table 1.

In TiO_2 thin-film memristors, the current passes through the device along the thickness (h) direction. Ideally the doping front has an area $S = L \cdot z$. To simulate the impact of LER on the electrical properties, the memristor device is divided into many small filaments between the two electrodes. Each filament i has a cross-section area ds and a thickness h. Figure 2 demonstrates a non-ideal 3D structure of a TiO_2 memristor (i.e., with geometry variations in consideration), which is partitioned into many filaments in statistical analysis.

As shown in Figure 2, ideally, the cross-section area of a filament is ds/S of the entire device area and its thickness is h. Thus, for filament i, the ideal upper bound and lower bound of the memristance can be expressed as

$$R_{i,H} = R_H \cdot \frac{S}{ds}, \text{and } R_{i,L} = R_L \cdot \frac{S}{ds}. \tag{3}$$

Here, $\theta_{i,s}$ represents the variation ratio on the cross-section area ds, which is caused by 2-D LER. Similarly, $\theta_{i,h}$ is the variation ratio on thickness h due to TF. The resistance of a filament is determined by its section area and thickness, *i.e.*, $R = \rho \cdot \frac{h}{s}$, where ρ is the resistance density. Therefore, the actual upper and the lower bound under the process variations can be expressed as

$$R'_{i,H} = R_{i,H} \cdot \frac{\theta_{i,h}}{\theta_{i,s}}, \text{and } R'_{i,L} = R_{i,L} \cdot \frac{\theta_{i,h}}{\theta_{i,s}}. \tag{4}$$

If a filament is small enough, we can assume it has a flat doping

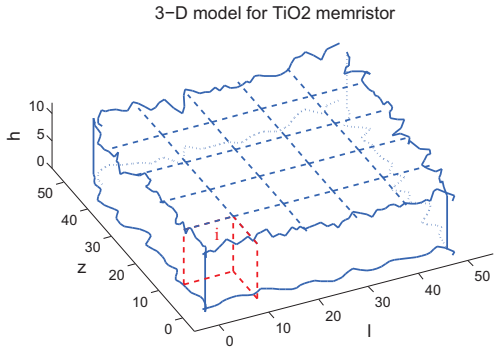

Figure 2: An example of 3D TiO_2 memristor structure, which can be partitioned into many filaments in statistical analysis.

front. Then, the actual doping front velocity in filament i considering process variations can be calculated by replacing the ideal values with actual values in Eq.(2). We have

$$v_i'(t) = \mu_v \cdot \frac{R'_{i,L}}{h'^2} \cdot \frac{V(t)}{M'_i(\alpha'_i)}. \quad (5)$$

Here h' and M'_i are the actual thickness and memristance of filament i. Then, we can get a set of related equations for filament i, including the doping front position

$$\alpha'_i(t) = \int_0^t v'(\tau) \cdot d\tau, \quad (6)$$

the corresponding memristance

$$M'_i(\alpha'_i) = \alpha'_i \cdot R'_{i,L} + (1 - \alpha'_i) \cdot R'_{i,H}, \quad (7)$$

and the current through the filament i

$$I'_i(t) = \frac{V(t)}{M'_i(\alpha'_i)}. \quad (8)$$

By combining Eq. (5) – (8), the doping front position in every filament i under process variations $a'_i(t)$ can be obtained by solving the differential equation

$$\frac{d\alpha'_i(t)}{dt} = \mu_v \cdot \frac{R'_{i,L}}{h'^2} \cdot \frac{V(t)}{\alpha'_i(t) \cdot R'_{i,L} + (1 - \alpha'_i(t)) \cdot R'_{i,H}}. \quad (9)$$

Eq. (9) indicates that the behavior of the doping front movement is dependent on the specific electrical excitations, e.g., $V(t)$.

For instance, applying a sinusoidal voltage source to the TiO_2 thin-film memristor such as

$$V(t) = V_m \cdot \sin(2\pi f \cdot t), \quad (10)$$

the corresponding doping front position of filament i can be expressed as:

$$\alpha'_i(t) = \frac{R_{i,H} - \sqrt{R_{i,H}^2 - A \cdot B(t) \cdot \frac{2}{\theta_{i,h}^2} + 2C \cdot A \cdot \frac{\theta_{i,s}}{\theta_{i,h}}}}{A}. \quad (11)$$

Where, $A = R_{i,H} - R_{i,L}$, $B(t) = \mu_v \cdot R_{i,L} \cdot V_m \cdot \cos(2\pi f \cdot t)$, and C is an initial state constant.

The term $B(t)$ accounts for the effect of electrical excitation on doping front position. The terms $\theta_{i,s}$ and $\theta_{i,h}$ represent the effect of both LER and TF on memristive behavior. Moreover, the impact of the geometry variations on the electrical properties of memristors could be affected by the electrical excitations. For example, we can set $\alpha(0) = 0$ to represent the case that the TiO_2 memristor starts from $M(0) = R_H$. In such a condition, C becomes 0, and hence, the doping front position $\alpha'_i(t)$ can be calculated as:

$$\alpha'_i(t) = \frac{R_{i,H} - \sqrt{R_{i,H}^2 - A \cdot B(t) \cdot \frac{2}{\theta_{i,h}^2}}}{A}, \quad (12)$$

which is affected only by TF and electrical excitations. LER will not disturb $\alpha'_i(t)$ if the TiO_2 thin-film memristor has an initial state $\alpha(0) = 0$.

The overall memristance of the memristor can be calculated as the total resistance of all n filaments connected in parallel. Again, i denotes the i^{th} filament. When n goes to ∞, we can have

$$R'_H = \frac{1}{\int_0^\infty 1/R'_{i,H} \cdot di} = R_H \cdot \frac{1}{\int_0^\infty \theta_{i,h}/\theta_{i,s} \cdot di}, \quad (13)$$

and

$$R'_L = \frac{1}{\int_0^\infty 1/R'_{i,L} \cdot di} = R_L \cdot \frac{1}{\int_0^\infty \theta_{i,h}/\theta_{i,s} \cdot di}. \quad (14)$$

The overall current through the memristor is the sum of the current through each filament:

$$I'(t) = \int_0^\infty I'_i(t) \cdot di. \quad (15)$$

The instantaneous memristance of the overall memristor can be defined as

$$M'(t) = \frac{V(t)}{I'(t)} = \frac{1}{\int_0^\infty 1/M'_i \cdot di}. \quad (16)$$

Since the doping front position movement in each filament will not be the same because h'_i varies due to TF (and/or the roughness of the electrode contact), we define the average doping front position of the whole memristor as:

$$\alpha'(t) = \frac{R'_H - M'(t)}{R'_H - R'_L}. \quad (17)$$

4. 3D MEMRISTOR MODELING

Analytic modeling is a fast way to estimation the impact of process variations on memristors. However, we noticed that in modeling some variations analytically, e.g. simulating the LER, may be beyond the capability of analytic model [12]. The data on silicon variations, however, is usually very hard to obtain simply due to intellectual property protection. To improve the accuracy of our evaluations, we create a simulation flow to generate 3-D memristor samples with the geometry variations including LER and thickness fluctuation. The correlation between the generated samples and the real silicon data are guaranteed by the sanity check of the LER characterization parameters. The flow is shown in Figure 3.

Many factors affecting the quality of the line edges show different random effects. Usually statistical parameters such as the auto-correlation function (ACF) and power spectral density (PSD) are used to describe the property of the line edges.

ACF is a basic statistical function of the wavelength of the line profile, representing the correlation of point fluctuations on the line edge at different position. PSD describes the waveform in the frequency domain, reflecting the ratio of signals with different frequencies to the whole signal.

Considering that LER issues are related to fabrication processes, we mainly target the nano-scale pattern fabricated by electron beam lithography (EBL). The measurements show that under such a condition, the line edge profile has two important properties: (1) the line edge profile in ACF figure demonstrates regular oscillations,

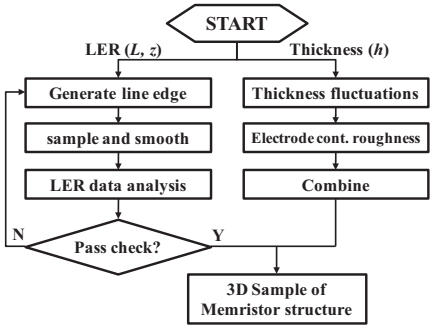

Figure 3: The flow of 3D memristor structure generation including geometry variations.

Table 2: The parameters/constraints in LER characterization.

Parameters		Constraints	
L_{LF}	0.8 nm	σ_{LER}	2.5nm $\sim$ 3.5nm
f_{max}	1.8 MHz	σ_{LWR}	4.0nm $\sim$ 5.0nm
L_{HF}	0.4 nm	Sk	0.1nm $\sim$ 0.2nm
/	/	Ku	2.5nm $\sim$ 3.5nm

which are caused by periodic composition in the EBL fabrication system; and (2) the line edge roughness mainly concentrates in a low frequency zone, which is reflected by PSD figure [12].

To generate line edge samples close to the real cases, we can equally divide the entire line edge into many segments, say, n segments. Without losing the LER properties in EBL process, we modified the random LER modeling proposed in [19] to a simpler form with less parameters. The LER of the i^{th} segment can be modeled by

$$\text{LER}_i = L_{LF} \cdot \sin(f_{max} \cdot x_i) + L_{HF} \cdot p_i. \quad (18)$$

The first term on the right side of Eq. (18) represents the regular disturbance at the low frequency range, which is modeled as a sinusoid function with amplitude L_{LF}. f_{max} the mean of the low frequency range derived from PSD analysis. Without loss of generality, a uniform distribution $x_i \in U(-1, 1)$ is used to represent an equal distribution of all frequency components in the low frequency range. The high frequency disturbances are also taken into account by the second term on the right side of Eq. (18) as a Gaussian white noise with amplitude L_{HF}. Here p_i follows the normal distribution $N(0, 1)$ [12]. The actual values of L_{LF}, L_{HF} and f_{max} are determined by ACF and PSD.

To ensure the correlation between the generated line edge samples with the measurement results, we introduce four constraints to conduct a sanity check of the generated samples:

- σ_{LER}: the root mean square (RMS) of LER;
- σ_{LWR}: the RMS of line width roughness (LWR);
- Sk: skewness, used to specify the symmetry of the amplitude of the line edge; and
- Ku: kurtosis, used to describe the steepness of the amplitude distribution curve.

The above four parameters are widely used in LER characterization and can be obtained from measurement results directly [12]. Only the line edge samples that satisfy the constraints will be taken as valid device samples. Table 2 summarizes the parameters used in our algorithm, which are correlated with the characterization method and experimental results in [12]. And Figure 4 shows the LER characteristic parameters distribution among 1000 Monte-Carlo simulations.

Even the main function has captured the major features of LER, it is not enough to mimic all the LER characteristics. The difference between real LER distribution and our modeling function results in the fact that some generated samples are not qualified compared to the characteristic parameters, or the constraints of the real LER profile. Thus, sanity check which screens out the unsuccessful results is necessary. Only those samples in red rectangles shown in Figure 4 satisfy the constraints and will be used for the device electrical property analysis. The criteria of the sanity check are defined based on the measurement results of real LER data.

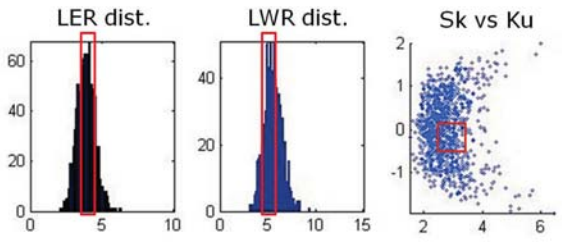

Figure 4: LER characteristic parameters distribution among 1000 Monte-Carlo simulations. Constraints are shown in red rectangles.

The thickness fluctuation is caused by the random uncertainties in sputter deposition or atomic layer deposition. It has a relatively smaller impact than the LER and can be modeled as a Gaussian distribution. Since the memristors in this work have relatively bigger dimensions in the horizontal plane than the thickness direction (shown in Table 1), we also considered roughness of electrode contact in our simulation: The means of the thickness of each memristor is generated by assuming it follows the Gaussian distribution. Each memristor is then divided into many filaments between the two electrodes. The roughness of electrode contacts is modeled based on the variations of the thickness of each filament. Here, we assume that both thickness fluctuations and electrode contact roughness follow Gaussian distributions with a deviation $\sigma = 2\%$ of thin film thickness.

Figure 2 is an example of 3D structure of a TiO_2 thin-film memristor generated by the proposed flow. It illustrates the effects of all the geometry variations on a TiO_2 memristor device structure. According to Section 3, a 2-D partition is required for the statistical analysis. In the given example, we partition the device into 25 small filaments with the ideal dimensions of $L = 10nm$, $z = 10nm$, and $h = 10nm$. Each filament can be regarded as a small memristor, which is affected by either only TF or both LER and TF. The overall performance of device can be approximated by paralleled connecting all the filaments.

5. IMPACT ON MEMRISTOR PROPERTIES

To evaluate the impact of process variations on the electrical properties of memristors, we conducted Monte-Carlo simulations with 10,000 qualified 3-D device samples generated by our proposed flow. A sinusoidal voltage source shown in Eq. (10) is applied as the external excitation. The initial state of the memristor is set as $M(\alpha = 0) = R_H$. The device and electrical parameters used in our simulations are summarized in Table 3. Both separate and combined effects of geometry variations on various memristor properties are analyzed, including:

- the distribution of R_H and R_L;
- the change of memristance $M(t)$ and $M(\alpha)$;
- the velocity of wall movement $v(\alpha)$;
- the current through memristor $i(t)$; and
- the I-V characteristics.

The $\pm 3\sigma$ (minimal/maximal) values of the device/electrical parameters as the percentage of the corresponding ideal values are summarized in Table 4. For those parameters that vary over time, we consider the variation at each time step of all the devices. The simulation results considering only either LER or TF are also listed.

Table 4 shows that the static behavior parameters of memristors, i.e., R_H and R_L, are affected in a similar way by both LER and thickness fluctuations. This is consistent to the analytical results

Table 3: TiO_2 memristor electrical parameters.

$R_L(\Omega)$	$R_H(\Omega)$	$\mu_v(\text{m}^2 \cdot \text{s}^{-1} \cdot \text{V}^{-1})$	V_m (V)	f (Hz)
100	16000	10^{-14}	1	0.5

Table 4: 3σ min./max. of TiO_2 memristor parameters

Sinusoidal Voltage	LER only		TF only		overall	
	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$
$R_H \& R_L$	-5.4	4.1	-5.5	4.8	-6.4	7.3
$M(\alpha)$	-5.4	4.1	-37.1	20.8	-36.5	24.1
$\alpha(t)$	0.0	0.0	-13.3	27.5	-14.7	27.4
$v(\alpha)$	0.0	0.0	-9.3	15.6	-10.4	16.9
$i(\alpha)$	-4.7	5.7	-9.3	15.7	-10.7	17.2
Power	-4.7	5.7	-8.8	14.1	-10.1	15.6

Square wave Voltage	LER only		TF only		overall	
	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$	$-3\sigma(\%)$	$+3\sigma(\%)$
$R_H \& R_L$	-5.3	3.7	-6.2	5.2	-6.6	6.9
$M(\alpha)$	-5.3	3.7	-17.8	13.2	-15.4	14.4
$\alpha(t)$	0.0	0.0	-12.1	16.6	-13.0	15.6
$v(\alpha)$	0.0	0.0	-11.6	17.7	-12.5	16.7
$i(\alpha)$	-4.0	5.2	-11.7	17.7	-12.6	17.6
Power	-4.0	5.2	-7.7	9.8	-8.5	10.1

in Eq. (13) and (14), which show that θ_s and θ_h have the similar effects on the variation of R'_H and R'_L.

However, thickness fluctuation shows a much more significant impact on the memristive behaviors such as $v(t)$, $\alpha(t)$ and $M(\alpha)$, than LER does. It is because the doping front movement is along the thickness direction: $v(t)$ is inversely proportional to the square of the thickness, and $\alpha(t)$ is the integral of $v(t)$ over time as shown in Eq. (5) and (6). For the same reason, thickness fluctuations significantly affect the instantaneous memristance $M(\alpha)$ as well.

Because the thickness of the TiO_2 memristor is relative small compared to other dimensions, we assume the doping front cross-section area is a constant along the thickness direction in our simulation. The impact of LER on $\alpha(t)$ or $v(t)$, which is relatively small compared to that of the thickness fluctuations, is ignored in Table 4.

An interesting observation is that as the doping front α moves toward 1, the velocity v regularly grows larger and reaches its peak at the half period of the sinusoidal excitation. This can be explained by Eq. (7): the memristance is getting smaller as α moves toward 1. With the same input amplitude, a smaller resistance will result in a bigger current and therefore a bigger variation on $v(t)$. Similarly, memristance $M(\alpha)$ reaches its peak variance when α is close to 1.

We also conduct 10,000× Monte Carlo simulations on the same samples by applying a square wave voltage excitation. The amplitude of the voltage excitation is ± 0.5V. The simulation results are also shown in Table 4. The results of the static behavior parameters, i.e., R_H and R_L, are exactly the same as those with sinusoidal voltage inputs because they are independent of the external excitations, The results of the memristive behavior parameters such as $v(t)$, $\alpha(t)$ and $M(\alpha)$ show similar trends as those with the sinusoidal voltage inputs. Based on Eq. (11), $\alpha(t)$'s variance is sensitive to the type and amplitude of electrical excitation, because $B(t)$ greatly affects the weight of the thickness fluctuation parameter. That is why the thickness fluctuation has a significantly impact on the electrical properties of memristors under sinusoidal and square voltage excitations.

6. A CASE STUDY

A memristor behaves similarly to a synapse in biological systems and hence can be easily used as the weighted connections in neural networks. Based on the memristor-based bidirectional synapse design, we implement a network serving as neuromorphic computing system with *units* (artificial neurons) and *weighted connections* (synapses). The neuron in this network is a binary threshold unit that produces only two different values to represent its state. A synapse works as a weighted connection to transmit a signal from

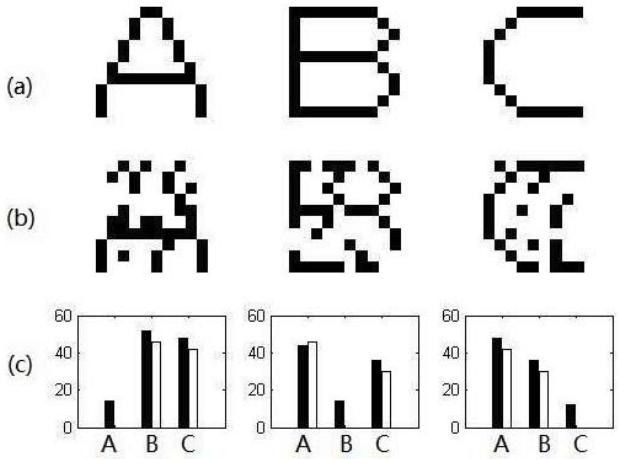

Figure 5: The neural network in pattern recognition: (a) the standard patterns; (b) the noised input patterns; (c) the comparison of the input noised images (black bars) or the output converged images (white bars) from their corresponding standard patterns.

one neuron to another. The activation function can be described as:

$$N_0 = \begin{cases} 1, & \text{if } \sum_{i=1}^{n}(N_i \times W_i) \geq threshold \\ 0, & \text{otherwise} \end{cases} \quad (19)$$

Here, the neuron N_0 collects signals from all the other neurons N_i through the weighted connections W_i. The state of N_0 could be *excitation* ($N_0 = 1$) or *inhibition* ($N_0 = 0$) that is determined by the relation between the summed weighted signals and the threshold. Here, we use bidirectional synapses in the design to build a fully connected neural network, in which any two connected neurons interact each other.

The proposed neural network can be used for pattern recognition: first, multiple standard input images are used to train the connection weights of the system till they reach convergence; after that, any input pattern will produce to a local minimum, which is a stable state corresponding to one the stored standard patterns. Such a network system can even be used to recognize the input image with defects.

In our experiment, we build a network with 100 (10×10) neurons and store the character images 'A', 'B' and 'C' shown in Figure 5(a) as the standard patterns. Each neuron in the network represents a pixel of the image. Then the defected images in Figure 5(b) are applied as inputs to initialize the network's state. Figure 5(c) show that each input has 13 defects compared to its corresponding stan-

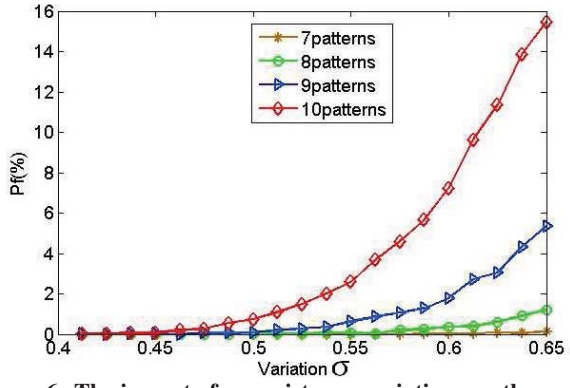

Figure 6: The impact of memristance variations on the probability of failure (P_f).

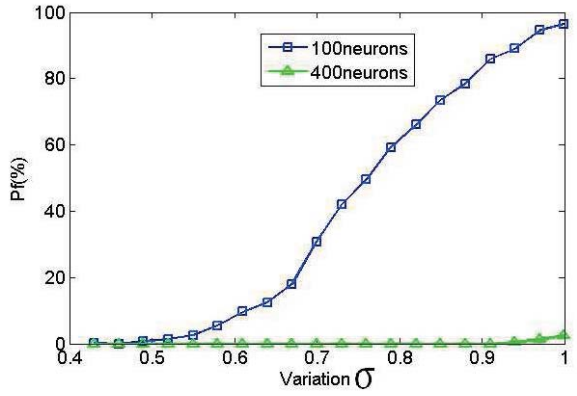

Figure 7: Increasing the network size can reduce P_f.

dard images (see black bars). The proposed system can completely eliminate the difference to zero and converge to one of the standard patterns, as demonstrated by the write bars in Figure 5(c).

The maximal allowed stored standard patterns (*capacity*) of this neural network design is determined by the amounts of neurons and connections. Moreover, the more patterns stored in the system, the higher precision of the connection weights is needed. Therefore, a large number of stored patterns and the high process variation on memristances will result in a higher failure probability (P_f).

To quantitatively evaluate the impact of memristance variations and robustness of the proposed neural network design, we conducted Monte-Carlo simulations for the network with 100 (10×10) neurons. Random variations following Gaussian distribution have been injected to the memristors. And σ is the standard deviation of the memristance. The system could fail to recognize the noised patterns or mismatch an input with other standard patterns due to the inaccurate connection weights. To test the failure probability under different conditions, we ran 10,000 Monte-Carlo simulations by varying the memristance variation σ when 7, 8, 9, or 10 patterns are stored in the system. In this experiment, each input image contain 21 defects among 100 pixels.

The simulation results in Figure 6 demonstrate that the proposed memristor-based neuromorphic system has a high tolerance on memristance variations. When $\sigma < 0.4$, which already exceeds the upper bound of memristance variation in Table 4, P_f of all the four configuration are close to the ideal condition at $\sigma = 0$. This indicates that even a large process variation exists in memristor devices, the performance of the proposed neuromorphic system is not affected much. Further increasing $\sigma > 0.5$, P_f grows significantly. As expected, under the same process variation condition, the system suffers a higher P_f when more patterns are stored.

For the same amount of stored patterns, a larger network with more neurons is more robust to process variations. Figure 7 compares the performance of the systems with 100 neurons (the blue line) and with 400 neurons (the green line). Both systems have 10 standard patterns. And the input defect rate remains at 21% for the two designs. The simulations show that the impact of process variations is smaller and therefore the required precision of connection weights is lower in a bigger network. Hence, in a neural network system design, the tradeoff between network capacity and robustness need to considered.

7. CONCLUSION

In this work, we evaluate the impact of geometry variations on the electrical properties of TiO_2-based memristors by conducting analytic modeling analysis and Monte-Carlo simulations. The responses of the static and memristive parameters under various process variations are evaluated and their implication for the electrical properties are analyzed. At the end, we propose a memristor-based neuromorphic computing system and use it as the case study of robustness analysis. Our experiment results show that the proposed design demonstrates high tolerance on process variation and input defects, which is consistent to the intrinsic property of neuromorphic systems.

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