REPORT DOCUMENTATION PAGE

Form Approved OMB NO. 0704-0188

1. REPORT DATE (DD-MM-YYYY)	2. REPORT TYPE	3. DATES COVERED (From - To)
	New Reprint	-

4. TITLE AND SUBTITLE
Development of MBE II–VI Epilayers on GaAs(211)B

5a. CONTRACT NUMBER
W911NF-09-2-0064

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER
611102

6. AUTHORS
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5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAMES AND ADDRESSES
Arizona State University
ORSPA
Arizona Board of Regents for Arizona State University
Tempe, AZ 85287 -6011

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
U.S. Army Research Office
P.O. Box 12211
Research Triangle Park, NC 27709-2211

10. SPONSOR/MONITOR'S ACRONYM(S)
ARO

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
54657-EL.3

12. DISTRIBUTION AVAILIBILITY STATEMENT
Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES
The views, opinions and/or findings contained in this report are those of the author(s) and should not contrued as an official Department of the Army position, policy or decision, unless so designated by other documentation.

14. ABSTRACT
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15. SUBJECT TERMS
HgCdTe, gallium arsenide, CdTe, IRFPA, II–VI semiconductors, MBE, large-area substrates

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	15. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			David Smith
UU	UU	UU	UU		19b. TELEPHONE NUMBER: 480-965-4540

Report Title

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REPORT DOCUMENTATION PAGE (SF298)
(Continuation Sheet)

Continuation for Block 13

ARO Report Number 54657.3-EL
Development of MBE II–VI Epilayers on GaAs(2 ...

Block 13: Supplementary Note

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Journal of ELECTRONIC MATERIALS, Vol. 41, No. 10, 2012
DOI: 10.1007/s11664-012-2218-z

Development of MBE II–VI Epilayers on GaAs(211)B

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Large-area, low-cost substrates are envisioned for next-generation HgCdTe infrared focal-plane arrays (IRFPA). Si, GaAs, Ge, and InSb have been previously examined as potential candidates. Fabrication of IRFPAs based on these substrates is limited by fundamental materials properties that potentially lead to lower detector performance and operability. Lattice and thermal mismatch between the substrate and epilayer are just two of several material factors that must be considered. We have reviewed these factors in the context of more recent data, and determined it worthwhile to revisit the use of GaAs substrates for epitaxial growth of HgCdTe. Our study starts with an evaluation of the surface quality (epireadiness) of commercially available (211) B-oriented GaAs substrates. Molecular beam epitaxial growth of CdTe buffer layers and subsequent HgCdTe absorber layers are performed in separate vacuum-interconnected chambers. The importance of optimization of the CdTe buffer layer growth for high-quality HgCdTe is detailed through surface morphology and x-ray studies. x-Ray diffraction rocking-curve full-width at half-maximum values as low as 52 arcsec have been obtained. Long-wave infrared $Hg_{1-x}Cd_xTe$ ($x = 0.23$) has been grown on these buffer layers, producing cross-hatch-dominated surface morphologies, with dislocation densities as low as $\sim 3 \times 10^6$ cm^{-2}. We have also obtained (for optimized layers), 80-K Hall-effect n-type carrier concentration and electron mobility of approximately $\sim 1.5 \times 10^{15}$ cm^{-3} and 1×10^5 cm^2 V^{-1} s^{-1}, respectively. Finally, we briefly compare GaAs and Si in light of our preliminary investigation.

Key words: HgCdTe, gallium arsenide, CdTe, IRFPA, II–VI semiconductors, MBE, large-area substrates

INTRODUCTION

Over 20 years of research[1–8] has been devoted to developing an alternative substrate to CdZnTe for heteroepitaxial growth of HgCdTe semiconductor alloys. High-density (>1 M pixels), dual-band detectors on large-area, low-cost, composite substrates have been targeted for next-generation infrared focal-plane arrays (IRFPAs). These substrates have included Si,[1–5] Ge,[6] GaAs,[7] and InSb,[8] each of which has inherent material properties that present significant obstacles for HgCdTe growth. The US Army Night Vision and Electronic Sensors Directorate (NVESD) has performed various studies on the use of these substrates to understand and to find methods to address fundamental materials issues.

The most challenging obstacle for Si, Ge, and GaAs substrates is that of lattice mismatch (−19%, −14%, and −14%, respectively) with the HgCdTe layer. Despite the relatively thick CdTe buffer layers (10 μm to 15 μm) initially grown on these substrates, the nominal threading dislocation (TD) density in the HgCdTe IR absorber layer is typically greater than 5×10^6 cm^{-2} as estimated by defect decoration etching.[8] While these TD densities can be tolerated

(Received February 14, 2012; accepted July 31, 2012; published online September 1, 2012)

by short- and mid-wavelength IR applications, they have been linked to higher dark currents and reduced detector operability for long-wavelength (LWIR) focal plane arrays.[9] For LWIR sensing, a TD density of 10^5 cm^{-2} or lower is highly desirable. Another materials property of concern for Si, Ge, and GaAs has been the thermal match (−92%, 14%, and 14%) with the buffer/absorber layers. The main finding of these studies suggests that thermal expansion mismatch has little effect on TD density, but is largely responsible for the residual stress characteristics.[10] The degree of lattice tilt (3° to 5°) in the heteroepitaxial layers has also been examined, with the observation that it is largely proportional to the lattice misfit.[11] With no obvious effect on the critical issue of high TD density, this factor may not be significant. Due to their nonpolar structures, Si and Ge substrate surfaces are typically terminated with As to achieve the preferred B-face orientation. Conversely, GaAs and InSb have zincblende crystal structures, such that the A or B face orientation is simply chosen. Therefore, InSb and GaAs have a distinct advantage in this respect. Of the four alternatives to CdZnTe discussed above, InSb is the only substrate that has near-perfect lattice and thermal matching to HgCdTe, in addition to having a zincblende structure. What has hampered its use is poor IR transmission properties and difficult surface preparation (i.e., nondestructive oxide removal is not easily achieved).[12] In addition, the threat of In diffusion must be addressed, since In is used as an *n*-type dopant in HgCdTe devices.

Of the alternative substrates described above, CdTe/Si has been the main focus of research at NVESD.[2,4,5,10] We have revisited the use of CdTe/GaAs composite substrates due to the availability of large-area (211)B wafers, and to recently reported progress in HgCdTe devices on GaAs platforms.[13] A potential advantage of GaAs(211)B over Si(211) is the ease of preparation. Since the GaAs native oxide can be removed at relatively low temperatures, all that is required for epitaxial growth is a high-quality surface polish. We have investigated bulk and surface properties of commercially available GaAs(211)B wafers. The CdTe/GaAs interface has been examined to determine the effect of residual polishing damage on epilayer growth. In addition, we provide a summary of HgCdTe and CdTe buffer layers in terms of MBE growth parameters, surface morphology, and crystallinity. Summaries for HgCdTe LWIR device layers are also provided in terms of morphology, crystallinity, cutoff wavelength (bandgap), and Hall-effect electron mobility and carrier concentration.

EXPERIMENTAL PROCEDURES

A two-pronged approach to investigating MBE HgCdTe/CdTe/GaAs has been initiated at NVESD. In the first case, CdTe and HgCdTe epitaxy are carried out in individual (VG-80) MBE chambers, both connected to an ultrahigh-vacuum ($<10^{-9}$ Torr) transfer tube. In the second case, CdTe and HgCdTe epitaxy are carried out in a single MBE chamber (Riber Compaq 21).[14] The dual-chamber approach (discussed in this work) may reduce contamination, in that the critical device layers are not subject to high-temperature steps used during growth of the CdTe buffer layers. The single-chamber approach limits handling, and thus may reduce defects caused by wafer transfer. However, the merits of these two approaches can be evaluated only after acquiring an especially large dataset, with metrics including defect densities and various contaminant concentrations.

Three-inch GaAs substrates are loaded, as-received, into the MBE chamber and heated to the native oxide desorption temperature (580°C) under an As_4 overpressure. The substrates are then cooled for a low-temperature CdTe nucleation step followed by an anneal. In an effort to encourage interaction and annihilation of threading dislocations, subsequent annealing cycles are implemented at regular intervals throughout the remainder of the CdTe growth. A typical cycle consists of 1 μm of CdTe deposition followed by Te-stabilized annealing for 5 min. Ramp rates were typically 0.5°/min. The CdTe thickness typically ranges from 9 μm to 13 μm. Substrate temperatures and other growth parameters (including thickness) have been examined and are discussed in greater detail below. After CdTe buffer growth, the CdTe/GaAs composite substrate is transferred *in vacuo* to a second MBE chamber for $Hg_{1-x}Cd_xTe$ growth. HgCdTe initiation takes place after a brief ~300°C anneal. The purpose of this step is to eliminate any species that may have adsorbed on the CdTe surface during vacuum transfer. A 1-μm- to 1.5-μm-thick MWIR buffer layer is grown, followed by a ~6-μm- to 8-μm-thick indium-doped LWIR absorber layer ($x = 0.23$). The intent of the MWIR buffer is to provide an intermediate lattice parameter, between the CdTe buffer and $Hg_{0.77}Cd_{0.23}Te$ absorber layers. Finally, a 0.5-μm-thick protective cap layer ($x \approx 0.3$) is grown. Spectroscopic ellipsometry is used during HgCdTe growth for control of composition and temperature.[4] The nominal HgCdTe growth temperature was 185°C. Reflection high-energy electron (RHEED) diffraction is used in both HgCdTe and CdTe epitaxy to monitor surface crystallographic structure. The importance and interpretation of evolving RHEED patterns during CdTe cyclic annealing have been recently reported.[15]

Ex situ characterization of GaAs, CdTe/GaAs, and HgCdTe/CdTe/GaAs structures have been carried out by several techniques. Surface morphologies were examined by Nomarski and atomic force microscopy. Near-surface chemistry was performed using x-ray photoelectron spectroscopy (XPS). Layer thicknesses and absorber layer composition were determined by Fourier-transform infrared (FTIR) spectroscopy, using a Nicolet AVATAR 370 IR spectrometer. The crystallinity of the epilayers was examined by x-ray rocking-curve full-width at half-maximum (RC-FWHM) measurements obtained using a Bede D1 x-ray diffractometer. Nanoscale

imaging via transmission electron microscopy (TEM), was obtained using a JEM-4000EX. Electron mobility and n-type carrier concentration were determined by 77-K Hall-effect measurements. It should be noted that actual surface temperatures during CdTe growth are expected to be lower than measured by the noncontact thermocouple as stated in this article.

RESULTS

We started our investigation by examining the quality of current commercially available GaAs(211)B. x-Ray RC-FWHM was used to assess the crystallinity of as-received wafers. The 3-inch wafers had an average value of $\sim 20 \pm 2$ arcsec, which is approximately 10 arcsec larger than GaAs wafers in the (100) and (111) orientations. This trend is consistent with commercially available Si and Ge wafers in the (211) versus the (100) orientation. Thus, to an extent, the relatively high-index (h,k,l) orientation contributes to the broadening of the x-ray line width. However, the x-ray line width might also be broadened by nanoscale roughness. Figure 1 shows atomic force microscopy (AFM) images for as-received (a) and chemical defect decorated (b)[16] GaAs. Polishing damage on a >5 nm scale is visible in Fig. 1a. From Fig. 1b, the observed etch pit density (threading dislocation density) was approximately $\sim 3 \times 10^3$ cm^{-2}, relatively consistent with that reported by the vendor.

We have also examined the chemistry before and after ramping up the GaAs substrate temperature for native oxide desorption. The common procedure is to carry out this step under an As_4 stabilizing flux (i.e., to prevent GaAs desorption). The beam-equivalent pressure used here is typically $\sim 2 \times 10^{-5}$ Torr as measured by an ion gage. Figure 2a and b show RHEED patterns of the GaAs(211) surface, as-received and after oxide desorption. The latter is the ideal pattern calculated for a (211) surface with electron beam direction along the ⟨110⟩ azimuth.[5] Surface analysis was performed in a vacuum-connected x-ray photoelectron spectroscopy (XPS) system. In Fig. 2c, XPS spectra are shown for the GaAs surface, as received and following the oxide desorption procedure. The complete elimination of the oxygen O 1s signal (after thermal desorption) indicates that chemical bonding of oxygen atoms is below the detection limit.

To investigate the effect of residual GaAs polishing damage on CdTe growth we performed cross-section TEM. CdTe/GaAs samples were cleaved, polished, and dimpled to achieve electron transparency at the CdTe/GaAs interface. Figure 3 shows a low-magnification bright-field image where the dense network of misfit, twinning, and threading dislocations produces significant diffraction contrast in the CdTe layer. For most lattice-mismatched heterostructures, the contrast in the epitaxial film will generally be highest near the interface with the substrate. Since the lattice-mismatch strain is disproportionately taken up by the epilayer, there is relatively little diffraction contrast in the substrate. Localized contrast observed near the top surface of the substrate is thus likely to be due to features inherent to the substrate. This is the case in Fig. 3a, where features near the GaAs surface are visible across a ~ 5-μm-wide region. A higher-magnification image (Fig. 3b) shows a ~ 150-nm-wide region where two "surface pits" are identified in the GaAs substrate. The voids in this image are as deep as 5 nm relative to the top surface, which is consistent with the apparent depth of polishing damage revealed by atomic force microscopy (Fig. 1a). The dark contrast surrounding the GaAs surface pits is indicative of defective CdTe growth. The semiperiodic contrast within the pits is due to moiré fringes that are caused by overlapping GaAs and CdTe crystal regions along the beam direction. Nonetheless, it should be noted that this defective growth does not appear to extend more than ~ 40 nm into the CdTe epilayer.

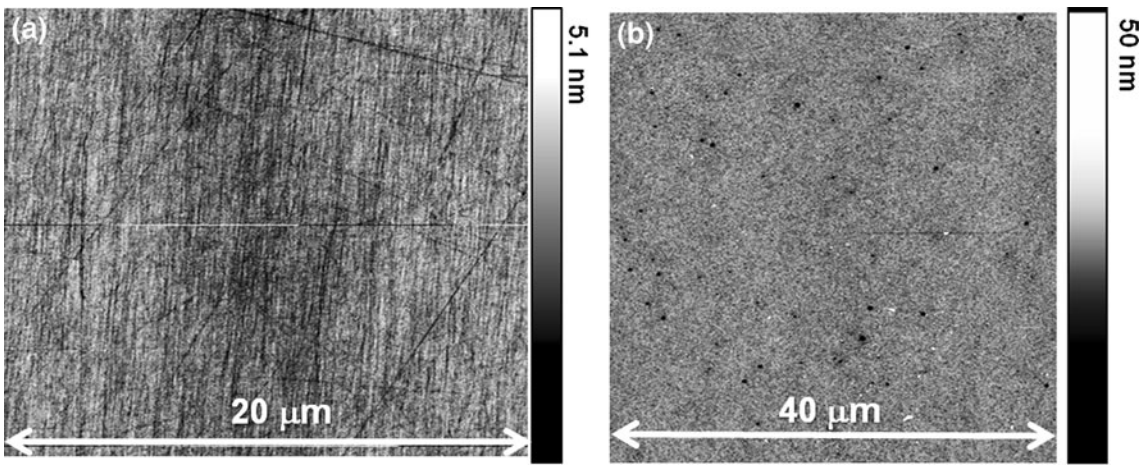

Fig. 1. AFM surface images of (a) as-received and (b) defect-decorated GaAs(211) wafer.

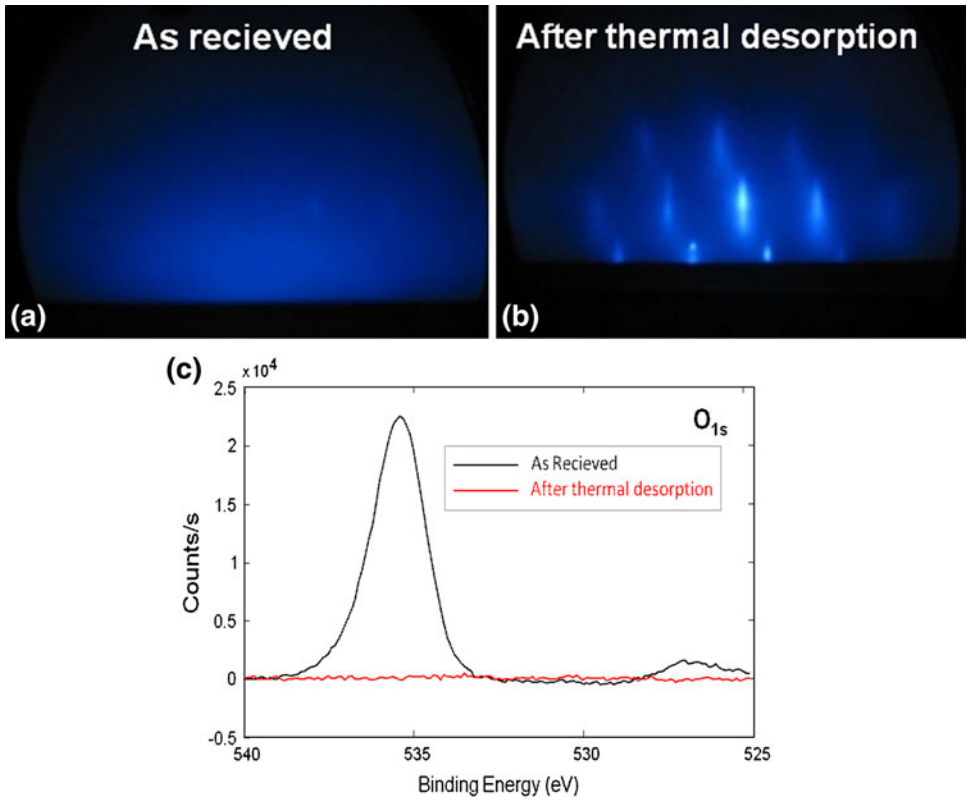

Fig. 2. RHEED patterns of GaAs(211): (a) as-received, and (b) after thermal oxide desorption. (c) XPS spectra showing the O 1s signal from the GaAs surface, as-received and after thermal desorption. XPS apparatus is vacuum-interlocked to the MBE chamber.

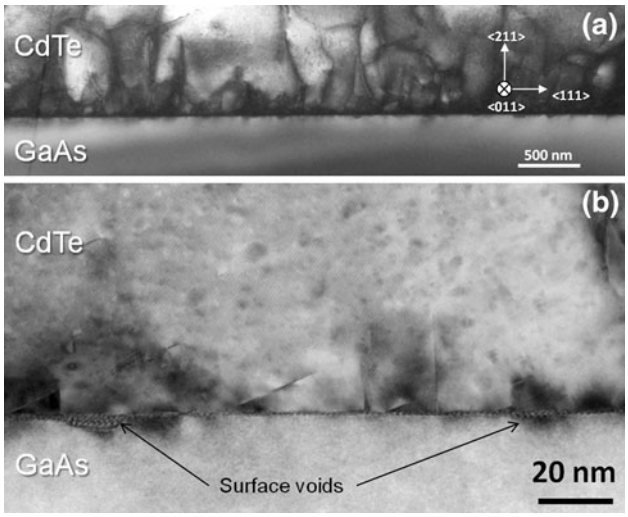

Fig. 3. Cross-section bright-field (BF)-TEM images of the CdTe/GaAs interface revealing top-surface GaAs defects possibly related to polishing damage on as-received GaAs(211) wafers (a). The higher-magnification image identifies polishing damage as "surface voids." The depth of the surface voids is similar to seen by AFM (Fig. 1a).

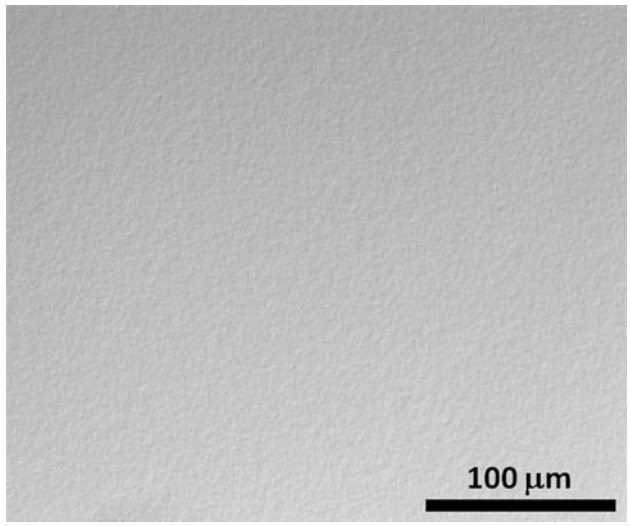

Fig. 4. Nomarski micrograph of CdTe/GaAs surface morphology.

The overall surface morphology of the MBE CdTe/GaAs buffer layers was examined by Nomarski microscopy. Figure 4 shows an image of an optimized buffer layer (growth details listed in Table I, run 41). At this magnification, the surface appears to be relatively featureless, and uniform over a 3-inch wafer. Based on atomic force microscopy measurements (not shown), the average surface roughness is 1.4 nm. Figure 5 shows an x-ray double-crystal rocking-curve (DCRC) FWHM map of an optimized CdTe/GaAs 3-inch wafer. A uniform FWHM of 68 arcsec has been measured throughout

Table I. Summary of selected CdTe/GaAs growth runs

Run no.	Growth Temp. (°C)[a]	Annealing Temp. (°C)[a]	Thickness (μm)	Growth Rate (μm h^{-1})	RC-FWHM (arcsec)
16	320–350	580	9.8	1.0	163
17	280/350	560	9.0	1.0	110
33	275/310	480	10.1	0.9	71
35	275/310	510	9.0	0.9	71
41	285/320	500	9.4	0.7	69
47	255/300	535	15.4	1.2	52

[a] Listed temperatures are based on non-contact thermocouple reading. Actual surface temperatures are expected to be lower.

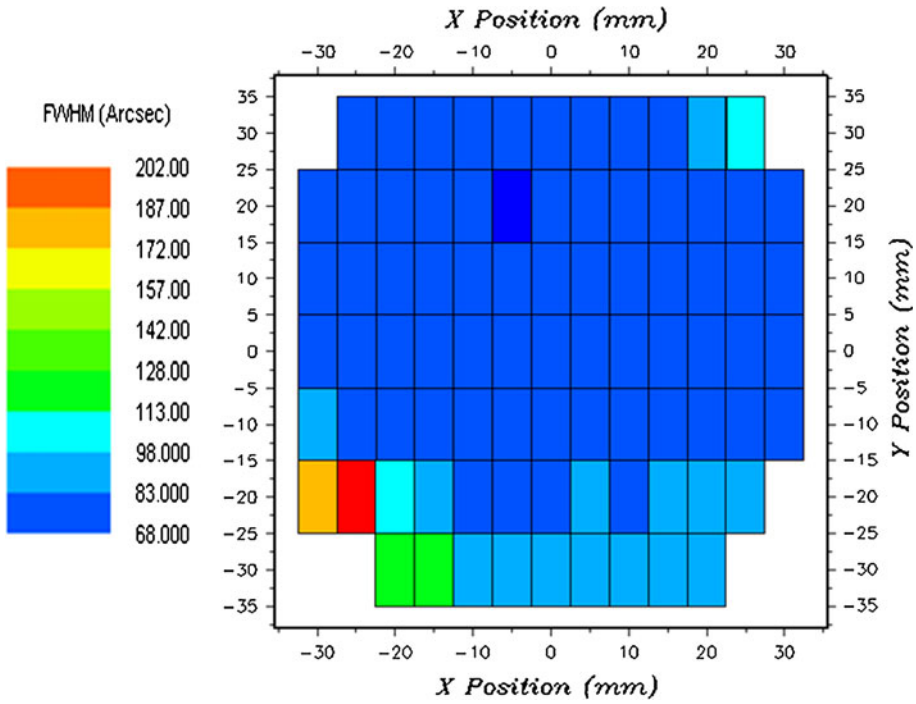

Fig. 5. x-Ray RC-FWHM map of optimal 3-inch CdTe/GaAs(211).

most of the CdTe buffer layer. Deviations from this average value are typically observed toward the edge of the wafer, and can be partially due to effects of wafer bowing. For typical 10-μm-thick layers, we observe relatively uniform ~60 arcsec over the full 3-inch wafer. The lowest value achieved at NVESD thus far is 52 arcsec (growth details listed in Table I, run 47). Based on cathodoluminescence (CL) images, the threading dislocation densities were in the range of high 10^6 cm^{-2} to low 10^7 cm^{-2} for the limited number of samples examined. It should be noted, however, that CL-based TD measurements are more likely to overcount (rather than undercount) TDs. This is due to the effective probe depth of the technique and existence of subsurface defects.[17,18]

Table I gives a summary of selected CdTe/GaAs growth runs including key MBE parameters. Most growth took place using low-temperature CdTe nucleation, annealing under a Te flux, followed by

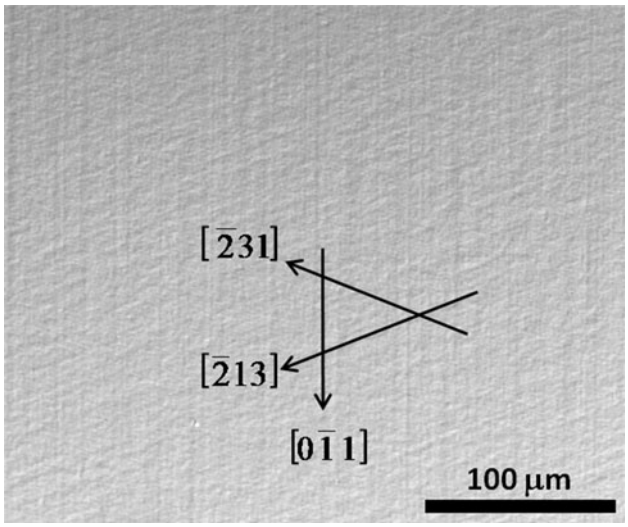

Fig. 6. Nomarski micrograph of HgCdTe surface morphology. Cross-hatch lines (indicative of smooth surfaces) are indicated.

Table II. Summary of selected consecutive HgCdTe/CdTe/GaAs growth runs

Run	CdTe Thick. (μm)	HgCdTe Thick. (μm)	RC-FWHM (arcsec)	FTIR x-value	EPD (cm^{-2})	80-K e-Mob. ($cm^2\ V^{-1}\ s^{-1}$)	Carrier Conc. (cm^{-3})
1	12.3	8.65	–	0.232	2.7×10^6	101,000	1.6×10^{15}
2	13.8	9.45	130	0.230	2.3×10^6	126,000	1.4×10^{15}
3	10.1	9.6	138	0.230	5.4×10^6	107,000	2.1×10^{15}
4	9.8	10.3	152	0.225	7.2×10^6	92,000	2.3×10^{15}

higher-temperature CdTe growth interrupted by periodic annealing. The intended purpose of low-temperature nucleation is to preserve the (211) growth orientation and potentially to "bury" residual GaAs surface defects under a thin amorphous-like layer. Based on RHEED, the crystallinity of this layer (nominally ~250 nm thick) gradually improves during growth and after a high-temperature anneal. This creates a better surface for subsequent CdTe deposition at our normal growth temperatures. For layer 16 in Table I, the temperature was gradually ramped from 320°C to 350°C during growth of the nucleation layer, and subsequent growth was carried out at the higher temperature. The crystallinity (RC-FWHM) of this layer was poor. It is possible that the nucleation layer lacked sufficient time to form and/or that the initial temperature was too high. We adopted a procedure in which the thin nucleation layer and CdTe layer were deposited at distinct temperatures (i.e., without gradual ramping). Of the growth parameters shown in Table I, the annealing and nucleation/growth temperature probably have the greatest influence on the epilayer crystallinity. Optimum buffer layers were achieved by using lower nucleation, growth, and annealing temperatures (run 47). The growth rate (within a 0.7 μm h^{-1} to 1.5 μm h^{-1} range) did not appear to have a measurable impact on RC-FWHM. The thickness dependence will be examined in a later study.

The surface morphology of MBE HgCdTe epilayers deposited on the CdTe/GaAs composite substrates was examined by Nomarski microscopy. Figure 6 shows an image of the HgCdTe surface, revealing cross-hatch line patterns. The origin of this cross-hatch morphology has been well characterized for (211)-oriented films.[19] Strain relief from lattice mismatch induces slip lines along the crystallographic directions indicated in the figure. These slip lines are not visible in surfaces roughened by hillocks and other defects. Therefore, a HgCdTe epilayer dominated by cross-hatch is indicative of a relatively smooth surface. The as-grown surface defect densities were typically ~1000 cm^{-2}. These defects primarily consist of discrete voids and tellurium precipitates. Optimum layers had threading dislocation densities as low as $\sim 2 \times 10^6$ cm^{-2}, determined by defect decoration etching.

Table II provides a summary of four consecutive HgCdTe/CdTe/GaAs growth runs. The target x-value was 0.23. This was monitored by spectroscopic ellipsometry and later examined by FTIR. The values show excellent agreement, suggesting good control of composition during growth. The RC-FWHM is typically ~130 arcsec. This higher value (compared with the underlying CdTe buffer layer) is likely due to the ~0.5-μm-thick cap layer atop the heterostructure. The small change in x-value between absorber and cap layers amounts to a slight change in lattice parameter that is not fully resolved in the x-ray (422) Bragg peak. Thus, the measured x-ray RC-FWHM essentially samples two lattice parameters, giving rise to deceptively high values.

Single-color, n-type HgCdTe layers were grown and examined by Hall-effect measurements at 80 K. Typical n-type carrier concentration and electron mobility were $\sim 2 \times 10^{15}$ cm^{-3} and 1×10^5 cm^0 V^{-1} s^{-1}, respectively, for a HgCdTe/GaAs sample with $x \approx 0.232$. The best values achieved for 80-K carrier concentration and electron mobility were 1.4×10^{15} cm^{-3} and 126,000 cm^2 V^{-1} s^{-1}. This provides sufficient material quality for subsequent device processing. Ensuing research efforts will involve fabrication of arsenic-implanted planar diodes in order to examine current–voltage characteristics.

CONCLUSIONS

We have performed an investigation of MBE HgCdTe/CdTe/GaAs(211), starting with an evaluation of commercially available GaAs(211)B substrates. While some polishing damage was revealed by AFM, it was confirmed by *in vacuo* XPS and RHEED that the surfaces were in fact "epiready." Cross-section transmission electron microscopy of the CdTe/GaAs interface confirmed the existence of residual GaAs polishing damage. Nonetheless, TEM images showed only shallow, localized defects in the CdTe epilayer associated with GaAs surface damage. The CdTe buffer layer growth procedure produced uniformly smooth surfaces over a 3-inch wafer, with RC-FWHM as low as 52 arcsec. State-of-the-art heteroepitaxial HgCdTe/CdTe/GaAs structures were achieved in a relatively short number of growth runs. HgCdTe cross-hatch morphology (indicative of high-quality surfaces) was demonstrated, and etch pit densities as low as 2.3×10^{-6} cm^{-2} were measured.

When compared with Si, it can be stated that GaAs sample preparation is considerably easier. The silicon native oxide requires chemical surface treatment for removal either outside or within the MBE vacuum chamber. GaAs can be loaded as-received, and the oxide is desorbed at readily accessible temperatures. While the as-received GaAs(211)B substrates have an inferior surface polish compared with Si(211), adequately smooth surface morphologies have been obtained for the deposited II–VI epilayers. On the other hand, we have not yet observed a distinct advantage with respect to threading dislocation densities in the HgCdTe layer. We also have not yet observed significant differences in 80-K Hall-effect characteristics (carrier concentration and electron mobility) for layers grown on GaAs and Si. Follow-on work will be focused on device fabrication using a planar implant architecture. Device characteristics for NVESD-fabricated diodes on Si(211) and GaAs(211)B will be the next step in performing a comparative study.

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