

A Comprehensive Surface Mount Technology Solution for Integrated Circuits onto Flexible Screen Printed Electrical Interconnects

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A Comprehensive Surface Mount Technology Solution for Integrated Circuits onto Flexible Screen Printed Electrical Interconnects

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II.**

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16.05.2014

Abstract

Mechanically flexible and one-dimensional electronic interconnects are nowadays a standard, enabling various applications, and offering a wide range of advantages. Taking planar one-dimensional flexible systems onto the next level of high-speed and high performance electronic systems, various efforts on connecting rigid integrated circuits (ICs), e.g. microcontrollers, batteries, sensors, actuators etc., to flexible interconnects exist. In this work, a comprehensive surface mount technology (SMT) for rigid and silicon dioxide based ICs onto flexible and glycol-modified Polyethylene Terephthalate screen-printed interconnects is developed. Here, the SMT solution addresses the following challenges: low thermal budget of Polyethylene Terephthalate, non-solderability of the screen-printed structures, aluminum coating of the IC, and small-sized pitches of the IC. Besides, various reliability aspects of the assembled electrical end product are investigated.

Index Terms

Electrical connector, conductive ink technology, low temperature, flip chip-on-flex, chip encapsulation, reliability testing

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I. INTRODUCTION

Mechanically flexible and one-dimensional electronic interconnects are nowadays a standard, enabling various applications such as invasive medical instruments ([2], [5]), and offering a wide range of advantages. In addition to reducing thermo-mechanical stresses within an electronic device [1], flexible interconnects allow high-density ([3], [4]) and compactness while ensuring lightweight [6].

Due to their acceptable thermal stability, Polyimides have established as a conventional substrate material for flexible interconnects, which can be metalized, for instance, by conventional high power sputtering and electroplating [17] or by lamination to metal foils [16]. Nevertheless, the demand for inexpensive polymers such as Polyethylene Terephthalate and Polycarbonate as part of cost-saving roll-to-roll manufacturing processes is continuously increasing. Since classical metallization processes mostly exceed the thermal budget of the aforementioned polymers, printing techniques and in particular screen printing of filled suspensions [18] allow the deposition of structured electrically conductive interconnects.

The world is moving towards the era of the internet of everything [21]. Intelligent and emotionally sensitive objects will surround every moment of our lives in order to complete our senses and enhance our performances. As we see some sparks of efforts appearing in the markets such as vending machines by mood, soft technology textiles [22] and electronic wallpapers ([23], [24]), there is still plenty to be established. Not only communication solutions but also inexpensive manufacturing processes and materials need to be developed in order to facilitate this transition as well. Consequently, taking planar one-dimensional flexible systems onto the next level of high-speed and high performance electronic systems becomes necessary.

Various efforts on connecting rigid integrated circuits (ICs), e.g. microcontrollers, batteries, sensors, actuators etc., to flexible interconnects exist. While the surface mount technology (SMT) clearly depends on the materials of the assembly, requirements on the end product remain the same, for instance mechanical bendability, thermal reliability and electrical functionality. So far, flip chip-on-flex systems have been realized by adopting flexible electrically conductive adhesives ([7], [8]), smaller chip sizes [10], thinned

ICs ([9], [11]) or by a combination of the above [12]. Embedding the assembled system into a sandwich structure enhances reliability of the chip-on-flex system, for instance by lamination or spin coating of a protective polymeric cladding onto a thinned IC [14]. Analogously to classical flip chip bonding onto organic printed circuit boards, underfilling and encapsulation play an important role in the reliable packaging of flip chip-on flex systems [15]. In the long run, rigid ICs will be replaced by printed components [13] moving towards homogeneously integrated systems.

Since handling of thinned ICs is known to be delicate and homogeneous integration is yet not possible for all kinds of components, the use of off-the-shelf and/or housed components of imposed size and material cannot be avoided. In the latter case, mismatches in coefficients of thermal expansion arise leading to a shorter lifetime of the assembly. Moreover, chemical incompatibility of substrate to component leads to some constraints in choosing the electrical bonding medium.

In this work, we aim at providing inexpensive and reliable flexible high-speed and high performance electronic systems. In particular, we target a roll-to-roll manufacturing process on inexpensive flexible films. Moreover, the end product is expected to be robust to environmental conditions and handling. Developing such a low-cost manufacturing technology would enable various applications such as electronic wallpapers (Fig. 1) as part of a security alarm system, flexible electrodes for wound mapping and flexible solar energy harvesting devices etc. Particularly, we develop a general SMT for rigid ICs onto screen-printed flexible and polymeric interconnects. We cope with the following challenges: low thermal budget of the polymer film, non-solderability of the screen-printed structures, aluminum coating of the IC and small-sized pitches of the IC. Then, we investigate various reliability aspects of the assembled end product.



Fig. 1. Electronic wallpaper (a two-dimensional distributed network of silicon ICs, spaced 25 mm apart, and screen-printed antennas) in a living room setting

II. ASSEMBLY COMPONENTS AND MATERIALS

A. Dummy ICs as a generalization for surface mount devices

In order to showcase the SMT solution for a variety of applications, silicon dioxide-based dummy ICs with crystal orientation $\langle 100 \rangle$ are used. The size of the IC chips is $4.25 \mu\text{m} \times 4.25 \mu\text{m} \times 600 \mu\text{m}$. Aluminum interconnects of around 600 nm are sputter deposited onto the silicon dioxide substrate. A layer of Chromium enhances adhesion between aluminum and silicon dioxide. By means of confocal microscopy and according to the measurement standards DIN EN ISO 4288:1998, the aluminum layer has a surface roughness represented by the arithmetic mean value R_a of $0.178 \mu\text{m}$. The latter is explained by the polished silicon dioxide surface, and the low thickness of aluminum.

The IC does have the sole functionality of electrical conductivity, and comes in four different designs (Fig. 2). Nevertheless, the pad size and the pad pitch are kept constant to be $530 \mu\text{m} \times 530 \mu\text{m}$ and $600 \mu\text{m}$, respectively. Moreover, the width of the interconnects is also kept constant at $250 \mu\text{m}$. Due to the dominance of the silicon material in the IC, the coefficient of thermal expansion of the IC is taken to be that of silicon, 3 ppm/K .

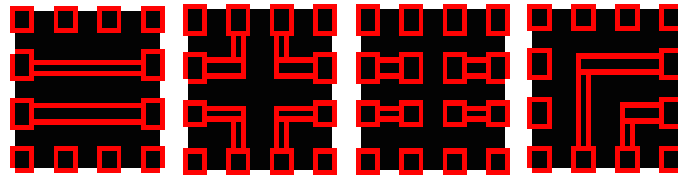


Fig. 2. Four interconnect designs of dummy ICs

B. Screen-printed interconnects onto flexible polymer film

The flexible substrate is a 75 μm glycol-modified Polyethylene terephthalate, which is characterized by a glass transition temperature of 150°C and a coefficient of thermal expansion of 38 ppm/K. Using an electrically conductive ink, corresponding circuitry to the dummy ICs is screen printed onto the polymer film and cured at 125 deg. C. for 20 minutes. The screen-printed coating is a silver micro-flake ink, which is thermally stable up to 200 deg. C. and resistant to scratching. The organic binder within the silver micro-flake ink promotes adhesion to the polymer film but also causes non-solderability (Appendix A: A Manufacturing Troubleshooter).

The screen-printed structures shrink due to the hard bake process remarkably in the thickness direction and also at the free surfaces. Due to evaporation of solvents and non-homogeneous shrinkage of the organic binder in the hard bake process, the free surfaces are inspected to be irregular. By means of confocal microscopy and according to the measurement standards DIN EN ISO 4288:1998, the screen-printed interconnects have a surface roughness represented by the arithmetic mean value R_a of 2.362 μm . After curing, the interconnects have an average thickness of 17 μm . Silver constitutes 80% of the screen-printed structures, and induces therefore low electrical resistance.

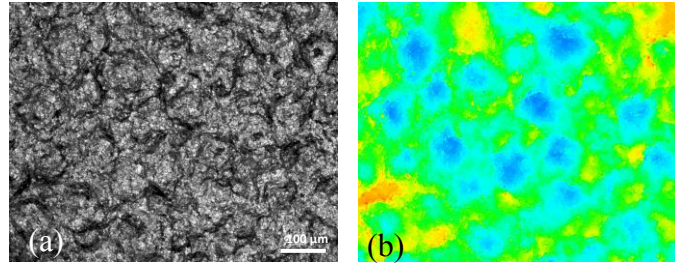


Fig. 3. Surface of screen-printed structures, laser intensity of surface structure (a), contour lines of surface structure (b)

III. SURFACE MOUNT TECHNOLOGY SOLUTION: METHODS OF MANUFACTURING

We demonstrate a SMT solution for the components presented in Section II. Due to non-solderability of the screen-printed coating, bonding by means of a thermally curing epoxy adhesive is chosen to assemble the IC to the flexible interconnects. We propose a SMT solution, which is conducted in the following chronological manner:

- A. Processing of aluminum interconnects of the IC,
- B. Dispensing of a snap-cure short circuit insulation between pads of the IC,
- C. Dispensing of a double stacked conductive epoxy between IC and flexible screen-printed interconnects,
- D. Micro-positioning of IC onto flexible screen-printed interconnects,
- E. Flip-chip bonding of IC onto screen-printed interconnects by means of thermo-compressive bonding or ultrasonic bonding,
- F. Moulding of a cylindrical non-filled underfill and encapsulation onto assembled IC.

A. Processing of aluminum

Aluminum oxide (Al_2O_3) grows on the sputter deposited aluminum due to storage of the ICs in ambient environment. The oxide layer, on one hand, decreases electrical conductivity from chip to substrate. On the other hand, hydroxyl groups form upon moisture absorption of the oxide layer and build links with polar groups present in the epoxy adhesive [19], and therefore, increase the strength of the adhesive joint.

Coping with the aforementioned trade-off, the aluminum surface is processed in order to decrease but not to completely diminish the thickness of the oxide layer. First, the IC undergoes an ultrasonic cleaning in an ethanol bath at room temperature and ultrasonic power of 50 Watts for 5 minutes. Then, the aluminum surface is blown dry with Nitrogen. Due to the thickness of the aluminum coating, the IC is dipped into a 30% hydrogen chloride (HCl) solution for 3-5 seconds, where $\text{Al}_2\text{O}_3 + 6 \text{HCl} = 2\text{AlCl}_3 + 3\text{H}_2\text{O}$. After etching, the IC is rinsed immediately in distilled water in order to dissolve aluminum chloride (AlCl_3). Then, the IC is blown dry with nitrogen to be immediately assembled. The processed aluminum layer is verified to exhibit a decrease of about 43% in average in electrical resistance compared to the non-processed aluminum layer.

B. Snap cure short circuit insulation

In this work, dispensing of the epoxy adhesive is done manually. Therefore, it is compulsory to avoid electrical connection between neighboring pads due to the expansion of the epoxy adhesive by capillary action or gravity. Therefore, and in order to allow long processing lags, an insulating mask of acrylated urethane is used. Functionality of the insulating mask is limited to a geometrical stopper during epoxy dispensing. Immediately after dispensing and preferably drop-by-drop in order to prohibit excessive flow, the acrylated urethane is snap cured by means of ultraviolet light (300-450 nm) at 3 W/cm^2 for 10 seconds (Fig. 4). Due to low surface roughness and therefore inhibited expansion of the epoxy adhesive, the insulating mask is placed onto the IC only. Moreover, in order to facilitate underfilling of the IC after assembly (Section III.E), no insulating mask is placed onto the polymer film.

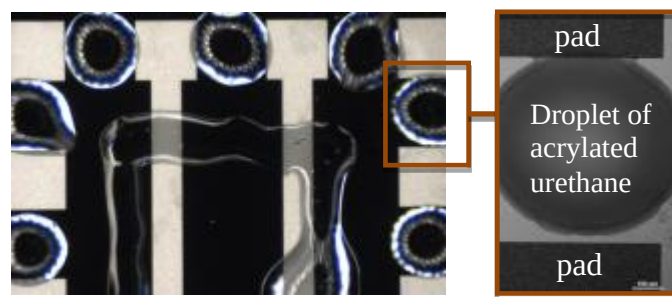


Fig. 4. Insulation mask between aluminum pads and interconnects

Planarity of the insulating mask is ensured by dispensing the same amount of acrylated urethane on each spot, and by immediate curing to maintain the original droplet thickness. In average, the height of the insulating mask is measured to be 165 μm . Here, the thickness profile along one plane of the insulating mask is given in Fig. 5. Since the application of this SMT is purely electronic, non-planarity can be tolerated to a higher extent, and compensated with the epoxy joints during flip-chip assembly. In the case of optical coupling onto the polymer film, planarity should be monitored rigorously, e.g. using shadow moire measurement techniques.

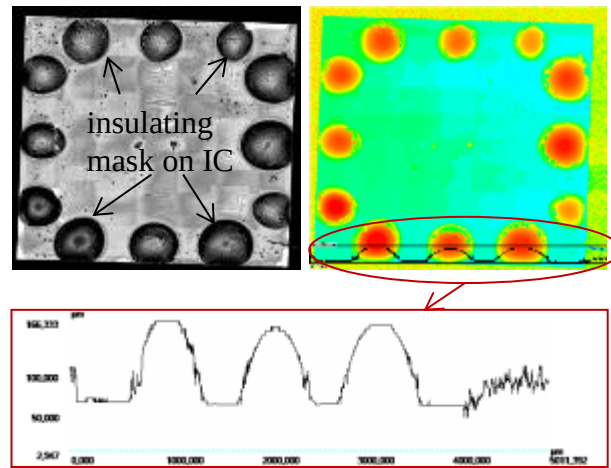


Fig. 5. Thickness profile of insulating mask

C. Double stacked epoxy joints

Since classical soldering, eutectic soldering and direct ultrasonic bonding are not possible, a two-component silver epoxy is used to bond the IC to the flexible interconnects. After curing, the epoxy exhibits 10 MPa in shear strength in average to both aluminum and the screen-printed interconnects, which is acceptable for an organic based adhesive according to the testing standards MIL-STD-883G.

Double or triple stacking of epoxy can create epoxy joints in the shape of an hourglass, having consequently an increased mean lifetime to failure [20]. In particular, we observe that the single stacked epoxy has a shear strength of 18 MPa per pad after assembly, in comparison to the double stacked epoxy that has a shear strength of 47 MPa per pad after assembly. Due to a larger surface area, the height of the epoxy joint allows most importantly for a larger thermal exchange. We implement the double-stacked

epoxy joint by dispensing and curing the epoxy on the IC, and flip-chip bonding the IC on uncured epoxy at the screen-printed side (Fig. 6). Furthermore, dispensing and curing the epoxy on each of the IC and the screen-printed interconnects and consequently flip chip bonding onto an uncured epoxy stack allow the implementation of a triple stacked epoxy joint.

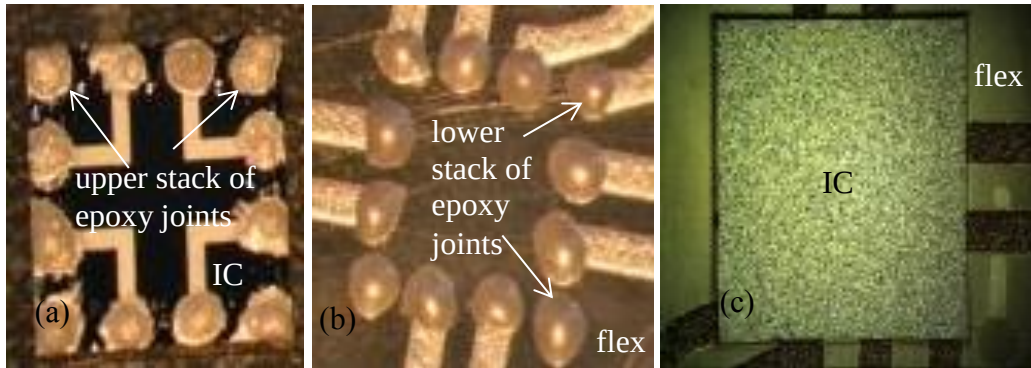


Fig. 6. IC after curing of epoxy (a), non-cured epoxy on screen-printed interconnects (b), IC flip-chip bonded to flexible interconnects.

D. Micro-positioning, thermo-compressive and ultrasonic flip-chip bonding

Using a die bonder with a sub-micron positioning precision, the IC is flip-chip bonded to the flexible interconnects at a compressive load of 10N per IC, i.e. a compressive pressure of 0.5 MPa. It is observed that higher loads push and flatten the non-cured epoxy, and lower loads do not exhibit sufficient contact between the components. Using a contact chip heating module, heating is applied to the chip and to the polymer as well in order to ensure homogeneous thermal distribution during flip-chip bonding.

Remarkably, the epoxy joints shrink during curing. In order to cope with the aforementioned artifact, chuck vacuum at the polymer side is completely omitted. Moreover, a drop of cyanoacrylate is dispensed onto the polymer film at the interface to the IC right before flip-chip bonding in order to enhance contact between the IC and the polymer during curing of the epoxy (Fig. 7).

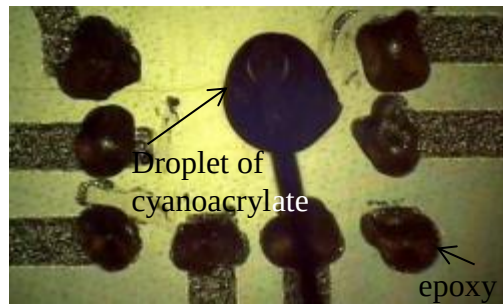


Fig. 7. Uncured epoxy and dispensing of cyanoacrylate onto screen-printed flex before flip-chip-bonding

Thermo-compressive curing (0.5 MPa, 150 deg. C at 20K/s, 15 minutes holding time) leads to 47 MPa shear strength per pad. Alternatively, ultrasonic bonding (0.5 MPa, 20 Watts, 4 seconds holding time, 150 deg. C., 20K/s) results in an average of 72 MPa shear strength per pad, and as importantly a decrease of 99.5% in assembly time. Notably, the properties of the cured epoxy do not depend on the bonding technique. Hence, the electrical resistance of the assembly does not differ. Ultrasonic bonding enhances reliability by enhancing interlocking of the epoxy and the screen-printed interconnects (Fig. 8). Besides, long thermal curing leads to a flow of the epoxy outside of the IC boundaries, and reduces the height of the epoxy joints.

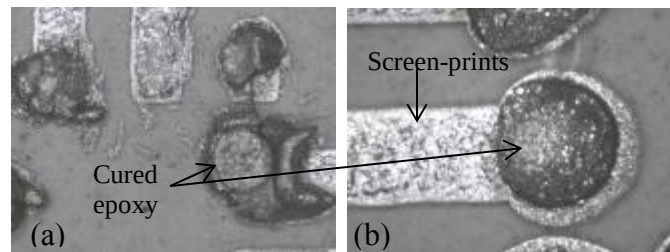


Fig. 8. Epoxy joints after shear test, assembly by means of thermo-compressive bonding (a), assembly by means of ultrasonic bonding (b)

E. Molded non-filled cylindrical underfill and encapsulation

A commercially available low temperature and clear two-component epoxy resin is used to underfill and encapsulate the IC. In order to minimize system warpage and not to damage the ICs, the epoxy resin is cured at 70 deg. C. for two hours. For the purpose of ensuring a cavityless encapsulation, the epoxy resin is

mixed and cured in a vacuum chamber at 100 mbar. The suitability of the epoxy resin to the assembly is characterized by the wetting behavior of the epoxy resin to polymer, IC and screen-printed ink. The wetting angle of the resin to the aforementioned components is indirectly specified by measuring the radius of a droplet of epoxy of an original radius of 300 μm after dispensing and settlement. According to the measurements listed in Tab. 1, wetting is established onto all components, preferably onto the polymer film. After curing, the epoxy resin exhibits high adhesion to the IC as well as to the polymer film.

	Back side of IC	Polymer	Screen-printed ink
Radius of epoxy resin droplet	690 μm	980 μm	950 μm

Tab. 1. Characterization of wetting of epoxy resin to IC, polymer film and screen-printed ink

In order to avoid stress concentrations, the underfill and encapsulation are molded onto the chip in a cylindrical shape using a moulding ring. The use of the ring is also beneficial in terms of limiting the expansion of the epoxy resin outside of the periphery of the IC. Accordingly, the underfill and encapsulation uniformly compensate for the high stresses within the epoxy joints due to material mismatches between the IC and the flexible substrate. For the silicon dioxide based IC described in Section II.A, a moulding ring with an inner diameter of 3.4 mm, an outer radius of 6 mm and a thickness of 2.1 mm is used. By keeping the inner diameter of the ring larger than the diagonal length of the chip, corner singularities of the chip are avoided. In order to facilitate demoulding, the circular ring is made of Polytetrafluoroethylene (PTFE). By making use of the lotus effect, the epoxy resin does not wet PTFE, and the ring can be removed effortlessly. Besides, the resin is non-filled, and remains elastic after the curing process. Consequently, demoulding does not damage the assembly.

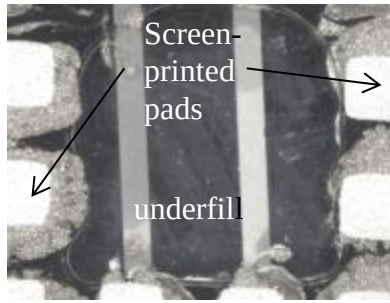


Fig. 9. Bottom view (through-polymer) of underfilled IC

Using capillary action, the region between IC and polymer is filled. Due to the presence of the short circuit insulation described in Section III.B, the epoxy resin does not fill the space between the joints (Fig. 9). The impact of the mismatch between acrylated urethane and the epoxy resin on the reliability of the assembly is studied in Section IV. Besides, the capillary action of the inner wall of the PTFE ring is favorable for flow of the epoxy resin. Therefore, the epoxy resin builds a convex parabolic upper surface centered in the middle of the top surface of the IC. The latter can be avoided or minimized by adjusting the height of the moulding ring to the height of the IC.

IV. SURFACE MOUNT TECHNOLOGY SOLUTION: METHODS OF RELIABILITY TESTING

Due to the symmetry of a distributed screen-printed film (e.g. as depicted in Fig. 1), reliability testing is conducted onto a single SMT unit of the size 30 mm x 60 mm. Since the SMT unit has free ends, worst-case reliability scenarios can be simulated [27]. We expect that the screen-printed film is to be handled in the shape of a roll, rolled and unrolled multiple times without operational deterioration. Moreover, the SMT unit should work under extreme environmental conditions such as high relative humidity. Besides, we assume that the IC components heat up to 80 deg. C. during operation. In order to verify the aforementioned assumptions, a population of five samples is used for each reliability test allowing for the deduction of a confident statement.

A. Bending cycling:

First, we expose the SMT unit to bending cycling for 15 consecutive hours with 57 bending cycles per minute, i.e. a total of 51300 bending cycles. Each bending cycle induces a bending offset of 20 mm of a

SMT unit as depicted in Fig. 11. The electrical resistance of the SMT unit is monitored using a 2-probe measurement setup (Fig. 10) having a measurement error of $\pm 0.4\%$. In order to constrain the recorded change in electrical resistance to the region of the IC, the probes are mounted at an offset of 10 mm from the IC. Moreover, we investigate two bending configurations (Fig. 11): (a) bending direction towards the chip, and (b) bending direction away from the chip.

The SMT unit passes the test, if electrical resistance during bending does not change by more than 5%. Moreover, no permanent change in electrical resistance should be recorded after the end of the bending cycling test. Also, no mechanical delamination of encapsulation should be observed.

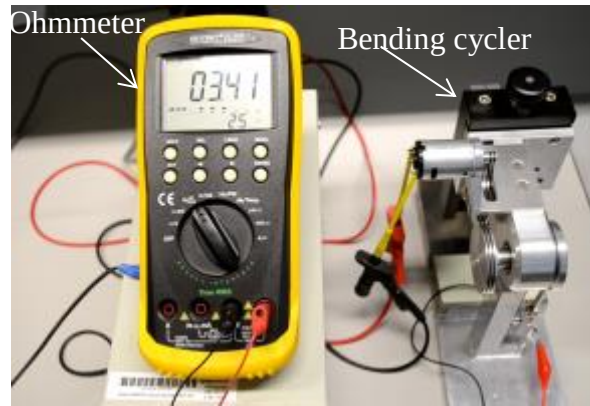


Fig. 10. Bending and resistance measurement setup

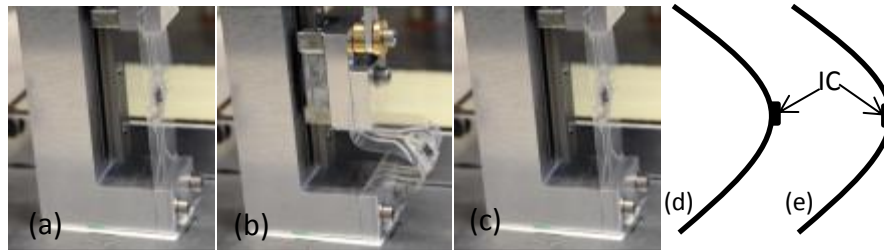


Fig. 11. Bending cycle: start of cycle (a), half cycle (b), end of cycle (c). Bending towards IC (d). Bending away from IC (e).

B. Hygro-thermal testing:

Next, we investigate the reliability of the SMT unit under severe environmental conditions. In particular, we conduct a hygro-thermal analysis of the assembly. In a climate chamber with constant relative humidity of 90%, we cycle chamber temperature between room temperature and peak temperature of the IC, i.e. 80

deg. C. Decreasing and increasing the temperature occurs at 5 K/min. Minimum and maximum temperatures are held constant for 30 minutes. Consequently, the duration of one hygro-thermal cycle is 1.3 hours. Electrical resistance is measured using a 2-probe setup having a measurement error of $\pm 0.4\%$.

The SMT unit passes the test, if no permanent change in electrical resistance is recorded after the end of the hygro-thermal testing. Besides, no chemical degradation of encapsulation should be observed.

C. Thermo-shock cycling:

Last, in order to verify the operation of the assembly at peak temperatures of the ICs, thermo-shock cycling according to the testing standards MIL-STD-883A is conducted. Fifty cycles of heating from -60 deg. C. to +88 deg. C. and cooling from +88 deg. C. to -60 deg. C. are conducted. Temperature shocks are performed within 10 seconds by lifting the samples from the hot chamber to the cool chamber, and vice versa. Each of the peak temperatures is kept constant for 20 minutes. Consequently, the duration of one cycle is about 40 minutes. While in Section III.B the insulating mask was tested according to the aforementioned standards, each of the individual materials described in Section II and III is analogously tested. Last, the complete assembly is subject to thermo-shock cycling. The SMT unit passes the test, if no permanent change in electrical resistance is recorded after the end of the hygro-thermal testing. Here, electrical resistance is measured using a 2-probe setup having a measurement error of $\pm 0.4\%$. Besides, no chemical degradation of encapsulation should be observed.

D. Chemical inertness to cleaning agent:

In order to determine an appropriate cleaning agent for all components and materials used in the SMT solution, all components are immersed in an ethanol (C_2H_6O) bath for 72 consecutive hours. The SMT unit passes the test, if no chemical, mechanical and electrical degradation are recorded.

V. RESULTS

In summary, the SMT unit did pass the reliability tests described in Sections IV.A, IV.B, IV.C and IV.D. During bending, the assembly bends harmonically without any impairment of electrical functionality. Also,

warpage of the residual system was not recorded. Due to the high adhesive strength of underfill and encapsulation to both of the IC and the polymer film, polymer and IC follow each other during bending. In the absence of underfill and encapsulation, the polymer film would be able to bend freely, whereas the IC would not be able to follow. Consequently, the epoxy joints would fail due to induced stresses above the ultimate strength of the epoxy material.

An absolute maximum of 0.8% of change in electrical resistance was recorded during bending for both bending configurations. No residual change in electrical resistance (Tab. 2) and no delamination of the encapsulation were observed at the end of bending cycling.

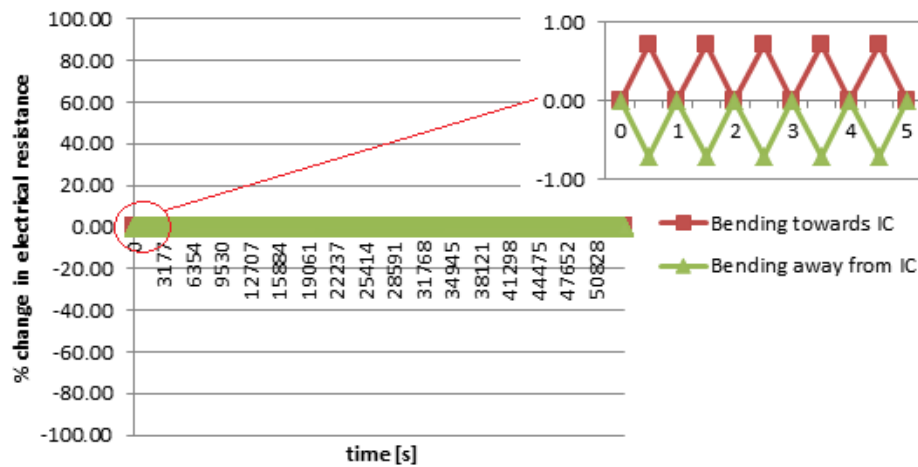


Fig. 12. Recording of % change in electrical resistance of assembly during bending cycling

In terms of hygro-thermal testing, no chemical degradation (Fig. 13) and no electrical impairment of the entire population were recorded after five hygro-thermal cycles (Tab. 2).

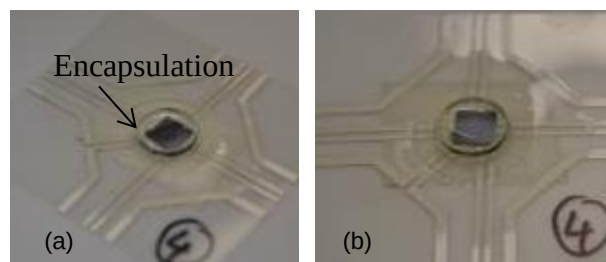


Fig. 13. SMT unit before (a) and after (b) hygro-thermal testing

Individually, but also interplaying with the other materials within the overall assembly, the thermal shock cycling did not lead to any electrical deterioration and in particular no increase of electrical resistance (Tab. 2). Also, a residual system warpage was not traceable. Most importantly, no delamination of the insulating mask from the underfill was observed.

	% residual change in electrical resistance
Bending cycling	0.0
Hygro-thermal testing	0.5
Thermal shock cycling	0.4
Error of measurement setup $\pm 0.4\%$	

Tab. 2. % residual change in electrical resistance after reliability testing

In terms of chemical inertness, ethanol C_2H_6O was identified as a compatible chemical agent for all materials described in Section II and III. No chemical, mechanical and electrical degradation were recorded.

VI. DISCUSSION

In this work, a conventional conductive epoxy adhesive was chosen as a bonding medium. Due to the latter reason and due to the use of the silver flake ink for the screen-printed interconnects, the assembled unit fulfills biocompatibility requirements in a limited manner ([29], [30]). Even though biocompatibility of substrate [31] is fulfilled, toxicity of the insulating mask [32] and encapsulation need to be considered

carefully, when implemented within biomedical applications.

Instead of a thermally curing epoxy, the use of an ultraviolet-curing epoxy adhesive is also possible. However, ultraviolet-transmissibility of the ICs in the case of vertical ultraviolet-light emission and UV-light reachability in the case of side-coupled ultraviolet-light emission need to be satisfied.

Instead of droplet dispensing of the insulating mask and/or the conductive epoxy adhesive, another method (e.g. screen-printing techniques or thin-film technology) might be worth exploring for large scale manufacturing purposes.

In this work, dummy ICs were processed as is, and therefore smaller sizes of the IC are readily possible. When increasing the size (thickness and contact area) of the IC, the encapsulation adds to the local weight of the assembled region, and represents a limitation to this SMT procedure.

If implemented in sandwich structures, laminating of cladding and/or functional films onto the assembled ICs by means of the presented method need to consider the cylindrical shape of the encapsulation.

The slow curing process of the encapsulation constitutes 65% of the entire SMT time. The latter is considered incompatible with large scale manufacturing. Therefore, the use of a snap-cure UV-curable system is considered to reduce the processing time significantly.

VII. SUMMARY

In this work, a cost-efficient implementation of a flexible screen-printed high-speed and high performance electronic systems is considered, where a distributed network of ICs are to be surface mounted to a screen-printed polymer film. In this context, and applicable to a wide range of flexible electronic systems, an efficient SMT solution for rigid dummy ICs of arbitrary size onto flexible, polymer-based and screen-printed interconnects was demonstrated. Notably, the SMT procedure was conducted under ambient conditions and without special processing of the rigid ICs. The SMT procedure comprised of four steps:

- A. Dispensing of a snap-cure short circuit insulation between pads of the IC,
- B. Dispensing of a double stacked conductive epoxy between IC and flexible screen-printed

interconnects,

- C. Micro-positioning and flip-chip bonding of IC onto flexible screen-printed interconnects by means of thermo-compressive bonding or ultrasonic bonding, and
- D. Moulding of a cylindrical non-filled underfill and encapsulation onto assembled IC.

Here, the SMT solution addressed the following challenges:

- A. Low thermal budget of the polymer film,
- B. Non-solderability of the screen-printed structures,
- C. Aluminum coating of the IC, and
- D. Small-sized pitches of the IC.

Most importantly, various reliability aspects of the assembled electronic unit by means of the aforementioned SMT solution were investigated. In particular, non-deteriorating electrical functionality under thermal shock cycling, hygro-thermal testing and bending cycling were verified. Last, ethanol was identified as a compatible chemical agent for the overall assembly.

APPENDIX A: A MANUFACTURING TROUBLESHOOTER

Q: Why not use a solder paste instead of an epoxy conductive adhesive?

A: A tin silver solder paste is used to solder the IC to interconnects, since the screen-printed interconnects are based on silver flakes. The reflow process fails, and the evaporation of the flux and the remnants of Sn and Ag particles on the interconnects are observed (Fig. 14). In the case of the IC, despite processing of aluminum as described in section III III.A, the solder paste does not wet the aluminum (Fig. 15). After reflow, the solder paste is observed to become shiny and concave. However, the solder balls can be easily lifted from the Aluminum pads, for instance using tweezers.

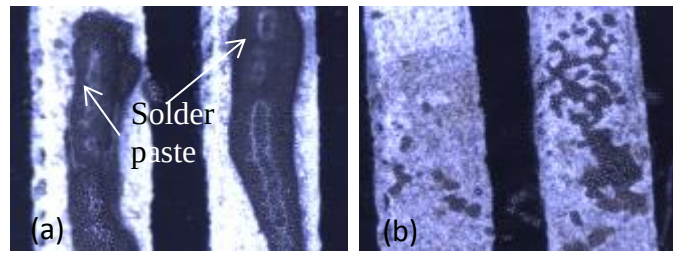


Fig. 14. Non-wetting of tin silver solder paste to screen-printed interconnects, solder paste after dispensing (a), solder paste after reflow (b)

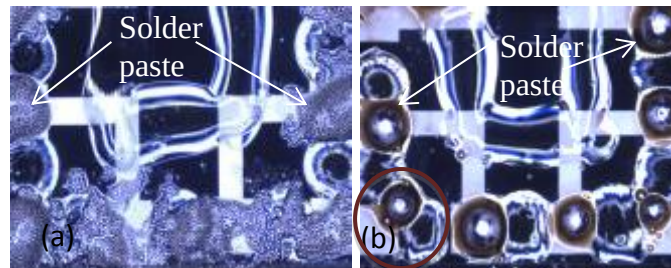


Fig. 15. Non-wetting of tin silver solder paste on IC, solder paste after dispensing (a), solder paste after reflow process (b).

Q: Why not use a low-temperature solder instead of an epoxy conductive adhesive?

A: An indium tin eutectic compound, a low-temperature solder, is chosen to solder the screen-printed interconnects. Indium is among a couple of other metals that is able to wet some organic materials but also aluminum [28]. Nevertheless, it was easily possible to peel off the indium tin compound after soldering, which is an indication for non-wetting (Fig. 16).

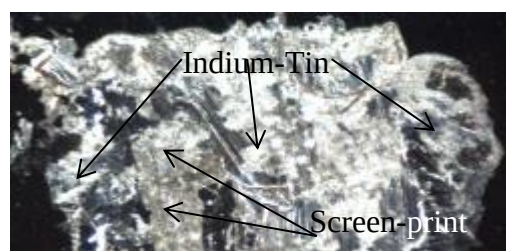


Fig. 16. Peeling-off of indium tin eutectic from screen-printed interconnects after reflow.

Q: Why not employ direct ultrasonic bonding to bond the IC to the screen-printed interconnects?

A: Ultrasonic bonding of some plastics to certain metals is possible, and is triggered by a mechanical interlocking of the plastic to the metal or vice versa. Here, the screen-printed interconnects have a rougher surface than the aluminum pads. Interlocking of aluminum into the rough screen-printed interconnects would not be possible due to the higher melting temperature of aluminum. Fig. 17 depicts the result of the ultrasonic bonding of the screen printed surface to the sputtered aluminum at 20 Watts and 10 N per IC, i.e. 0.5 MPa, for 4 seconds. Due to mechanical vibration, the screen-printed material cracks, breaks and scratches the aluminum surface. Lower ultrasonic powers lead to the same result. Higher ultrasonic powers are not supported by the equipment used in this work.

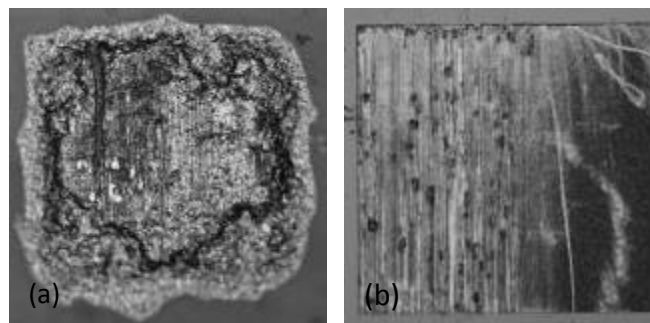


Fig. 17. Direct ultrasonic bonding of aluminum pad to screen printed pad, screen printed pad after bonding attempt (a), aluminum pad after bonding attempt (b)

Q: Why is the insulating mask peeling off?

A: The insulating mask is made of acrylated urethane, which is not heat resistant for temperatures higher than 100 deg. C. Moreover, it exhibits a mismatch of thermal expansion of 135 ppm/K to the IC and 100 ppm/K to the flexible substrate. Thermo-shock cycling according to the testing standard MIL-STD-883A confirms the aforementioned statement (Fig. 18). Therefore, the mask cannot be considered as a mechanical support to the assembly. In order to enhance adhesion of the acrylated urethane to silicon dioxide, a dehydration process of the ICs need to be conducted right before dispensing. In particular, silicon

dioxide chips are dehydrated at 100 deg. C. for 2 minutes on an open heating plate, and cooled down to 35 deg.C. on a metal plate.

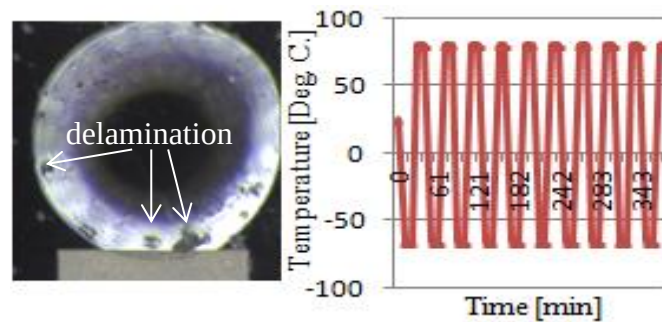


Fig. 18. Delamination of an acrylated urethane droplet after thermo-shock cycling

Q: Why is the encapsulation resin expanding under the moulding ring?

A: Due to the light-weight of the PTFE ring, a slight amount of epoxy resin flows under the ring during the curing process (Fig. 19). While this artifact does not inhibit demoulding, a thin epoxy coating extends the effective area of the encapsulation. Moreover, the low pressure environment does not completely outgas the air bubbles under the ring once polymerization starts. Therefore, a compressive load should be applied onto the ring in order to prevent the PTFE ring from floating and the epoxy resin from expanding.

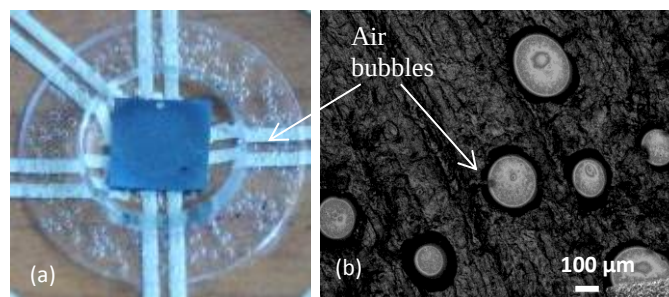


Fig. 19. Air bubbles caught within epoxy resin under ring (a), detailed view of air bubbles (b)

Q: Why is demoulding of the encapsulation not working properly?

A: Polymerization of the epoxy resin continues after the curing process in room temperature. Hence, when waiting too long after the curing process, the epoxy resin exhibits a larger hardness and demoulding might damage the assembly. One most occurring failure mode is a complete lift-off at the weakest link of the

assembly, which is the interface between polymeric substrate and screen-printed ink (Fig. 20).

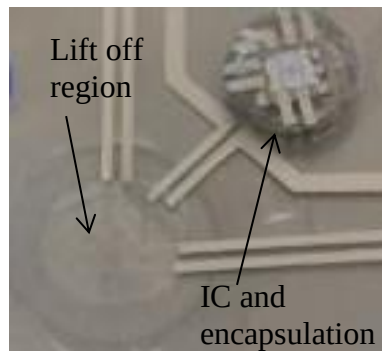


Fig. 20. Example of demoulding failure due to hardness of underfill: lift off of screen printed interconnects

REFERENCES

- [1] Hyung Suk Yang and Muhannad S. Bakir, “3D integration of CMOS and MEMS using mechanically flexible interconnects (MFI) and through silicon vias,” in IEEE ECTC, Las Vegas, NV, 2010, pp. 822-828.
- [2] Jeyakumar Subbaroyan and Daryl R. Kipke, “The role of flexible polymer interconnects in chronic tissue response induced by intracortical microelectrodes – a modeling and an in vivo study”, in IEEE EMBS, New York City, NY, 2006, pp. 3588-3591
- [3] Joerg-Uwe Meyer, Thomas Stieglitz, Oliver Scholz, Werner Haberer, and Hansjoerg Beutel (2001, Aug.). High density interconnects and flexible hybrid assemblies for active biomedical implants“, in IEEE Trans. on Advanced Packaging [Online], 24(3), pp. 366-374. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=938305>
- [4] Jason O. Fiering, Peter Hultman, Warren Lee, Edward D. Light and Stephen W. Smith (2000, May). “High-density flexible interconnect for two-dimensional ultrasound arrays”, in IEEE Trans. on Ultrasonics, Ferroelectrinc, and Frequency Control [Online], 47(3), pp. 764-770. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=842067>

- [5] Ki-Tae Park and Masayoshi Essahi (1999, Dec.). “Multilink active catheter with polyimide-based integrated CMOS interface circuits”, in Jour. Of MEMS [Online], 8(4), pp. 349-357. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=809048>
- [6] Thomas Stieglitz, Hansjoerg Beutel and J.-Uwe Meyer (2000, June). “Microflex – A new assembling technique for interconnects”, in Journal of Intelligent Material Systems and Structures [Online], 11(6), pp. 417-425. Available: <http://jim.sagepub.com/content/11/6/417.full.pdf+html>
- [7] Rongwei Zhang, Yiqun Duan, Wei Lin, Kyoung-Sik Moon, C. P. Wong, “New electrically conductive adhesives (ECAs) for flexible interconnect applications” in 59th IEEE ECTC, San Diego, CA, 2009, pp. 1356-1360.
- [8] Rongwei Zhang, Kyoung-sik Moon, Wei Lin, Josh C. Agar, Ching-Ping Wong, (2011, Feb.), “A simple low-cost approach to prepare flexible highly conductive polymer composited by in situ reduction of silver carboxylate for flexible electronic applications”, in Composites Science and Technology [Online], 71(4), pp. 528-534. Available: <http://www.sciencedirect.com/science/article/pii/S0266353811000297>
- [9] Kevin Y. Chen, Robert L. D. Zenner, Michael Arneson, and David Mountain, (2000, Feb.), “Ultra-thin electronic device package”, in IEEE Trans. on Advanced Packaging [Online], 23(1), pp. 22-26. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=826758>
- [10] John D. Prymak and Jim Bergenthal, (1995, March), “Capacitance Monitoring while Flex Testing”, in IEEE Trans. On Components, Packaging and Manufacturing Technology [Online], 18(1), pp. 180-186. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=370753>
- [11] K. Hungar and W. Mokwa, (2008, Jan.), “Gold/tin soldering of flexible silicon chips onto polymer tapes”, in Journal of Micromechanics and Microengineering [Online], 18 (6), pp. 1-7. Available: <http://iopscience.iop.org/0960-1317/18/6/064002>

- [12]Erwin Yacoub-George, Andreas Drost, Dieter Hemmetzberger, Dieter Bollmann, Robert Faul, and Karlheinz Bock, "Interflex: challenges and solutions to fabricate a double-sided wiring layer for a "system in foil", in SSI, Vienna, Austria, 2014, pp. 131-138.
- [13]Tsuyoshi Sekitani, Hiroyoshi Nakajima, Hiroki Maeda, Takanori Fukushima, Takuzo Aida, Kenji Hata, and Takao Someya, (2009, May), "Stretchable active-matrix organic light emitting diode display using printable elastic conductors", in Nature Materials [Online], 8, pp. 494-499. Available: <http://www.nature.com/nmat/journal/v8/n6/pdf/nmat2459.pdf>
- [14]E. Bosman, G. Van Steenberge, B. Van Hoe, J. Missine, J. Vanfleteren and P. Van Daele , (2010, March), "Highly reliable flexible active optical links", in IEEE Photonics Technology Letters [Online], 22 (5), pp. 287-289. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5378595>
- [15]R.A. Filion, B. Burdick, P. Piacente, L. Douglas, D. Shaddock and R. Saia, "Reliability Evaluation of Chip-on-Flex CSP devices," in International Conference on Multichip Modules and High Density Packaging, Denver, CO, 1998, pp. 242-246.
- [16]A.K.S. Ang, E.T. Kang, K.G. Neoh, K.L. Tan, C.Q. Cui and T.B. Lim, (2000, Jan.), "Low-temperature graft copolymerization of 1-vinyl imidazole on polyimide films with simultaneous lamination to copper foils", in Polymer [Online], 41 (2), pp. 489-498. Available: <http://www.sciencedirect.com/science/article/pii/S0032386199001810>
- [17]Syh-Ming Ho, Tsung-Hsiung Wang, Han-Lung Chen, Ker-Ming Chen, Syh-Ming Lian and Aina Hung, (2003, Mar.), "Metallization of polyimide film by wet process", in Journal of Applied Polymer Science [Online], 51 (8), pp. 1373-1380. Available: <http://onlinelibrary.wiley.com/doi/10.1002/app.1994.070510803/pdf>
- [18]Weiwei Yin, Dong-Hyun Lee, Jaesoo Choi, Chinho Park and Sung Min Cho, (2008, Nov.), "Screen printing of silver nanoparticle suspension for metal interconnects", in Korean J. Chem. Eng. [Online], 25 (6), pp. 1358-1361. Available: <http://link.springer.com/article/10.1007/s11814-008-0223-y#page-1>

- [19]G. Ramarathnam, M. Libertucci, M. M. Sadowski, and T. H. North, (1992, Dec.), “Joining of Polymers to Metal”, in Journal of AWS. [Online], pp. 483-s-490-s. Available: http://www.aws.org/wj/supplement/WJ_1992_12_s483.pdf
- [20]Xingsheng Liu and Guo-Quan Lu, (2003, Jun.), “Effects of solder joint shape and height on fatigue lifetime”, in IEEE Transactions on Components and Packaging Technologies [Online], 26(2), pp. 455-465. Available: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1218243>
- [21]Luigi Atzori, Antonio Iera, and Giacomo Morabito, (2010, Oct.), “The Internet of Things: A survey”, in Computer Networks [Online], 54(15), pp. 2787-2805. Available: <http://www.sciencedirect.com/science/article/pii/S1389128610001568>
- [22]Paula Gould, (2003, Oct.), “Textiles gain intelligence”, in Materials Today [Online], 6(10), pp. 38-43. Available: <http://www.sciencedirect.com/science/article/pii/S1369702103010289>
- [23]Jeffrey Huang and Muriel Waldvogel, “Interactive wallpaper,” in ACM SIGGRAPH, New York, NY, 2005, pp. 172-176.
- [24]Leah Buechley, David Mellis, Hannah PErner-Wilson, Emily Lovell, and Bonifaz Kaufmann, “Living wall: programmable wallpaper for interactive spaces”, in ACM International Conference on Multimedia, New York, NY, 2010, pp. 1401-1402
- [25]A. Waterman, Y. Lee, D.A. Patterson, and K. Asanovic, (2011, May), “The RISC-V Instruction Set Manual, Volume I: Base User-Level ISA”, in EECS Department University of California, Berkeley, Tech. Rep. UCB/EECS-2011-62 [Online], Available: <http://www.eecs.berkeley.edu/Pubs/TechRpts/2011/EECS-2011-62.pdf>
- [26]Flavio Bonomi, Rodolfo Milito, Jiang Zhu and Sateesh Addepalli, “Fog computing and its role in the internet of things”, in Proceedings of the MCC workshop on Mobile cloud computing, New York, NY, 2012, pp. 13-16

- [27]M. Akin, E. Pichler and L. Rissing, „Design guidelines for efficient eutectic soldering onto low Tg polymeric multimode light waveguides”, in International Conference on System-integrated Intelligence, Bremen, Germany, 2014.
- [28]H. Armandula, (2011, May), “Indium bonding of magnets to aluminum flags”, in California Institute of Technology and Massachusetts Institute of Technology, Tech. Rep. LIGO-T060057-00-D [Online], Available: <http://www.ligo.caltech.edu/docs/T/T060057-00.pdf>
- [29]L. Pauksch, S. Hartmann, M. Rohnke, G. Szalay, V. Alt, R. Schnettler, K. S. Lips, (2014, Jan.), „Biocompatibility of silver nanoparticles and silver ions in primary human mesenchymal stem cells and osteoblasts“, in Acta Biomater. [Online], 10 (1), pp. 439-449. Available: <http://www.ncbi.nlm.nih.gov/pubmed/24095782>
- [30]D. W. Han, Y. Wo, M. H. Lee, J. H. Lee, J. Lee, J. C. Park, (2012, Jul.), „In-vivo and in-vitro biocompatibility evaluations of silver nanoparticles with antimicrobial activity“, in Journal of Nanoscience and Nanotechnology, 12 (7), pp. 5205-5209. Available: <http://www.ncbi.nlm.nih.gov/pubmed/22966546>
- [31] H. Seitz, S. Marlovits, I. Schwendenwein, V. Vecsei, U. Losert (1996, Jun.), „Biocompatibility of polyethylene terephthalate – PET- (Trevira strong) – an in-vivo study of the sheep knee“, in Biomedical Technology, 41(6), pp. 178-182. Available: <http://www.ncbi.nlm.nih.gov/pubmed/8766395>
- [32]M. Pavlova, M. Dragonova, (1993, Oct.), “Biocompatible and biodegradable polyurethane polymers”, in Biomaterials, 14(13), pp. 1024-1029. Available: <http://www.ncbi.nlm.nih.gov/pubmed/8286669>