9 kV, 1 cm×1 cm SiC SUPER GTO TECHNOLOGY DEVELOPMENT FOR PULSE POWER

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Abstract

Power devices made on Silicon Carbide (SiC) are expected to offer significant advantages over silicon due to the unique material properties. With the continuing improvement in both material quality (defect density and carrier lifetime) and SiC device fabrication process, SiC power devices are increasingly fabricated with higher blocking rating and larger die size. This paper describes the benefits of using SiC Gate Turn-Off thyristors (GTO) in power electronics, especially for pulse power applications, reviews the development history and the current state of the art, and outlines the future perspective for developing large area GTOs with high blocking voltage of > 10 kV.

Experimental results for the state-of-the-art 9 kV, 1 cm^2 SiC GTOs are presented. Static and dynamic characteristics are described. A forward drop of 3.7 V at 100 A (100 A/cm^2) is measured at 25°C. A slight positive temperature coefficient of the forward drop is present at 300 A/cm^2 indicating the possibility of paralleling multiple devices for higher current capability. The device exhibits extremely low leakage currents at high temperatures. The turn-on delay is found to be a strong function of the gate current, cathode-anode current and voltage. A peak current of 12.8 kA conducted with a pulse width of 17.4 μs indicating the superiority of the SiC GTOs for pulse power applications.

I. INTRODUCTION

Large-area silicon thyristors are being manufactured today with single devices on a 100-mm-diameter wafer with current handling capability of 3-4 kA and blocking voltages approaching 10 kV. GTOs on silicon have also been developed over the past 30 years due to the advantages over thyristors in the higher switching speed and the ability to turn off the current without reversal of the anode to cathode voltage.

Due to the excellent conductivity modulation in the drift region, Si thyristors and GTOs are suitable for certain applications which require switching of high peak current. The issues with Si devices are their long rise time and limited temperature they are allowed to operate at due to the low thermal conductivity of the silicon material.

The pulse power systems require the power switches to operate at high speed and high temperatures to meet the demand for smaller and higher power density power electronics. 4H-Silicon Carbide (4H-SiC) is a wide bandgap semiconductor that offers a factor of 10 higher breakdown electrical field compared to silicon which enables the drift layer of the GTO approximately one 10^{th} of a silicon thyristor with a comparable voltage rating. This implies that full conductivity modulation of the drift layer in a 4H-SiC GTO can be achieved with a minority carrier lifetime that is two orders of magnitude shorter than that is available in silicon devices, which translates into three orders of magnitude improvement in turn-off characteristics [1-4]. In addition, the excellent thermal conductivity (4.9 for SiC vs. 1.5 W/cm·°C for Si) can effectively spread power dissipation without overheating and allows lighter cooling systems.

II. PROGRESS IN SIC GTOs

4H-SiC GTOs have been demonstrated by CREE, Inc., Northrop Grumman, and a few universities since the late of 90s for very high voltage applications in utility (for example - Fault Current Limiters) and pulse power applications [5-7]. The devices were made on n-type 4H-SiC substrates resulting in an npnp structure, which is inverse of the conventional pnpn structure used in silicon technology. This is necessary in SiC due to the high resistance of the p-type SiC substrates. The limitations on epilayer thickness and the device footprint have generally limited these results to a few thousand volts of blocking voltage and several amps. The small size was partially attributed to the presence of the high density of micropipes in the SiC crystal.

In the last several years, SiC technology has made tremendous strides in reducing the defect density which has enabled larger SiC GTO chip size as shown in Figure 1. The micropipe density (MPD) has been reduced from >10 cm^{-2} in 90s to <1 cm^2 in early of 2005, and eventually zero MPD at present [8].

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14. ABSTRACT

Power devices made on Silicon Carbide (SiC) are expected to offer significant advantages over silicon due to the unique material properties. With the continuing improvement in both material quality (defect density and carrier lifetime) and SiC device fabrication process, SiC power devices are increasingly fabricated with higher blocking rating and larger die size. This paper describes the benefits of using SiC Gate Turn-Off thyristors (GTO) in power electronics, especially for pulse power applications, reviews the development history and the current state of the art, and outlines the future perspective for developing large area GTOs with high blocking voltage of > 10 kV. Experimental results for the state-of-the-art 9 kV, 1 cm2 SiC GTOs are presented. Static and dynamic characteristics are described. A forward drop of 3.7 V at 100 A (100 A/cm2) is measured at 25¢XC. A slight positive temperature coefficient of the forward drop is present at 300 A/cm2 indicating the possibility of paralleling multiple devices for higher current capability. The device exhibits extremely low leakage currents at high temperatures. The turn-on delay is found to be a strong function of the gate current, cathode-anode current and voltage. A peak current of 12.8 kA conducted with a pulse width of 17.4 £gs indicating the superiority of the SiC GTOs for pulse power applications.

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CREE has steadily increased both the diameter and quality of SiC wafers, and the development of power GTOs reflects such progress.

Figure 2 compares the 3" and 4" wafers with 7 mm×7 mm GTOs.

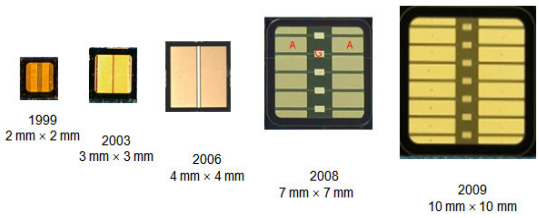


Figure 1. Increase in SiC GTO chip size over the past ten years demonstrated at CREE, Inc.

The total number of the devices has been increased from 37 on a 3" wafer to 61 on a 4" wafer. This evolution has significantly reduced the cost of the unit device, and will help commercialization in the future.

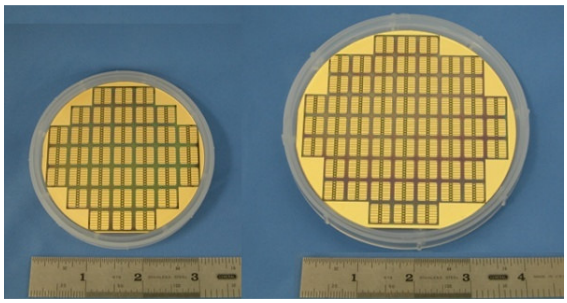


Figure 2. Evolution of 7 mm×7 mm SiC GTOs made on 3" and 4" SiC wafers at CREE, Inc.

The blocking voltage of SiC GTOs is dependent upon the thickness and doping concentration of the drift layer. Epitaxial growth is the most important part of the high-yield, high-performance devices. At the early stage of the development, the drift layer was ~ 50 µm with a doping concentration of ~1×10^{15} cm^{-3} which limited the blocking voltage of <5 kV. The recent improvements in the growth process have resulted in a thick epilayer of > 100 µm with <2×10^{14} cm^{-3} doping concentration in the drift layer. As the result, the blocking voltage has been steadily increased from 5 kV in 2003, 6 kV in 2007, to 9 kV in 2009. In addition, the carrier lifetime has been significantly increased from <0.5 µs to ~2 µs which facilities full conductivity modulation of the thick drift layer.

The main obstacle for insertion of SiC GTOs in the power systems has been the presence of degradation in forward voltage drop (i. e. increase in on-resistance) [9-10]. The recombination-induced stacking faults (SFs) have been identified as a prime cause. When nucleation sites are available, SF development results in performance degradation of SiC GTOs. These SFs originate from basal plane dislocations (BPDs). A high density of SFs results in an increase of the forward voltage drop after forward conduction. Clearly, the reduction of BPDs is vital for developing stable SiC GTOs. Numerous efforts have been made in the growth of thick epilayers and much reduced BPD density (<2 cm^{-2}) has been demonstrated on SiC substrates. As a result, the forward voltage drift issue, which had plagued the SiC bipolar devices for many years has largely been solved by minimizing Basal Plane Dislocations (BPDs). This has resulted in a stable forward voltage drop in GTOs as shown in Figure 3.

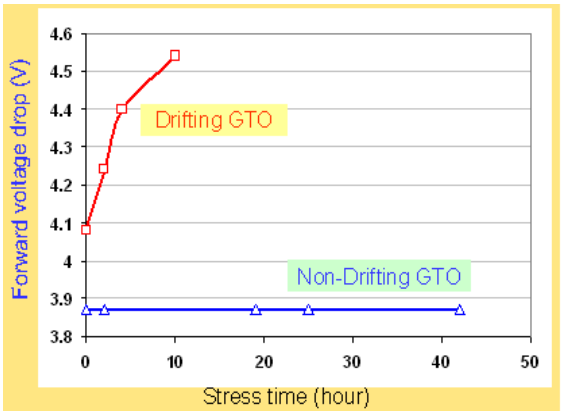


Figure 3. Drift in forward voltage (at 100 A/cm^2) has been almost eliminated by minimizing Basal Plane Dislocations in SiC epilayers. SiC GTOs were 7 mm×7 mm with 6 kV blocking voltage. Stress conditions: I_{AK} = 25 A DC.

Above progress in both materials and device fabrication has paved the way for developing large area SiC GTOs with high voltage as described in the following section.

III. DEVICE DESIGN AND FABRICATION OF 9 KV GTOs

A typical device cross-section of a 9 kV SiC GTO is shown in Figure 4. This device is built on an n^+ SiC substrate. As a result, unlike silicon GTOs, SiC GTOs have Anode on the top and Cathode on the bottom. All the epilayers were grown in a single run and optimized for high turn-on gain. The device has an asymmetrical structure with blocking in the forward direction only. A p-type buffer layer doped at 5×10^{16} cm^{-3}, 4 um thick was grown on a SiC substrate. Over this, a p^- layer of 90 um thickness was grown. The doping of this layer was <2×10^{14} cm^{-3}. Following this was the growth of n-type base layer, doped at ~1×10^{17} cm^{-3}. The thickness of the base layer was 2 um. Finally a highly doped p^+ anode layer of thickness 2 µm was grown.

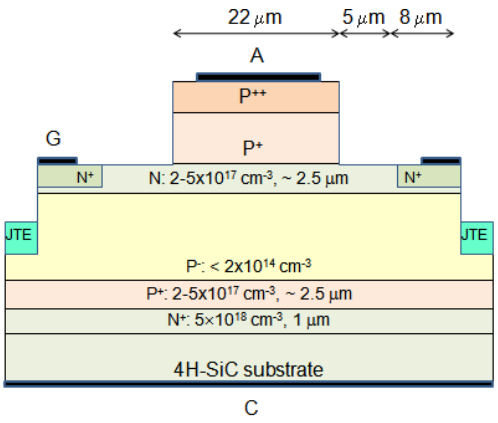
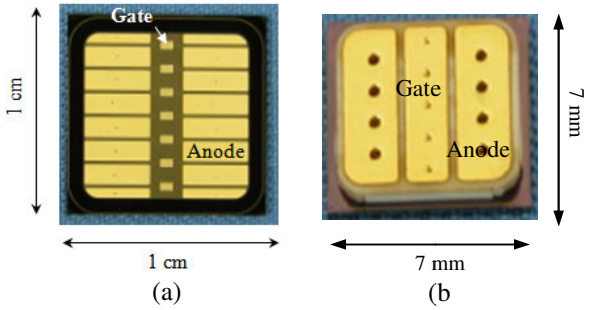


Figure 4. A simplified device cross-section showing the five epilayer thyristor structure.

The anode layer was first etched using reactive ion etch followed by the etching of the mesa for device isolation. The gate contact implant was carried out next, using nitrogen with a box like profile with a maximum energy of 360 keV. Multiple zone JTE implants using nitrogen implantation followed by a high temperature anneal. The first passivation layer consisted of 1 μm of PECVD oxide. The anode, gate and the backside ohmic contacts were formed using annealed Nickel. The overlayer metal (Ti/Ni/Au) with a 4 μm of gold was patterned on the front and the same overlayer was deposited on the back. An 8 μm thick polyimide layer was patterned on the front to open the bond pads for anode and gate terminals.

A picture of a 1 cm × 1 cm SiC GTO is shown in Figure 5a. It has seven gate pads to evenly distribute the gate current during switching. In pulse power applications, SiC GTOs conduct a very high current density of > 10 kA/cm^2, which makes it critical for such devices to be packaged with low inductance. An integrated package technology called thinPak [11] has been successfully realized on 7 mm×7 mm SiC GTOs, as shown in Figure 5b. Such a package replaces wire bonds with a ceramic lid that simultaneously makes multiple redundant gate and cathode contacts with ultralow package impedance.



Figures 5. (a) A picture of the 1cm×1 cm SiC GTO; (b) a photographic image of a 7 mm×7 mm SiC GTO with ThinPak.

IV. RESULTS AND DISCUSSION

A. On-state I-V characteristics

The forward conduction characteristics are shown in Figure 6 as a function of temperature. A forward drop of 3.7 V at 100 A (100 A/cm^2) is measured at 25°C. A very useful feature of this device is that at high current densities (>300 A/cm^2), a positive temperature coefficient in differential on-resistance is obtained which allows for stable parallel operation for pulsed power applications which typically operate at 10-20 kA/cm^2.

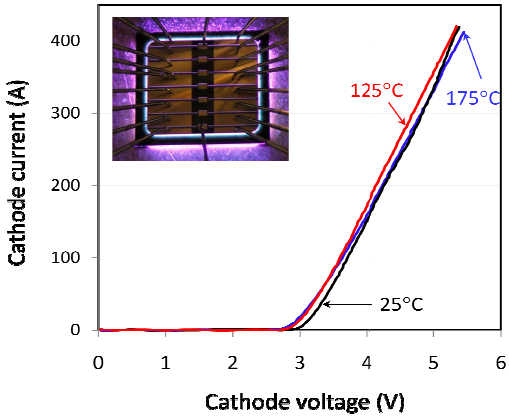


Figure 6. Output characteristics of a 9 kV SiC GTO at different temperatures with I_G = 50 mA. Chip size: 1 cm^2. The insert shows the blue light emission due to the recombination of electrons and holes in the active region.

B. Blocking I-V Characteristics

Figure 7 shows the forward blocking characteristics of the 1 cm^2 SiC GTO at different temperatures. A blocking voltage was measured up to 9 kV with a leakage current of < 1 μA. The leakage current decreased at 75°C and 125°C, which is attributed to the reduced impact ionization at elevated temperatures. The increased leakage current at 175°C is suspected to be a leakage in the package.

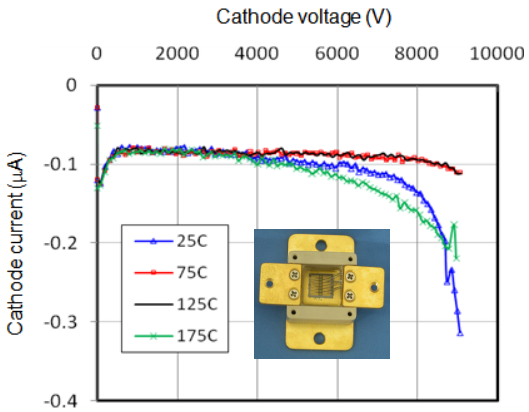


Figure 7. Blocking I-V characteristics of the SiC GTO. Insert shows the packaged GTO for high voltage tests.

The leakage current of a commercial 1.6 kV, 165 A 12.4 mm×12.4 mm Si SCR is shown in Figure 8. Comparing the blocking characteristics between the SiC GTO and Si SCR clearly shows that the SiC GTO has significantly less leakage current. Furthermore, as temperature increases, the leakage current of the Si SCR gets high enough to trigger the device. Referring to Figure 8, the device self-triggered at 150°C when the reverse voltage just passes 600 V. In contrast, SiC GTOs have been taken to 300°C and no self trigger from leakage current was observed.

The consequences of above phenomenon are very significant for pulsed power applications. At high peak current, die heating is typically adiabatic. When the device is repetitively pulsed in rapid succession, the temperature of the die will increase. The higher temperature capability of the SiC GTO allows significantly higher number of shots. This is crucial for applications such as rapid firing rail guns.

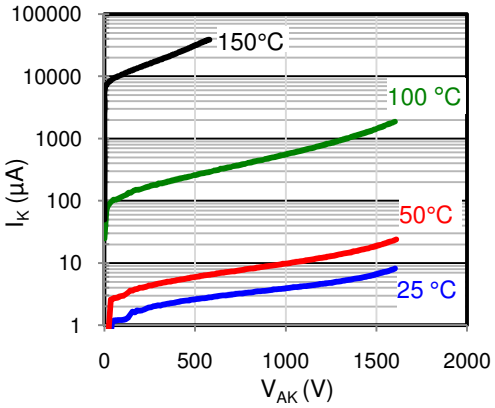


Figure 8. Blocking I-V characteristics of a commercial 1600 V Si SCR at different temperatures.

C. Turn-on Characteristics

The schematic circuit diagram for turn-on switching measurements is shown in Figure 9 with a load resistor of 10 Ω and a capacitor of 3 μF.

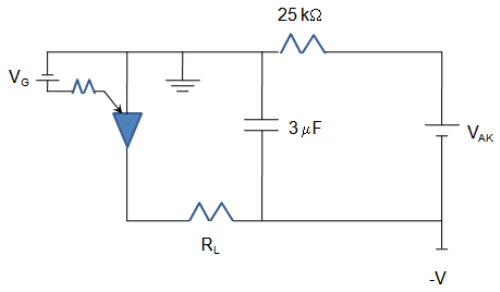


Figure 9. Circuit diagram for turn-on characterization.

Experimental results have shown that the turn-on delay time is largely dependent on the gate current, cathode-anode current and voltage, and the operating temperature. For example, Figure 10 compares the turn-on delay time dependence on the gate current. A significant delay is observed between the time when the gate signal is applied and when the anode-to-cathode current begins to rise.

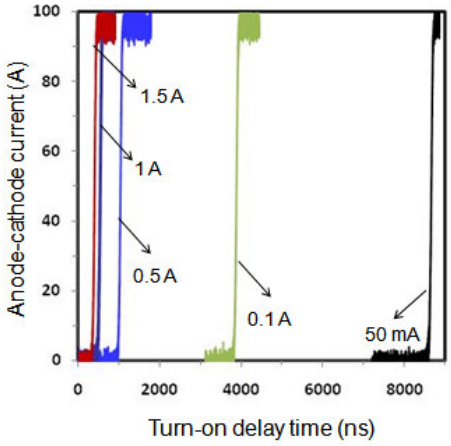


Figure 10. Turn-on waveform as a function of the gate current. V_{AK} = 1000 V; R_L = 10 Ω.

This delay is large (>4000 ns) for a gate current of <0.1 A, but significantly reduces to 120 ns for a gate current of 1.5 A. The delay is predominantly caused by the time it takes to complete the internal feedback loop between the two transistors.

The turn-on delay time is reduced with a high anode-cathode current as shown in Figure 11. For example, a turn-on delay time of 500 ns was measured at a anode-current current of 100 A.

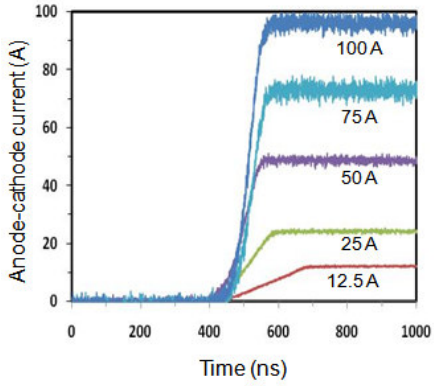


Figure 11. Turn-on delay time dependence on the anode-cathode current. V_{AK} = 1000 V; I_G = 1 A.

D. Pulse Power Characteristics

A circuit schematic diagram for pulse current measurement is shown in Figure 12. The circuit uses a negative voltage source to allow the anode to be grounded, thus affording a ground referenced gate drive. The circuit is a basic series resonant pulse generator consisting of the test 1 cm^2 SiC GTO, a CREE 4.5 kV, 1

cm^2 SiC PiN diode, D1, with snubber capacitor and resistor, a CREE 6 kV, 0.25 cm^2 SiC PiN antiparallel diode, a series resonant circuit composed of capacitor, C1, and inductor, L1. C1 consists of 60 µF, 8 kV SB Electronics Power Ring polypropylene capacitors. L1 is a single turn inductor providing a total circuit inductance of 500 nH. Capacitor C1 is initially charged up to approximately -1.4 kV.

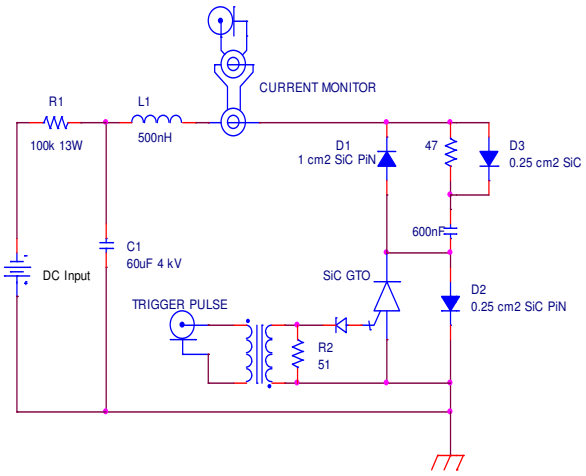


Figure 12. Schematic circuit diagram for pulsed current test.

A trigger pulse is applied (5 A for 4 µs) turning on the SiC GTO. A sinusoidal current begins to flow through the loop formed by C1, the SiC GTO, diode D1, and L1. The voltage across C1 is essentially inverted when the sinusoidal current crosses zero. This causes diode D1 to commutate from conduction to blocking, thus terminating the current through the SiC GTO.

The current through this loop is monitored by a two stage current transformer. The primary current transformer consists of 10 turns of AWG 8 wire around a VACUUMSCHMELZE T60006-L2050-W516 nanocrystalline core. The secondary current transformer is a Pearson 411. A photograph of the test setup is shown in Figure 13.

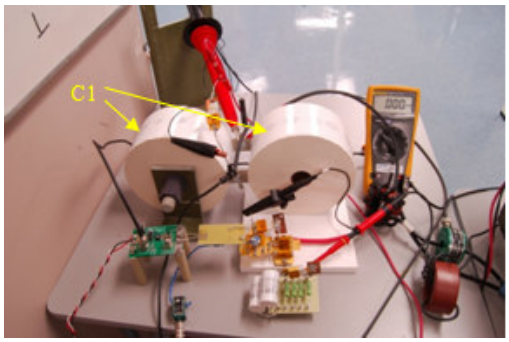


Figure 13. A photographic image of the test setup.

A close-up showing the SiC GTO, PiN diodes D1 and D2 is shown in Figure 14.

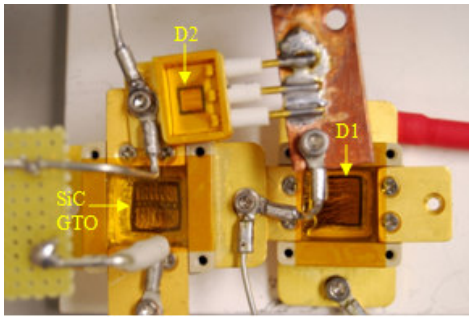


Figure 14. SiC GTO, D1 and D2 close up.

The current waveform is shown in Figure 15. The peak current was 12.8 kA, which translates to a 12.8 kA/cm^2 current density flowing through both the SiC GTO and D1. The available components limited the maximum current to 12.8 kA and the devices survived. Therefore, the upper current density limit under these conditions can be even higher than this value.

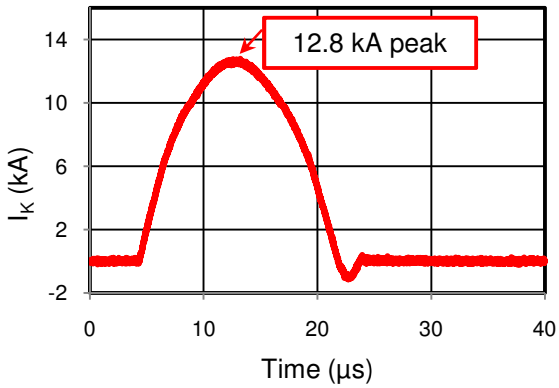


Figure 15. SiC GTO and D1 current waveform. The base width is 17.4 µs.

V. FUTURE PERSEPCTIVE

Compared to other devices made on SiC such as MOSFET, IGBT, etc., SiC GTO is the favorable device for large current (>1000 A), ultra-high voltage (15-25 kV), pulse power applications due to its superior conductivity modulation in the drift layer. Compared to Si thyristors, the SiC GTOs exhibit extremely low leakage currents, which stay low at elevated temperatures. Significant progress in SiC materials and the growth of thick epilayers with much reduced BPD density (<2 cm^{-2}) have paved the way for SiC GTOs to be operated in a stable manner. The devices have demonstrated excellent current sharing capability in both DC and pulsed conditions. On the other hand, there are several issues which need to be solved before large area, high voltage SiC GTOs with stable performance can be realized and inserted in pulse power systems.

The first issue is the presence of BPD in SiC substrate and epilayers. Reliability tests have shown that a large amount of SiC GTOs currently suffer from a degradation

of forward drop due to recombination-induced stacking faults in the drift layer. Over the last few years, tremendous progress has been made in reducing the density of BPDs in SiC epilayers. Today, this problem has been greatly reduced. However, further work is needed to completely eliminate the influence of BPDs in SiC bipolar devices.

The second important issue has to do with the fact that an ambipolar lifetime of at least 5 µs with better than 5% uniformity across the device is required for high voltage SiC GTOs. In silicon, one would typically need 1 ms of lifetime for 6 kV devices. Today, the mean lifetime in thick SiC epilayers, is approximately 1.5 µs but it is highly non-uniform across the wafer as shown in Figure 16. The defects limiting the lifetime need to be identified, eliminated and then a means of obtaining a uniform lifetime (for example, irradiation) needs to be established.

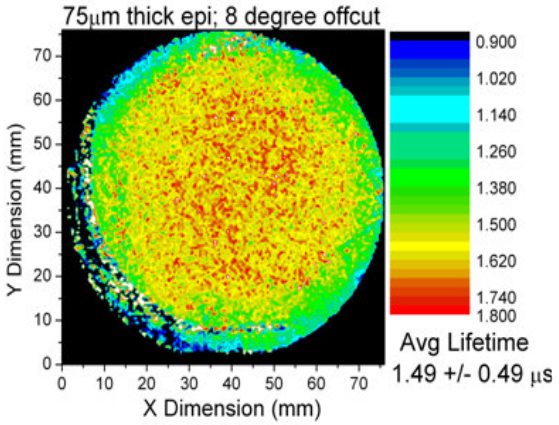


Figure 16. Carrier lifetime measured by PL on a commercially available 3" 4H-SiC wafer used for 7 kV SiC GTO fabrication. (Courtesy: Drs. J. Caldwell and R. Stahlbush at NRL, Washington, D.C.)

Lastly, there is a need to reduce the doping of thick epilayers to below 10^{14} cm^{-3} for 20 kV class of GTOs. Today, a doping of 2×10^{14} cm^{-3} can be routinely obtained.

VI. SUMMARY

Power GTOs made on SiC have been emerging for such applications due to the superior material properties of SiC. SiC GTOs in the range of 10-20 kV will facilitate reduced series stack and cooling requirements in pulse power applications such as Fault Current Limiters and Rail Guns. In addition to faster switching, reduced conduction and switching losses and reduced cooling requirements, SiC GTOs are less prone to thermal runaway owing to low leakage currents inherent in SiC due to its wide bandgap.

With the successful demonstration of 9 kV, 1 cm^2 SiC GTOs, an important milestone has been reached in the development of the SiC Technology. These devices can turn-on 100 A with a delay of 120 ns for a gate current of 1.5 A. A peak current of 12.8 kA (corresponding to 12.8 kA/cm^2) was conducted. The superiority of switching time and peak current handling capability makes the SiC GTOs a promising candidate for pulse power applications.

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