



**SUBTRACTIVE PLASMA-ASSISTED-ETCH PROCESS FOR DEVELOPING
HIGH PERFORMANCE NANOCRYSTALLINE ZINC-OXIDE THIN-FILM-
TRANSISTORS**

THESIS

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AFIT-ENG-MS-15-M-027

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Abstract

Thin-Film-Transistors (TFTs) employing undoped zinc-oxide (ZnO) thin-films are currently being investigated by the Air Force for microwave switching applications. Since the on-resistance (R_{on}) of the device scales with channel length (L_C), ZnO TFT optimization should be focused on reducing L_C , therefore minimizing the associated insertion losses. In this research, deep sub-micron scaling of ZnO TFTs was undertaken using a subtractive reactive-ion-etch (RIE) process. Under optimum processing conditions, ZnO TFTs with L_C as small as 155 nm were successfully demonstrated. The active ZnO channels of the TFTs were patterned by selective SF_6 -RIE of a tungsten ohmic film through electron-beam defined openings in a polymethyl-methacrylate (PMMA) based resist. Through electrical testing, the width normalized R_{on} of ZnO TFTs with 155 nm channels was extracted as $3.6 \, \Omega \cdot \text{mm}$ and the devices were found to operate at drain current densities and transconductance values of 830 mA/mm and 121 mS/mm, respectively. Additionally, a total width-normalized source and drain parasitic resistance of $2.1 \, \Omega \cdot \text{mm}$ was observed using a gated transfer length method (TLM), indicating the tungsten-ZnO interface is low resistance. This demonstration of high performance and low R_{on} suggests the potential for ZnO TFTs in switching and microwave power applications.

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Thomas M. Donigan

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SUBTRACTIVE PLASMA-ASSISTED-ETCH PROCESS FOR DEVELOPING HIGH PERFORMANCE NANOCRYSTALLINE ZINC-OXIDE THIN-FILM- TRANSISTORS

I. Introduction

Background

The thin-film transistor (TFT) is a type of field-effect device that is similar in both structure and operation to the well known metal-oxide semiconductor field-effect-transistor (MOSFET), which has driven the explosion of digital logic technology over the last half century [1]. However, unlike MOSFETs which utilize bulk single-crystal semiconductors as both the structural and active current carrying layer [2]. The active layer in a TFT consists of an amorphous, polycrystalline or nanocrystalline semiconductor thin-film which may be deposited onto a wide variety of host substrates and is compatible with low temperature fabrication processes [3]. The unique structure and associated fabrication processes of TFTs, which are discussed in detail in Chapter II, enables TFTs to be employed in areas where the use of single-crystal MOSFETs would be impractical. Examples include implementing electronic control and sense functions on large-area, non-planar or even flexible surfaces. Yet, due to the reduced electronic properties associated with semiconductor thin-films when compared to their single-crystal counterparts, TFTs have historically found limited use outside of low speed and low power applications [4].

As with single-crystal MOSFETs, silicon is currently the most widely used material for TFT development. TFTs based on amorphous-silicon (*a*-Si) thin-films can

easily be fabricated on glass and other large area substrates, and have been used for decades in active matrix display technologies [5]. However, *a*-Si TFTs suffer from extremely low electron mobility, typically on the order of 1-2 cm²/Vs, making them unsuitable for use in high speed and high power circuits which require significantly higher drive currents [6]. The performance of silicon based TFTs can be improved by utilizing a polycrystalline-silicon (*poly*-Si) thin-film as the active channel layer. Still, *poly*-Si TFTs present their own challenges including high fabrication temperatures (typically in excess of 600°C), or expensive laser crystallization fabrication processes [7].

Recently, TFTs based on metal-oxide semiconductors, such as zinc-oxide (ZnO), have emerged as possible alternatives to Si based TFTs. Metal-oxide TFTs have demonstrated high electron mobility while maintaining low temperature fabrication processes [8, 9, 10, 11], thus resolving the existing trade-off between process temperature and device performance found in Si based TFTs. Moreover, the microwave amplification potential of ZnO TFTs has recently been demonstrated, and it is expected that cut-off frequencies greater than 10-GHz are possible with continued device improvements [12, 13]. These studies indicate the potential use of ZnO TFTs in high speed and high power applications of interest to the military.

Motivation

Many of the most demanding military and aerospace electronics applications are space-, weight-, and power-constrained [14]. New electronic technologies that meet these constraints at a low cost are critical to maintaining a leading position in air and space military systems. Thin-film electronics, based on high performance TFTs, have the

opportunity to not only increase the effectiveness of existing electronic subsystems, but also offer the possibility of developing novel electronic functions in non-traditional areas. These include wireless communication, digital logic, signal processing or even high power switching applications over large area or non-planar surfaces. Unfortunately, existing TFT technologies based on α -Si cannot provide the performance requirements necessary to meet the demands of advanced circuits. Therefore, one of the most important aspects of developing advanced thin-film electronics is extending TFT device capabilities to high power and RF levels of performance.

Currently, TFTs based on metal-oxide semiconductor thin films such as ZnO are being aggressively pursued as replacements to α -Si TFTs due to their superior electronic characteristics [15, 16]. With their demonstrated high mobility and high carrier velocity, ZnO TFTs have huge potential for use in advanced electronic applications. Yet, outside of the work by Bayraktaroglu *et al.* at the Air Force Research Laboratory [17, 18], research in ZnO TFT development is almost exclusively focused on developing transparent ZnO TFTs for the commercial display market [19, 20], which does not have the demanding power and RF requirements of advanced military systems. In addition, the display market imposes fabrication restrictions on ZnO TFT development, such as the use of transparent electrodes, process temperatures below 150°C and the use solution processed ZnO thin-films for low cost production. These fabrication restrictions limit the RF and switching performance of the device. Therefore, the ultimate performance level of ZnO TFTs remains unclear.

Problem Statement

In order for ZnO TFTs to be integrated into high performance and RF switching circuits, they need to exhibit low insertion losses and operate at high RF. Since the device on-resistance scales with channel length, a primary decision in ZnO TFT optimization should be focused on reducing the channel length. Scaling down the channel length not only reduces the on-resistance of the device, therefore minimizing insertion losses, it also a means to boost RF performance. Unfortunately, techniques for device scaling of ZnO TFTs have been restricted due to the processing and lithographic methods used for device fabrication, which have not been optimized for developing devices with channel lengths below 1 μm . Therefore, in order to extend the performance levels of ZnO TFTs for use in high performance and RF switching applications, novel fabrication methods capable of producing devices with nanometer-scale channel lengths needs to be investigated.

Justification

Traditionally, channel length definition of ZnO TFTs has been achieved by shadow mask, wet chemical etching, or metal lift-off fabrication processes, resulting in relatively long channel length devices [21]. Shadow mask techniques offer little pattern definition control and are limited to large feature sizes. Wet chemical etching is difficult due to ZnO's high etch rate in common acid based etchants. Finally, lift-off is a simple damage free process for patterning devices, however, edge issues with lift-off patterning causes difficulty in fabricating devices with feature sizes below 0.5 microns. An alternate approach is to use a subtractive plasma-etch process to define the active channel length of

the device. However, for the plasma-etch process to be a viable solution for patterning ZnO TFTs with nano-scale channel lengths, the etch process needs to pattern low resistance source and drain contacts with high anisotropic etch profiles without damaging the underlying ZnO film.

Approach

A recent effort by Herold identified various ohmic materials that can be selectively etched against ZnO using a plasma-etch process in order to avoid the scaling limitations found in lift-off defined devices [22]. This study provides foundational research upon which nanometer-scale ZnO TFTs can be fabricated, with particularly promising results employing *tungsten* and a *titanium-tungsten* alloy as ohmic contacts to ZnO. The initial results from the study indicate ZnO TFTs with channel lengths below 200 nm are possible utilizing a subtractive plasma-etch process to define the source and drain ohmic contacts. However, functioning devices were never realized due to unforeseen fabrication errors, leaving many remaining questions on the performance of subtractive etched ZnO TFTs. Furthermore, the contact resistance of *tungsten* and *titanium-tungsten* on ZnO has not yet been characterized. The goal of this research is therefore to build on the reported results, in an effort to assess the feasibility of developing high performance ZnO TFTs with nanometer-scale channel lengths using a subtractive plasma-etch process.

Methodology

In order to evaluate the subtractive plasma-etch process, substrate gated ZnO TFTs were fabricated using an optical lithographical defined etch mask before

developing shorter channel length devices using electron-beam lithography. Both optical and electron-beam lithographically defined devices were fabricated by using a reactive-ion-etch (RIE) process in order to etch ohmic films using the underlying ZnO channel layer as an etch stop. The source and drain contacts of ZnO TFTs with optical lithographically defined channel lengths were patterned using multiple fluorine-based RIE chemistries under varying plasma power conditions. The devices were then analyzed using scanning electron microscopy (SEM) and tested for their (DC) electrical characteristics. After completing fabrication and characterization of ZnO TFTs with micron scale channel lengths, ZnO TFTs with sub-micron channels were fabricated and characterized by RIE of ohmic films through an electron beam lithographically defined etch mask.

Summary

The growing interest in employing TFTs in advanced electronic applications has spawned research in developing high performance ZnO TFTs. However, in order for these devices to be employed in high performance and switching applications, they need demonstrate low on-resistance in order to minimize insertion losses while also operating at high RF. Since the device on-resistance and frequency performance scales with channel length, a primary decision in ZnO TFT optimization should be focused on reducing the channel length. Thus, innovative fabrication methods focused on geometry scaling of ZnO TFTs needs to be investigated. This research is aimed at developing a subtractive plasma-etch process for fabricating ZnO TFTs with nanometer-scale channel lengths. Subsequent chapters will detail TFT device theory and fabrication processes, the

methodology for experimental design and testing, results and analysis of the experimental data, and recommendations for continued research.

II. Background and Literature Review

Chapter Overview

This chapter reviews and discusses fundamental background and literature information applicable to ZnO TFT development. The chapter itself is divided into four main subsections: *Thin-Film-Transistors*, *Zinc-Oxide*, *Contacts to ZnO*, and *Fabrication Processes and Definitions*. The *Thin-Film-Transistor* subsection introduces the physical and electrical parameters of the TFT, including its structure, theory of operation, and important figures of merit used for electronic evaluation. Additionally, particularly relevant research in the development in high performance TFTs is discussed. The *Zinc-Oxide* subsection examines the general parameters of ZnO, including its crystal structure, electronic properties, and ZnO thin-film deposition methods. The *Contacts to ZnO* subsection details the formation and testing of low resistance ohmic contacts. Finally, the *Fabrication Processes and Definitions* section introduces applicable surface micromachining fabrication methods that are used throughout this work, including ohmic film deposition process, optical and electron-beam lithography, pattern transfer, and wet- and plasma-etching techniques.

Thin-Film-Transistors

Device Overview

In its simplest form a TFT is comprised of a semiconductor thin film, dielectric material and three metal electrodes (gate, source and drain). All of which are deposited onto a host substrate using low temperature deposition processes. The semiconductor thin-film is placed between the source and drain electrodes, and a dielectric is used to isolate the gate electrode from the semiconductor thin-film. By varying the voltage potential between the gate and source electrodes, the conductivity of the semiconductor thin-film can be modulated. This modulation, known as the “field effect”, is due to the injection of carriers at the semiconductor-dielectric interface caused by the capacitor formed by the gate electrode, gate dielectric, and semiconductor [4].

Figure 1 illustrates the basic structure and working principles of a TFT. A voltage applied to the gate electrode (V_G) modulates the conductivity of the semiconductor thin-film, thereby producing a corresponding variation in current flow from drain to source [23].

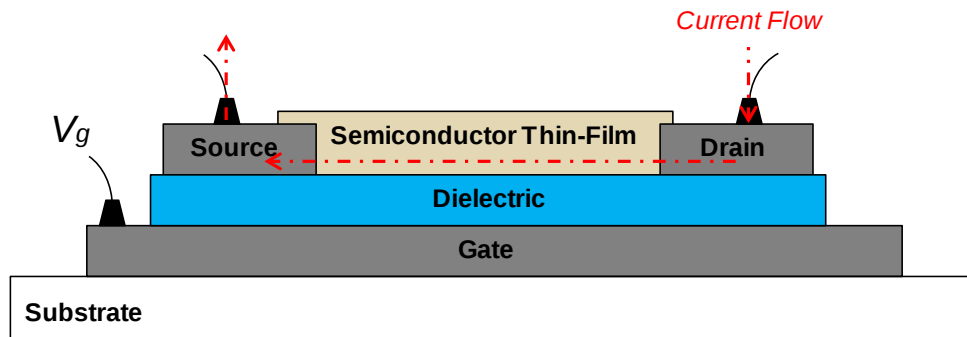


Figure 1: A basic illustration of a TFT. The device operates by applying a voltage to the gate electrode, which modulates the conductivity of the semiconductor thin-film, thereby producing a corresponding variation in drain to source current. Modified from [24]

The electrical characteristics of a TFT are highly dependent on the material composition and crystal structure of the active semiconductor channel layer. Unlike bulk semiconductors which are single-crystal, the semiconductor thin-film used in TFTs is typically amorphous or polycrystalline [25]. In single-crystal form, all the atoms within the material are arranged in a strict repeating pattern, free of defects and grain boundaries. In polycrystalline form, the material is comprised of a collection of small, randomly oriented, single-crystals (or crystallites). Finally, in amorphous form, the chemical bonds of the atoms within the semiconductor material all have random lengths and orientations. Figure 2 illustrates a two-dimensional schematic representation of single-crystal, polycrystalline and amorphous material [26].

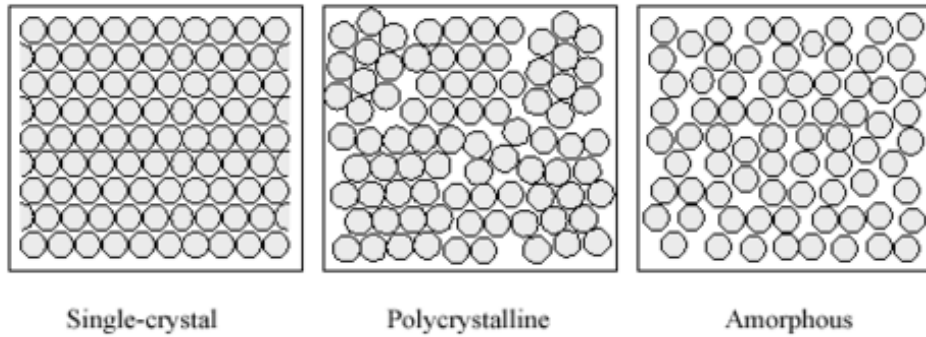


Figure 2: Two-dimensional schematic representation of single-crystal, poly-crystal and amorphous material [26].

The presence of defects and grain-boundaries in amorphous and polycrystalline semiconductor thin-films causes scattering of the carriers. As a result, the carrier mobility of a TFT is typically orders of magnitude less when compared to single-crystal a MOSFET [25]. This mobility decrease is true for silicon based devices. However, it has been theorized that the carrier transport in ionically bonded metal-oxide, semiconductors

is relatively unaffected by bond length or disorder [27]. Therefore, metal-oxide thin-films can exhibit mobilities that are on par with their single crystal counterparts, making them ideal for use in high performance TFTs. The electron transport properties of ZnO thin-films are discussed in detail in the Zinc-Oxide subsection.

Structure

Fully functioning TFTs can be produced in one of four basic structures which are illustrated in Figure 3: (a) staggered bottom-gate, (b) co-planer bottom-gate, (c) staggered top-gate, and (d) co-planar top-gate. Although slightly different in design, each structure contains the basic parts of a TFT device. The staggered and co-planer terms refer to the relative position of the source and drain electrodes with respect to the gate electrode. A modified version of the staggered bottom-gate structure is also shown in (e) called a substrate-gated structure. The substrate-gated structure uses a conductive material, such as a heavily doped silicon wafer, to serve as both the substrate and gate electrode. Although the substrate-gated structure does not allow for the integration of multiple devices on single substrate, the structure is useful for material characterization and process development. Additionally, the substrate-gated structure reduces fabrication complexity, substantially reducing the data cycle time and enabling more consistent results. Therefore, the substrate-gated structure was used extensively throughout this research.

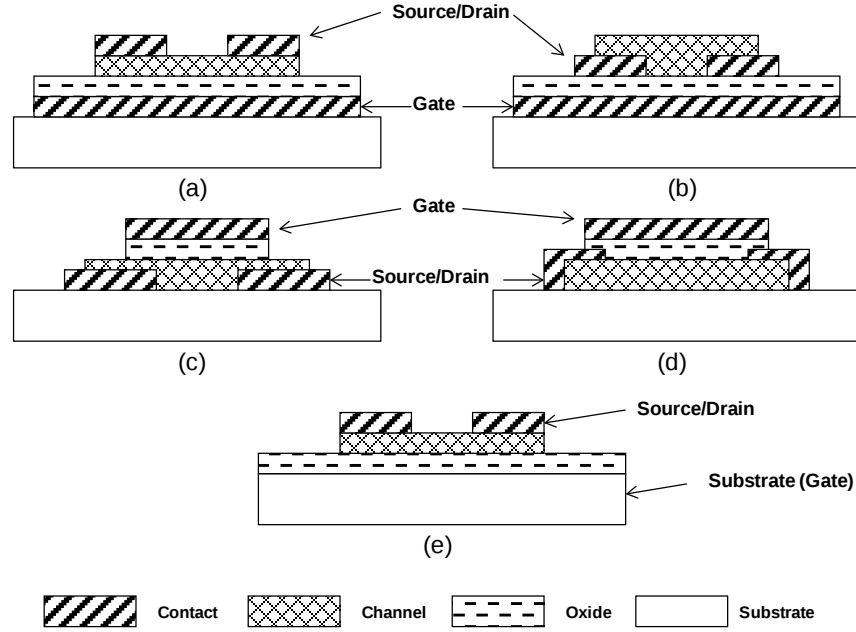


Figure 3: Basic thin-film transistor structures: (a) staggered bottom-gate, (b) co-planar bottom-gate, (c) staggered top-gate, (d) co-planar top-gate, and (e) modified staggered-bottom gate structure employing a conductive substrate as the gate electrode.

Theory of Operation

TFTs are classified as n-type devices, where the conducting carriers are electrons, or p-type devices, where the conducting carriers are holes, and operate in either enhancement or depletion mode [2]. An n-type depletion mode device requires a negative gate bias to turn the device OFF. Conversely, an n-type enhancement mode device requires a positive gate voltage to induce current flow, thus turning the device ON. For most switching applications, enhancement mode operation is preferable since no gate voltage is required to turn the device off which minimizes power dissipation. Since ZnO occurs naturally as n-type, this section will focus on n-type operation.

The ideal operation of a TFT can best be described by analyzing the energy band diagram of the metal-oxide-semiconductor (MOS) capacitor made up by the gate

electrode, gate dielectric and semiconductor material [2]. Figure 4 shows the energy band diagrams of the MOS interface of a typical n-type enhancement mode TFT. Under ideal conditions, when there is no applied voltage on the gate, the energy bands are in a flat-band condition, shown in (a). When a negative voltage is applied to the gate electrode, free electrons are repelled away from the semiconductor/dielectric interface, forming a region of positive charge known as the depletion region (i.e. depleted of free electrons), causing the energy bands of the semiconductor material to bend up, shown in (b). Applying a positive voltage attracts free electrons towards the semiconductor/gate dielectric interface, resulting in an accumulation of negative charge along the interface causing the energy bands to bend down, shown in (c). When a sufficiently large positive voltage is applied to the gate, enough free carriers have accumulated along the semiconductor/dielectric interface, creating a channel for current to flow from drain to source [2].

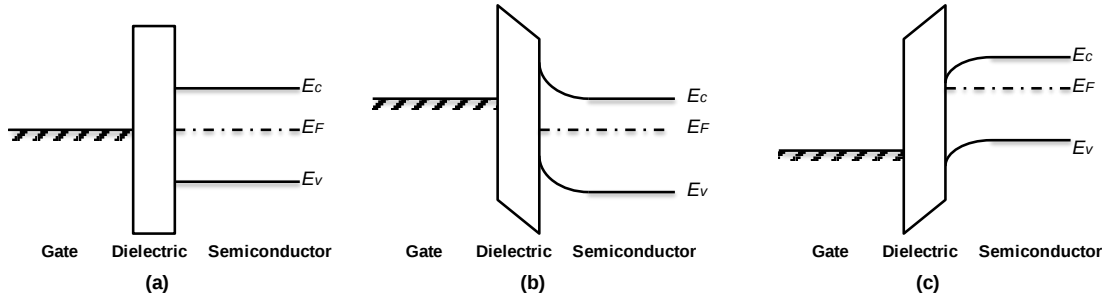


Figure 4: Energy band diagrams for a typical n-type, enhancement-mode TFT. (a) Under ideal conditions when $V_G = 0$ the system is in flat-band. (b) When, $V_G < 0$, a depletion of carriers along the semiconductor/dielectric interface causes the energy bands to bend up when. (c) Accumulation of carriers creates a downward band bending when $V_G > 0$.

The electrical operation of a TFT is typically quantified in the form of drain current (I_D) as a function of gate voltage-to-source (V_{GS}) and drain-to-source voltage

(V_{DS}), using the square-law model [28]. In this model, when V_{GS} is below the threshold voltage (V_t), the channel is completely depleted of free electrons, and no current is allowed to flow from drain-to-source. Increasing V_{GS} attracts free electrons towards the semiconductor/dielectric interface creating a channel for current flow. When $V_{GS} \geq V_t$, enough electrons have accumulated to form a conductive channel, turning the device ON. The ON state is further classified into the linear and saturation regions. In the linear region of operation (i.e. $V_{DS} \leq V_{GS} - V_t$), the source-to-drain current increases linearly with drain voltage and the device acts as a voltage controlled resistor. When the saturation voltage is reached (i.e. $V_{DSat} = V_{GS} - V_t$), the drain current saturates and is independent of V_{DS} and the device acts as a voltage controlled current source. Mathematically, the square-law model is illustrated in Equation 2.1 [4].

$$I_D = \begin{cases} 0 & \dots & V_{GS} \leq V_t \\ \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right] & \dots & V_{DS} \leq V_{GS} - V_t \\ \frac{1}{2} \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_t)^2 \right] & \dots & V_{DS} > V_{GS} - V_t \end{cases} \quad (2.1)$$

Where μ is the channel mobility, W/L is the ratio of the width to length of the channel, and C_{ox} is the gate oxide capacitance per unit area. C_{ox} is determined by both the dielectric constant and the thickness of the gate dielectric material. Mathematically, C_{ox} is given by [4]:

$$C_{ox} = \frac{\epsilon_0 \epsilon_{r,ox}}{t_{ox}} \quad (2.2)$$

Where $\epsilon_{r,ox}$ is the relative permittivity (or dielectric constant) of the gate dielectric, $\epsilon_0 = 8.854 \times 10^{-14}$ F/cm is the vacuum permittivity, and t_{ox} is the gate dielectric thickness.

Equation 2.1 is accepted as the ideal TFT or metal-insulator-semiconductor field effect transistor (MISFET) equation [28]. Figure 5 below illustrates a typical common source I_{DS} - V_{DS} transfer characteristic for an ideal n-type enhancement mode TFT.

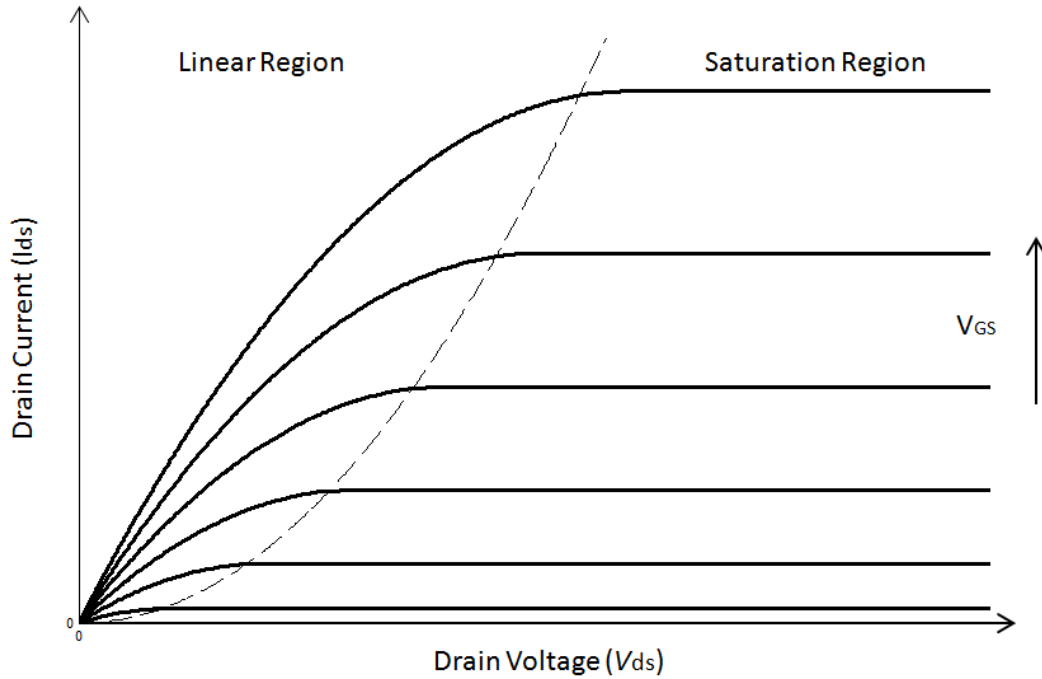


Figure 5: Illustration of the ideal drain-current versus drain-voltage (I_{DS} - V_{DS}) transfer characteristics curve at increasing gate voltage (V_{GS}) steps for an n-type enhancement mode TFT using the square law model.

Figures of Merit

Electrical characterization of a TFT involves analyzing a set of measured data to evaluate device performance. This process typically includes the extraction of the following device parameters: threshold or turn-on voltage, on-to-off current ratio, sub-threshold swing, transconductance, channel mobility and device on resistance.

The TFT parameter that is most often used to quantify device turn-on is V_t , and can be extracted by fitting measured I_D - V_G data to the ideal TFT equation. However, as detailed by Hoffman, conventional threshold voltage extraction of ZnO TFTs leads to invalid results since the mobility of the channel is dependent on gate voltage [23, 29]. To overcome this issue, TFT turn-on for ZnO TFTs is instead quantified using the device turn-on voltage (V_{on}). V_{on} is defined as the value of V_{GS} when I_D first increases from its minimum off value on a $\log(I_D)$ - V_{GS} plot. Drain current on-to-off ratio (I_{ON-OFF}) is the ratio of the maximum to minimum drain current while the device is operating in saturation (i.e. with a large V_{DS}).

The sub-threshold swing (S_{ss}), defined as the gate voltage required to increase the drain current by a factor of ten, is extracted from the TFT transfer characteristic using the following equation [30]:

$$S_{ss} = \left(\frac{d \log(I_{DS})}{dV_{GS}} \right)^{-1} \quad (2.3)$$

The sub-threshold swing also provides important information about the quality of a TFT, and can also be used to estimate the interface trap state density (N_t) near the semiconductor/dielectric interface using the following equation [31]:

$$N_t = \left[S_{ss} \cdot \log(e) \left(\frac{q}{k_B T} \right) - 1 \right] \left[\frac{C_{ox}}{q} \right] \quad (2.4)$$

Where, k_B is Boltzmann's constant, T is the temperature, q is the elementary charge of an electron, e is Euler's number equal to approximately 2.7182 and C_{ox} is the gate capacitance per unit area. The extraction of V_{on} , I_{ON-OFF} , and S_{ss} for a typical ZnO TFT fabricated for this thesis is shown in Figure 6.

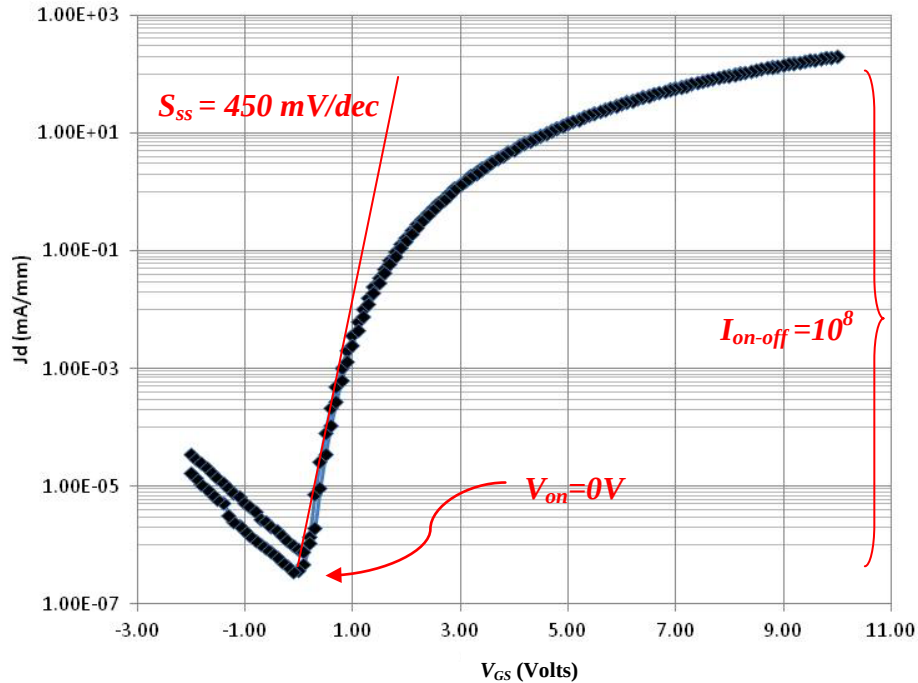


Figure 6: Extraction of V_{on} , I_{ON-OFF} , and S_{ss} for a typical ZnO TFT for a typical ZnO TFT fabricated in this thesis.

The transconductance (G_m) quantifies the drain current variation with a gate-source voltage variation while keeping the drain-source voltage constant, or [28]:

$$G_m \triangleq \left. \frac{\Delta I_{DS}}{\Delta V_{GS}} \right|_{V_{DS}=\text{const}} \quad (2.5)$$

In general, the transconductance is a measure of the amount of gain the device is able to deliver. In the linear and saturation regions the transconductance is given by [28]:

$$G_m = \mu C_{ox} \frac{W}{L} V_{DS} \Big|_{\text{linear}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_t) \Big|_{\text{saturation}} \quad (2.6)$$

Mobility is an important electrical property since it directly affects both the current-drive capability and maximum frequency operation of the device. As a parameter, mobility provides an assessment of how efficiently electrons move through the channel of the device [23]. The evaluation of TFT mobility involves fitting measured current-voltage data to a mathematical expression obtained through manipulation of the ideal TFT equation. Field-effect mobility (μ_{fe}) is obtained when the device is operating in the linear region (i.e. small V_{DS}) and is defined by [28]:

$$\mu_{fe} = \frac{L}{W} \frac{g_m}{C_{ox} V_{DS}} \quad (2.7)$$

Using Ohms law, the source-to-drain on resistance (R_{on}) of a device can be derived from the slope of the transistors I_D - V_D output characteristics while operating in the linear region (i.e. low V_{DS}) [32]:

$$R_{on} \triangleq \left. \frac{\Delta V_{DS}}{\Delta I_{DS}} \right|_{V_{GS}=const} \quad (2.8)$$

The high frequency performance of a TFT is typically characterized by the unity-gain cutoff frequency $f_t = g_m / 2\pi(WLC_{ox} + C'_{par})$. Assuming the parasitic capacitance (C'_{par}) is only due to the gate-drain and gate-source overlap regions, evaluating f_t in the linear region, yields [28]:

$$f_t \cong \frac{\mu V_{DS}}{2\pi L^2} \cong \frac{v_s}{2\pi L} \quad (2.9)$$

Where v_s is the carrier saturation velocity under high electric fields.

The equations for I_D , G_m , R_{on} and f_t , highlight the importance of the active semiconductor layer having a high effective-mobility (μ) and saturation-velocity (v_s) for maximizing performance. Additionally, the equations extracted from the square law model show that I_D , G_m , R_{on} and f_t , scale with L_C .

Research in High Performance TFTs

TFTs employing an amorphous-silicon (*a*-Si) active layer have been used for decades for pixel selection circuits in active matrix displays. However, the low electron mobility of these devices makes them unsuitable for high power or high RF applications. Polycrystalline silicon (*poly*-Si) thin films can be used to increase device performance, but typically require fabrication temperatures in excess of 600°C or expensive laser crystallization methods [33].

Given the limitations of Si based TFTs, researchers have begun investigating the use of alternative materials for the active layer in TFTs, most notably metal-oxide semiconductors. TFTs employing amorphous metal-oxide semiconductor thin films have demonstrated high field effect mobility ($>15 \text{ cm}^2/\text{Vs}$) while maintaining low temperature fabrication processes [15, 21, 9, 34]. The improved electron mobility of metal-oxide TFTs is attributed to the ionic bonding property of the semiconductor. As described by Hosono [35], the ionic bonding property of metal-oxides results in electron carrier transport that is largely unaffected by the bond angle or bond length of the atoms with the material. It has therefore been theorized that the electronic properties of amorphous metal-oxide semiconductor thin-films can be comparable to their single crystal counterparts, making them suitable for fabricating high mobility TFTs [35].

Recently, Roubdari *et al.* demonstrated a 10-stage half-bit shift register using amorphous indium-gallium-zinc-oxide (*a*-IGZO) TFT technology that was successfully driven at a maximum clock frequency of 40 kHz [36]. The shift registers were fabricated utilizing bottom-gate *a*-IGZO TFT structures with channel lengths down to 10 μm . Additionally, Geng *et al.* fabricated an 11-stage ring oscillator utilizing both single- and

dual-gate *a*-IGZO TFTs with 2 μm channels that exhibited oscillating frequencies of 334 and 781 kHz, respectively [37]. These efforts demonstrate the potential use of amorphous metal-oxide TFTs in digital logic technology.

Still, amorphous-oxide-semiconductors have limitations in current density and switching on/off ratios, and are therefore not sufficient for high performance RF digital or analog circuits. Conversely, undoped ZnO thin films are considered to be polycrystalline rather than amorphous, with extremely small crystals on the order of 20-50 nm [18]. Undoped nanocrystalline-ZnO thin-films have been shown to be suitable for the fabrication of TFTs capable of reaching small signal microwave performance by Bayraktaroglu *et al.* [13, 12, 18]. Figure 7 shows a scanning electron microscope (SEM) image of a ZnO TFT fabricated by Bayraktaroglu *et al.* along with the extracted small-signal microwave characteristics.

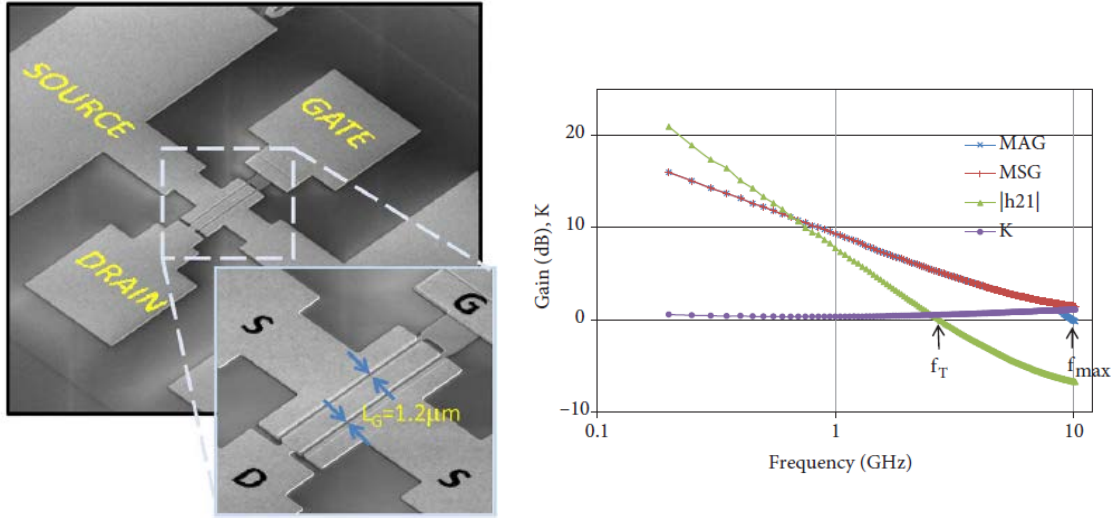


Figure 7: SEM image and small-signal microwave characteristics of a nanocrystalline ZnO microwave TFT with $L_C = 1.2 \mu\text{m}$ and $W_G = 2 \times 150 \mu\text{m}$ developed by Bayraktaroglu *et al.* [13, 18].

The nanocrystalline-ZnO TFTs developed Bayraktaroglu *et al.* were fabricated on highly resistive Si substrates employing a staggered, two-finger, bottom gate structure. A metal lift-off technique was used to pattern source drain ohmic contacts resulting in an active channel length of 1.2 μm . From the measured s-parameters, the maximum available gain (f_{max}) and the unity-gain cutoff frequency (f_t) were determined to be 10 GHz and 2.9 GHz, respectively. According to the authors', this is believed to be the highest frequency operation obtained with any oxide thin-film transistor technology.

Zinc Oxide

Zinc oxide (ZnO) is a II-VI compound semiconductor that is utilized in a wide array of electronic applications. The following sub-sections detail the electronic properties, crystal structure, carrier transport and thin film deposition processes.

Electronic Properties

ZnO has a unique electronic property set, which includes a wide and direct bandgap, large exciton binding energy, high thermal conductivity, and high electron mobility and saturation velocity [38]. At room temperature the band-gap (E_g) of ZnO is ~ 3.3 eV. For comparison the room temperature band gap of common semiconductor materials such as silicon (Si) and gallium-arsenide (GaAs) are 1.1 eV and 1.42 eV respectively [2]. Advantages associated with a large band gap include higher breakdown voltages, the ability to sustain large electric fields, as well as high-temperature and high-power operation. The wide band-gap, in the ultra-violet range of the electromagnetic

spectrum, has also led to the development of optically transparent ZnO based TFTs for use in transparent electronics [20, 39, 16].

Table 1 compares key structural and electronic properties of single crystal ZnO, gallium-nitride (GaN) and Si. GaN is a III-V wide band gap semiconductor material with a band-gap, lattice parameters and optical properties that are very close to that of ZnO. Therefore, many potential electronic and optoelectronic applications of ZnO overlap with GaN. In fact, although GaN is a more mature technology, ZnO is often considered to be an alternative to GaN for several device applications due to its lower production cost [40].

Table 1: Key Properties of single-crystal ZnO, GaN and Si

Parameter	ZnO [41]	GaN [42]	Si [2]
Band gap (eV)*	3.37 (d)	3.39 (d)	1.124 (i)
Lattice Structure	Wurtzite	Wurtzite	Diamond
<i>a</i> parameter (Å)	3.250	3.189	5.43
<i>c</i> parameter (Å)	5.205	5.185	-
<i>c/a</i> ratio (ideal = 1.633)	1.601	1.626	-
Density (g/cm ³)	5.675	6.095	2.328
Melting Point (°C)	1975	2500	1412
Thermal conductivity (W/(cm·K))	0.6	1.3	1.41
Electron mobility (cm ² /vs)	200	900	1417
Saturation velocity (10 ⁷ cm/s)	3.0	2.5	2.3
Breakdown voltage (10 ⁶ /cm)	5.0 [42]	5.0	0.3

**d*= direct, *i*=indirect

One particularly relevant property of ZnO for use in potential military applications is its demonstrated radiation resistance [43]. It has been shown that high energy bombardment by electrons, protons and heavy ions causes much less damage in ZnO compared to other semiconductor materials such as Si, GaAs and even GaN. Additionally, low level defects caused by the radiation have been removed by annealing

at relatively low temperatures. This property makes ZnO especially attractive for space, and nuclear applications where radiation hardened electronics are necessary.

Crystal Structure

Under ambient conditions, ZnO crystallizes in the hexagonal wurtzite structure. The wurtzite ZnO crystal lattice is made up of two interconnecting sub-lattices of Zn^{2+} and O_2^- with a tetrahedral bonding structure, where each zinc atom is surrounded by four oxygen atoms and vice versa [44]. The wurtzite ZnO crystal lattice is illustrated in Figure 8. The lattice constants are $a = 3.25 \text{ \AA}$ and $c = 5.2 \text{ \AA}$, with c/a ratio of 1.60 which is close to the ideal value of $c/a = 1.633$ for a hexagonal cell and a mass density of $d=5.675 \text{ g/cm}^3$ [41]. Although tetrahedral bonding is typically associated with covalently bonded semiconductors, such as in Si and GaAs, the bonding in ZnO is highly ionic due to the large difference in the electronegative values of the two molecules (0.91 for Zn and 3.5 for O). The ionic bonding property of ZnO accounts for the preferential formation of the wurtzite structure rather than the zincblende structure, and gives rise to vastly different electron transport when compared to other covalently bonded semiconductors [41].

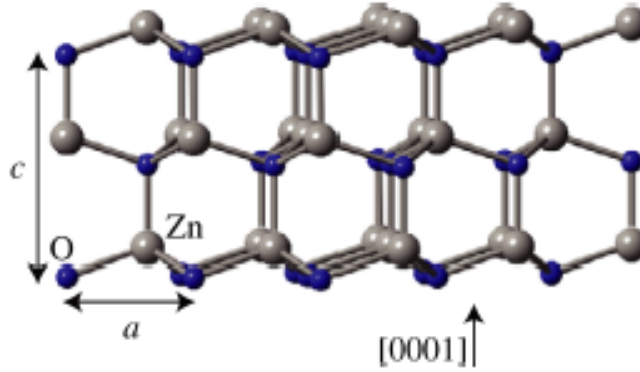


Figure 8: Hexagonal wurtzite crystal structure of ZnO. The lattice constants are $a = 3.25$ Å and $c = 5.2$ Å, with c/a ratio of 1.60 which is close to the ideal value of $c/a = 1.633$ for a hexagonal cell [38]

Electron Transport

In ZnO, the conduction band minimum (E_m) is primarily composed of vacant Zn^{2+} s-orbital's, which results in a conduction path for electron transport that is unaffected by bond angle [27]. This implies that the electron transport of ZnO (and other metal-oxide semiconductors) is unaffected when transitioned from its single-crystal to amorphous phase. In contrast, the conduction band in covalently bonded semiconductors, such as Si and GaAs, is based on hybrid sp^3 -orbitals which have strong sensitivity to bond angle and length, resulting in a decrease in electron mobility in the amorphous compared to single-crystal state. Figure 9 illustrates the orbital drawing an ionic and covalently bonded semiconductor in both the single-crystal and amorphous phase [45]. The theorized high mobility of metal-oxide semiconductors in their amorphous state is one of the main reasons they are attracting significant attention for replacing α -Si TFTs. However, undoped ZnO thin films are regarded to be polycrystalline rather than amorphous, with extremely small crystals on the order of 20-50 nm [18].

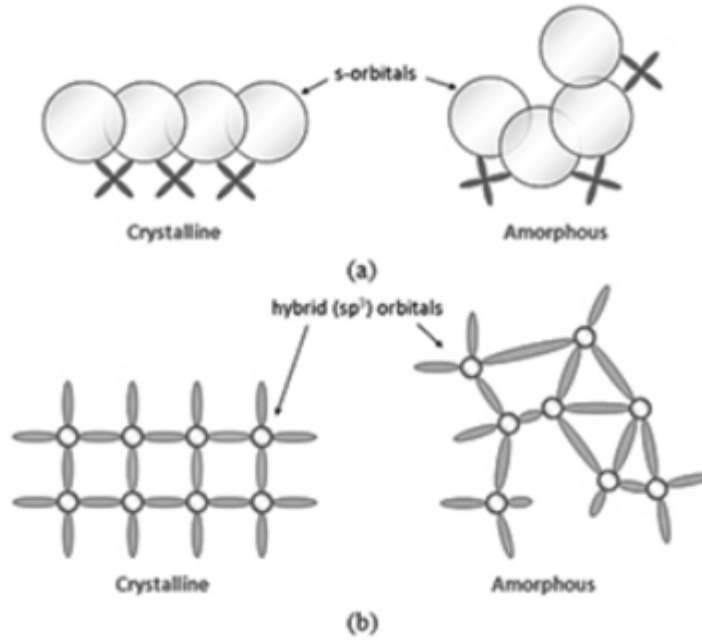


Figure 9: Schematic orbital drawing of the electron pathway in (a) ionic-bonded oxide semiconductors and (b) covalently bonded semiconductors in both the single-crystalline and amorphous phase [45].

Intrinsic Defects

Although undoped ZnO is theorized to be an intrinsic semiconductor, it occurs naturally as n-type [46]. The native n-type doping plays a critical role in the operation of ZnO TFTs, and has led the inability to create reliable p-type films [40]. The background electron carrier concentration of undoped ZnO thin films is typically 10^{16} - 10^{17} cm^{-3} , but has been found to be as high as 10^{22} cm^{-3} [40]. The electron hall mobility of ZnO varies, depending on the growth method, but is typically on the order of $200 \text{ cm}^2/\text{Vs}$ at room temperature [40]. The cause of the native n-type doping is not directly understood and still debated in literature. However, the theory most often cited is that samples are grown under Zn-rich conditions, giving rise to zinc interstitials or oxygen vacancies [47].

Doping characterization of ZnO thin-films is outside of the scope of this research. Focus will concentrate on utilizing available ZnO thin-films deposited at AFRL for device fabrication.

Thin-Film Growth

ZnO thin-films can be deposited by several methods including radio frequency (RF) sputtering, atomic layer deposition (ALD), pulsed laser deposition (PLD), molecular beam epitaxial (MBE) growth, and chemical vapor deposition (CVD) [48]. Recently, solution processed films have attracted a significant amount of attention from research groups due to the high throughput and low cost associated with this process, making it suitable for large scale production [19, 49]. However, ZnO thin films deposited by RF sputtering, PLD and MBE typically exhibit higher mobility than solution processed films.

Under most deposition conditions, ZnO thin-films grow in nanocrystalline form with the c-axes (001) plane of the crystallites oriented perpendicular to the film plane [50]. Due to the orientation of the ZnO thin-film, the electrical transport within the ZnO thin-film, under most applications, is therefore perpendicular to the c-axes of the crystallites. Grain boundaries within polycrystalline semiconductor films typically negatively affect carrier transport due to scattering at the grain boundaries, resulting in a decrease in overall carrier mobility [25]. However, recent studies published by Lorenz *et al.* show that ZnO films deposited by a multistep PLD on c-plane sapphire exhibit mobility values that are comparable to single-crystal ZnO [51]. Additionally, ZnO TFTs employing ZnO thin-films deposited by PLD have shown mobility values which are comparable with that of single crystal ZnO MODFETs [12]. These studies point to higher

structural quality and a lower grain barrier defect density in PLD grown ZnO thin films compared to other deposition methods.

PLD uses high-power laser pulses to melt, evaporate and ionize a single crystal zinc oxide target held under vacuum. This laser ablation process creates a plasma plume consisting of zinc and oxygen ions. The reactive material within the plasma then collects on the surface of a sample, which is placed near the plasma and heated to temperatures between 100-500°C, and condenses to form a ZnO thin film [52]. PLD has been used to grow ZnO thin films on several different substrates including sapphire, glass and aluminum-oxide (Al_2O_3) at temperatures ranging from 200-450°C [53]. The ZnO TFTs developed in this research utilize ZnO thin-films grown by the PLD method at AFRL. Details of the deposition process are outlined in Chapter III.

Contacts to ZnO

As described in the *Thin-Film-Transistors* subsection, source and drain contacts for ZnO TFTs are formed by depositing a metal directly on the ZnO active channel layer. The electrical characteristics of ZnO TFT relies heavily on the formation of ohmic source and drain contact metallization schemes with low contact resistance. When a metal is brought into intimate contact with a semiconductor, electron transfer between the materials occurs until a thermal equilibrium is formed. The electrons transferred and their direction is dependent upon the metal and semiconductor work function (ϕ_M and ϕ_{SC} , respectively) and the electron affinity (χ_{SC}) of the semiconductor [2]. The ZnO thin-films deposited by PLD utilized for device fabrication in this work are n-type, therefore only metal contacts to n-type semiconductors will be discussed in this section.

Ohmic Contacts

The type of contact achieved when a metal is brought with intimate contact of a semiconductor material is governed by the simple Schottky model:

$$q\phi_B = (\phi_M - \chi_{SC}) \quad (2.10)$$

Where ϕ_B is the Schottky barrier height, ϕ_M is the work function of the metal, and χ_{SC} is the electron affinity of the semiconductor.

In order for a metal-semiconductor junction to form a low resistance Ohmic (non-rectifying) contact, ϕ_B needs be near 0 eV [2]. Thus from Equation 2.10, ϕ_{SC} when $\phi_{SC} > \phi_M$ an ohmic contact is formed. Conversely, if $\phi_{SC} < \phi_M$ a rectifying contact is formed. Figure 10 illustrates the band-diagrams of a metal-semiconductor junction prior and after intimate contact. Figure 10.a illustrates the formation of a rectifying contact, while Figure 10.b illustrates the formation of an Ohmic contact.

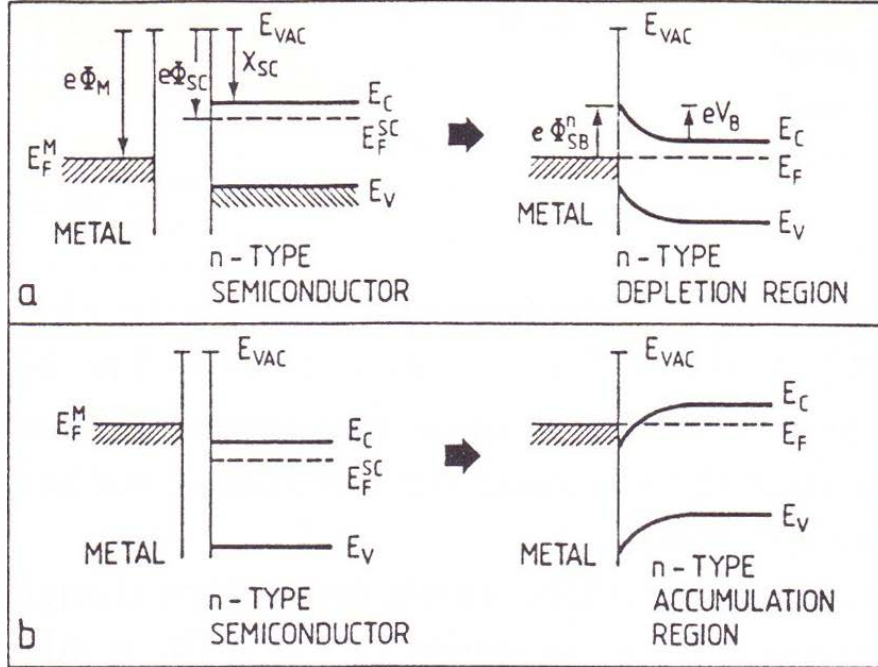


Figure 10: Band diagrams of metal semiconductor junctions shown prior and after intimate contact. a) A Schottky barrier is formed when $\phi_{SC} < \phi_M$. b) A low resistive Ohmic contact is formed when $\phi_{SC} > \phi_M$. Modified from [54]

Ohmic contacts have been demonstrated on n-type ZnO for a wide variety of metals. A list of metal contact schemes for producing ohmic contacts to ZnO was collected by Ip *et. al.*, and is reproduced in Table 3 [55]. Additionally, evaporated Titanium and sputtered tungsten contacts have been reported to achieve low resistant ohmic contact to n-type ZnO by Lim *et. al.* [56].

Table 2: Various Ohmic contact schemes for n-type ZnO

ZnO Type	Metal Contact Scheme	Contact resistance ($\Omega \cdot \text{cm}^2$)
n-ZnO (Al doped)	Ti/Au	2.0×10^{-4}
	Zn/Au	2.4×10^{-4}
	Al	8.0×10^{-4}
	Al/Pt	1.5×10^{-5}
	Re/Ti/Au	1.7×10^{-7}
n-ZnO (P doped)	Ti/Al/Pt/Au	3.9×10^{-4}
n-ZnO (Ga doped)	Pt/Ga	3.1×10^{-4}

Rectifying Contacts

Many different metals, such as Au, Ag, and Pd have been used to form relatively high Schottky barriers of 0.6-0.8eV with n-type ZnO [55]. Contacts that display rectifying or blocking behavior are undesirable for patterning ZnO TFT source and drain contacts as they prevent currents from flowing in one direction. A list of metal contact schemes for producing rectifying contacts was collected by Ip *et. al.*, and is reproduced in Table 3 [55]. These metals must be avoided for fabricating n-type ZnO TFTs.

Table 3: Schottky contacts to n-type ZnO and their respective barrier heights, reproduced from Ip *et.al.* [55]

ZnO Type	Metal	ϕ_B (eV)
n-ZnO on Si	E-beam Au (Schottky)	0.59
n-ZnO on Al_2O_3	E-Beam Ag (Schottky)	0.69-0.83
	E-Beam Au (Schottky)	0.84
	E-Beam Pd (Schottky)	0.59-0.68
	E-beam Au (Schottky)	0.37-0.66
n-ZnO on GaN/ Al_2O_3	E-beam Au (Schottky)	0.37-0.66
n-ZnO bulk	E-beam Au (Schottky)	0.84
	E-Beam-Pt (Schottky)	0.79

Transfer Length Method

There are several methods used for measuring the associated contact resistance of a metal-semiconductor junction, including a four-probe Kelvin connection and a transfer length measurement (TLM). However, due to ZnO's large band-gap and associated high intrinsic resistance of the material, a gated- TLM method is required.

In a gated-TLM method, the total resistance of a MOS device is modeled by three resistors in series: the source resistance, the channel resistance, and the drain resistance [57]. The source resistance (R_{Source}) and drain resistance (R_{Drain}) are shown in Figure 11, with the channel resistance (R_{CH}) contained in the TFT symbol and not explicitly shown. R_{Source} and R_{Drain} are independent of V_{GS} and L_C , whereas R_{CH} is controlled by the voltage across the gate and is directly proportional to the L_C the device.

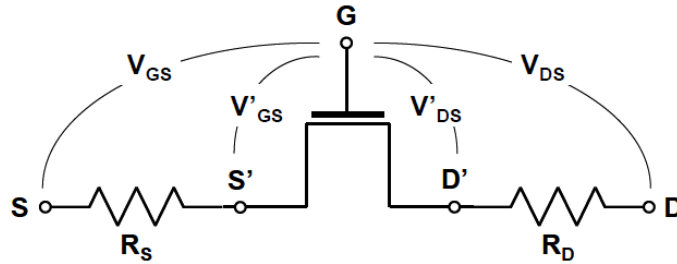


Figure 11: A TFT with source and drain resistances, the channel resistance is contained within the TFT symbol (modified from [57]).

As shown by shown by Schroder [57], the gated-TLM method involves measuring the R_{on} (sometimes called the measured or total resistance) of devices with various channel lengths operating in the linear region. The R_{on} of a device is then given by [57]:

$$R_{on} = \frac{\Delta V_D}{\Delta I_D} = R_{CH} + R_{Source} + R_{Drain} \quad (2.11)$$

Where R_{CH} is the channel resistance in Ohms (Ω), and R_S and R_D are the parasitic source and resistances, respectively. Replacing $R_{CH} = R_s \frac{L_C}{W_C}$ and $R_{SD} = R_{Source} + R_{Drain}$

Equation 3.1 becomes [57]:

$$R_{on} = R_s \frac{L_c}{W_c} + R_{SD} \quad (2.12)$$

Where R_s is the sheet resistance of the ZnO channel in $\Omega/\square$, R_{SD} is the total parasitic source and drain resistance on both sides of the device, and L_C and W_C are the channel length to width, respectively. Therefore, by plotting R_{on} at various gate voltages versus L_C ; the total parasitic source and drain series resistance (R_{SD}) can be extracted from the $L_C = 0$ point on the line of best fit between the points. Additionally, R_s can be extracted from the slope of $(\rho_s/W_C = \Delta R_{on}/\Delta L_C)$ of the line of best fit on the same R_{on} versus L_C plot.

A secondary benefit of the gated-TLM process is that the intrinsic field effect mobility ($\mu_{fe,i}$) and threshold voltage (V_{ti}) can be extracted. From the ideal TFT equation R_s can be expressed as a function of mobility and gate voltage by [58]:

$$R_s = \frac{1}{\mu_{fe,i} C_{ox} (V_G - V_{t,i})} \quad (2.13)$$

Where $\mu_{fe,i}$ is the intrinsic mobility, C_{ox} is the gate capacitance per unit area and v_{ti} is the intrinsic threshold voltage. Thereby, plotting the inverse of R_s versus gate voltage, the intrinsic threshold voltage (V_{ti}) and field effect mobility can be extracted from the x-intercept and slope, respectively. The intrinsic TFT parameters (V_{ti} and $\mu_{fe,i}$) represent the electrical characteristics of the conduction channel without the influence of parasitic source and drain series resistances [58]. Thus, by extracting $\mu_{fe,i}$ the electron transport characteristics of the ZnO thin-film can be directly measured.

Fabrication Processes and Definitions

The ZnO TFTs fabricated in this thesis were completed using standard surface micromachining fabrication processes. Surface micromachining includes the deposition of thin-films of various materials (including metals, dielectrics and semiconductors) and utilizing lithography, lift-off and etching techniques to define geometric shapes within and on those films. The following sections provide a brief overview of the microelectronic fabrication processes used throughout this work.

Film Deposition

The fabrication of ZnO TFTs involves many steps in which thin-films of various materials are deposited on the substrate surface. Deposition of material thin-films, including metals, semiconductors and dielectrics can be accomplished using various methods. Some examples include DC and RF sputtering, chemical vapor deposition (CVD) and electron-beam evaporation. Evaporation and sputtering require vacuum systems operating at low pressure, whereas CVD can be performed under vacuum or

atmospheric pressure. Deposition of ZnO thin films was discussed previously; therefore this section will discuss deposition of ohmic materials. Ohmic metal deposition in this thesis was accomplished using sputtering and evaporation.

Sputtering

Sputtering is achieved by bombarding a target with energetic ions, such as Ar^+ [59]. The atoms on the surface of the target are knocked loose through a ballistic exchange of momentum with the energetic ions, and are then transported to the substrate where deposition occurs. Due to the low substrate temperatures used, sputtering is an ideal method to deposit contact metals for TFTs. However, because sputtering is a physical process, it can also be used for depositing a wide variety of other materials, including dielectrics and semiconductor materials. For electrically conductive materials such as Aluminum, tungsten and titanium, a simple DC power source is used, in which the target acts as the cathode in a diode system [60]. For dielectric materials, an RF plasma must be used. The sputtering process typically results in a conformal film with good step coverage even on vertical sidewalls.

Electron Beam Evaporation

In electron-beam evaporation systems, a high-intensity beam of electrons is focused on a source target containing the material to be evaporated [59]. The energy from the electron beam is used to melt a small portion of the surface of the target. The melted material then evaporates off of the source target and covers the sample with a thin layer. The deposition rate is controlled by changing the current and energy of the electron beam

[60]. Unlike sputtered films, evaporation results in a non-conformal film over the surface of the substrate which becomes discontinuous on vertical walls. Although this non-conformal coverage causes issues in some topologies, it can be used as an advantage when performing an additive lift-off process for patterning films.

Lithography

Lithography is used to define regions where etching or film deposition will take place, and is at the heart of microelectronic and transistor fabrication processes. There are several variations of lithography, two of which are used for device fabrication in this thesis: optical and electron-beam lithography. Optical (or photo) lithography uses light to transfer a geometric pattern from a photomask to a light-sensitive polymer, called a photoresist, which is coated on the sample surface. Electron-beam lithography is a direct write process which uses a focused beam of electrons to draw custom patterns on the surface of a substrate coated with an electron-beam sensitive polymer.

Optical Lithography

Figure 12 illustrates a schematic of a simplified contact optical lithography system [61]. The system uses an optical source to shine light through a photomask. The photomask image is then projected onto the surface of a sample which is coated with a light-sensitive polymer, called a photoresist. The chemical structure of the photoresist is modified when exposed to the incident light. For positive tone resists, the polymer bonds of the material decompose when exposed to light. Conversely, in a negative tone resist, the chemical bonds are strengthened (polymerized) when exposed to light. After

exposure, the weakly bonded areas of resist are dissolved using a solvent solution, called a developer, reproducing the mask pattern in the resist [60].

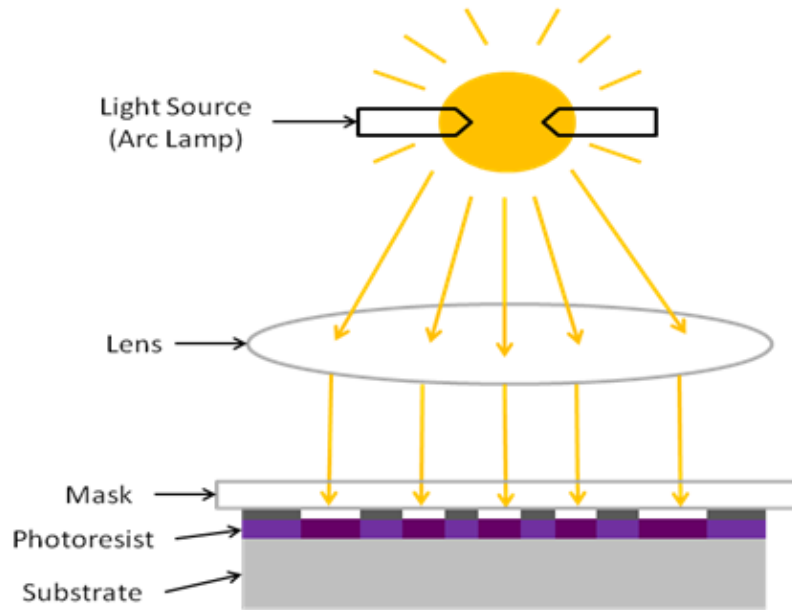


Figure 12: Cross sectional diagram showing a simple contact exposure lithography system [61]

Standard contact optical lithography can pattern features with resolutions no smaller than the wavelength (λ) of the light source used for exposure [60]. The Karl Suss MA6 Mask Aligner located in the AFRL clean room utilizes an ultra violet (UV) source with $\lambda = 365$ nm, thus mask feature sizes are limited to approximately 0.5 μm . To overcome this limitation, other optical lithography sources with shorter wavelengths or projection and immersion printers which use diffraction can be used to reduce the minimum feature size. However, these systems are not utilized in this work.

Electron-Beam Lithography

Due to the limits of the optical lithography, electron beam (e-beam) lithography will be used to scale critical dimensions of ZnO TFTs in this thesis. E-beam lithography uses a focused beam of electrons to deliver energy to the resist. As with optical lithography, the energy changes the solubility of the resist enabling selective removal of the exposed regions through developing. However, unlike standard optical lithography this is a “direct write” process, meaning there is no need for a photomask. Additionally, due to the higher energy of the electron beam, e-beam lithography can be used to produce line-widths below 50 nm [62].

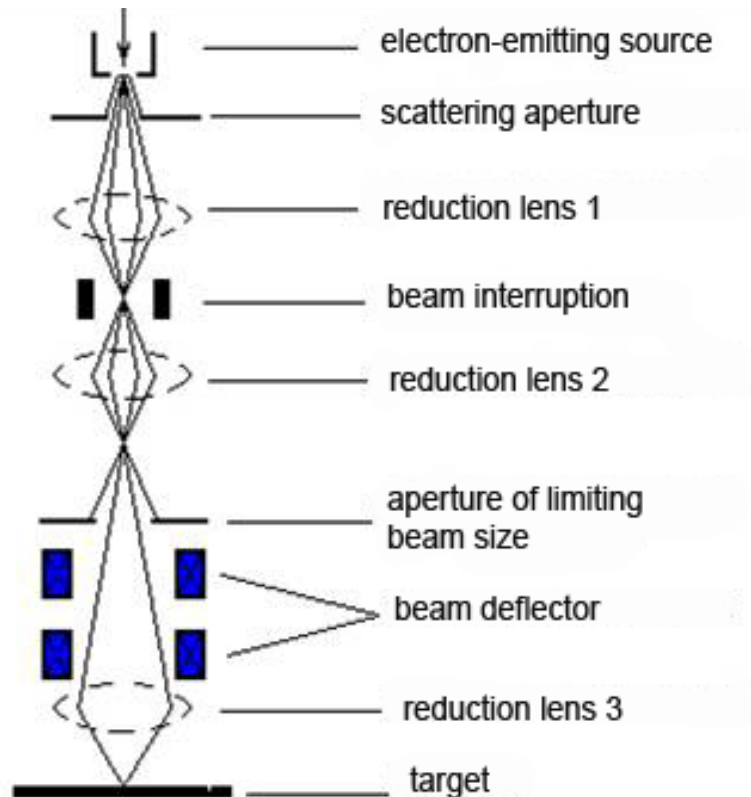


Figure 13: Simplified cross-sectional schematic of an electron-beam lithography exposure system [63]

Figure 13 illustrates a basic schematic for an e-beam lithography scanning system [63]. In this system, high energy electrons are produced at the source (or cathode) through thermionic or field emission. Next, the generated electrons are formed into a narrow beam using a series of electrostatic apertures and lenses. The focused electron beam strikes the surface of a sample coated with an electron sensitive resist. The electron energy is then transferred to the resist, decomposing the polymer bonds, making the exposed regions of the resist more soluble. The weakly bonded areas of resist are then dissolved using a solvent solution called a developer, reproducing the mask pattern in the resist. Examples of common e-beam resists include polymethyl-methacrylate (PMMA) and ZEP-520a [64, 65].

Pattern Transfer

After a pattern is formed in a resist, the next step involves transferring that pattern to the substrate. This is typically accomplished through an additive lift-off process or a subtractive etch process. The etch-back process can be accomplished using either an immersion wet-etch or plasma-etch method. In both the lift-off and subtractive etch processes, the objective is to reproduce a patterned ohmic thin-film on a substrate. However, due to its ability to produce sub-micron line widths, the subtractive process utilizing a plasma-etch method dominates production pattern transfer [66]. Figure 14 compares the processing steps for patterning ohmic contacts to ZnO using a subtractive back-etch process to an additive lift-off process.

In the subtractive process, an ohmic metal film is first deposited as a uniform layer over the entire ZnO surface. Next, to pattern the ohmic contacts, an etch mask is

formed on top of the ohmic film using lithography. The etch mask is utilized as a stencil that protects the underlying ohmic material from attack during the etch process. Etching of the unprotected areas can either be accomplished utilizing a wet-etch or gaseous plasma-etch process. After etching is complete, the remaining mask is stripped off, leaving behind the desired pattern. In the additive process, the pattern is formed at the same time the metal film is deposited. First, a resist pattern mask is formed on the ZnO surface using lithography. The desired ohmic film is then deposited over the mask and onto the uncovered ZnO areas. After deposition, the remaining resist is removed, “lifting-off” the unwanted metal from the masked areas, leaving behind the desired metal pattern.

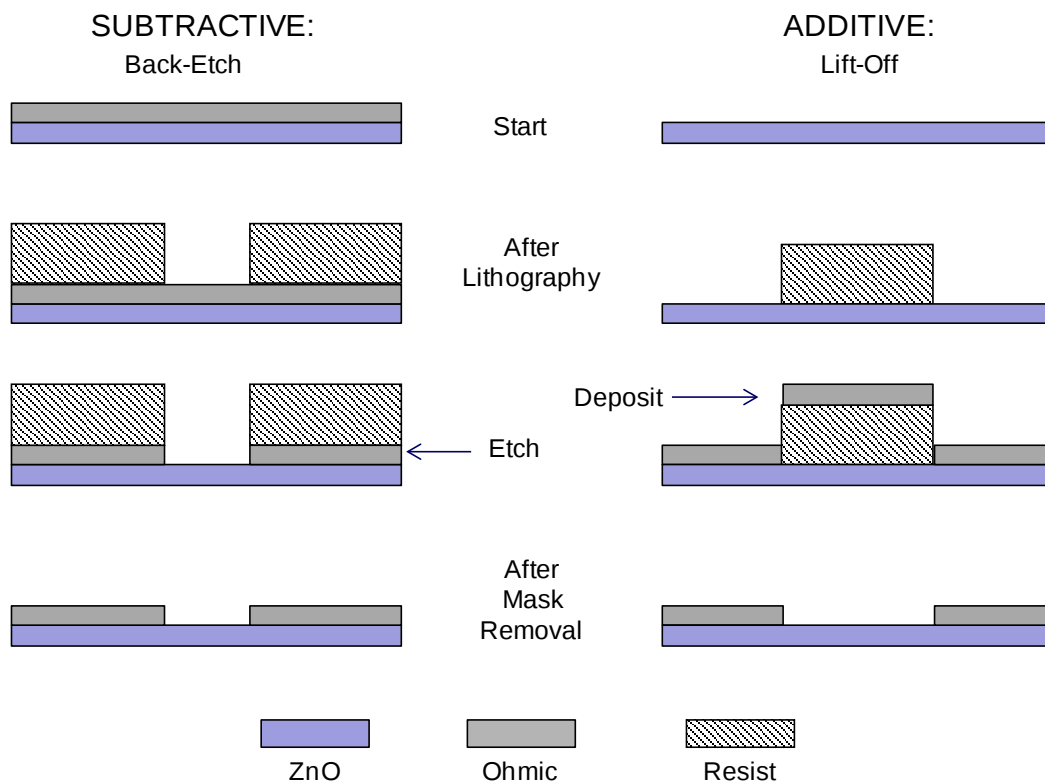


Figure 14: Cross sectional schematic detailing the processing steps for an additive lift-off process versus a subtractive back-etch process for patterning ohmic films on ZnO.

ADDITIVE: Lift-Off

In a typical bi-layer lift off process, a photoresist stack is first coated on the surface of the sample through spin coating. The resist stack is then selectively exposed and developed; thereby defining areas where metal is to be deposited. A metal film layer is then deposited over the entire surface of the wafer. Any material deposited on top of the photoresist layer is then subsequently removed along with the remaining resist using a solvent stripper, leaving the patterned material on the substrate surface. However, for the lift-off process to work properly there must be a small gap between the upper and lower films, otherwise tearing and incomplete liftoff will occur [59]. This is accomplished by forming an undercut in the bottom resist layer. Also, given the need for a gap between the metal areas, conformal metal deposition methods, such as sputtering, is not well-suited to a bi-layer lift-off process [60]. Figure 15 illustrates cross sectional SEM images detailing a typical lift-off process [67].

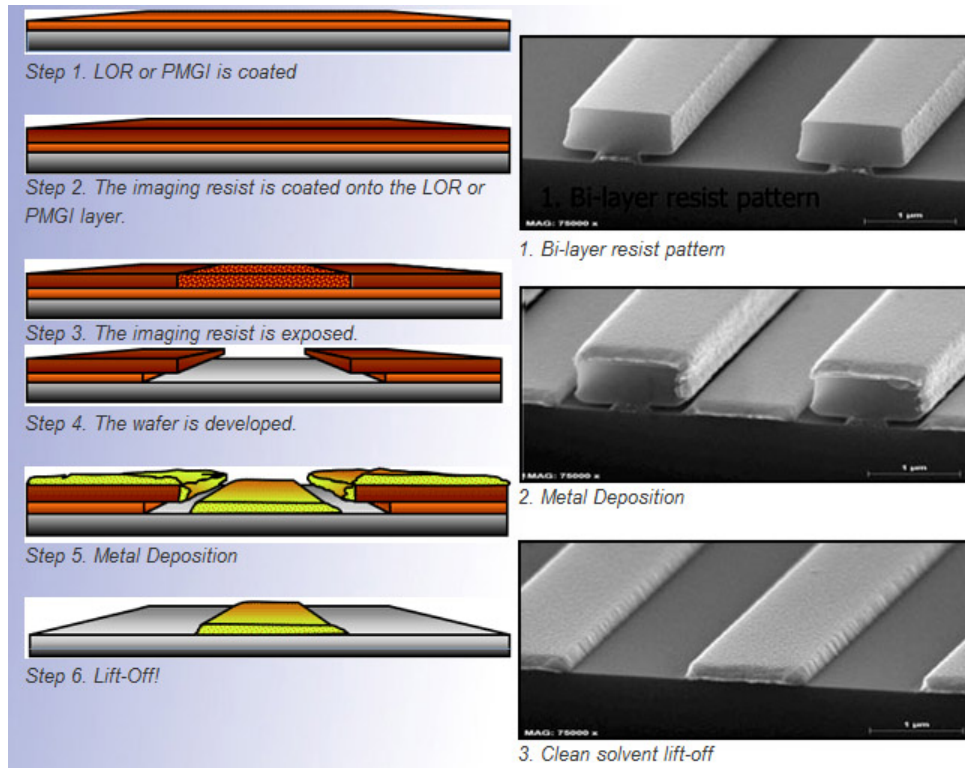


Figure 15: Series of drawings and SEM images detailing a typical bi-layer lift-off process [67]

The lift-off process is a simple damage free method for patterning metal structures and is often utilized in cases where etching of metal material would have undesirable effects on the underlying layer [60]. However, during processing the lifted off metal may redeposit on the surface of the wafer, reducing the overall yield. Most importantly, for device scaling, due to the need for an undercut in the resist stack, lift-off processing is typically limited to geometries of approximately 0.5- μm , and is therefore not a suitable process for defining the active channel for high RF ZnO TFTs requiring channel lengths below 200 nm.

SUBTRACTIVE: Wet Etching

Wet etching is a purely chemical process in which the sample is immersed in a reactive solution in order to remove unwanted material from the substrate surface [60]. In this process the patterned resist is used as an etch mask, blocking the unexposed regions of the sample from being chemically attacked and etched away. Two important figures of merit for etching are: selectivity and isotropy. Selectivity is the measure of the material etch rate versus the masking material. Isotropy is a measure of the etch uniformity in both the lateral and vertical directions. Typically, etches that are both highly selective and anisotropic (e.g. highly directional) are preferable for accurate pattern transfer.

Although wet etching can be a highly selective process and typically does not damage the substrate, it suffers from serious drawbacks; most notably a lack of anisotropy and poor process control. Anisotropy (A) is a measure of the vertical etch rate versus the lateral etch rate of a material, and is given by [60]:

$$A = 1 - \frac{R_L}{R_V} \quad (2.14)$$

where R_L and R_V are the lateral and vertical etch rates respectively. A process is perfectly anisotropic if the lateral etch rate is zero (i.e. $A=1$). Conversely, $A=0$ means that the lateral and vertical etch rates are identical.

Most wet etch processes have a very low anisotropy ($A \cong 0$), which results in significant undercutting of the etch mask and an increase in feature size [60]. Figure 16 depicts a typical isotropic etch profile compared to an anisotropic etch profile. As depicted, the isotropic etch undercuts the etch mask, resulting in an increase in feature

size when compared to the mask. Conversely, an anisotropic etch creates a near vertical etch profile, retaining the exact dimensions of the masking layer.

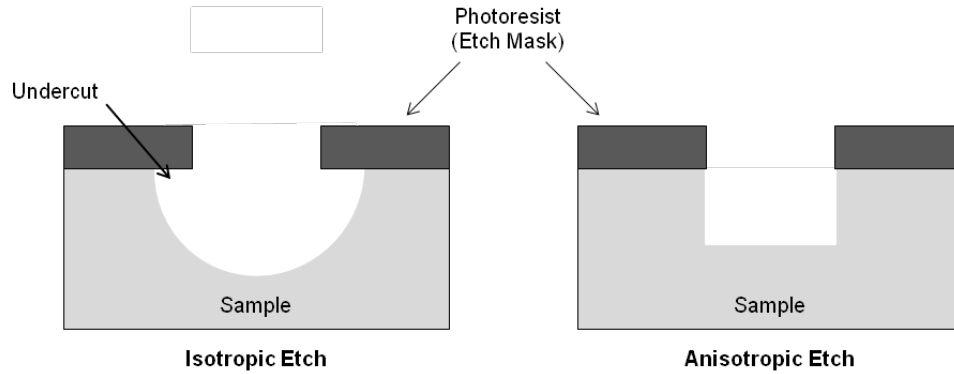


Figure 16: Cross sectional illustration of an isotropic etch profile showing undercutting of the etch mask versus an anisotropic etch profile.

Although wet etching is material and process specific, it typically has very low anisotropy and results in undercutting of the mask. Thus, wet etching is typically limited to feature sizes no smaller than 2 μm . Wet etching is further complicated when attempting to define source and drain ohmic contacts for nanocrystalline ZnO TFTs due to the inherent high etch rate of ZnO in common wet-etchant solutions. For these reasons, wet etching was not pursued for fabricating ohmic source and drain contacts for high performance ZnO TFTs in this thesis.

SUBTRACTIVE: Plasma Etching

Due to the large amount of undercutting associated with wet etching, modern fabrication processes requiring small geometries (below 1 μm) avoid wet chemical etching and instead use a plasma etch process. Etching in a plasma environment has several advantages compared to wet chemical etching. These advantages include less

chemical waste, improved process control and the possibility of high anisotropies [60]. These factors make plasma etching a more repeatable process than wet chemical etching and are critical for defining sub-micron features sizes.

Reactive ion etching (RIE) is one of the most widely used plasma etching technologies due to its capability of producing highly anisotropic etch profiles [68]. RIE uses a chemically reactive plasma to both physically and chemically remove material from the surface of a sample. A simplified RIE plasma system is shown in Figure 17 [69]. In this system, etch gases flow into a chamber at vacuum pressure until a stable chamber pressure is reached. Next, application of RF power ionizes the gas molecules creating a plasma. A plasma is a mixture of excited neutral species, ions and electrons created in a high-frequency electric field [66]. The ignition of the plasma results in a difference in charge between the plasma and the electrodes which contain the plasma. The difference in charge corresponds to a formation of an electric field between the electrodes and the plasma. Thus, the ions within the plasma are accelerated through the electric field towards the masked sample. Once on the sample surface, the ions chemically react with the exposed film and physically attack the sample through the transfer of kinetic energy [66]. By proper choice of the reactant gases, electric field power, and chamber pressure, the etching reaction can be made anisotropic so that nearly vertical sidewalls are formed at the edges of the mask.

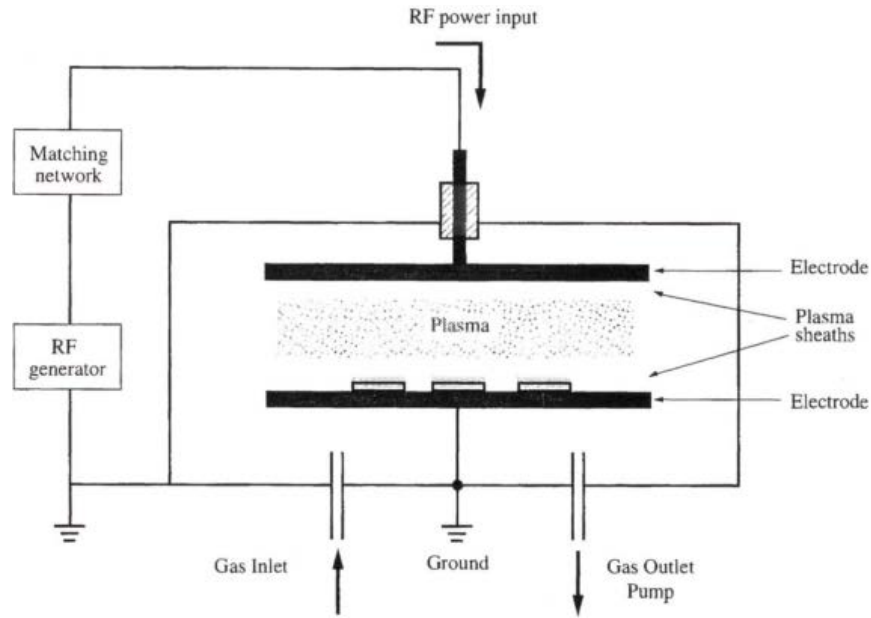


Figure 17: A simplified schematic of a common plasma RIE system [69]

One major issue with RIE plasma process is that the sample is exposed to energetic radiation bombardment. This radiation consists of ions, electrons, ultraviolet photons and soft-x-rays, with energies ranging from tens to hundreds of volts [66]. When the high energy radiation from the plasma strikes the sample surface, it can induce damage, altering the electrical characteristics of the material and degrading device performance. In general, the significance of these effects increases with particle energy [66]. Therefore, the electric field power and chamber pressure need to be optimized in order to reduce radiation effects, while also maintaining an anisotropic etch profile. However, it has been shown that high energy bombardment by electrons, protons and heavy ions causes much less damage in ZnO compared to other covalently bonded semiconductor materials [43].

Due to its ability to create anisotropic etch profiles, RIE plasma etching will be utilized in this thesis for patterning source/drain ohmic contacts and defining the active channel of ZnO TFTs. For the RIE process to be effective, the etch gas chosen needs to chemically react with the ohmic material to be removed without damaging the underlying ZnO layer. Additionally, etch mask materials must be chosen that can withstand the high energy ions and photons associated with the plasma-etch process.

Summary

This chapter presented background literature and previous research critical to the understanding of ZnO TFT design fabrication and characterization. The structure and operating principles of TFTs were first introduced and important figures of merit were discussed. Relevant literature in ZnO TFT development was also explored, with an emphasis on device scaling for high RF performance. Finally, various microfabrication techniques were discussed, including photolithography and pattern transfer techniques. Particular attention was given to plasma and RIE etching processes which is required for scaling device critical dimensions. As a whole, the ideas and knowledge presented in this chapter form a basis for the decisions made in the ensuing methodology chapter.

III. Methodology

Chapter Overview

This chapter presents and discusses the materials, equipment, device fabrication and testing methodology utilized to evaluate the subtractive plasma-etch process for developing nanocrystalline-ZnO TFTs.

Materials and Equipment

The TFTs for this research were fabricated and tested in a class 100 cleanroom located at the Air Force Research Lab (AFRL), Sensors Directorate, Wright Patterson Air Force Base, Ohio. The following paragraphs provide an overview of the materials and equipment utilized for device fabrication and testing.

Lithography Mask Set

The Air Force Research Laboratory (AFRL), Sensor Directorate, has developed a photolithographic mask-set capable of fabricating fully-functional ZnO TFTs for DC and RF characterization. A reduced version of this mask-set was utilized for device fabrication in this thesis. The mask-set was designed to be used with the Karl Suss MA6 Mask aligner and allows for rapid device fabrication for process and device investigation. Contact resistance, mobility, transconductance and other important device information can be obtained from devices fabricated using AFRL's existing maskset. The fabricated devices employ an inverted staggered, two gate finger structure, with various channel lengths (L_C) ranging from 10- μm down to 1- μm . The channel width (W_C) of the fingers is

150- μm with L_C fixed for each finger. Figure 18 illustrates a typical two-gate finger ZnO TFT fabricated in this thesis.

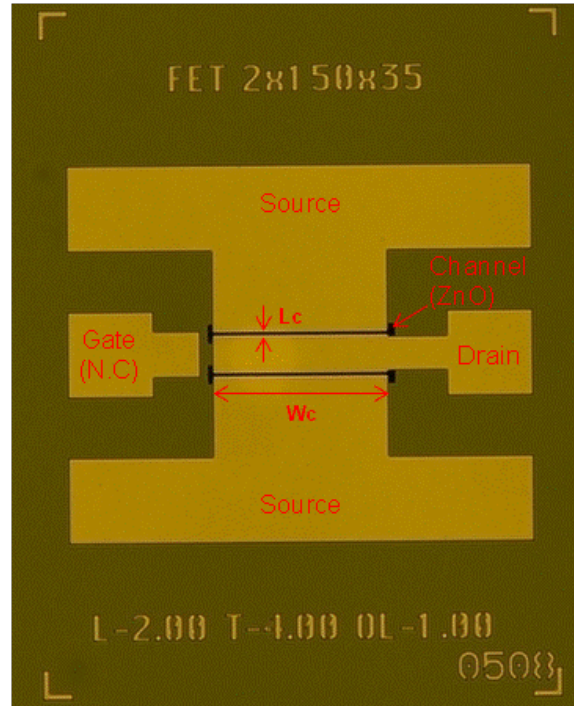


Figure 18: Optical image of a ZnO TFT fabricated in this thesis using AFRL's existing photo-mask set. The sources, drain and non-functional gate pad are labeled, along with the active ZnO channel, channel width (W_c) and channel length (L_c).

Zinc-Oxide Thin Films

The ZnO films thin-films used throughout this thesis were deposited by pulsed laser deposition (PLD) at AFRL. Several previous studies were conducted on the PLD films at AFRL which show that the ZnO films are composed of spontaneously ordered and closely packed 30-50nm diameter grains which are predominately c-axis (002) orientated [18, 17].

The PLD system used was a Neocera Pioneer 180, with a KrF excimer laser ($\lambda=$ 248 nm operating at 30 Hz with a 10 ns pulse duration and an energy density of 2.6-

J/cm². The base chamber pressure of the system was set to 1×10^{-7} Torr with a 10 mTorr O₂ partial pressure throughout the deposition process. The target was a sintered ZnO ceramic disk (99.999%) measuring 50-mm in diameter and 6-mm thick. The 3" Si substrate with 20 nmAl₂O₃ isolation layer was rotated at 20°/sec while the ZnO target was rotated at 40°/sec, raster velocity of $\pm 2^\circ$ at 5°/sec. The distance from target to the substrate was 9.5 cm and shifted by approximately 5 cm off the rotation axis. Laser raster velocity with an inverse velocity profile was accomplished through laser focusing optics mounted to and controlled by a programmable traveling optical train mechanism. This inverse velocity profile results in a constant laser footprint size on the target throughout its scanning speed range. These parameters combined yielded a film with 8% variation in thickness on the substrate.

After deposition, the ZnO thin-films were annealed in atmosphere at 400°C for one hour. The bake temperature and time resulted from a design of experiments in an attempt to identify the optimal grain size resulting in the highest current density of ZnO semiconductor for best device performance [18].

Source and Drain Contact Materials

Tungsten and titanium-tungsten (10:90 alloy) films were chosen as ohmic contact materials to be selectively etched against ZnO for patterning source and drain contacts in this thesis. Both tungsten and titanium-tungsten are used extensively in microelectronic applications for interconnects and electrical contacts. Additionally, a previous study demonstrated that both tungsten and titanium-tungsten films can be etched in a fluorinated plasma with high selectivity (>35:1) to ZnO [22]. The tungsten and titanium-

tungsten ohmic films were prepared using a sputter-deposition method in a Denton Discovery 18 Sputtering System. The power was 250W. The inert gas used was Ar at a flow rate of 75.8 sccm, resulting in a chamber pressure of 4.0-mTorr. The metal was sputtered for 270 seconds to achieve a thin-film 1000-Å nominal thickness, resulting in a deposition rate of 3.70 Å/sec.

Aluminum-Oxide

Aluminum-Oxide (Al_2O_3) was utilized as the gate-dielectric material for fabricating ZnO TFTs in this thesis. Al_2O_3 is considered a high- k material with an ideal dielectric constant of 9.34, compared to 3.9 for SiO_2 . The higher dielectric constant of Al_2O_3 enables a larger C_{ox} value to be achieved using the same gate dielectric thickness that would be possible using SiO_2 [70]. More importantly, unlike SiO_2 which etches readily in fluorine based plasmas, Al_2O_3 will not be attacked during the RIE process.

The Al_2O_3 films used for device fabrication in this thesis were deposited using an atomic layer deposition (ALD) technique. ALD is a vapor-phase deposition process that is based on the controlled reactions between the vapor-phase precursor molecules and the substrate surface [71]. Al_2O_3 films grown by the ALD method are typically highly amorphous and highly insulating. Additionally, the ALD process can be accomplished on a variety of substrates, including oxides, metals, and semiconductors. For device fabrication in this work, the Al_2O_3 films utilized were deposited by ALD on heavily doped 3" n-type Si (1-10 $\Omega\cdot\text{cm}$) at 177°C, resulting in a 20 nm thick Al_2O_3 film.

RIE Plasma System

Etching of tungsten and titanium-tungsten was accomplished using a Unaxis 790 series RIE Plasma Processing System. The 790 series RIE tool at AFRL has several available etch gases including sulfur-hexafluoride (SF_6), carbon-tetrafluoride (CF_4), oxygen (O_2) and argon (Ar). A mass-flow controller (MFC) maintains the flow rate of each gas. The pressure is controlled separately by a butterfly valve between the chamber and the pump. The maximum available RF power is 300 Watts.

The 790 series tool allows for various etch recipes, which include chamber pressure, gas flow, and power. The RIE recipes used for device fabrication throughout this thesis were SF_6 and CF_4 mixed with O_2 , or more simply CF_4/O_2 . For experimental simplicity, the flow rates of SF_6 or CF_4 were fixed to 40 sccm, and the O_2 percentage in CF_4 gas was 7.5% for all RIE chemistries. The chamber pressure was fixed to 40 mTorr. Varying RF power settings ranging from 50-200W were utilized for device fabrication, resulting in a total of eight different etch recipes used throughout this thesis. Table 4 details the RIE recipes used throughout this research. The displayed DC bias was recorded from the 790 series RIE Plasma tool 15 seconds after the plasma was ignited. In general the displayed DC bias gives a rough estimate of the magnitude of the induced electric field between the plasma sheath and the electrode where the sample is placed, thus providing insight into the magnitude of the ion bombardment energy of the etch. However, while the DC bias is a useful control variable for monitoring or characterizing the process, it is as much a function of the reactor geometry and matching network parameters as it is of the ion bombardment energy [66].

Table 4: Various RIE etch recipes used for device fabrication.

Etch Gas	Gas Flow Rate (sccm)	Chamber Pressure (mTorr)	RF Power (Watts)	*DC Bias (Volts)
CF ₄ /O ₂	40/2	40	200	465
CF ₄ /O ₂	40/2	40	150	223
CF ₄ /O ₂	40/2	40	100	184
CF ₄ /O ₂	40/2	40	50	111
SF ₆	40	40	200	205
SF ₆	40	40	150	130
SF ₆	40	40	100	85
SF ₆	40	40	50	40

Material Etch Rate Study

Prior to device fabrication an etch study was conducted to calculate the etch rate of tungsten and titanium-tungsten in each recipe outlined in Table 4. The etch study was conducted by depositing 5000 Å of each ohmic material (e.g. W and TiW) on SiO₂ covered 4" n-type Si wafers. A patterned layer of NANOTM PMGI SF11 resist patterned using optical lithography was used as an etch mask. After patterning, the sample was scored in 4x4 cm² samples etched using the 790 series plasma tool using a CF₄/O₂ or SF₆ plasma at RF powers ranging from 50-200W. Any remaining resist was then removed using MICRPOSITTM 1165 stripper heated to 70°C for 2 min, and the sample was rinsed in de-ionized (DI) water and dried with N₂. Etch rates were calculated by measuring the step height at the etch boundary using a stylus profilometer divided by the etch time. The profilometer measurements were taken using a KLA Tencor P-16 profilometer.

Figure 19 and Figure 20 detail the calculated etch rates of tungsten and titanium-tungsten in both the CF₄/O₂ and SF₆ etch chemistries versus RF plasma power.

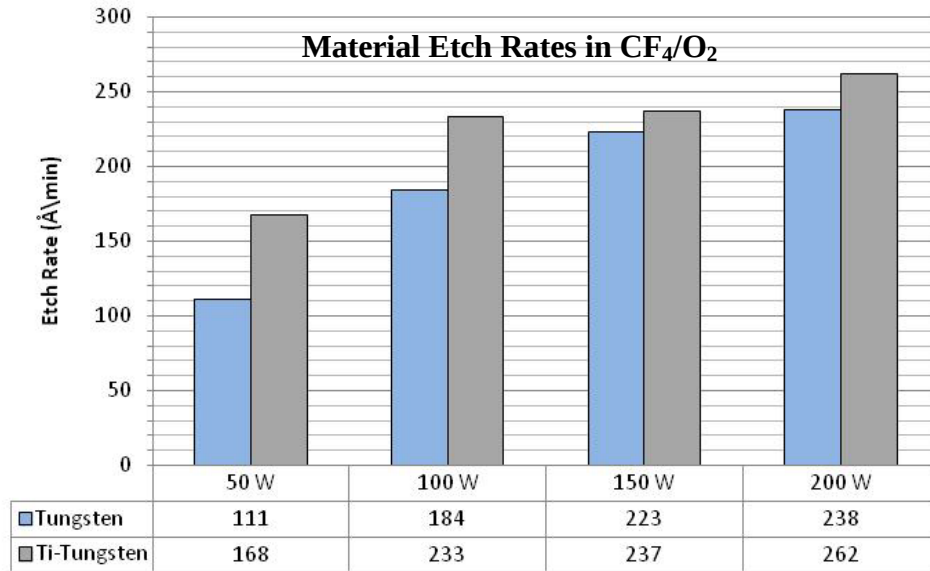


Figure 19: Calculated etch rates of tungsten and titanium-tungsten using various CF₄/O₂ etch recipes in the Unaxis 790 series RIE Plasma Processing System

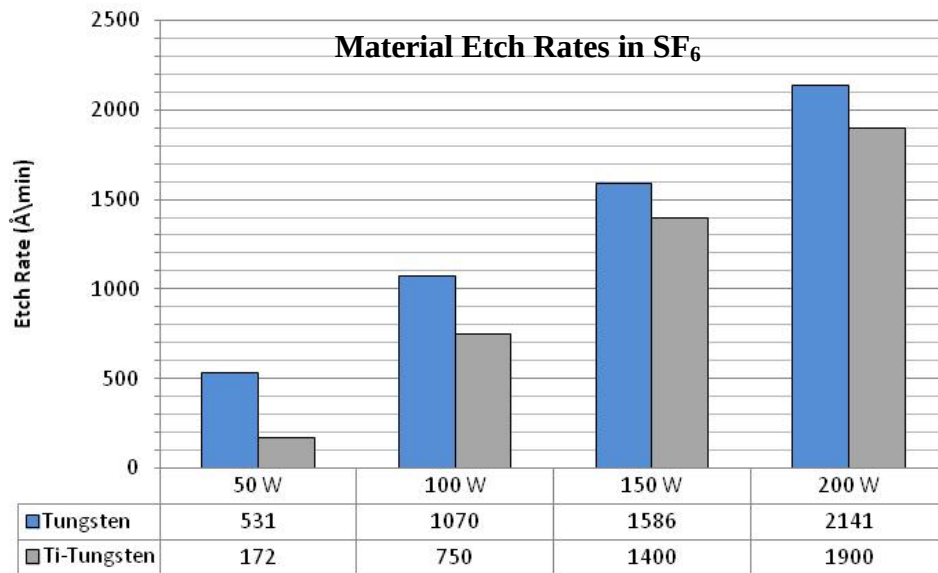


Figure 20: Calculated etch rates of tungsten and titanium-tungsten using various SF₆ etch recipes in the Unaxis 790 series RIE Plasma Processing System

Device Fabrication

Substrate gated ZnO TFTs utilizing a subtractive plasma-etch process for DC analysis were fabricated on 3" n-type Si wafers. The devices employed a two-gate finger structure, with channels defined by etching ohmic material against ZnO using the RIE recipes detailed in Table 4. Both optical and e-beam lithographical defined devices were fabricated.

Optical Lithographical Defined Devices

ZnO TFTs utilizing a subtractive plasma-etch process were initially fabricated using an optical lithographical defined metal etch mask, resulting in devices with channel lengths ranging from 10 μm to 1 μm . The metal etch mask consisted of a Ti/Pt/Au/Ni (200/300/2500/200 Å) metal film patterned by standard bi-layer lift-off method.

Fabrication Overview

The optically defined devices were prepared by depositing 20 nm of Al_2O_3 on 3" n-type Si (1-10 $\Omega\cdot\text{cm}$) wafers which served as the gate dielectric and gate electrode, respectively. Next, the semiconductor active layer, consisting of a 50 nm ZnO thin film was deposited by PLD. The entire sample was then annealed at 400°C for one hour in atmosphere. After anneal, 1000 Å of ohmic metal (either tungsten or titanium-tungsten) was deposited over the entire sample using a sputter deposition method. Next, a Ti/Pt/Au/Ni (200/300/2500/200 Å) metal stack was evaporated over the entire sample and defined using a standard bi-layer lift-off method. The metal stack was utilized for

both source and drain ohmic pads as well as an etch mask in the RIE process to define the channel.

Device isolation was accomplished by using a NANOTM PMGI SF11 resist patterned by DUV lithography while utilizing MICRPOSIT S1805 as the imaging resist. After developing the PMGI and stripping the S1805 in acetone, the ohmic material in the field was etched in the Unaxis 790 series RIE Plasma tool using a SF₆-RIE at 15W. The field ZnO was then etched away using a 1000:1 ratio of DI:HCl for 25 seconds. The remaining resist was stripped in micropsit 1165 PR stripper, rinsed in DI water, dried with N₂, and ashed in O₂ for 2 min. Each sample was then scored in 4 cm² pieces and the device channels were opened using the metal pattern as an etch mask using one of the RIE chemistries detailed in Table 4. A 50% over-etch time was utilized for each RIE chemistry. Figure 22 illustrates the typical device fabrication process.

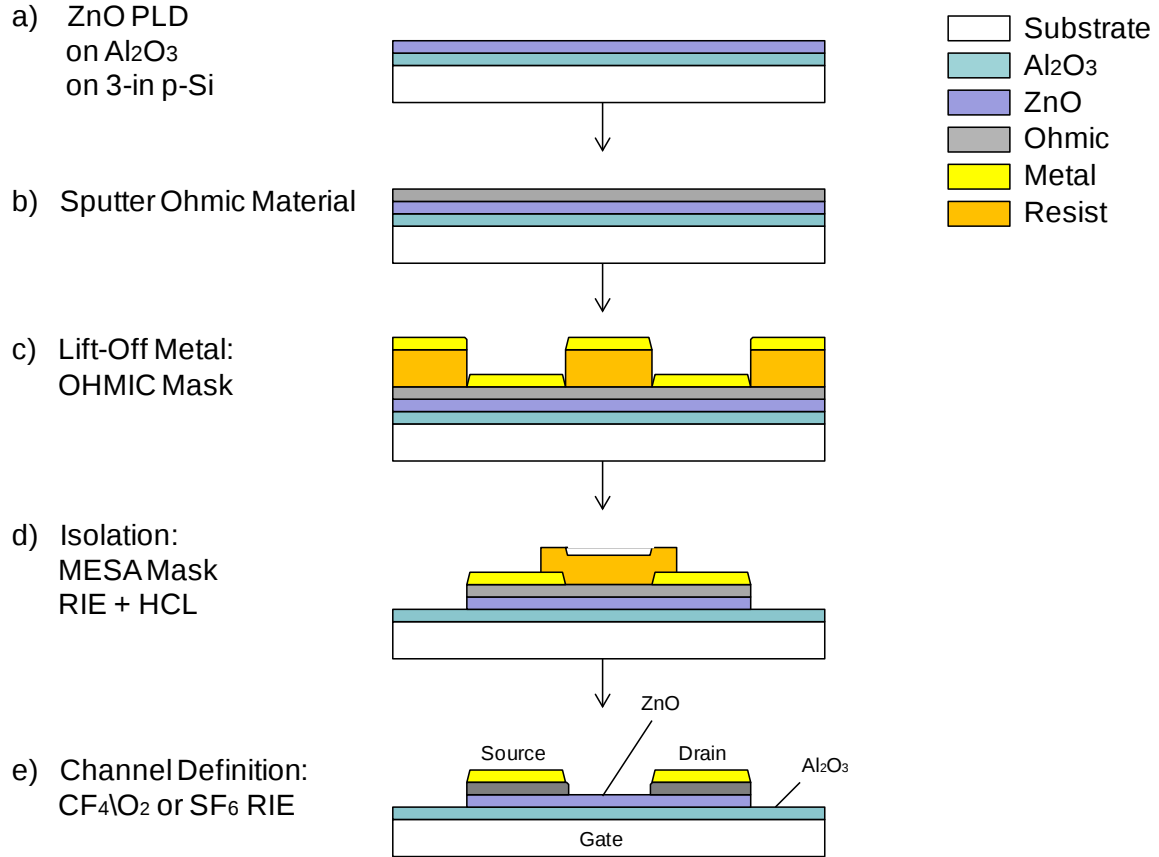


Figure 21: Cross sectional illustration of the process flow for fabricating optical lithographically-defined ZnO TFTs using a subtractive plasma-etch for defining source/drain contacts in this thesis.

Electron-Beam Lithographical Defined Devices

Based on the results from the optically defined devices; electron-beam defined devices were fabricated and tested.

Fabrication Overview

ZnO TFTs with electron beam lithographically defined channels were prepared by depositing 20 nm of Al₂O₃ on 3" n-type Si (1-10 $\Omega\cdot\text{cm}$) wafers, to serve as the gate-dielectric and gate electrode, respectively. Next, the semiconductor active layer, consisting of a 50 nm ZnO thin film was deposited by PLD. The entire sample was then annealed at 400°C for 1-hour in atmosphere. After anneal, 1000 Å of tungsten was deposited over the entire sample using a sputter deposition method. Next, a Ti/Pt/Au/Ni (200/300/2500/200 Å) metal stack was evaporated over the entire sample and defined using the standard bi-layer lift-off method.

Device isolation was accomplished by patterning NANOTM PMGI SF11 resist using the MESA mask from the quick-lot process and MICROPOSITTM S1805 as the imaging resist. After developing the PMGI and stripping the S1805 in acetone, the ohmic material in the field was etched in the Unaxis 790 series RIE Plasma tool using the SF₆:150W chemistry. The field ZnO was then etched away using a 1000:1 ratio of DI:HCl for 25 seconds. The remaining resist was stripped in 1165 resist stripper, and the sample was ashed and cleaned.

The sample was then scored and spin coated with an electron beam sensitive resist. Two different resists were used in the study ZEP520A and 495PMMA-A6. The sample was then exposed using a JEOL JBX-9500FS electron-beam lithography system

and developed. The device channels were then opened using a SF₆-RIE etch recipe at 200W for a time 50% over-etch, utilizing the patterned e-beam polymer resist as an etch mask. After channel opening, the remaining resist was stripped in MICROPOSITTM 1165 resist stripper, ashed, and cleaned before undergoing SEM analysis and device testing. Figure 22 illustrates the fabrication process for developing substrate-gated electron-beam lithographically defined ZnO TFTs in this thesis.

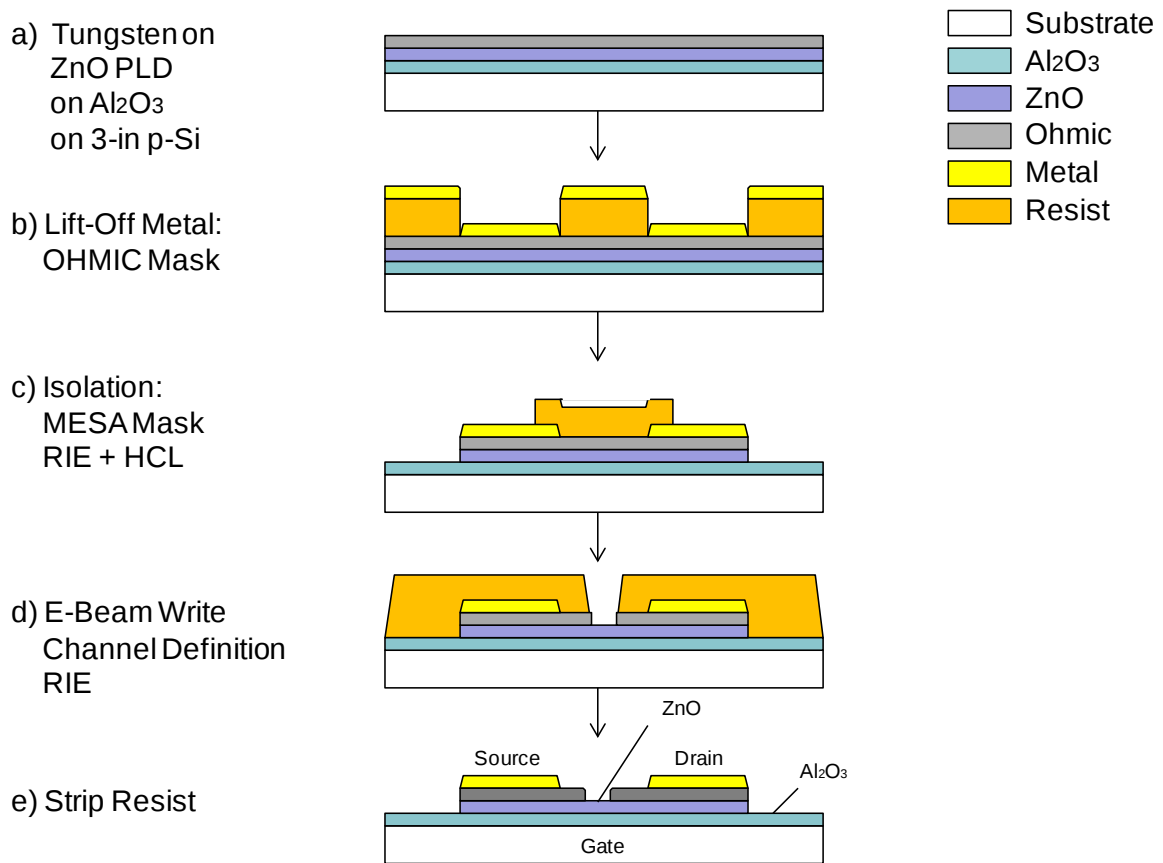


Figure 22: Cross sectional illustration of the process flow for fabricating electron-beam lithographically-defined ZnO TFTs using a subtractive plasma-etch for defining source/drain contacts in this thesis.

SEM Analysis

The devices fabricated in this researched were examined under scanning electron microscopy (SEM) using a Hitachi SU-70 and FEI Strata DB235 for imaging and cross sectional milling, respectively. Prior to cross sectional milling, a platinum film was deposited over the area of interest in order to reduce the curtaining effect. SEM imaging provides detailed channel length information as well as qualitative information regarding the quality of the ZnO film in the active channel layer. Figure 23 shows a schematic cross section of a device with the area of interest that is investigated during SEM analysis.

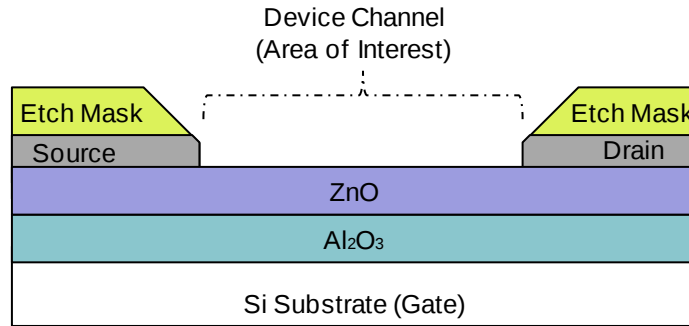


Figure 23: Representative drawing of an SEM cross section showing area interest

Device Testing

Completed ZnO TFTs were tested for their electrical capabilities using a fully-automated cascade probe system and a HP442 parameter analyzer to gather DC measurement data. The cascade probe system has a chuck-biasing capability through a triax connection at the back of the probe station, which was utilized for biasing the gate. A schematic drawing of a ZnO TFT biased in a common-source connection is shown in Figure 24, with gate voltage (V_G), drain voltage (V_D), gate current (I_G) and drain current

(I_D) labeled. The common-source setup was utilized for all DC measurements. From the measured data, important figures of merit were extracted, including current density (I_D), transconductance (G_m), field effect mobility (μ_{fe}) and on-resistance (R_{on}).

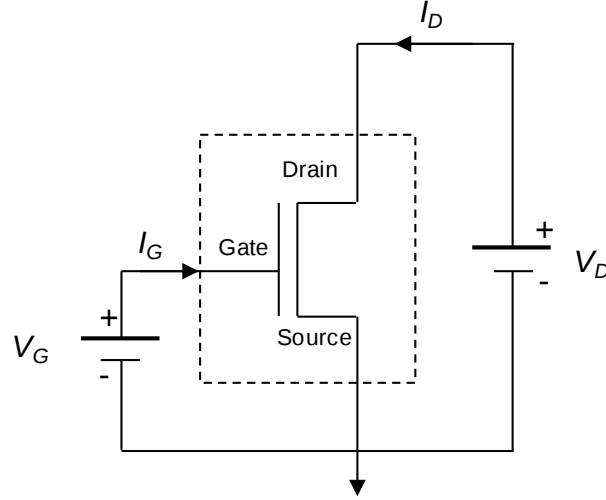


Figure 24: TFT in a common-source connection.

I_D and G_m were captured by sweeping V_G from 0 to 10V in 0.2V steps while maintaining a constant V_D ($= 0.2V$ and $10V$) and measuring the resultant I_D . The field effect mobility (μ_{fe}) was extracted from the data using Equation 2.7 and assuming an ideal dielectric constant of Al_2O_3 of 9.34. The DC I-V family-of-curves were captured by sweeping V_D from 0 to 10V in 0.2V increments at a fixed V_G and measuring the resultant drain current (I_D). The device R_{on} ($= \Delta V_D / \Delta I_D$) and output conductance ($G_D = \Delta I_D / \Delta V_D$) were extracted from the I_D - V_D data with device operating in the linear region and saturation region, respectively. I_D , G_m , R_{on} and G_D were all normalized by channel width.

Summary

This chapter detailed the tools and equipment, fabrication processing steps and device characterization testing methodology used for ZnO TFTs in this research. The following chapter will present the data and observations found during device fabrication and testing.

IV. Results and Analysis

Chapter Overview

In the previous chapter, the process for fabricating and testing ZnO TFTs in this thesis was introduced. In this chapter, the data and observations found during device fabrication and testing are presented and analyzed. In order to present the findings and observations in a logical order, the chapter is divided into five main sections. First, ZnO TFTs with titanium-tungsten and tungsten source and drain contacts patterned by multiple CF_4/O_2 and SF_6 RIE powers are presented. Next, the lift-off comparison study compares the electrical characteristics of ZnO TFTs with ohmic source and drain contacts patterned by RIE to ZnO TFTs with lift-off defined source and drain contacts. Finally the electron-beam device studies presents the results and observations found during attempts at patterning ZnO TFTs with nano-scale channel lengths using e-beam lithography.

Tungsten Device Study

ZnO TFTs fabricated by etching a 1000 Å *tungsten* film using a RIE to define source and drain contacts were fabricated as described in Chapter III. RIE of the *tungsten* film was accomplished using the Unaxis 790 series plasma processing system utilizing a fluorine based etch chemistry. Table 5 outlines the etch chemistry and plasma system parameters utilized for device fabrication along with the corresponding etch rate of *tungsten*.

Table 5: RIE chemistries and corresponding etch rates for *tungsten*

Etch Gas	Gas Flow Rate (sccm)	Chamber Pressure (mTorr)	RIE Power (Watts)	Tungsten Etch Rate ($\text{\AA}/\text{min}$)
CF_4/O_2	40/2	40	200	238
CF_4/O_2	40/2	40	150	223
CF_4/O_2	40/2	40	100	184
CF_4/O_2	40/2	40	50	111
SF_6	40	40	200	2141
SF_6	40	40	150	1586
SF_6	40	40	100	1070
SF_6	40	40	50	531

Optical Analysis

Optical images of a sample taken during device fabrication are shown Figure 32. The images were taken using a Ziess Axio optical microscope under 20x optical zoom. The image on the left shows a device prior to channel opening. While the image on the right shows the same device after RIE of the exposed *tungsten* in the channel. Etching was accomplished using a SF_6 -RIE at 200W for a timed 45 second etch, representing a 50% over-etch time. The RIE process appears to have completely removed all of the exposed tungsten, with no noticeable damage to the underlying ZnO layer. However, damage to the ZnO film cannot be analyzed under this magnification, thus SEM analysis was conducted. Samples etched using the remaining CF_4/O_2 and SF_6 recipes for a timed 50% over-etch displayed similar results.

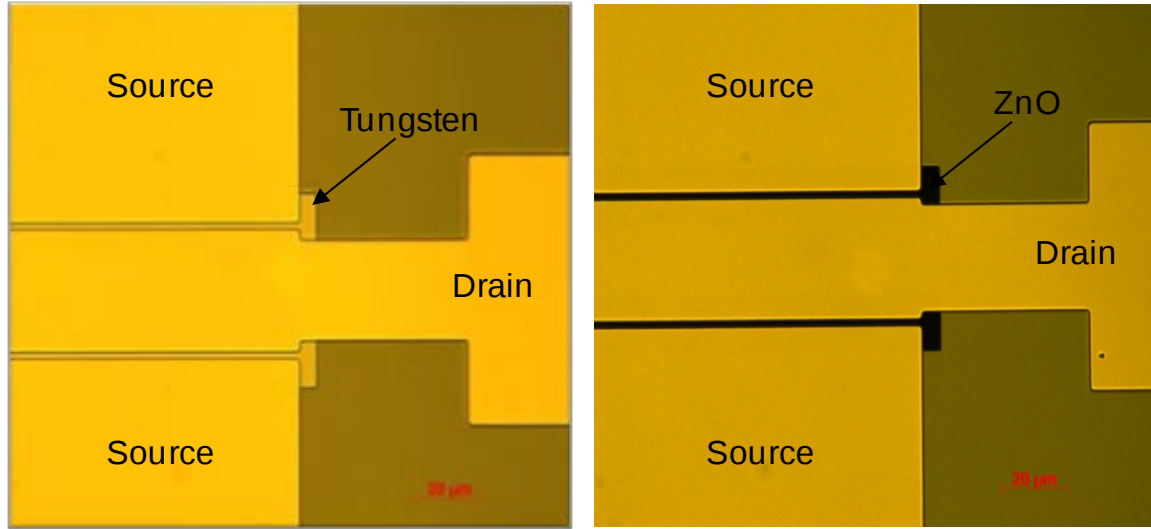


Figure 25: Optical image of a ZnO TFT taken under 50x-magnification prior to channel opening (left) and after removing the exposed *tungsten* using a SF₆-RIE at a 150W plasma power.

SEM Analysis

The substrate gated ZnO TFTs were analyzed using a Hitachi SU-70 and FEI Strata DB235 for SEM imaging and milling, respectively. For consistency, the devices with as drawn channel lengths (L_C) = 2- μ m (defined as the distance between the source and drain pad opening on the photomask) were analyzed on each sample. Prior to cross sectioning a platinum film was deposited over the area of interest in an attempt to reduce the curtaining effect. Figure 26 shows a top down SEM image of a completed device, with annotations indicating where cross sectional analysis was conducted. In order to interpret the data, the devices fabricated using the CF₄/O₂ etch chemistries are first presented, followed by the results using the SF₆ etch chemistries.

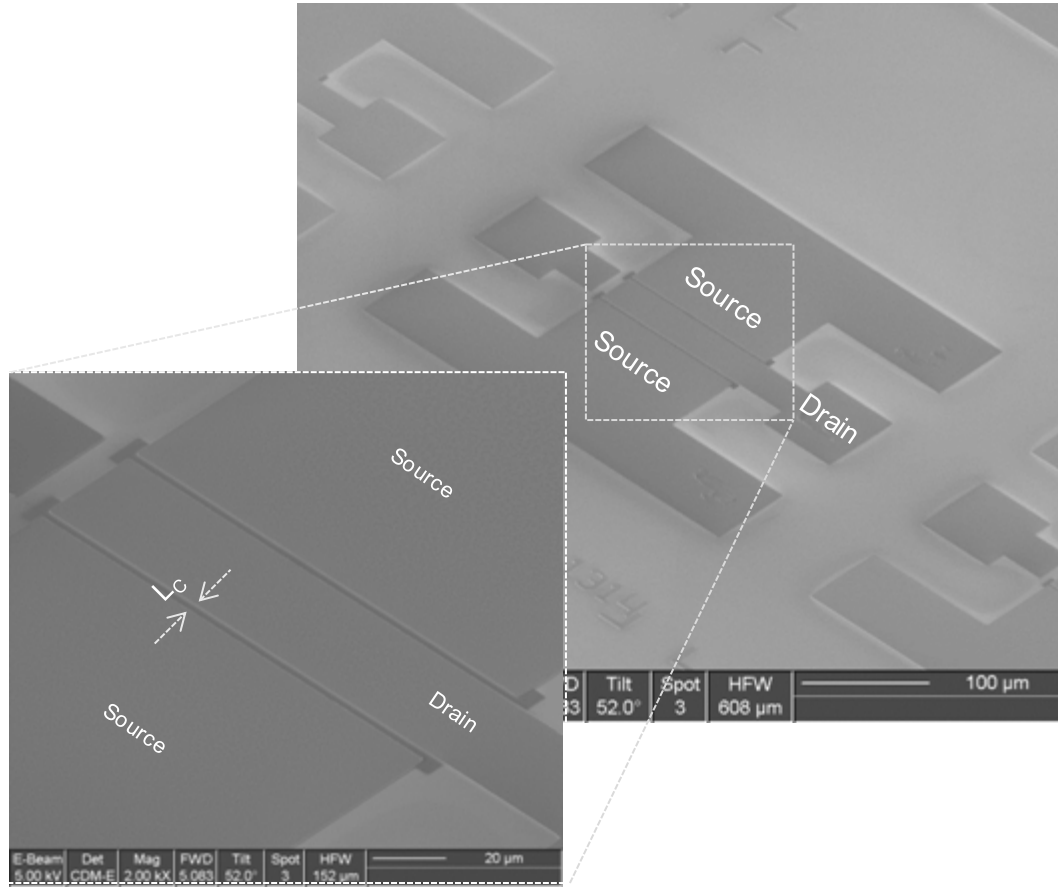


Figure 26: SEM image of a ZnO TFT fabricated in this thesis showing the channel region (L_c) where cross sectional SEM analysis was conducted.

CF₄/O₂ RIE Plasma Etched Devices

Cross sectional SEM images of ZnO TFTs fabricated using a CF₄/O₂ RIE chemistry a 200W and 50W power are shown in Figure 27. The SEM images show the exposed tungsten film in the channel area was completely removed under both RIE conditions. Additionally, a very high anisotropic etch profile using the CF₄/O₂ RIE at 200W was achieved. However, a relatively small undercut of less than 30 nm of the Ti/Pt/Au/Ni contact pad which was used as an etch mask is observed using the CF₄/O₂ RIE at a 50W power setting. Undercutting of the etch mask is undesirable when attempting to pattern short channel ZnO TFTs.

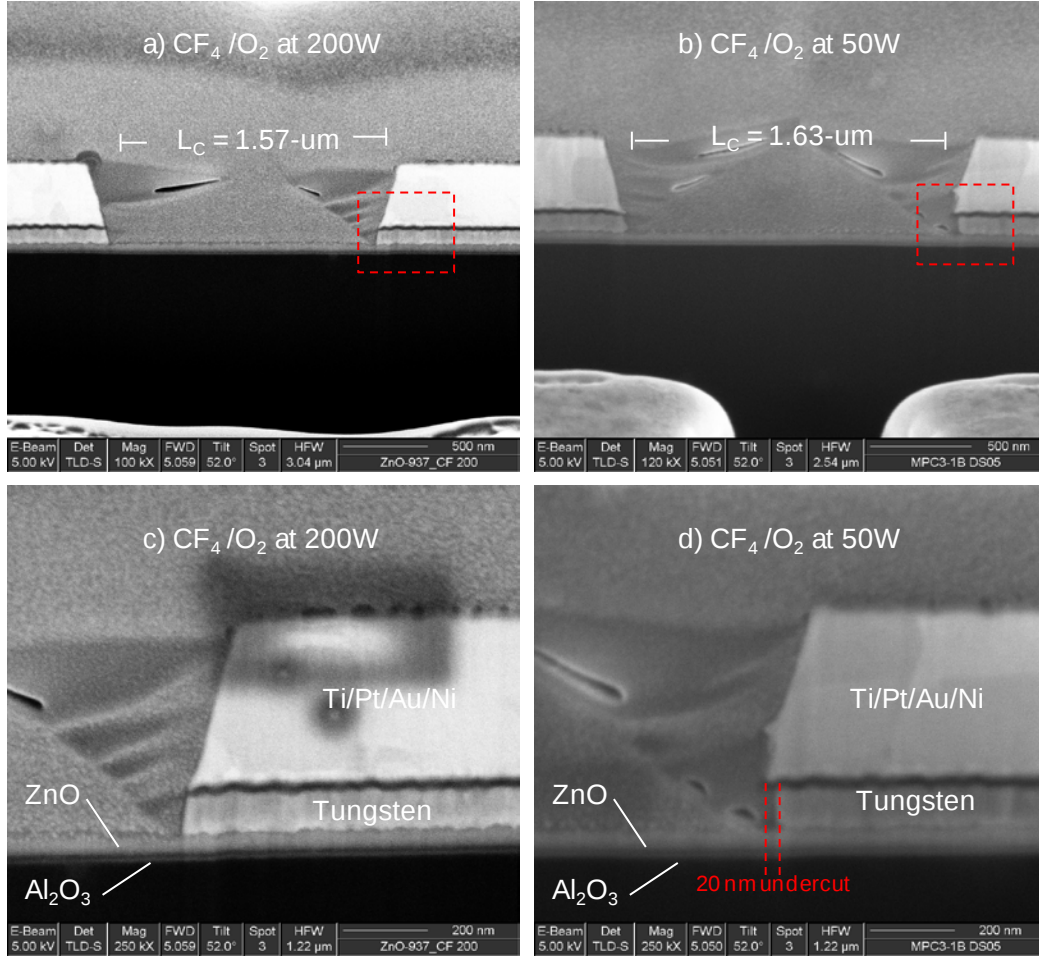


Figure 27: SEM cross sectional images showing the channel region and the source and drain contacts of a ZnO TFT patterned using a subtractive CF_4/O_2 RIE process a) Channel area of a device patterned using a CF_4/O_2 RIE at 200W. b) Channel area of a device patterned using a CF_4/O_2 RIE at 50W. c) Drain contact of a device patterned using a CF_4/O_2 RIE at 200W d) Drain contact of a device patterned using a CF_4/O_2 RIE at 50W

The effective channel length (L_C), defined as the distance from source to drain was measured on each sample using the Hitachi SU-70 SEM under 100kX magnification. Table 7 shows the effective channel length under all CF_4/O_2 RIE power settings. The data show that decreasing the power the CF_4/O_2 RIE chemistry effectively increases the channel length of the device. The increase in channel length is due to undercutting of the etch mask. The channel length increase was calculated as 3.8% from a device patterned

using the CF_4/O_2 RIE at 200W compared to 50W setting. The increase in channel length indicates a CF_4/O_2 RIE at powers below 100W are not suitable for etching tungsten films to define the source and drain contacts for ZnO TFTs with nanometer channel lengths.

Table 6: Measured effective channel length using the Hitachi SU-70 SEM for ZnO TFTs fabricated using a subtractive plasma-etch process under various RIE recipes. The flow rate of CF_4 and O_2 were fixed to 40 sccm and 2 sccm respectively, and the power was fixed to 40 mTorr for each RIE power condition.

RIE Gas	RIE Power	Measured L_C (μm)	Mask Undercut (μm)
CF_4/O_2	200	1.57	0
CF_4/O_2	150	1.59	0
CF_4/O_2	100	1.61	0.01
CF_4/O_2	50	1.63	0.02

The ZnO film thickness was also measured using the SEM tool at a 250kX magnification. Any thinning of the channel area would indicate the CF_4/O_2 RIE process is attacking the underlying ZnO film which is used as an etch stop during the CF_4/O_2 RIE process. At the 250kX magnification, the ZnO film thickness was measured at 54 nm (+/- 3 nm), both within the channel region and underneath source and drain contacts under all CF_4/O_2 RIE power conditions. The measured ZnO thickness confirms the CF_4/O_2 RIE process did not attack or thin the ZnO film within the channel, indicating a highly selective etch was achieved, even at the high power CF_4/O_2 RIE conditions.

SF_6 RIE Plasma Etched Devices

Cross sectional SEM images of ZnO TFTs with tungsten source and drain contacts patterned using a SF_6 RIE at the 200W and 50W power conditions are shown in Figure 28. The SEM images show the exposed tungsten film was completely removed in the channel area under both RIE conditions. Additionally, no undercutting of the etch

mask was observed using the SF₆ RIE at 200W, indicating a very highly anisotropic etch was achieved. However, a significant undercut of 160 nm, measured using the Hitachi SEM at a 250kX magnification, was observed on a device patterned using the SF₆ RIE at a 50W power setting. The large undercut indicates the RIE process is dominated by a chemical attack of the tungsten film, rather than a physical process, using a SF₆ RIE at 50W.

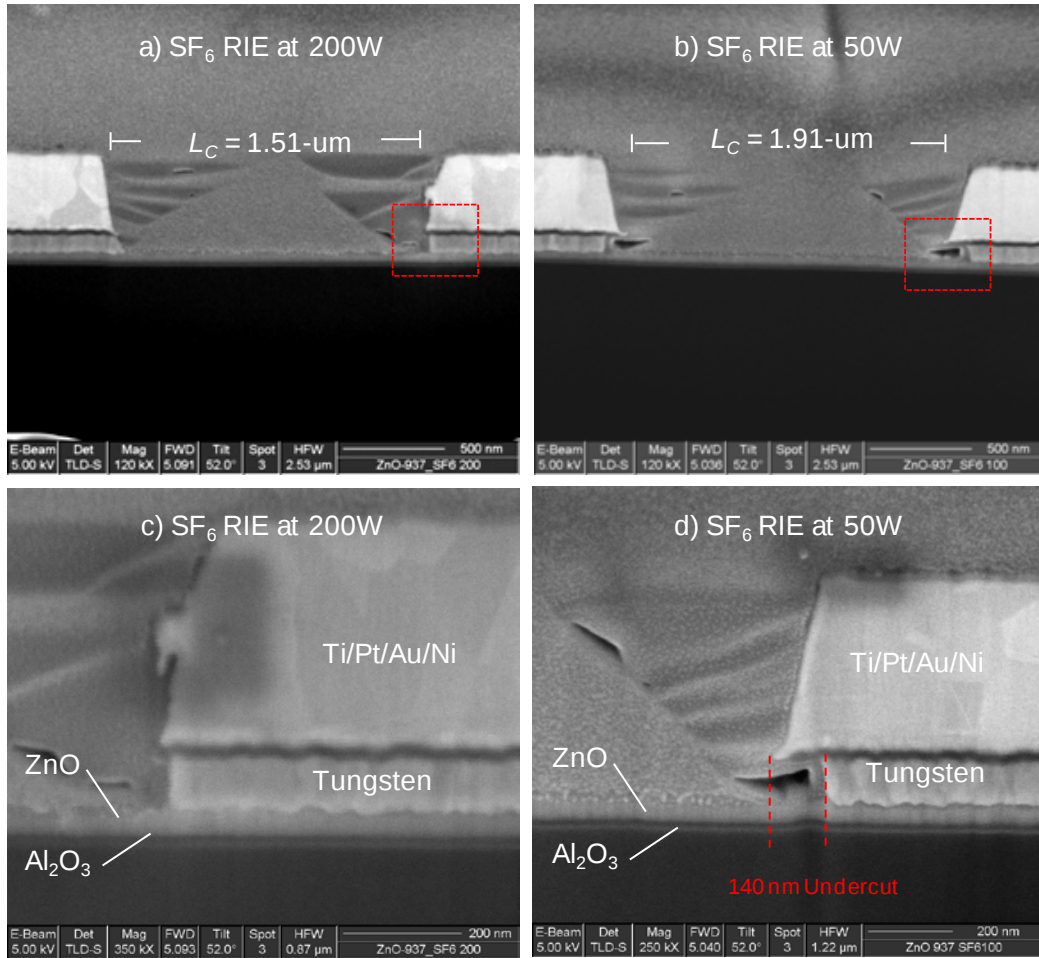


Figure 28: SEM cross sectional images showing the channel region and the source and drain contacts of a ZnO TFT patterned using a subtractive SF₆ RIE process at a plasma power of 200W and 50W. a) Channel area of a device patterned using a SF₆ RIE at 200W. b) Channel area of a device patterned using a SF₆ RIE at 50W. c) Drain contact of a device patterned using a SF₆ RIE at 200W d) Drain contact of a device patterned using a SF₆ RIE at 50W

The effective L_C was measured on each sample using the Hitachi SU-70 SEM under 100kX magnification. Table 7 shows the effective L_C under each SF_6 RIE power setting. From the data, decreasing the power of SF_6 RIE effectively increases the channel length of the device due to undercutting of the etch mask. A total change in the effective channel length of 22% was calculated between the devices fabricated using a SF_6 RIE at 200W compared to a SF_6 RIE at 50W. The observed increase in channel length indicates a SF_6 RIE at RF powers below 150W are not suitable for etching tungsten films to define the source and drain contacts for ZnO TFTs with nanometer scale channel lengths.

Table 7: Measured effective channel length using the Hitachi SU-70 SEM for ZnO TFTs with tungsten source and drain contacts patterned using a subtractive SF_6 -RIE under various power conditions. SF_6 flow rate and chamber pressure were fixed to 40 sccm and 40 mTorr for each RIE power condition, respectively.

RIE Gas	RIE Power	Measured L_C (μm)	Mask Undercut (μm)
SF_6	200	1.51	0
SF_6	150	1.59	0.01
SF_6	100	1.81	0.08
SF_6	50	1.91	0.14

The ZnO film thickness was also measured using the SEM tool at a 250kX magnification. Any thinning of the channel area would indicate the RIE process is attacking the underlying ZnO film which is used as an etch stop during the RIE process. At the 250kX magnification, the ZnO film thickness was measured at 54 nm (+/-3 nm), both within the channel region and underneath source and drain contacts under all SF_6 RIE power conditions. The measured ZnO thickness confirms the SF_6 RIE process did not attack or thin the ZnO film within the channel, indicating a highly selective etch was achieved, even at the high power SF_6 RIE conditions.

DC –IV Analysis.

The completed ZnO TFTs were tested using a fully automated cascade probe system and HP4142 parameter analyzer to gather DC measurement data. Each sample measured roughly 4 cm^2 , with approximately 20 die sites per sample. Prior to probing, a small subset of the die sites on each sample were manually tested using a Tektronix programmable curve tracer and it was discovered that the devices exhibited high leakage current. After undergoing a 10 min 250°C hot-plate bake at atmosphere, the leakage current dropped to undetectable levels for all devices. The results reported in this section were captured after a 10 min 250°C hotplate bake from the devices with as drawn $W_C = 2 \times 150 \text{ }\mu\text{m}$ and $L_C = 2 \text{ }\mu\text{m}$.

The width normalized drain-current versus drain-voltage (I_D - V_D) at $V_G = 2, 6$ and 10 volts for all the devices across each the sample is shown in Figure 29. The samples patterned utilizing the CF_4/O_2 RIE recipes are shown on the left while the samples patterned using the SF_6 RIE recipes are shown on the right.

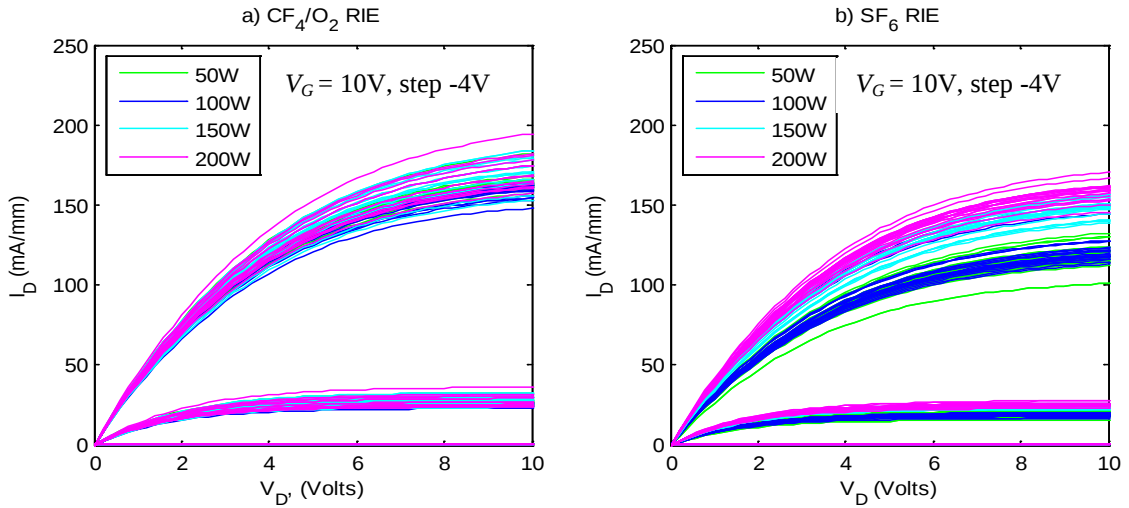


Figure 29: Plots showing the drain-current versus drain-voltage (I_D - V_D) at $V_G=2, 6$ & 10V of ZnO TFTs with tungsten source and drain contacts patterned by (a) CF_4/O_2 -RIE and (b) SF_6 -RIE under varying plasma power settings. As drawn $L_C = 2.0 \text{ }\mu\text{m}$ for all devices.

From the I_D - V_D data, a linear increase of I_D is observed at low V_D values, indicating the *tungsten* source and drain contacts are ohmic and do not exhibit any blocking behavior. Additionally, the ZnO TFTs saturate at high V_D with an output conductance ($G_D = \Delta I_D / \Delta V_D$) of $\sim 1\text{mS/mm}$ at $V_G = 10\text{V}$ calculated by taking from the line of best fit between V_D from 8V to 10V. However, a reciprocal dependence of I_D on plasma power is observed for devices patterned using the SF_6 -RIE chemistry. From the data, the TFTs patterned using SF_6 -RIE chemistry at 50W show a 27% decrease in I_D compared to devices patterned using the SF_6 -RIE chemistry at 200W. This decrease in I_D corresponds to the change in L_C measured using the Hitachi SEM for devices patterned using these chemistries. Therefore, it can be concluded the reduction of I_D at the 50W and 100W RIE powers is due to an increase in channel length caused by undercutting of the etch mask using the low power SF_6 recipes.

Figure 30 shows the width normalized drain current versus gate voltage (I_D - V_G), at $V_D = 10\text{V}$ (top) and the log of the drain current versus drain voltage ($\log(I_D)$ - V_G), at $V_D = 0.2\text{V}$ (bottom). Again, the samples patterned utilizing the CF_4/O_2 RIE chemistries are shown on the left while the samples patterned using the SF_6 RIE recipes are shown on the right.

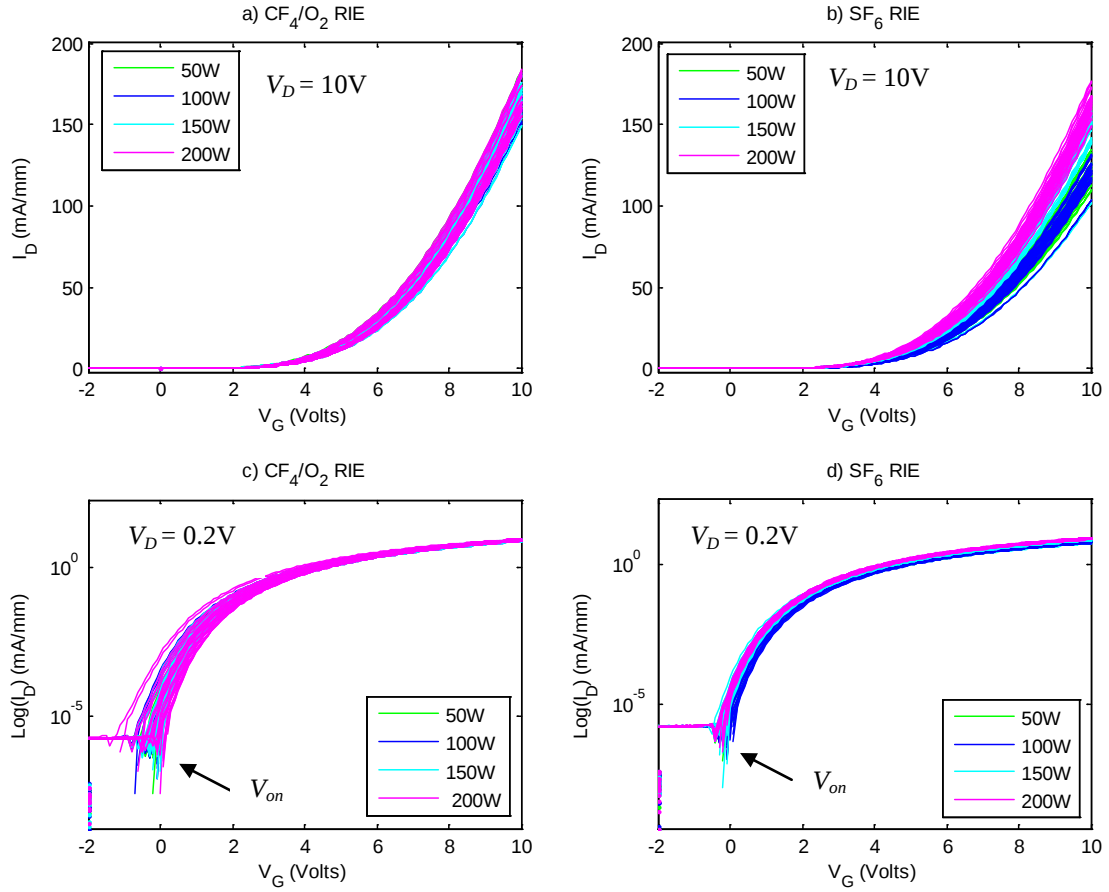


Figure 30: Plots showing the drain-current versus gate-voltage (I_D - V_G) on a linear and semi-log scale for ZnO TFTs with tungsten source and drain contacts patterned by CF_4/O_2 RIE and SF_6 RIE under varying plasma power settings. As drawn $L_C = 2.0 \mu m$ for all devices. a) I_D - V_G at $V_D = 10V$ b) I_D - V_G at $V_D = 10V$ c) $\log(I_D)$ - V_G at $V_D = 0.2V$, d) $\log(I_D)$ - V_G at $V_D = 0.2V$

The on-voltage (V_{on}), which is the gate voltage at the onset of the initial sharp increase in current on the ($\log(I_D)$ - V_G) plot, is approximately -0.2V for all devices. V_{on} is the gate voltage required to fully deplete the channel of free electrons [23]. A shift in V_{on} would indicate traps or other defect states at the ZnO/ Al_2O_3 interface. The off current (I_{OFF}) and gate leakage (I_G) of all devices was measured as $I_{OFF} < 10^{-6}$ mA/mm and $I_G < 10$ pA at a $V_D = 0.2V$ and $V_G = 10V$. An increase in I_{OFF} would indicate additional trap

states along the back of the ZnO channel. Therefore, from the data, it can be concluded the trap states along the ZnO/Al₂O₃ interface or along the backside of the channel are not influenced by variations in the RIE gas chemistry or power.

Using the collected DC-IV data, the average maximum field effect mobility ($\mu_{fe,max}$), current density and ($I_{d,max}$) and transconductance ($G_{m,max}$) was calculated across each sample. The average $\mu_{fe,max}$ was calculated from the I_D - V_G data at V_D =0.2 volts and V_G = 10 volts using Equation 2.7. The oxide capacitance per unit area (C_{ox}) was calculated as 413 nF/cm² using an oxide thickness (t_{ox}) of 20 nm(measured using the Hitachi SU-70 SEM) and assuming an ideal dielectric constant ($\epsilon_{r,ox}$) for Al₂O₃ of 9.34. Table 8 shows the calculated parameters for each etch-recipe utilized for device fabrication.

Table 8: Extracted maximum current-density ($I_{D,max}$), transconductance ($G_{m,max}$) and field-effect-mobility ($\mu_{fe,max}$), for ZnO TFTs with tungsten source and drain contacts patterned by CF₄/O₂ and SF₆ RIE under varying plasma power settings.

RIE Gas	RIE Power (W)	Measured L_C (μ m)	$\mu_{fe,max}$ (cm ² /Vs)	$I_{d,max}$ (mA/mm)	$G_{m,max}$ (mS/mm)
CF ₄ /O ₂	200	1.57	33.39	170.4	52.5
CF ₄ /O ₂	150	1.59	33.36	171.1	48.7
CF ₄ /O ₂	100	1.61	32.62	167.3	48.8
CF ₄ /O ₂	50	1.63	32.25	164.8	50.3
SF ₆	200	1.51	31.43	165.4	51.5
SF ₆	150	1.59	30.18	149.9	46.0
SF ₆	100	1.81	30.43	124.7	39.2
SF ₆	50	1.91	30.65	120.5	37.8

Figure 30 illustrates the calculated field effect mobility (μ_{fe}) and transconductance (G_m) as a function of gate voltage for a representative device fabricated using the CF₄/O₂ and SF₆ RIE chemistries at both 200 W and 50 W. Both μ_{fe} and G_m display a continuous

increase with gate bias, reaching their respective maximum values at $V_G = 10\text{V}$. Indicating higher mobility values at higher V_G settings are possible.

The calculated $\mu_{fe,max}$ value of approximately $33\text{ cm}^2/\text{Vs}$ achieved using the subtractive RIE process is similar to typical results reported in literature for ZnO TFTs. The ZnO TFTs reported in literature have cited μ_{fe} values ranging from $2.3\text{ cm}^2/\text{Vs}$ [72] to $110\text{ cm}^2/\text{Vs}$ [13]. However, these values were cited for devices using different gate dielectric and gate voltage settings, therefore it is difficult to make a direct comparison. Still, the measured μ_{fe} in this work (as well as values reported in literature) is significantly lower than the calculated theoretical room temperature hall mobility of $205\text{ cm}^2/\text{Vs}$ for single-crystal ZnO [38]. Recent studies published by Lorenz *et al.* show that ZnO films deposited by a multistep PLD on c-plane sapphire exhibit mobility values that are comparable to single-crystal ZnO [51]. The study by Lorenz *et al.* indicates that increases in mobility and device improvement can be expected with further optimization to the ZnO deposition used for thin-film growth in this work. However, modifications to the ZnO PLD process are outside of the scope of this work.

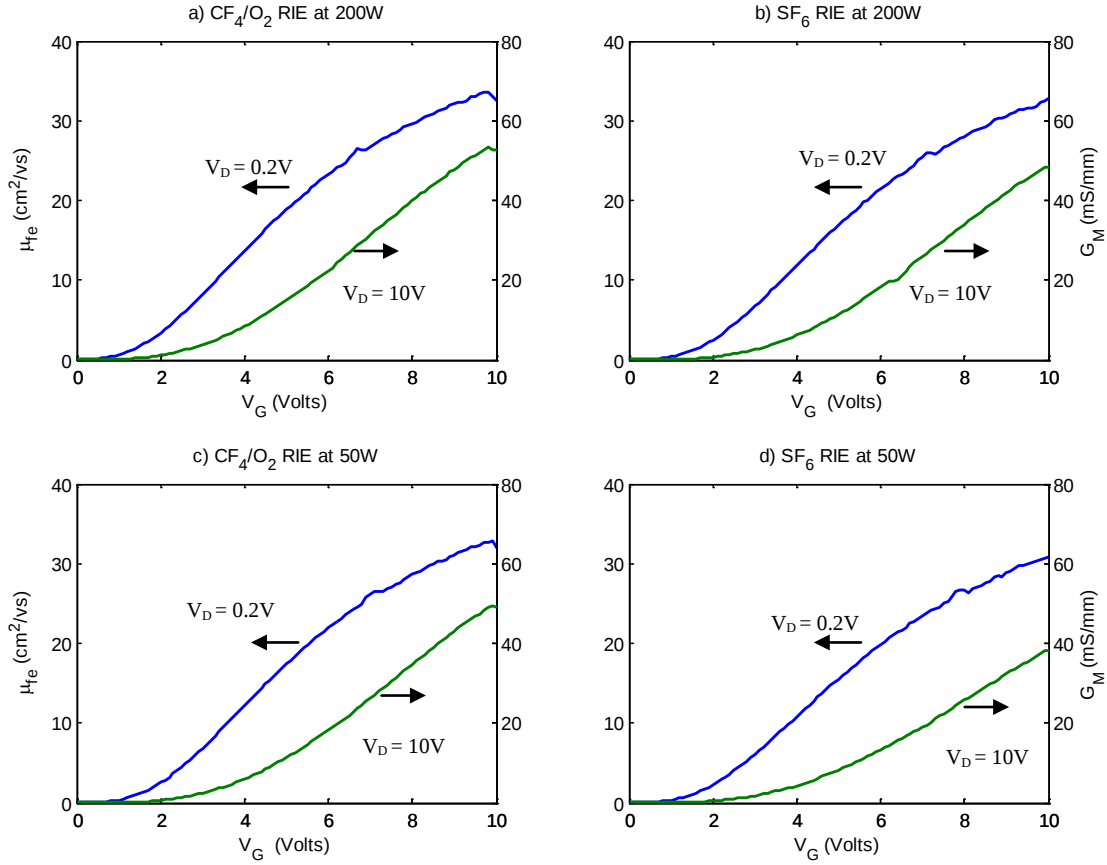


Figure 31: Plots showing the field effect mobility (μ_{fe}) and transconductance (G_m) versus gate voltage for ZnO TFTs with tungsten source and drain contacts patterned by (a) CF_4/O_2 RIE at 200W, (b) SF_6 RIE at 200W, (c) CF_4/O_2 RIE at 50W, and (d) SF_6 RIE at 50W. A decrease in G_m is observed at the 50W plasma settings due to an increase in the effective channel length caused by isotropic etching at low plasma power conditions.

Results Overview

ZnO TFTs were successfully fabricated using a RIE process to define tungsten ohmic contacts using the underlying ZnO film as an etch stop. From the SEM data, the SF_6 and CF_4/O_2 RIE chemistries at 200W resulted in the highest anisotropic etch profiles. Additionally no thinning of the ZnO channel layer was observed indicating that a highly selective etch was achieved. The observed anisotropic etch profiles patterned using the CF_4/O_2 and SF_6 RIE chemistries at 200W result in the shortest channel lengths and

therefore the highest observed I_D and G_M . Conversely, ZnO TFTs fabricated using a SF_6 and CF_4/O_2 RIE chemistries at a 50W and 100W power setting to pattern tungsten source and drain contacts displayed significant lateral etching, effectively increasing the channel length of the device, and reducing the maximum I_D and G_M of the device. The data indicates the SF_6 and CF_4/O_2 RIE chemistries at 200W provide the ideal chemistry for patterning short channel length ZnO TFTs studied in this work.

Additionally, from the measured DC-IV data μ_{fe} was extracted as approximately $31 \text{ cm}^2/\text{Vs}$ at $V_G = V_D = 10 \text{ V}$, independent of the RIE chemistry or power utilized for channel etching. Mobility provides a measure of the efficiency with which electrons move through the channel of the ZnO TFT. Therefore, it can be inferred that the carrier transport of the ZnO channel is unaffected based on the RIE chemistry or power used for device fabrication.

Titanium-tungsten Device Study

ZnO TFTs fabricated by etching a $1000 \text{ \AA}$ *titanium-tungsten* (TiW) film using a RIE process to define source and drain contacts were fabricated as described in Chapter III. RIE of the TiW film was accomplished using the Unaxis 790 series plasma processing system utilizing a fluorine based etch chemistry. Table 9 outlines the etch chemistry and plasma system parameters utilized for device fabrication along with the corresponding etch rate of TiW. The original intent of the study was to investigate the electrical characteristics of ZnO TFTs using a subtractive RIE process; however fabrication issues were encountered during processing which prevented functional devices from being realized.

Table 9: RIE chemistries and corresponding etch rates for *titanium-tungsten*

Etch Gas	Gas Flow Rate (sccm)	Chamber Pressure (mTorr)	RIE Power (Watts)	Titanium-Tungsten Etch Rate (Å/min)
CF ₄ /O ₂	40/2	40	200	262
CF ₄ /O ₂	40/2	40	150	237
CF ₄ /O ₂	40/2	40	100	233
CF ₄ /O ₂	40/2	40	50	168
SF ₆	40	40	200	1900
SF ₆	40	40	150	1400
SF ₆	40	40	100	750
SF ₆	40	40	50	172

Optical Analysis

Optical images of a sample taken during device fabrication are shown Figure 32. The images were taken using a Ziess Axio optical microscope after attempting to remove the exposed *titanium-tungsten* using the SF₆-RIE at a 200W power setting. The optical image shows a significant amount of residual material remaining on the surface of the sample after the RIE process. The Residual material was also observed on samples etched using a SF₆ and CF₄/O₂ RIE at plasma powers ranging from 50W to 200W.

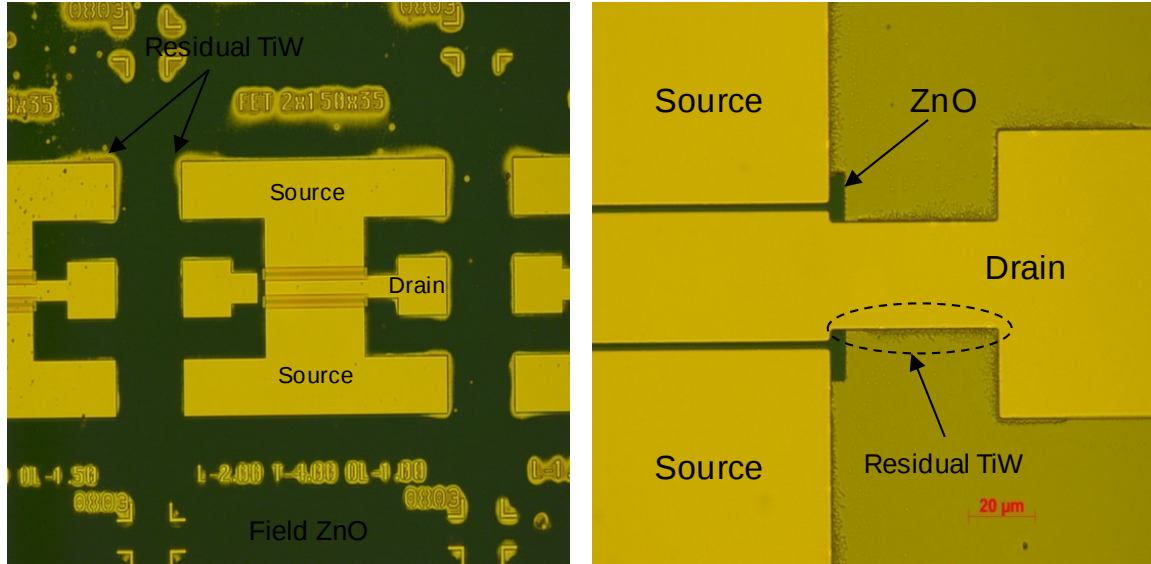


Figure 32: Optical images showing residual titanium-tungsten ohmic material remaining on the sample surface after SF_6 -RIE utilizing the Unaxis 790 Series Plasma System.

The residual material was attempted to be removed using DI water, acetone, IPA, 1165 and plasma ashing in O_2 for four minutes. However, the material remained on the sample surface under all treatments. Figure 33 shows a region of the ZnO channel after ashing the sample in O_2 for 4-min at 250W power. Plasma ashing in O_2 should effectively remove any organic material on the sample; therefore the remaining residual material is believed to be TiW or pure Ti that was either not completely etched or re-deposited during the RIE process.

TiW and Ti can be removed using a wet etch process consisting of hydrofluoric (HF) or hydrochloric (HCL) acid. However, wet etching is typically associated with isotropic etch profiles which are not suitable for patterning nanometer features. Furthermore, the high etch rate of ZnO in acidic based etchants make this course of action unfeasible, as the ZnO channel layer would be completely removed during the wet

etch step. For reference, device mesa isolation was accomplished using HCL:DI (1:1000) wet etch to remove the field ZnO.

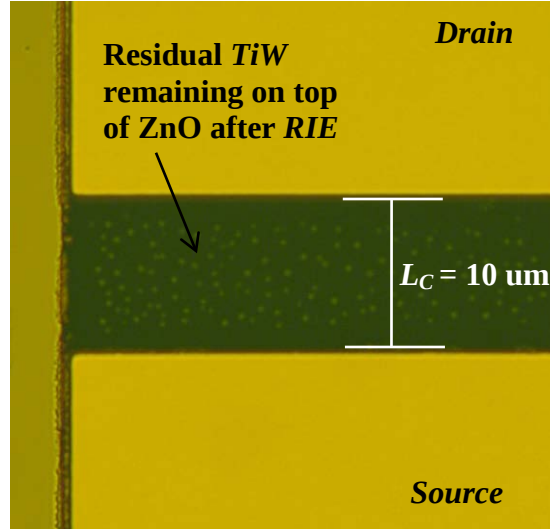


Figure 33: Optical image showing residual titanium-tungsten ohmic material remaining in the channel area after SF_6 -RIE and plasma ashing in O_2

Although the cause for the incomplete removal of the TiW on the sample is not completely understood, one theory is that the exposed ohmic contacts are accumulating a significant amount of charge during the RIE process, preventing the fluorinated ions within the plasma from reacting with the TiW film. The remaining material in the channel may cause fringing currents, or possibly shorting of the device as the channel length. Other plasma etch processes, such as inductively coupled plasma (ICP) etching, rather than RIE, should be pursued in further studies in attempt to pattern TiW source and drain contacts for ZnO TFTs. However, this was not pursued due to time constraints on this work.

Lift-Off Comparison Study

In this study the electrical characteristics of ZnO TFTs fabricated using AFRL's standard lift-off process for patterning source and drain contacts were compared to ZnO TFTs with contacts patterned using a subtractive RIE process. The lift-off samples were prepared by depositing 20 nm of Al₂O₃ on 3" n-type Si (1-10 $\Omega\cdot\text{cm}$) wafers, to serve as the gate-dielectric and gate electrode, respectively. Next, the semiconductor active layer, consisting of a 50 nm ZnO thin film was deposited by PLD. The entire sample was then annealed at 400°C for 1-hour in atmosphere. After anneal, evaporated Ti/Pt/Au/Ni (200/300/3500/200 Å) source and drain contacts were patterned using a bi-layer lift-off method. The lift-off defined ZnO TFTs were then electrically tested as defined in chapter III. The extracted electrical characteristics were compared to ZnO TFTs with RIE defined tungsten source and drain contacts patterned using a CF₄/O₂ and SF₆ RIE at 200W

DC-IV Analysis

The electrical characteristics of ZnO TFTs with $W_C = 2 \times 150 \mu\text{m}$ and $L_C = 1.5 \mu\text{m}$ are shown in Figure 34. The field effect mobility (μ_{fe}) was calculated from the I_D - V_G data at low V_D ($=0.2\text{v}$) using Equation 2.7. The oxide capacitance per unit area (C_{ox}) was calculated as 413 nF/cm² using an oxide thickness (t_{ox}) of 20 nm (measured using the Hitachi SU-70 SEM) and assuming an ideal dielectric constant ($\epsilon_{r,ox}$) for Al₂O₃ of 9.34.

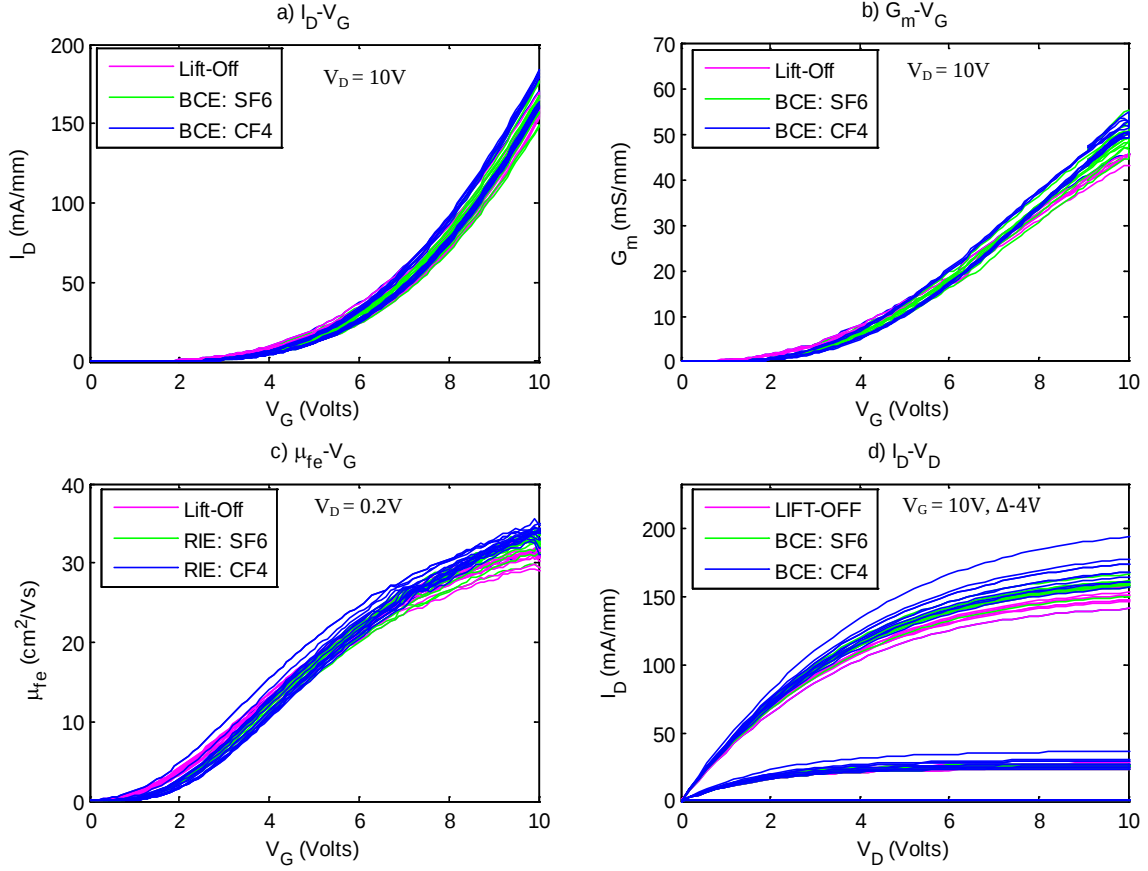


Figure 34: Plots showing the electrical characteristics for ZnO TFTs with tungsten source and drain contacts patterned by CF_4/O_2 and SF_6 RIE compared to ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off. a) I_D - V_G b) G_m - V_G . c) μ_{fe} - V_G . d) I_D - V_D .

From the data, ZnO TFTs with lift-off and subtractive RIE defined source and drain contacts display similar behavior. A maximum I_D and G_m of approximately 165 mA/mm and 50 mS/mm is reached at $V_D = V_G = 10V$, respectively, for all devices. From the I_D - V_D data, a linear dependence on I_D versus V_D is observed at low V_D values (i.e. in the linear region of operation) indicating that the RIE defined tungsten as well as lift-off defined Ti/Pt/Au/Ni contacts are ohmic. From the I_D - V_D data, the width normalized R_{on} was calculated as $\sim 24 \Omega \cdot mm$ for all devices. Finally, μ_{fe} was calculated at $\sim 31 \text{ cm}^2/Vs$ for

all devices, indicating the electron transport of the ZnO film is not altered during the RIE process. Table 10 shows the $I_{D,max}$, $G_{m,max}$ and $\mu_{fe,max}$ taken at $V_G = V_D = 10V$ for each device variation. The device data show no statistical difference between the subtractive etched defined devices and the lift-off defined devices.

Table 10: Extracted maximum current-density ($I_{D,max}$), transconductance ($G_{m,max}$) field-effect-mobility ($\mu_{fe,max}$) and on-resistance (R_{on}) for ZnO TFTs with tungsten source and drain contacts patterned by CF_4/O_2 and SF_6 RIE compared to ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off

	$\mu_{fe,max}$ (cm^2/Vs)	$I_{d,max}$ (mA/mm)	$G_{m,max}$ (mS/mm)	R_{on} (Ω)
Lift-Off	30.01 (+/- 0.85)	162.2 (+/- 12.5)	48.6 (+/- 6.3)	24.8 (+/- 0.72)
CF_4/O_2 RIE at 200W	33.39 (+/- 0.53)	170.4 (+/- 9.5)	52.5 (+/- 1.7)	23.9 (+/- 0.83)
SF_6 RIE at 200W	31.43 (+/- 0.96)	165.4 (+/- 6.3)	51.5 (+/- 1.8)	24.5 (+/- 0.75)

Sheet Resistance Extraction

Figure 35, shows the extracted I_D-V_D characteristics for both the lift-off and subtractive plasma-etched ZnO TFTs with optically measured channel lengths ranging from 4.8 μm down to 0.8 μm . From the I_D-V_D data, the average R_{on} ($= \Delta V_D / \Delta I_D$) across each sample was extracted from the linear best fit (V_{DS} between 0 and 0.25V) at each L_C .

From the extracted R_{on} data, and using a gated transfer-length-method (TLM), the sheet resistance (R_s) of the ZnO channel and parasitic source and drain resistances was extracted. Sheet resistance provides insight into the electrical characteristics of the conducting ZnO channel without the influence of parasitic series resistances. Thus, by

extracting R_s for both lift-off and the subtractive-etched defined devices, a change in the electrical characteristics of ZnO film caused by the plasma-etch process can be identified.

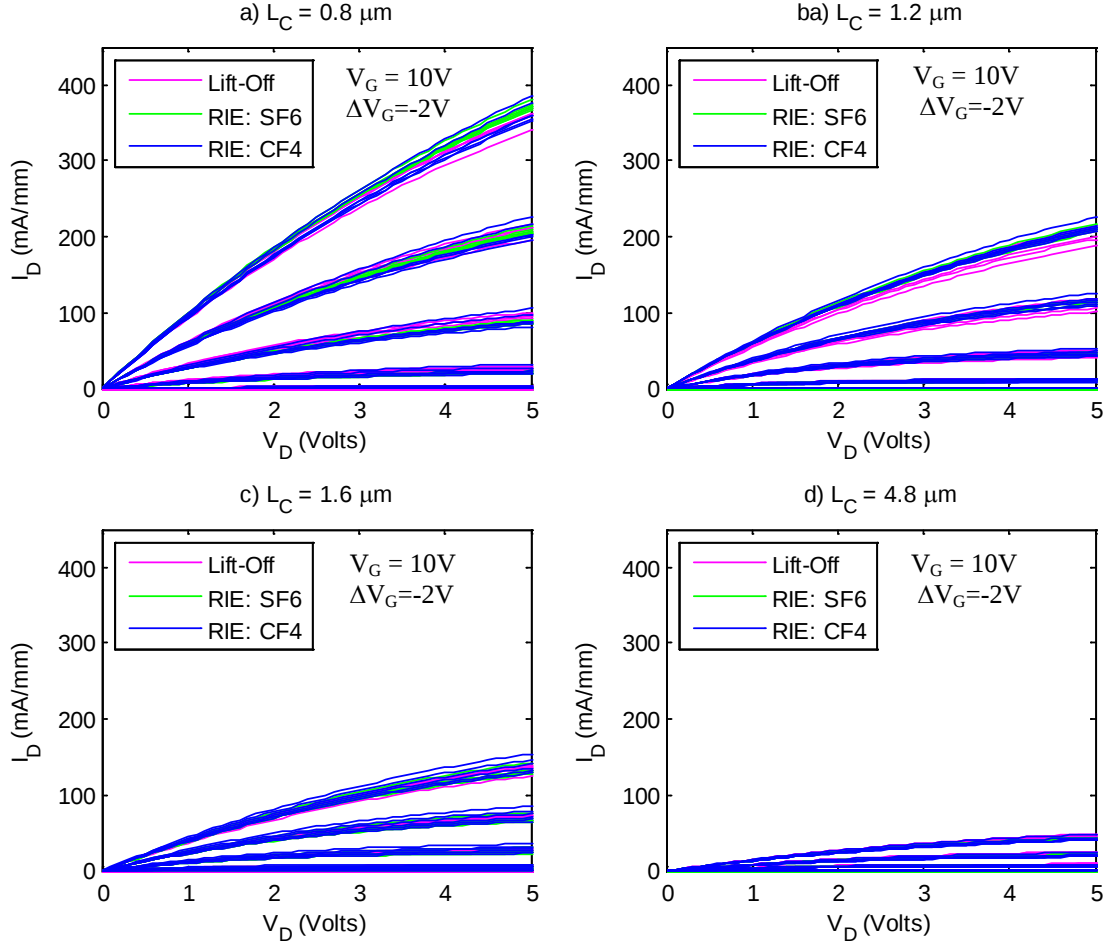


Figure 35: Plots showing the drain-current versus drain-voltage (I_D - V_D) transfer characteristics for ZnO TFTs with tungsten source and drain contacts patterned by CF_4/O_2 and SF_6 RIE compared to ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off. a) $L_C = 0.8 \mu\text{m}$. b) $L_C = 1.2 \mu\text{m}$. c) $L_C = 1.6 \mu\text{m}$. d) $L_C = 4.8 \mu\text{m}$.

Figure 36 shows the average width normalized R_{on} plotted as a function of channel-length (L_C) for the lift-off defined devices and subtractive RIE defined devices. From the data, R_s was calculated as the slope of the line of best fit ($R_s = (\Delta R_{on} / \Delta L_C) W_C$) between the points at each gate voltage setting.

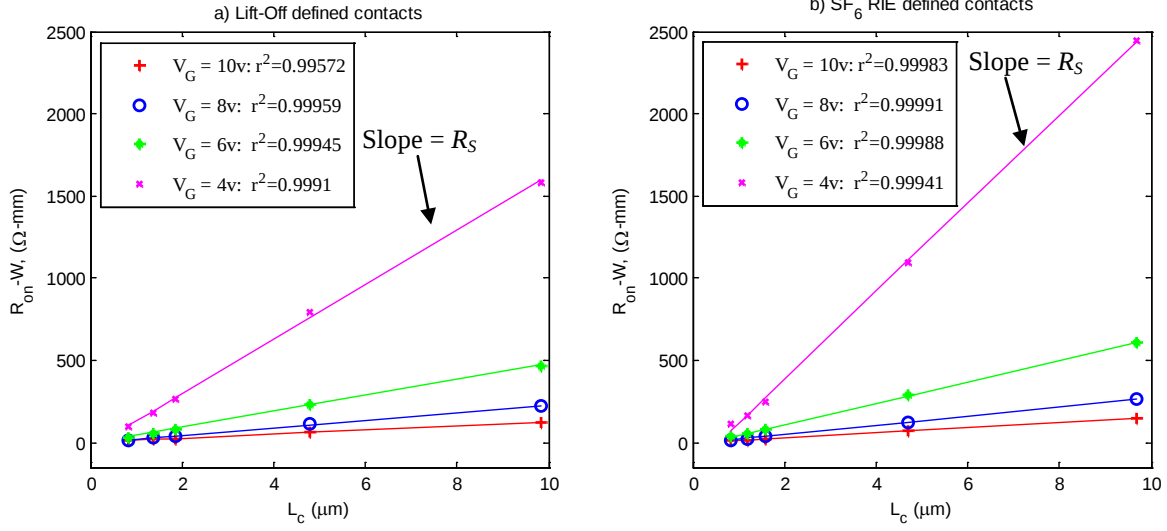


Figure 36: Average width normalized on-resistance versus channel length ($R_{on}W-L_C$) for a) ZnO TFTs with Ti/Pt/Au/Ni source and drain contacts patterned by lift-off compared to b) ZnO TFTs with tungsten contacts patterned by SF₆-RIE. Symbols represent experimental and lines represent experimental and fitted data, respectively.

Figure 37 shows the extracted sheet resistance versus gate voltage (R_s-V_G) for the subtractive RIE and the lift-off defined devices. The data show R_s is approximately 1.5 times higher for the subtractive RIE defined devices at low V_G ($= 4V$) compared to the lift off defined devices. An increase in R_s may indicate a reduction in the effective carrier mobility in the ZnO film of the subtractive-etched devices, possibly due to the ZnO film being exposed to the RIE chemistry. However, R_s converges to approximately 15-kΩ/□ for all device variations at high V_G ($= 10V$).

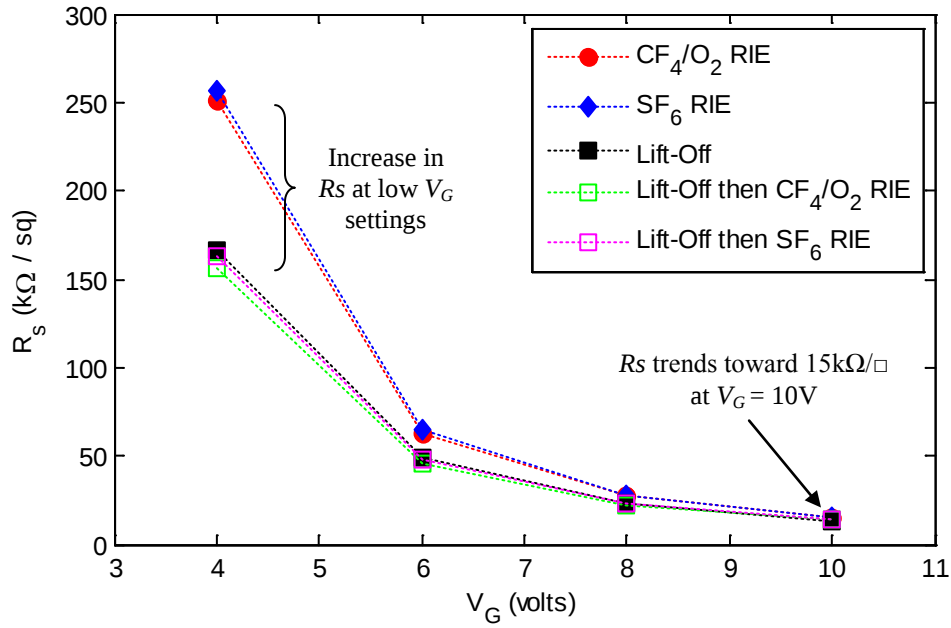


Figure 37: Comparison of the average extracted sheet resistance versus gate voltage (R_s - V_G) for ZnO TFTs with tungsten source and drain contacts patterned by CF_4/O_2 and SF_6 RIE compared to ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off. Symbols represent experimental data.

In order to evaluate the effects on the RIE plasma process on the ZnO film directly, the lift-off defined sample was scored into two sections and subsequently exposed to the CF_4/O_2 or SF_6 RIE chemistry at a 200 W plasma power setting. A 2 min and 30 second exposure time was utilized for the CF_4/O_2 or SF_6 RIE, respectively. These etch times represent the time required to etch 500 Å of tungsten. After exposure to the RIE plasma chemistry, the samples were annealed at 250°C at atmosphere for 10-min and retested. As shown in Figure 37 there was no measurable change in the gate voltage dependent sheet resistance for the lift-off defined devices pre- and post- exposure to either RIE chemistry.

Additionally, using Equation 2.13 an attempt to extract intrinsic field effect mobility and threshold voltage was accomplished by plotting $1/R_s$ versus V_G . However,

as shown in Figure 38, $1/R_s$ does not scale linearly with V_G as is suggested by equation 2.13. This is attributed to the fact that Equation 2.13 is typically utilized to evaluate the conduction channel of *a*-Si TFTs, which have vastly different transport characteristics compared to nanocrystalline-ZnO TFTs. As shown by Hoffman [29], the field effect mobility (μ_{fe}) in ZnO TFTs is not constant, but instead a function of V_G , which is not accounted for in Equation 2.13.

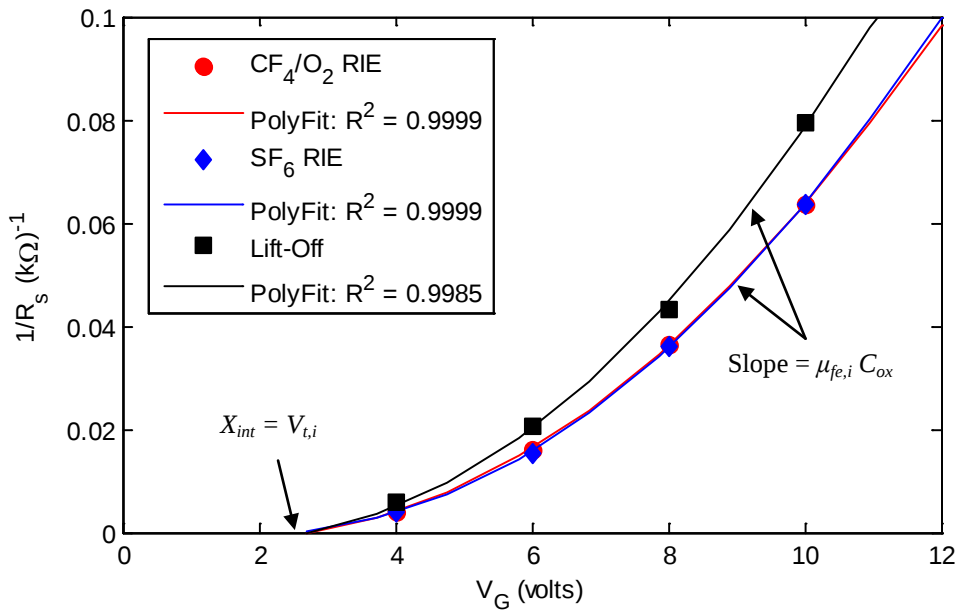


Figure 38: Plot showing the inverse of the sheet resistance versus gate voltage ($1/R_s$ - V_G) for ZnO TFTs with tungsten source and drain contacts patterned by CF₄/O₂ and SF₆ RIE compared to ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off. Symbols and lines represent experimental data and the best-fit 2nd order polynomial, respectively.

Therefore, the process used to extract V_{ti} and $\mu_{fe,i}$ was to fit a 2nd order polynomial to the measured data. Extrapolating the best-fit 2nd order polynomial to $1/R_s = 0$, yields a V_{ti} of 2.7V and 2.96V for the lift-off and subtractive-etched defined devices, respectively. Additionally, the instantaneous derivate of the 2nd order polynomial fit at $V_G = 10V$ was calculated. Dividing the instantaneous derivate by C_{ox} ($= 413 \text{ nF/cm}^2$) yields a $\mu_{fe,i}$

value of $46.1 \text{ cm}^2/\text{Vs}$ and $38.4 \text{ cm}^2/\text{Vs}$ at $V_G = 10\text{V}$ for the lift-off and subtractive etched defined devices, respectively. The change in the intrinsic field effect mobility compared to the mobility extracted using the DC-IV data suggests contact resistance is non-negligible. Therefore, it is expected the contact resistance to degrade device performance as L_C is scaled.

Device Scaling Comparison

The channel lengths of the optical lithographically defined ZnO TFTs fabricated in this thesis were limited by the lift-off defined ohmic metal pads. Figure 39 shows the extracted I_D - V_G characteristics at $V_D = 8\text{V}$ for ZnO TFTs with lift-off defined Ti/Pt/Au/Ni and subtractive RIE defined tungsten source and drain contacts with as drawn L_C ranging from $4.8 \text{ }\mu\text{m}$ to $0.8 \text{ }\mu\text{m}$. The data show I_D increases with L_C as suggested by the square law model shown in Equation 2.1. The highest achieved I_D and G_M values of $\sim 500 \text{ mA/mm}$ and $\sim 100 \text{ mS/mm}$ being observed on devices with $L_C = 0.8$ at bias conditions of $V_G = 10\text{V}$ and $V_D = 8\text{V}$.

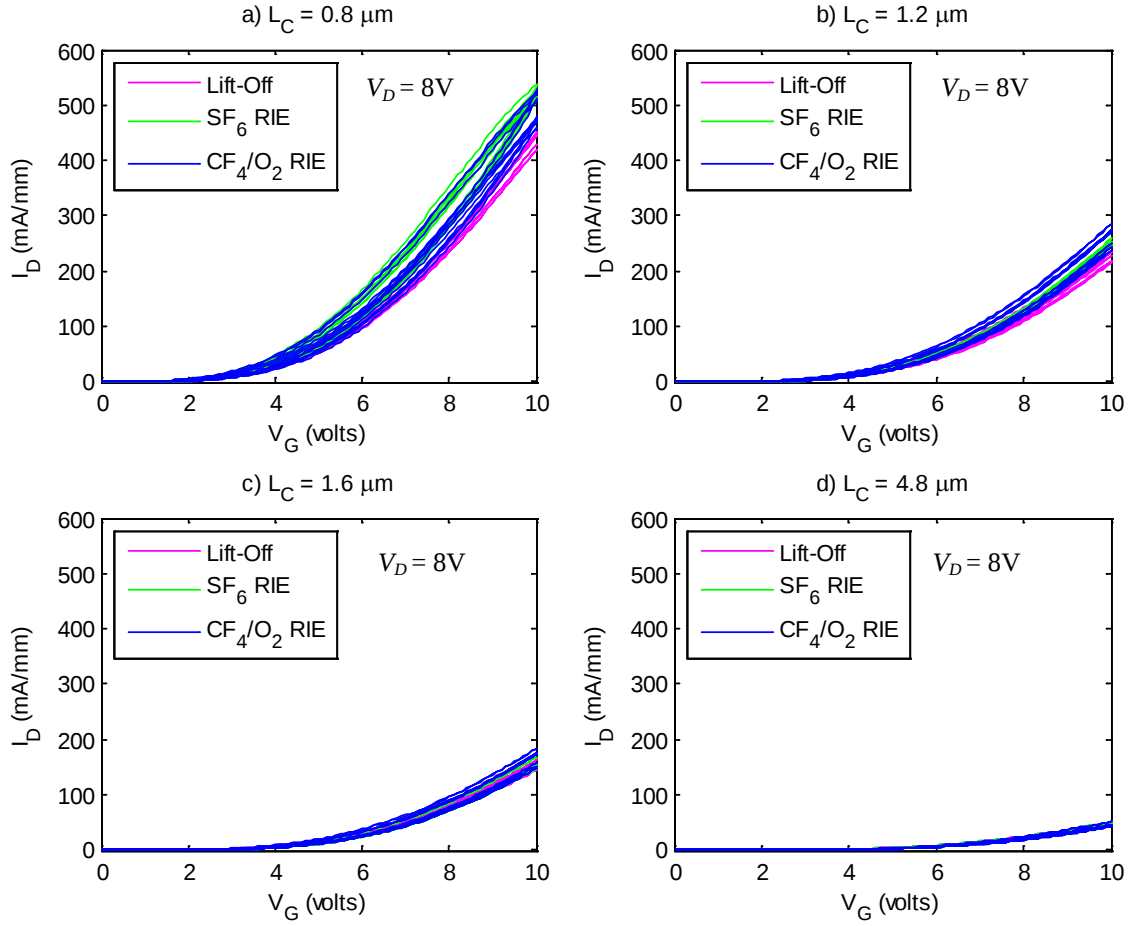


Figure 39: Plots showing the drain current density versus gate-voltage (I_D - V_G) for ZnO TFTs with tungsten source and drain contacts patterned by CF_4/O_2 and SF_6 RIE compared to ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off. a) $L_C = 0.8 \mu\text{m}$. b) $L_C = 1.2 \mu\text{m}$. c) $L_C = 1.6 \mu\text{m}$. d) $L_C = 4.8 \mu\text{m}$.

From the transfer characteristics, the average I_D across each sample at each L_C was extracted at $V_G = 10\text{V}$ and $V_D = 8\text{V}$. Figure 39 illustrates the maximum I_D for for ZnO TFTs with tungsten source and drain contacts patterned by CF_4/O_2 and SF_6 RIE compared to ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off on a log-log plot. All device variations show the same I_D dependence on L_C , suggesting that device scaling is not influenced by the surface states at the Al_2O_3 -ZnO interface or at the back surface of

the ZnO thin-film [17]. Additionally, assuming the scaling holds as L_C is decreased; I_D values above 1 A/mm can be expected with L_C below 500 nm.

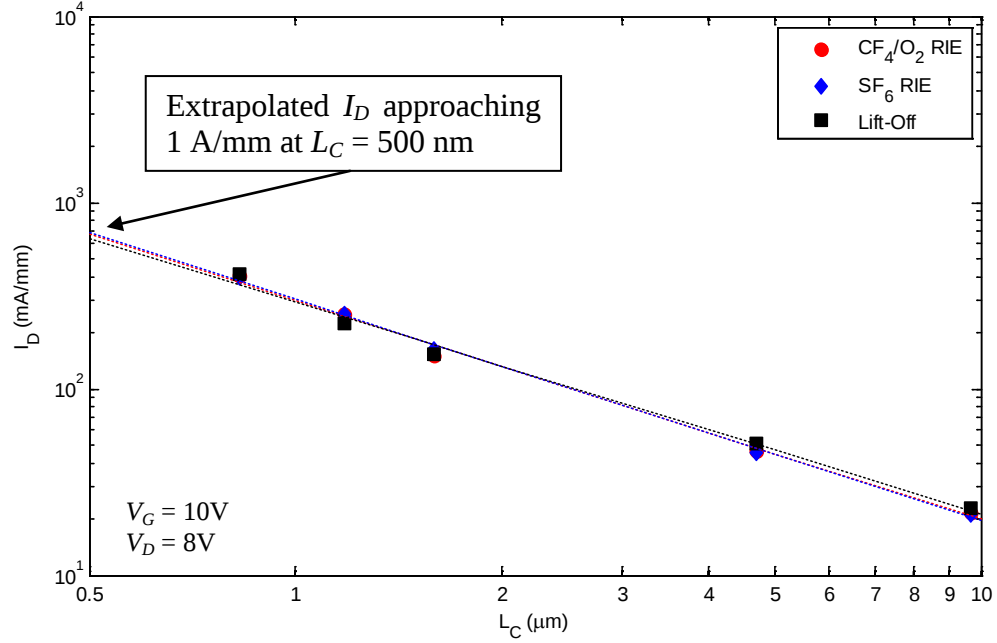


Figure 40: Drain current density dependence on channel length shown on a log-log plot for ZnO TFTs with tungsten source and drain contacts patterned by CF₄/O₂ and SF₆ RIE compared to ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off. Symbols and lines represent experimental data and the best-fit line, respectively. Extrapolation of the Data shows ZnO TFTs with LC below 500 nm may operate at I_D values above 900 mA/mm.

Results Overview

The data extracted from the DC-IV curves show, no statistical difference in $I_{D,max}$, or $G_{m,max}$ when comparing the ZnO TFTs with tungsten source and drain contacts patterned by CF₄/O₂ and SF₆ RIE compared to ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off with measured channel lengths of 1.5 μm . From the data it can be concluded the RIE processes does not alter the DC electrical performance of the device. However, an increase in R_S at low V_G ($= 4\text{V}$) settings was observed on the subtractive RIE devices when compared to the lift-off defined devices. This is possibly due to a

reduction of the carrier mobility in the ZnO channel layer in the subtractive RIE defined devices with tungsten source and drain contacts.

An experiment directly measure the effect of the CF_4/O_2 and SF_6 RIE process on the ZnO active channel layer was conducted by exposing the lift-off defined ZnO TFTs to the RIE chemistry. The data show no measurable change in R_S for the devices with after being exposed to the RIE chemistry. The results indicate the change in R_S cannot be attributed to damage induced during the RIE process. Thus, the increase in measured R_S and resultant reduction in mobility at low V_G settings is therefore attributed to process variation. However, additional studies with larger sample sizes are needed to confirm this prediction.

Finally, ZnO TFTs with tungsten source and drain contacts patterned by CF_4/O_2 and SF_6 RIE and ZnO TFTs with Ti/Pt/Au/Ni contacts patterned by lift-off demonstrate the same I_D and R_{on} dependence on L_C described by the square law model. The scaling dependence of I_D and R_{on} on L_C for ZnO TFTs with L_C of $0.8\ \mu\text{m}$ fabricated in this work are not limited by large contact resistance values, velocity saturation, or other short channel effects. Therefore, assuming the dependence holds as L_C is decreased, current densities above $1\ \text{A/mm}$ are possible by scaling L_C below $500\ \text{nm}$.

E-Beam Device Study Using ZEP

ZnO TFTs with subtractive RIE defined tungsten contacts were patterned utilizing ZEP520a as an etch mask were fabricated as detailed in Chapter III. Due to the high etch rate of organic resists in O_2 rich plasmas, only the SF_6 RIE chemistry at a 200W power setting was utilized for device fabrication. Prior to device fabrication, an etch study was

conducted to calculate the etch rate and selectivity of ZEP520a in a SF₆-RIE process. Table 11 details the nominal spin on thickness, etch rate, and selectivity (*tungsten*:ZEP520a) found during the study.

Table 11: ZEP520a spin on and etch characteristics in the SF₆ RIE at a 200W plasma power

Nominal Spin on Thickness (Å)	3600
Etch Rate (Å/min)	700
Selectivity (W:resist)	2.7:1

Based on the results from the etch study, samples were prepared using a single layer of ZEP520a with 50, 100, 200 and 300 µm lines opened in the resist using the JEOLX e-beam system. A timed 45 second etch utilizing the SF₆-RIE at 200W was expected to completely remove the exposed *tungsten*. However, under SEM investigation it was found that the 45 second etch-time was insufficient to effectively clear the channel area. The incomplete removal of the *tungsten* film is believed to be due to a loading affect, which effectively decreases the etch rate of *tungsten* when etching extremely small geometries. A loading effect was observed by Picard *et al.* when etching of *tungsten* in pure SF₆ as well as in SF₆-O₂ mixture [73].

In this work, the loading effect is believed to be due to an increase in the reactive material on the sample when using organic based resist as an etch mask (compared to previous devices which were fabricated utilizing a metal etch mask). The additional orgainc material on the sample reacts with the plasma chemistry, reducing the number of reactive species in the plasma, therefore slowing down the etch rate of tungsten. As a

result of the reaction limited etch process, a timed 105 second etch using SF₆-RIE at 200W was required to completely clear the *tungsten* film. However, it is expected that the etch rate will vary depending on the size of the sample. Therefore, additional studies are needed to characterize the etch rate of full 3" or 4" wafers.

SEM Investigation

The sample was analyzed using a Hitachi SU-70 and FEI Strata DB235 for SEM imaging and milling immediately following the RIE process. Figure 41 shows a cross sectional SEM image immediately following the etch process, prior to stripping the ZEP520a resist. The image shows the ZEP520a held up during the SF₆-RIE process and the *tungsten* film appears to have been completely removed from channel area. The etch profile of the *tungsten* is nearly perfectly isotropic, even with the increased etch time required, resulting in a channel opening of 320 nm measured using the Hitachi SU-70. However, the ZnO film within the channel area appears to have been damaged during the SF₆-RIE process.

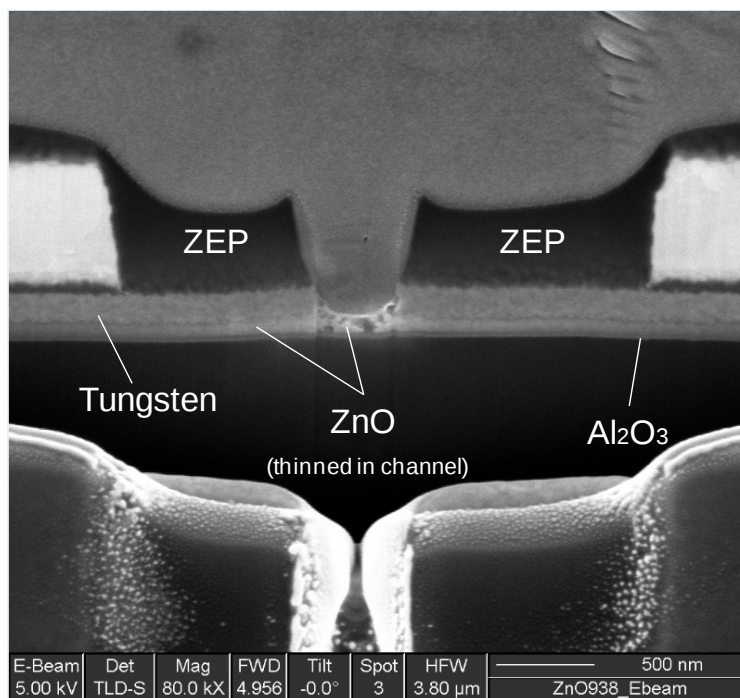


Figure 41: Cross sectional SEM images detailing the channel area of a ZnO TFT with tungsten source and drain contacts patterned by SF_6 -RIE prior to stripping the ZEP-520 etch mask. SEM imaging show the ZnO thin-film in the channel was damaged during the RIE process possibly due to an interaction with the ZEP-520a e-beam resist used as an etch mask during the RIE.

Figure 42 shows cross sectional SEM images of a device after stripping the remaining ZEP520a in 1165 stripper heated to 90°C for 2-minutes. The images clearly shows the ZnO channel was attacked, although the attack is not uniform throughout the channel. In some areas, the ZnO appears to be completely removed, while in others the full thickness is observed.

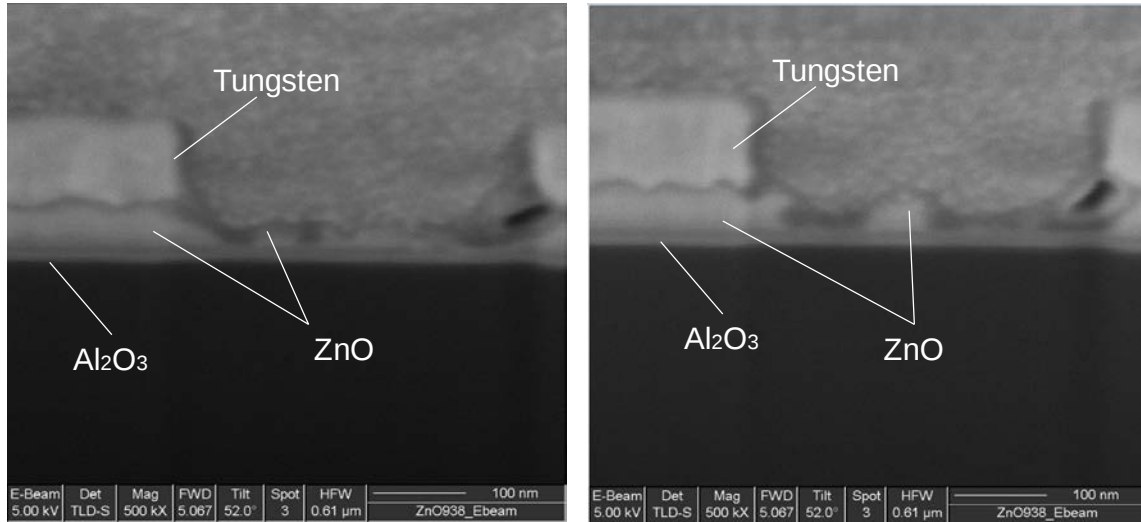


Figure 42: Cross sectional SEM images detailing the channel area of two different ZnO TFTs with tungsten source and drain contacts patterned by SF_6 -RIE after stripping the ZEP-520 etch mask. SEM imaging show the ZnO thin-film in the channel area was damaged during the RIE process possibly due to an interaction with the ZEP-520a resist used as an etch mask during the RIE process. The devices have a SEM measured $L_C = 358$ nm.

From the data it is apparent the attack is taking place during the the SF_6 -RIE process. Although the root cause is not yet understood, it is believed to be due to a chemical reaction with ZEP520a resist occurring during the SF_6 -RIE process. According to the material safety data sheet (MSDS), the copolymer compound within ZEP520a contains chloromethyl-acrylate (ClCH_3) [64]. Therefore, if the ZEP520a decomposes or outgasses during the RIE process, chlorine (Cl) could be released, resulting in Cl contamination in the plasma. ZnO is known to etch readily in chlorine-containing plasmas, with reported etch rates in excess of $1000\text{-}\text{\AA}/\text{min}$ [74]. Outgassing of the ClCH_3 copolymer within ZEP-520a, and the resultant chlorine contamination in the plasma, would explain why an attack on the ZnO film is being observed. Additionally, no measurable thinning of the ZnO film was observed using the the SF_6 -RIE at 200W to

pattern tungsten source and drain contacts to ZnO TFTs using a Ni etch mask. Suggesting the ZEP-520a is responsible for the attack on the ZnO film.

DC-IV Analysis

Although the SEM images show the ZnO channel was attacked during the the SF₆-RIE process, the devices were still operational, indicating at least a partial ZnO conductive channel exists from source to drain. Figure 43 shows the transfer characteristics of representative device on the sample, with an SEM measured channel length (L_C) of 358 nm. The device exhibits a maximum I_D and G_m of 600 mA/mm and 110-mS/mm, respectively, at $V_D = 5V$ and $V_G = 10V$. The device also exhibits a low width normalized R_{on} value of 7.95 $\Omega \cdot \text{mm}$ at $V_G = 10V$, extracted from the linear best fit line at V_D between 0 and 0.25V. Based on the data, the device displays I_D steps with decreasing V_G and trend towards a saturation region with higher V_D . The device also pinches-off at $V_G = -1.8V$ with an off current of 4.0×10^{-6} mA/mm, resulting in an on-off current ratio (I_{ON-OFF}) of approximately 1×10^8 .

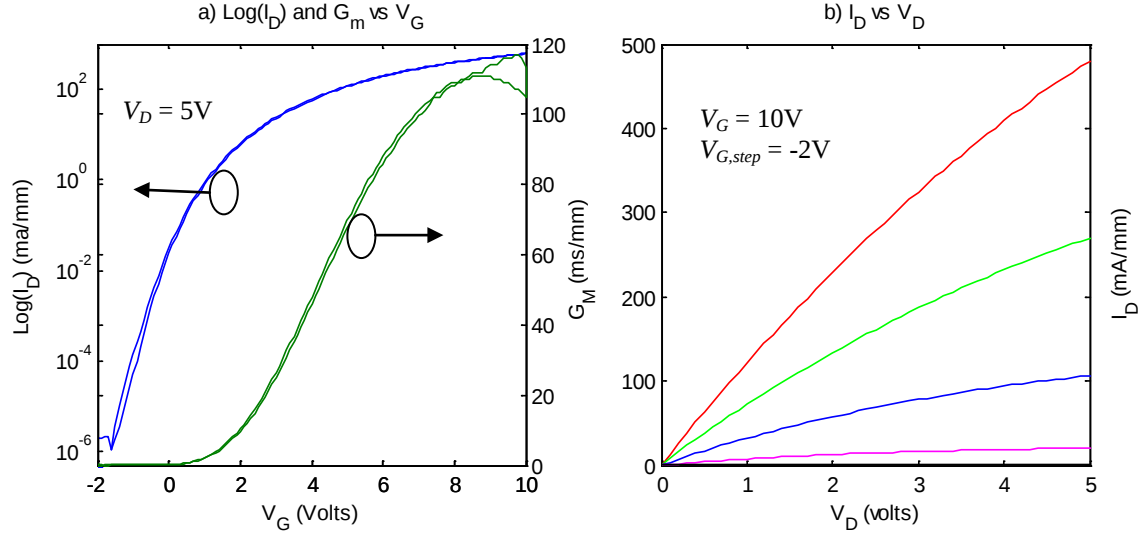


Figure 43: Plots showing the transfer characteristics of a ZnO TFT with tungsten source and drain contacts defined by SF_6 -RIE. a) $\text{Log}(I_D)$ and G_m versus V_G . b) I_D versus V_D at $V_G = 10V$, $V_{G,step} = 2V$. A thinned ZnO channel was observed during SEM caused by unexpected attack during the RIE process. $L_C = 348$ nm.

Results Overview

Through SEM investigation it was found that the ZnO film in the channel was attacked during the the SF_6 -RIE process. The cause for the unexpected etching is theorized to be a result of the ClCH_3 co-polymer compound within ZEP-520a which is outgassing during the RIE process, resulting in a Cl-contaminated plasma. ZnO is known to etch readily in chlorine containing plasma processes with etch rates above $1000 \text{ \AA}/\text{min}$ [74]. Still, even with the compromised channel, ZnO TFTs with channel lengths of 358 nm reached a maximum $I_{D,max}$ of 600 mA/mm at $V_D = 5V$ and $V_G = 10$, and a width normalized R_{on} value of $7.95 \text{ } \Omega \cdot \text{mm}$. The high current and transconductance densities and low R_{on} indicate a highly conductive channel exists between the source and the drain, even with significant attack of the active ZnO channel being observed. However, the yield on the sample was extremely low, therefore utilizing ZEP520a as a mask during

SF₆-RIE process is not a repeatable solution for patterning ZnO TFTs. One interesting result from the study suggests that ZnO TFTs could be fabricated using a significantly thinner ZnO channel layer (possibly down to single nm thicknesses) without degrading device performance.

E-Beam Device Study Using PMMA

ZnO TFTs with subtractive RIE defined tungsten contacts were patterned utilizing a polymethyl-methacrylate (PMMA) etch mask were fabricated as detailed in Chapter III. Due to the high etch rate of organic resists in O₂ rich plasmas, only the SF₆-RIE chemistry at a 200W power setting was utilized for device fabrication. Prior to device fabrication, an etch study was conducted to calculate the etch rate and selectivity of PMMA in a SF₆-RIE process. Table 12 details the nominal spin on thickness, etch rate, and selectivity (*tungsten*:ZEP520a) found during the study. However, due to the loading effect found while attempting to pattern devices using ZEP520a as an etch mask, it was expected longer etch times would again be required to completely clear the tungsten. As a result a double thickness layer of PMMA was used to ensure it would hold up to the RIE process.

A timed 45 second etch utilizing the SF₆-RIE at 200W was expected to completely remove the exposed *tungsten*. However, again it was found that the 45 second etch-time was insufficient to effectively clear the channel area. The decrease in etch time is attributed to loading effect caused by utilizing an organic based resist as an etch mask, rather than a Ni mask. As a result of the reaction limited etch process, a timed 105

second etch using SF₆-RIE at 200W was once again required to completely clear the *tungsten* film.

Table 12: PMMA and ZEP spin on and etch characteristics in the SF₆ RIE at a 200W plasma power

Nominal Spin on Thickness (Å)	2900
Etch Rate (Å/min)	2800
Selectivity (W:resist)	0.7:1

SEM Investigation

Figure 44 shows a top down SEM image of a completed device after stripping the remaining PMMA with sources and drain labeled. Inset shows a magnified view of the channel area illustrating the channel is inset from the ohmic source/drain pads.

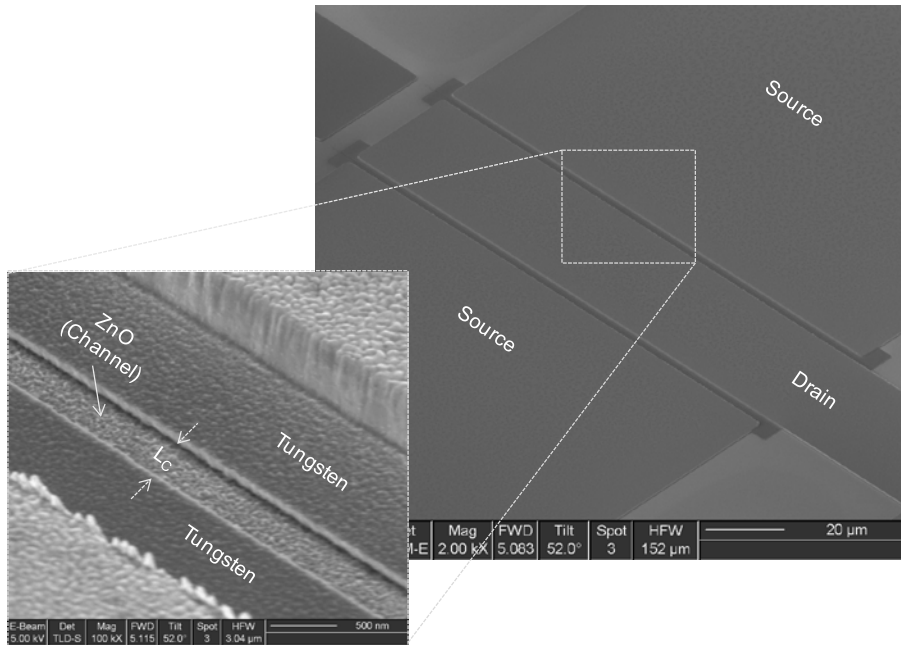


Figure 44: SEM image of a completed ZnO TFT with tungsten source and drain contacts patterned by SF₆-RIE. Inset shows detailed region of the channel area.

Figure 45 shows cross sectional SEM images of the channel area with the PMMA resist layer still in tack for varying channel length devices. The image data show the PMMA etch mask held up during the SF_6 -RIE process and that the *tungsten* was completely removed from channel area. The etch profile is highly anisotropic, although slight undercutting is observed, resulting in an increase of the channel length of 22 nm (measured from the difference in channel opening from the top of the tungsten film compared to the tungsten/ZnO interface). Additionally, no thinning or attack of the ZnO film was observed indicating a highly selective etch was achieved.

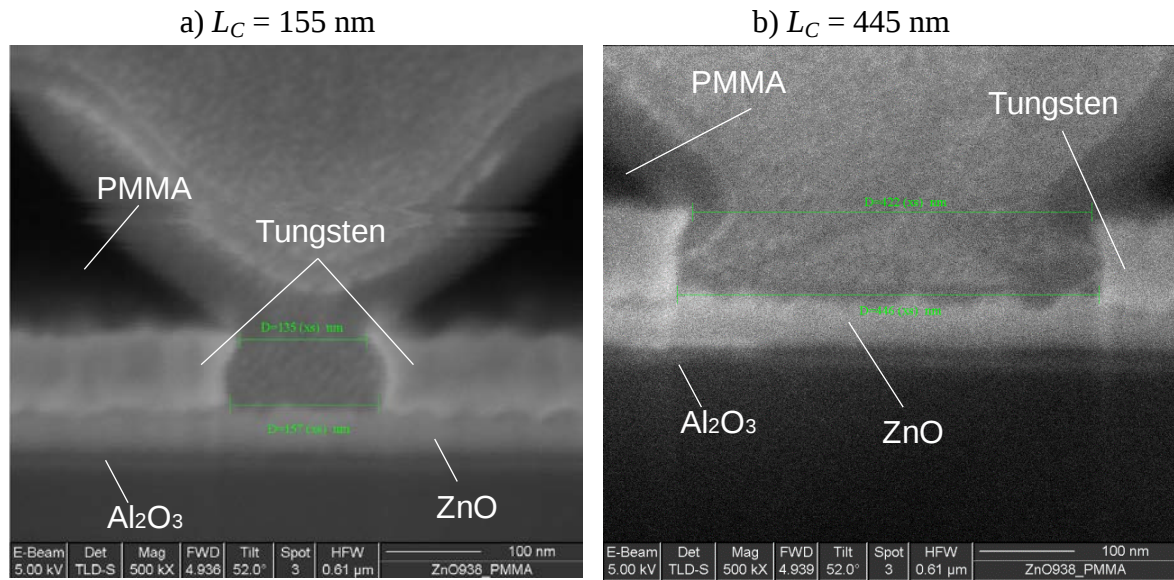


Figure 45: Cross sectional SEM images detailing the channel area ZnO TFT with tungsten source and drain contacts patterned by SF_6 -RIE prior to stripping the PMMA etch mask. SEM images show no damage to the ZnO channel layer occurred during the RIE process. a) 155 nm channel b) 445 nm channel.

Figure 46 shows top down SEM images of the channel area of the completed devices. The ZnO grains can clearly be seen in the channel area. Using the Hitachi SEM under 200-kX power the channel length of each device was measured at multiple

locations along the channel. The device image data show a uniform channel length throughout the width of the device. The subtractive SF_6 -RIE process yielded devices with channel lengths ranging from 425 nm down to 155 nm, measured using the Hitachi SEM tool.

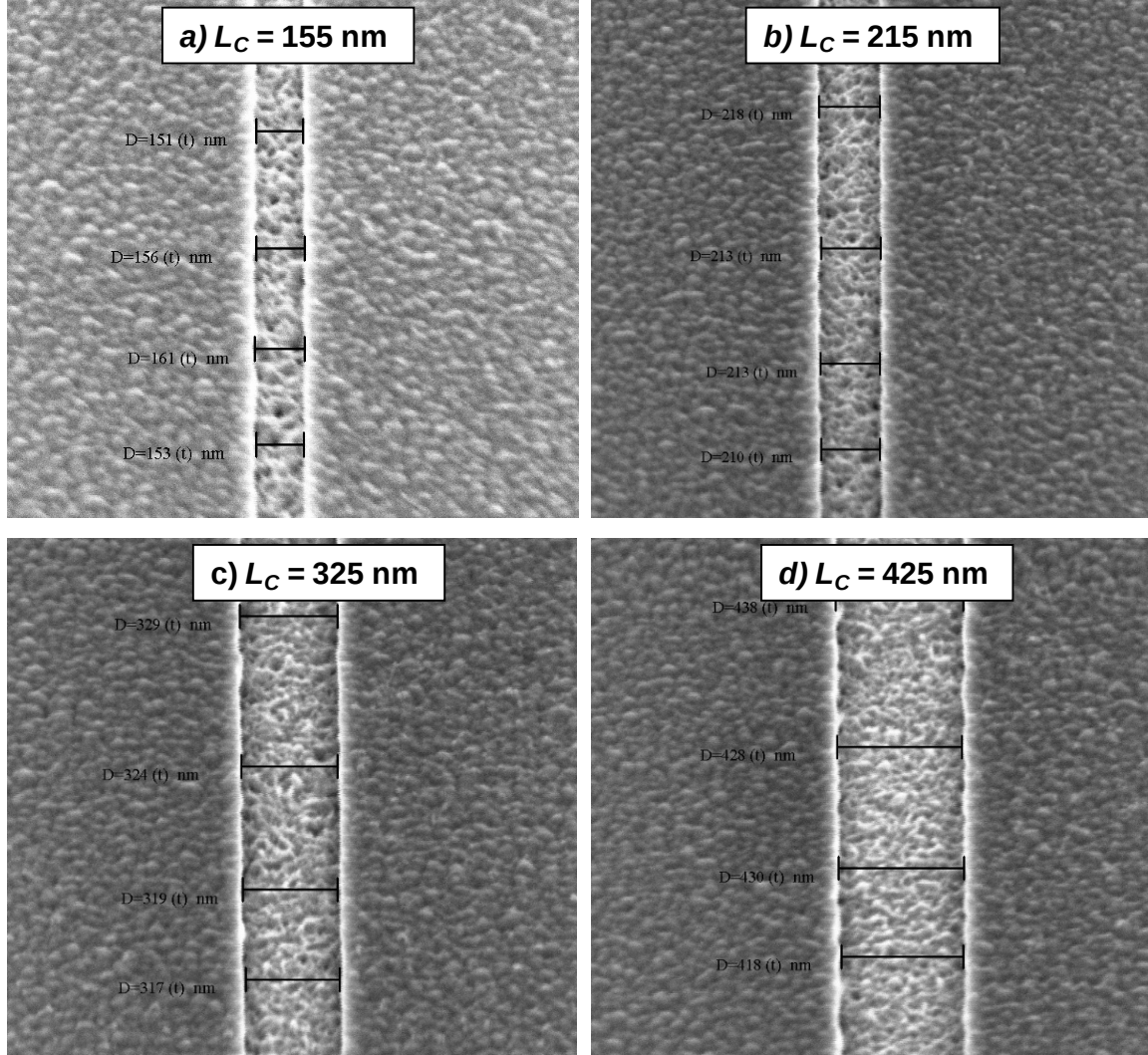


Figure 46: Top down SEM images of the channel region of ZnO TFTs with tungsten source and drain contacts patterned by SF_6 -RIE. The process yielded devices with a) $L_C = 155$ nm. b) $L_C = 215$ nm. c) $L_C = 325$ nm. d) $L_C = 425$ nm.

DC-IV Analysis

The completed sample was tested using a fully automated cascade probe system and HP4142 parameter analyzer to gather DC measurement data. The sample measured roughly 4 cm^2 , with approximately 20 die on the sample. Within each die, devices had varying channel lengths (L_C) ranging from 155 nm to 425 nm (measured using the Hitachi SEM) with a fixed channel width of $W_C = 2 \times 150 \text{ }\mu\text{m}$. Prior to device testing the sample was annealed at 250°C in atmosphere for 10 min.

The drain-current versus drain-voltage (I_D - V_D) at $V_G = 10\text{V}$, $V_{G,step} = -2\text{V}$, for all devices across the sample are shown in Figure 47. As expected, the ZnO TFTs exhibit n-type behavior with increasing I_D at higher V_G values. A linear dependence of I_D on V_D is observed at low V_D values indicating the *tungsten* source and drain contacts are Ohmic and do not exhibit any blocking behavior. However, the devices do not achieve saturation, due to lateral breakdown limitations of the short channels. From the data, a width normalized $R_{on} = 3.6 \text{ }\Omega\cdot\text{mm}$ for devices with $L_C = 155 \text{ nm}$ operating at $V_G = 10\text{V}$ was extracted.

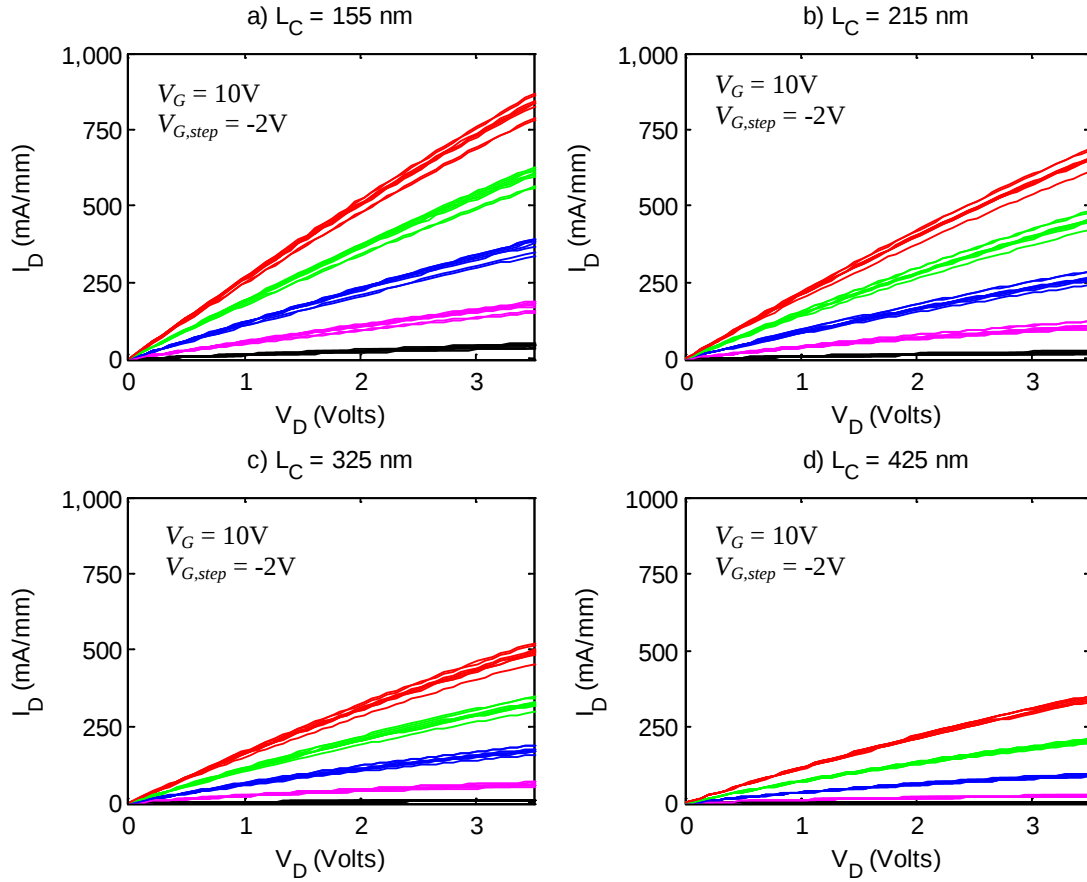


Figure 47: Plots showing the drain-current versus drain-voltage (I_D - V_D) transfer curves at $V_G = 10$ V, step -2 V, for ZnO TFTs with tungsten source and drain contacts. The channels were defined by selective SF_6 -RIE of tungsten using a e-beam defined PMMA resist as the etch mask. a) $L_C = 155$ nm. b) $L_C = 215$ nm. c) $L_C = 325$ nm. d) $L_C = 425$ nm.

The drain current density (I_D) and transconductance (G_m) plotted as a function of V_G , with $V_D = 3.5$ V are shown in Figure 48. The data show ZnO TFTs with $L_C = 155$ nm, reach a maximum I_D and G_m of 830 mA/mm and 120-mS/mm at $V_G = 10$ V and $V_D = 3.5$ V. Such high I_D values indicate that a highly conductive channel is induced in these devices. The data also show a continued increase in I_D as L_C is scaled, which is predicted using the square law model detailed in Equation

1.1. The dependence of I_D on L_C indicates velocity saturation has not been reached even at the high lateral fields associated with the 155 nm L_C devices.

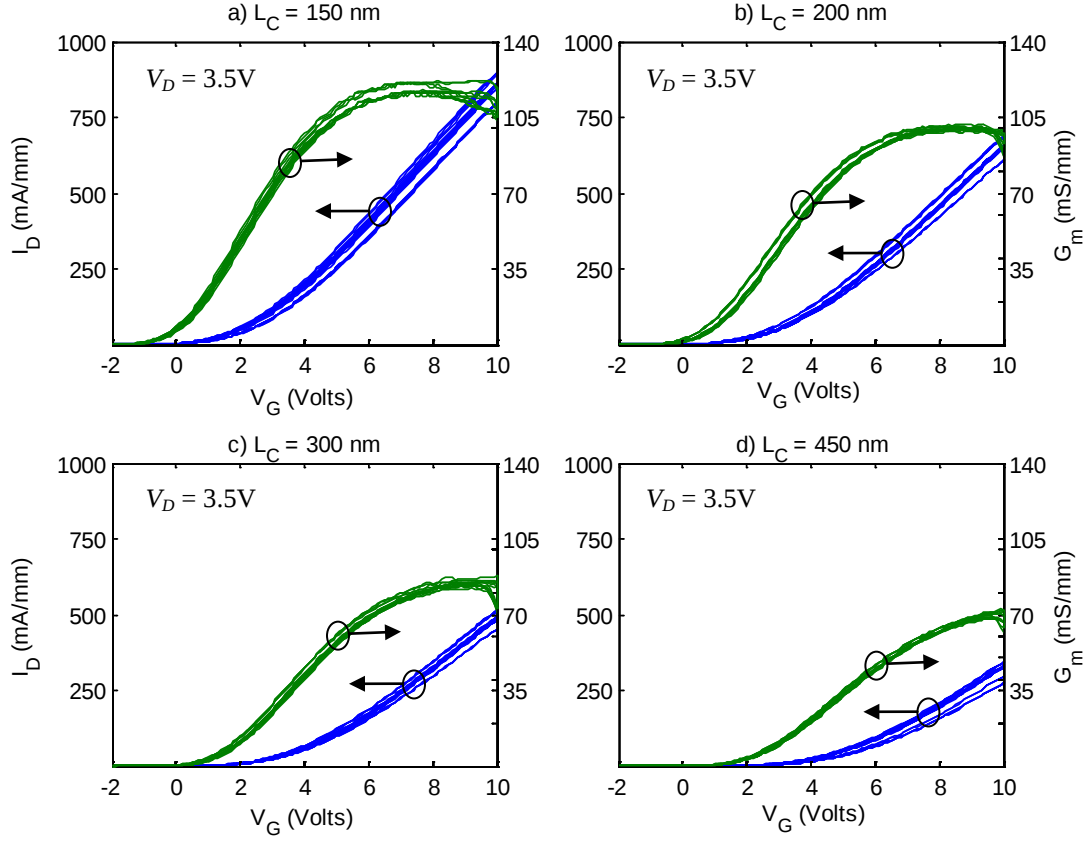


Figure 48: Plots showing the drain current density (I_D) and transconductance (G_m) as a function of V_G for ZnO TFTs with tungsten source and drain contacts. The channels were defined by selective SF_6 -RIE of tungsten using a e-beam defined PMMA resist as the etch mask. a) $L_C = 155$ nm b) $L_C = 215$ nm c) $L_C = 325$ nm d) $L_C = 425$ nm.

Although, continued increase in I_D versus V_G is observed with L_C scaling, the data show G_M saturates at high V_G values (> 8 V) for devices with L_C below 425 nm. G_M is a measure of the amount of gain the device is able to deliver. Thus the frequency performance of ZnO TFTs with L_C below 425 nm is expected to roll off at high V_G values. However, due to the high practice capacitance associated with the substrate gated structure used in this thesis, RF characterization was not feasible. Instead, future devices

should be fabricated employing a metal-gated structure in order to reduce the source to drain and drain to gate overlap capacitance values.

The cause for the observed saturation of G_M at high V_G values for ZnO TFTs is believed to be due to surface scattering of the carriers. Since the carrier transport in ZnO TFTs is done exclusively through electron transport, which is confined to the ZnO/Al₂O₃ interface. Increasing V_G values attracts electrons to the ZnO/Al₂O₃ interface, causing the carriers to scattering along the interface. The scattering effect is more pronounced as L_C is reduced, since the longitudinal electric field component (i.e. V_D) becomes smaller due to the lateral extension into the channel region. Scattering of the carriers results in a decrease in the effective mobility of the channel, corresponding to the observed saturation of G_M at high V_G values. A reduction in μ_{fe} and the resultant saturation of G_M is a common problem for short channel MOSFETs, and is one of many observed variations from the square law model often termed short channel effects as L_C is scaled below 1 μm [75].

Figure 49 shows I_D and μ_{fe} plotted as a function of V_G with the ZnO TFTs operating in the linear region (i.e. at $V_D = 0.2\text{V}$). The I_D data is plotted on a log-scale. From the data, a reduction in μ_{fe} is observed as L_C is decreased. The observed reduction in μ_{fe} is directly attributed to the scattering of the carriers along the ZnO/Al₂O₃ interface at high V_G values detailed above. Additionally, the presence of source and drain contact resistance can attribute the reduction in μ_{fe} . As L_C is decreased, the channel resistance is also decreased; however, the series source and drain resistances are independent of L_C . Therefore, the effect of parasitic resistance values associated with the source and drain contacts are more pronounced on a shorter channel device than a longer channel device.

Thus the effective mobility is decreased in short channel devices where the channel resistance is on the same order as the series source and drain resistance [76].

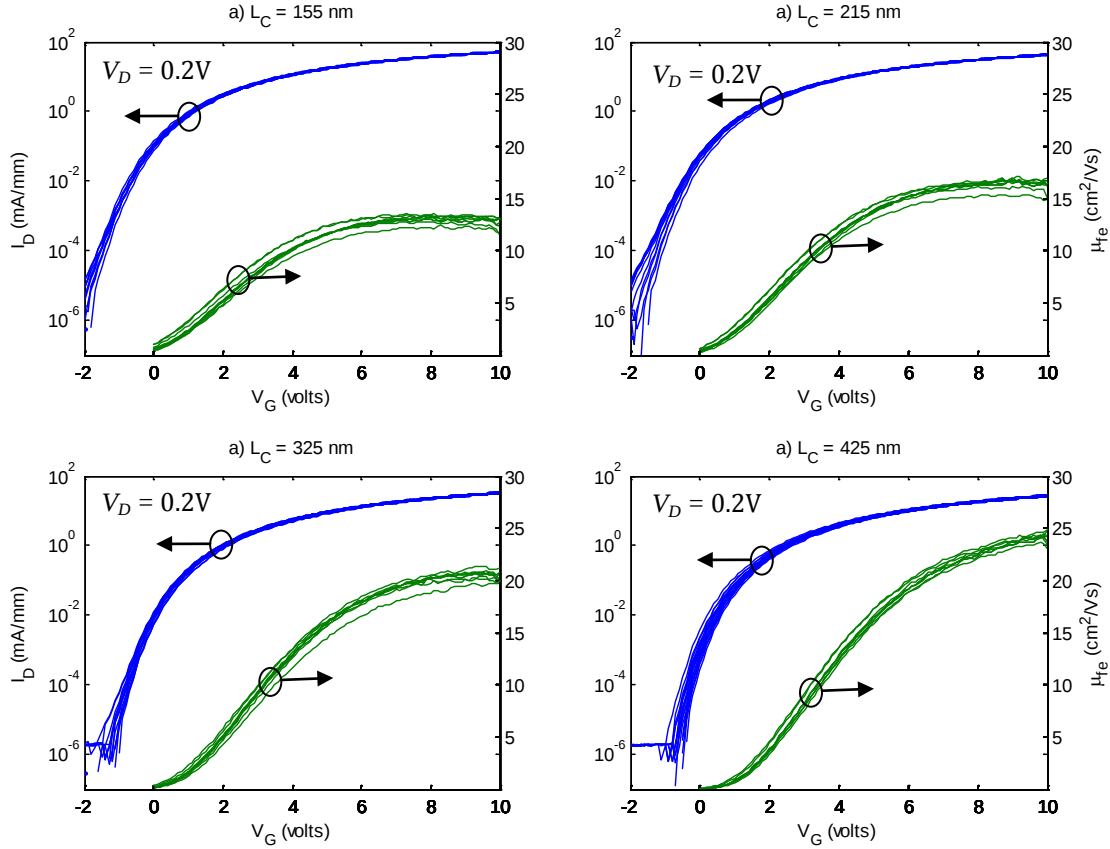


Figure 49: Plots showing the drain current density (I_D) and mobility (μ_{fe}) as a function of V_G in the linear region of operation (i.e. $V_D = 0.2V$) for ZnO TFTs tungsten source and drain contacts patterned by SF_6 -RIE through openings in a PMMA defined etch mask. A shift in V_{on} is observed as the channel length is decreased. a) $L_C = 155$ nm b) $L_C = 215$ nm c) $L_C = 325$ nm d) $L_C = 425$ nm.

A negative shift in the turn on voltage (V_{on}), defined as the V_G value that I_D displays its initial increase on a log-scale, is also observed as L_C is decreased. The device data depicted in Figure 49 demonstrates ZnO TFTs with L_C below 300 nm are not completely pinched-off at $V_G = -2V$. For switching applications, enhancement mode operation (i.e. positive V_{on}) is desirable, as no gate voltage is required to turn the device

off, thus minimizing power loss. Additionally, in high power applications enhancement mode operation is a requirement for safety reasons. If the gate connection were to be damaged, enhancement mode operation would ensure the switch would be in the off position. Thus, the observed negative shift in V_{on} is undesirable. However, devices with positive V_{on} values could possibly be fabricated using different ZnO PLD conditions or post growth annealing [13, 12]. However, modifications to the ZnO PLD process were outside the scope of this work.

Contact Resistance Extraction

Figure 50.a shows the average calculated R_{on} plotted as a function of channel-length. The average R_{on} across the sample was calculated from the linear fit from $V_D = 0$ and 0.25V using the I_D - V_D data shown in Figure 47. The smallest width-normalized R_{on} was calculated as 3.6 Ω ·mm for devices with a measured L_C of 155 nm. The low R_{on} opens the possibility of integrating ZnO TFTs in high performance switching applications, as minimizing R_{on} is critical to ensuring a switch with low insertion loss [77].

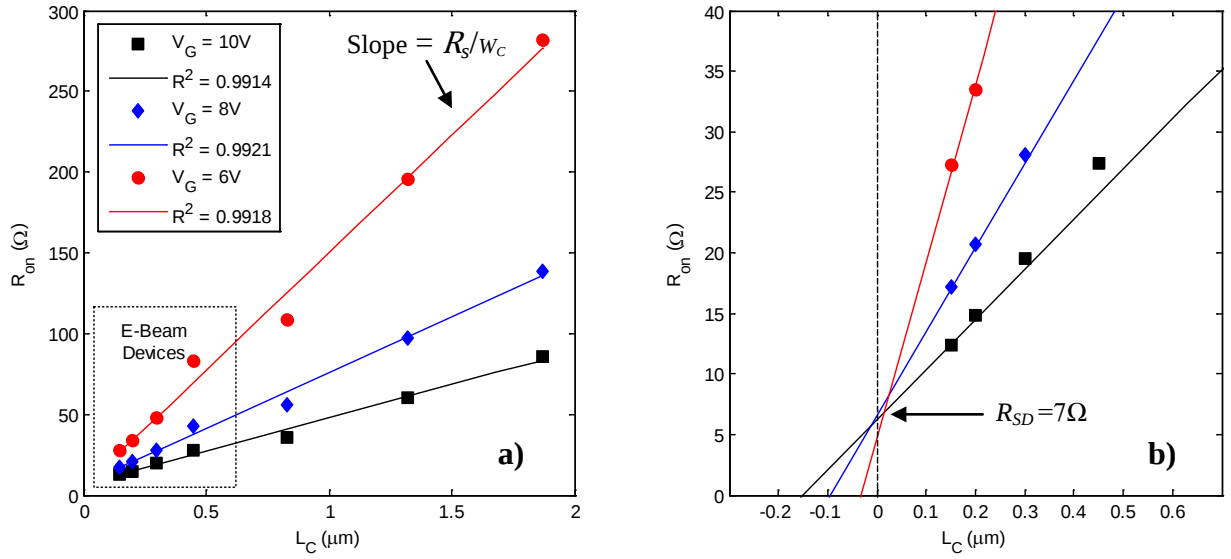


Figure 50: Plots showing R_{on} as a function of L_C for subtractive RIE defined ZnO TFTs with tungsten source and drain contacts at multiple V_G settings. A width-normalized R_{on} was calculated as $3.6 \Omega \cdot \text{mm}$ for devices with a measured $L_C = 155 \text{ nm}$, shown in (a). Additionally a width normalized $R_{SD} = 2.1 \Omega \cdot \text{mm}$ was extracted using gated-TLM, shown in (b). Symbols and lines represent data points and linear best fit, respectively.

From the data, a linear dependence of R_{on} versus L_C is observed. By calculating the linear extrapolation of the data points at $V_G = 6, 8$, and $10V$, a common cross point at $L_C = 0$ was extracted. From gated-TLM, detailed in Equation 2.12, the intersection at $L_C = 0$ is interpreted as the total parasitic source/drain resistance. The extraction of R_{SD} is illustrated in Figure 50.b. Normalizing the data by channel width yields $R_{SD} = 2.1 \Omega \cdot \text{mm}$, indicating the ZnO-tungsten interface is a low resistive ohmic contact. The sheet resistance (R_s) was also extracted from the slope of the linear best-fit lines at each V_G , again using Equation 2.12. Figure 51 illustrates the extracted R_s plotted as a function of V_G . From the data, a minimum channel sheet resistance for the ZnO TFTs was observed as $13.1\text{-k}\Omega/\square$ at a $V_G = 10V$.

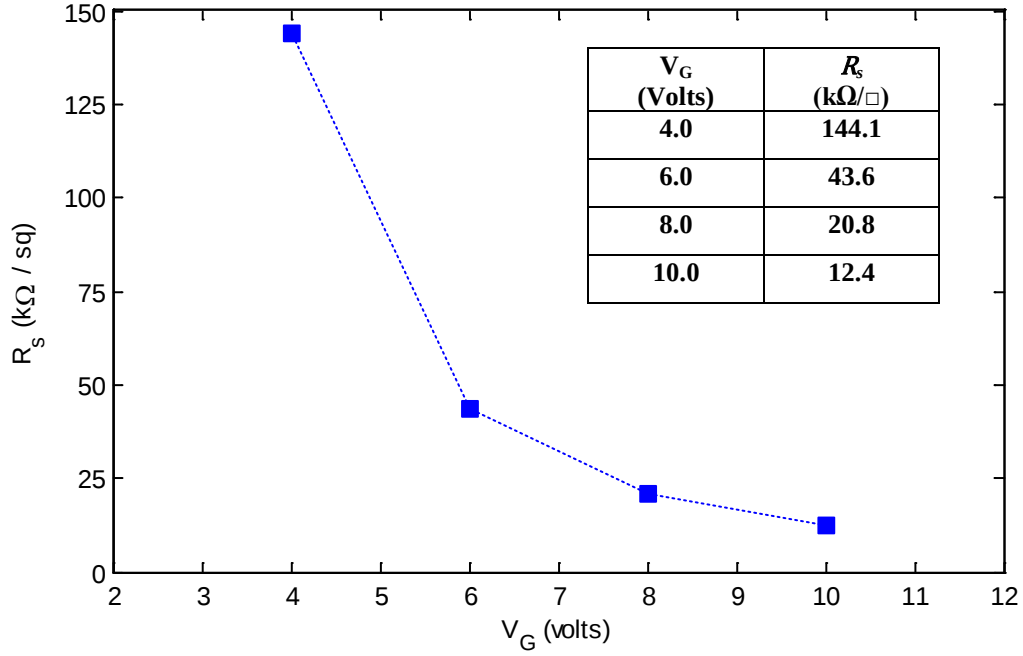


Figure 51: Plot showing the extracted sheet resistance (R_s) as a function of gate voltage for subtractive RIE defined ZnO TFTs with tungsten source and drain contacts. From the data, a minimum $R_s = 13.1\text{-}k\Omega/\square$ at a $V_G = 10\text{V}$ was observed.

Although an extracted R_{SD} of $2.1\ \Omega\cdot\text{mm}$ is low, and confirms the tungsten/ZnO interface is ohmic. R_{SD} composes over 50% of the total on-resistance of a 155 nm ZnO TFT. Therefore, significant improvement in R_{on} can be expected by reducing R_{SD} . Decreasing the contact resistance of a metal-semiconductor junction is often accomplished by rapid thermal annealing, however Lim *et.al.* demonstrated that post deposition annealing of sputtered tungsten films on n-type ZnO at temperatures above 700°C produces rectifying behavior with schlocky barrier heights of 0.45 eV [56]. Therefore, annealing of the samples is not expected to reduce R_{SD} . Instead, selective doping of the ZnO thin-film could be accomplished in order to lower the barrier height between the ZnO thin-film and tungsten. Additionally, investigation into other contact metals that can be selectively etched using a fluorine based RIE should be investigated in

attempt to reduce the contact resistance between the ZnO thin film and source and drain contacts.

Lateral Break-Down Voltage

An attempt to measure the lateral breakdown voltage (V_{BD}) of the devices was undertaken. V_{BD} was extracted using the HP442 parameter analyzer by ramping I_D from 0.0 to 1.0 $\mu\text{A}/\text{mm}$ at a fixed $V_G = -2\text{V}$ (so the device is in pinch-off). V_{BD} was thus defined as the V_D value when I_D reached 1 mA/mm . For an accurate lateral V_{BD} value to be extracted, two parameters must be met. First, the gate dielectric must not break down prior to the ZnO channel, and second, the device must be in pinch-off. As shown in Figure 49, devices with L_C below 300 nm do not completely pinch-off at $V_G = -2\text{V}$, and therefore were not measured.

Figure 52 illustrates the extraction of V_{BD} on a 320 nm subtractive RIE defined ZnO TFT. From the data, the gate current (I_G) also starts to exponentially increase at $V_D = 9\text{V}$, however I_G is two-orders of magnitude lower than I_D , indicating the majority of the current is conducting from drain to source through the ZnO thin-film (not from drain to gate, through the Al_2O_3 dielectric). Thus, breakdown is occurring laterally (due to a breakdown of the ZnO thin-film), not due to breakdown of the gate dielectric. From the data, the V_{BD} was extracted as 8.5V. Converting to electric field ($E = V/L$), the critical electrical field breakdown is 26.7 $\text{V}/\mu\text{m}$. The observed electric field breakdown is consistent with longer channel devices previously fabricated at AFRL.

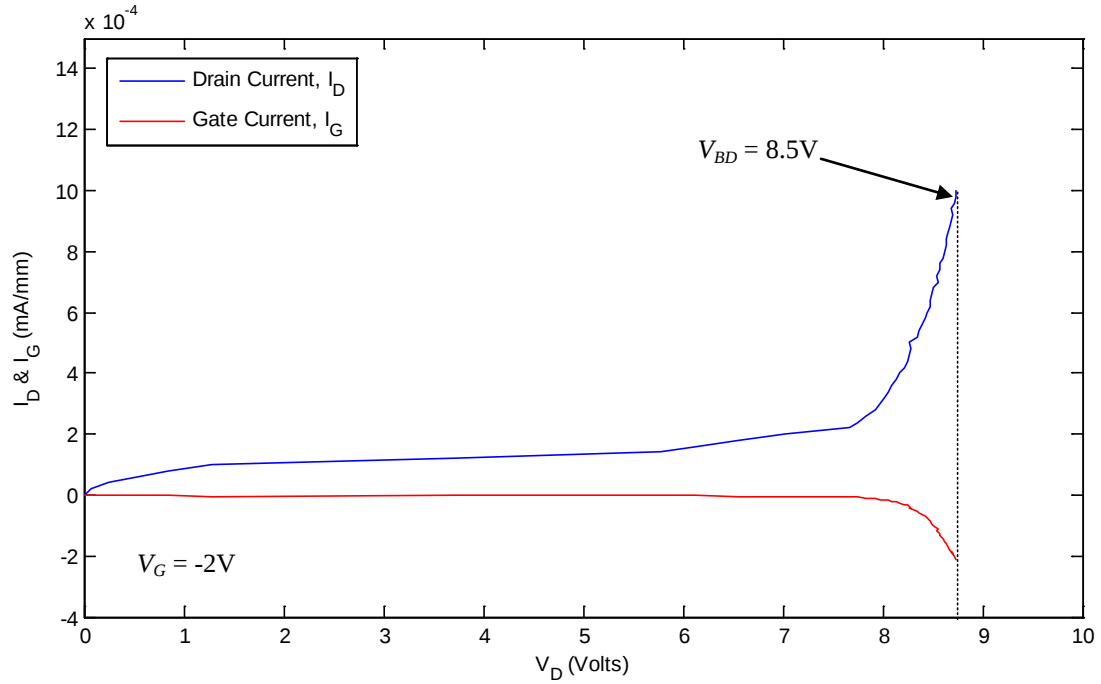


Figure 52: Plot showing the extraction of lateral breakdown voltage (V_{BD}) for a subtractive plasma-etched defined ZnO TFT with a 320 nm channel. An exponential increase in drain current is observed at a drain voltage of 8.5V indicating lateral breakdown of the ZnO thin-film channel.

The low observed lateral breakdown voltage is a series issue if ZnO TFTs are to be utilized in high performance switching applications. A typical switch needs to withstand voltage swings anywhere from 10V up to hundreds of volts depending on the application. The low lateral breakdown of the fabricated ZnO TFTs could be overcome in some applications by stacking multiple devices to form a switch arm [77]. However, stacking of devices requires additional fabrication complexity and increases associated capacitance, ultimately degrading the performance of the circuit. Instead research into extending the lateral breakdown field of the ZnO thin film should be pursued.

The observed lateral field breakdown of $26.7 \text{ V}/\mu\text{m}$ is over an order of magnitude lower than the theoretical electric field breakdown for single-crystal ZnO [42], leaving

significant opportunity for extending device performance. One theory for the low observed lateral field breakdown is that a leakage path on the backside of the channel exists between the source and drain of the device. Minimizing the back-side conduction path could be accomplished by using a thinner ZnO film, enabling the applied gate voltage to control the backside of the channel. Another option is to apply a passivation layer over the completed device. Device passivation is common practice for TFTs used in the display market [30]. Furthermore, passivation and post-heat treatments on bottom-gate IGZO and ZnO TFTs has been shown to significantly improve device performance, including an increase in sub-threshold slope, decrease in hysteresis, and positive shift of the threshold voltage [78, 79].

Results Overview

An attempt to pattern ZnO TFTs with nano-scale channel lengths by selective SF₆-RIE of tungsten through an e-beam defined etch mask was undertaken. SEM analysis of the devices show etching of the ZnO channel occurred during the SF₆-RIE process when utilizing ZEP520a as an e-beam defined mask. However, no thinning or attack was observed when using a PMMA electron sensitive resist as the etch mask during the SF₆-RIE process. Therefore, it is hypothesized that the ClCH₃ copolymer make-up of ZEP520a is breaking down during the RIE process, resulting in Cl-contamination in the plasma causing the ZnO to be attacked. Additionally, no attack of the ZnO thin-film was observed when fabricating ZnO TFTs with micron scale channel lengths using a Ni etch mask during the SF₆-RIE process. These observations point to an interaction with ZEP520a and the RIE process as the cause for the ZnO attack.

Next, through selective SF₆-RIE of tungsten films through openings in an e-beam defined PMMA resist, ZnO TFTs as small as 155 nm were successfully fabricated. The data show ZnO TFTs with 155 nm channels are capable of reaching drain current densities of over 800 mA/mm at $V_G = 10\text{V}$ and $V_D = 3.5$. Additionally, the width normalized R_{on} of ZnO TFTs with 155 nm channels was measured at $3.6\ \Omega\text{mm}$ with an observed total parasitic source and drain resistance (R_{SD}) of $2.1\ \Omega\text{mm}$ using gated-TLM. The low R_{on} observed in this work is a requirement for use in switching applications which require low insertion losses.

Unfortunately, the fabricated ZnO TFTs display a relatively low lateral breakdown of $26.7\ \text{V}/\mu\text{m}$, which is over an order of magnitude lower than single crystal ZnO. Research in extending the lateral breakdown of the devices is required if ZnO TFTs are to be used in high performance or RF switching applications. However, even a modest increase in the lateral electric field breakdown of the ZnO thin-film would enable ZnO TFTs to operate at drain current values over 1 A/mm. Figure 53 shows that average maximum drain current density versus channel length (I_D - L_C) on a on a log-log plot for ZnO TFTs with tungsten source and drain contacts patterned using a SF₆-RIE. Two trend lines are shown, one for ZnO TFTs operating at $V_D = 3.5\text{V}$ and another for ZnO TFTs operating at $V_D = 8\text{V}$. Based on the data, doubling the lateral field electric field breakdown to $52\ \text{V}/\mu\text{m}$, would enable ZnO TFTs with 155 nm channels to operate at $V_D = 8\text{V}$. Utilizing the extrapolated best fit curve, ZnO TFTs with 155 nm channels operating at $V_G = 10\text{V}$ and $V_D = 8\text{V}$ could theoretically operate at drain current densities over 2.9 A/mm at a total width DC power ($=I_D \times V_D$) of 23 W/mm. The combination of

low R_{on} and high performance of ZnO TFTs fabricated in this work demonstrates the potential for ZnO TFTs to be used in high performance and RF switching circuits.

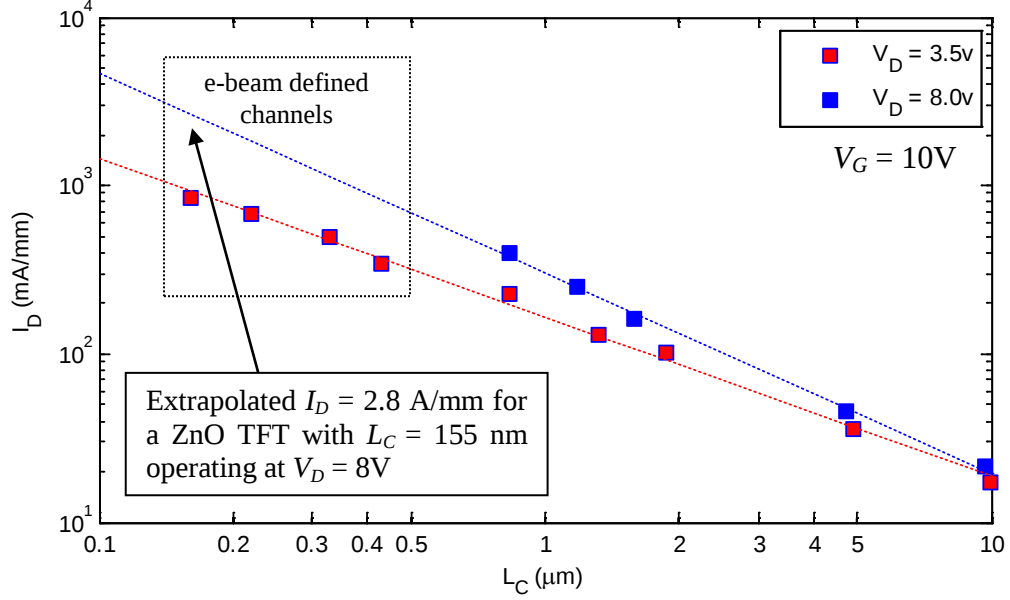


Figure 53: Plot showing drain current density dependence on channel length (I_D - L_C) on a log-log scale for ZnO TFTs with tungsten source and drain contacts patterned by SF_6 -RIE operating at $V_D = 3.5$ and 8.0V . Symbols and line represent measured data and best fit, respectively.

Summary

This chapter presented the data and observations found during device fabrication and testing. The following chapter details conclusions found during research, the significance of the work present and recommendations for continued research.

V. Conclusion and Recommendations

Chapter Overview

This chapter provides a summary of the research conducted, significance of the work and recommendations for continued research.

Summary of Research

The work presented in this thesis advanced the understanding of fabricating high performance ZnO TFTs with nanometer scale channel lengths. The results show sputtered tungsten is a promising ohmic contact material that can be etched against ZnO using a fluorine-based RIE in order to define the active current carrying channel of the device. SEM investigation of the fabricated ZnO TFTs with subtractively RIE defined tungsten source and drain contacts revealed a highly anisotropic etch profile was achieved using a CF_4/O_2 and SF_6 RIE etch chemistry with a plasma platen power of 200W. Additionally, no thinning of the underlying ZnO channel area was observed indicating a highly selective etch was achieved. However, decreasing the RIE power below 150W for both the CF_4/O_2 and SF_6 RIE chemistries resulted in lateral etching and undercutting of the etch mask. The observed lateral etching resulted in an increase in the measured effective channel length and a decrease in electrical performance of the device.

Next, the DC electrical characteristics of ZnO TFTs with micron scale channel lengths employing tungsten source and drain contacts defined by CF_4/O_2 and SF_6 RIE at a 200W plasma power were investigated. The data show ZnO TFTs with tungsten contacts patterned using a subtractive CF_4/O_2 and SF_6 RIE process display similar electrical performance to ZnO TFTs with lift off defined Ti/Pt/Au/Ni contacts. From the DC-IV

data, no change in I_D , G_M and μ_{fe} was observed in ZnO TFTs patterned using the different methodologies. Therefore it can be concluded that the CF_4/O_2 or SF_6 RIE process does not damage or degrade the electrical characteristics of the ZnO thin film.

Next, fabrication of ZnO TFTs with nanometer scale channel lengths was attempted by subtractive SF_6 -RIE of tungsten against ZnO through e-beam defined openings in ZEP520a and a PMMA resist. When utilizing ZEP520a, unexpected attack of the ZnO film during the RIE process was discovered by SEM. It is theorized that the ClCH_3 co-polymer within ZEP520a outgases during the RIE process, resulting in chlorine contamination in the plasma. ZnO is known to etch readily in Cl-containing plasmas, thus the Cl contamination is responsible for the attack of the active ZnO thin film. Conversely, no thinning or attack of the ZnO channel was observed using a e-beam defined PMMA etch mask which does not contain a Cl co-copolymer.

Finally, ZnO TFTs with SEM measured channel lengths as small as 155 nm were successfully demonstrated by selective SF_6 -RIE of tungsten through e-beam defined opening in PMMA. Electrical testing of the devices show ZnO TFTs with 155 nm channels operate at maximum densities and transconductance values over 830 mA/mm and 120-mS/mm, respectively. From the I_D - V_D data, a width normalized R_{on} of $3.6 \Omega \cdot \text{mm}$ at a $V_G = 10\text{V}$ was calculated, with a total observed width normalized parasitic source and drain resistance of $2.1 \Omega \cdot \text{mm}$, indicating the tungsten/ZnO interface is of low resistance. Moreover, the data show DC current and power densities of 2.8 A/mm and of 23 W/mm, respectively, are possible with a modest increase to the lateral field breakdown of the ZnO thin-film. The demonstration of high current, extrapolated high power and low R_{on}

of ZnO TFTs in this work suggests the potential for ZnO TFTs in switching or RF power applications of interest to the military.

Recommendations for Future Work

The stated goal of developing a subtractive RIE process for patterning ZnO TFTs with nano-scale channel lengths in this thesis was met; however, several issues remain open. First, the subtractive SF₆-RIE process using an e-beam defined PMMA etch mask was not optimized. A loading effect was observed during the SF₆-RIE process when attempting to etch tungsten through e-beam defined openings in a PMMA resist. This loading effect decreased the etch rate of tungsten in the SF₆-RIE. Therefore, research needs to be conducted to optimize the RIE process and ensure repeatable results. Furthermore, higher viscosity PMMA solutions, or possibly other electron-beam sensitive resists, should be utilized rather than relying on a double thickness of 495-PMMA-A6. Additionally, a design of experiments should be completed in order to optimize the exposure and develop times of the PMMA. This would allow for continued device scaling, possibly enabling devices with channel lengths below 50 nm.

Next, although a low width-normalized R_{SD} of 2.1 $\Omega\cdot\text{mm}$ was observed using gated-TLM, indicating the tungsten/ZnO interface is low resistance. The extracted R_{SD} represents nearly 50% of the total R_{on} of a 155 nm ZnO TFT. Therefore, research into reducing the contact resistance should be investigated. Studies could include the use of other refractory metals that can be etched using a fluorine based plasma process. Both molybdenum (Mo) and tantalum (Ta) have been shown to etch in fluorine plasmas [80]. Additionally, sputtered TiW films should be revisited. One possible solution to the issues

of etching TiW in this work would be to use a TiW target with a lower concentration of titanium during the sputter deposition step. Additionally, other plasma processes such as inductively coupled plasma (ICP) could be attempted. Finally, selective doping of the ZnO thin film could be accomplished in an attempt to lower the barrier height of the ZnO/tungsten interface.

Additionally, in future experiments, ZnO TFTs employing a metal gated topology, rather than the substrate gated topology used in this work, need to be investigated. A metal-gated topology would reduce the high source-to-gate (C_{GS}) and drain-to-gate capacitances (C_{DS}) associated with the substrate gated topology. Reducing C_{GS} and C_{DS} is critical for high frequency operation. Therefore, the use of a metal gated topology would allow for ZnO TFTs with nanometer scale channel lengths patterned by RIE to be tested for their RF levels of performance. Inserting previously observed mobility values of ZnO thin-films of $110 \text{ cm}^2/\text{Vs}$ [17] along with the SEM measured channel lengths of 155 nm patterned in this work into the unity gain cutoff frequency equation shown in Equation 1.9, ZnO TFTs with 155 nm channels could theoretically operate at cutoff frequencies over 60 GHz, making them suitable for microwave electronic applications.

Finally, the low observed lateral breakdown of $26.7 \text{ V}/\mu\text{m}$ needs to be addressed if ZnO TFTs are to be utilized in high performance and RF switching applications. One theory for the low observed lateral field breakdown is due to a leakage path on the backside of the channel. Minimizing the back-side conduction path could be accomplished by using a thinner ZnO film, enabling the applied gate voltage to control the backside of the channel. Another option is to apply a passivation layer over the

completed device. Passivation treatments on bottom-gate IGZO TFTs has been shown to significantly improve device performance, including an increase in sub-threshold slope, decrease in hysteresis, and positive shift of the threshold voltage [78]. Other research groups have investigated using SiO₂ or Si₃N₄ as passivation layers as well [79]. However, even a modest increase in the lateral electric field breakdown on the ZnO thin-film would enable ZnO TFTs to operate at drain current values over 1 A/mm. The data collected in this work demonstrate that ZnO TFTs with 155 nm channels operating at $V_G = 10\text{V}$ and $V_D = 8\text{V}$ could reach drain current densities over $I_D = 2.9\text{ A/mm}$ at a total width DC power ($=I_D \times V_D$) of 23 W/mm.

Significance of Research

Thin-film electronics, based on high performance ZnO TFTs, have the opportunity to not only increase the effectiveness of existing electronic subsystems, but also offer the possibility of developing novel electronic functions in non-traditional areas. One example for future ZnO TFT technology of particular interest to the military is in wireless communications systems or radar applications. In wireless communications and radar systems a front-end module (FEM) is used as an interface between the antenna and RF transceiver. A FEM typically consists of power amplifiers, switches, low-noise amplifiers, control circuitry, and passive elements [77]. Traditionally, the power amplifiers and switches in a FEM are manufactured using single-crystal GaAs or GaN MMIC technology which are then connected to Si based control circuitry through expensive wire-bonding or flip-chip technology. An alternative solution is to use ZnO TFT technology to replace some of the FEM components.

Utilizing ZnO TFT technology could enable complete wireless communication systems to be fabricated on large area or even flexible substrates. Additionally, high performance ZnO TFTs could be integrated directly on GaAs or GaN MMICs. Integration of ZnO TFT technology with existing MMIC technology would reduce weight, decrease form factor of the completed module and ultimately lower production costs. Since R_{on} scales with channel length, a primary decision in ZnO TFT optimization for switching technology is reducing the channel length in order to decrease insertion losses. In this research, deep sub-micron scaling of ZnO TFTs was investigated using a novel fabrication process for patterning the source and drain contacts. The low R_{on} and extrapolated high DC power densities of ZnO TFTs fabricated in this work demonstrate the potential of ZnO TFT technology for developing high performance and RF switching circuits required for wireless communication and radar system applications.

Appendix A: List of Symbols

C_{ox}	oxide capacitance per unit length	R_{SD}	parasitic source and drain resistance
G_m	transconductance	S_{ss}	sub-threshold swing
f_t	unity-gain cutoff frequency	t_{ox}	gate-oxide thickness
I_D	drain current	μ_{fe}	field-effect mobility
I_G	gate current	V_{BD}	breakdown voltage
L_C	channel length	V_D	drain voltage
R_{ch}	channel resistance per unit length	V_G	gate voltage
R_{Drain}	parasitic drain resistance	V_{on}	on voltage
R_{on}	source-to-drain on-resistance	V_t	threshold voltage
R_s	sheet resistance	W_C	channel width
R_{Source}	parasitic source resistance		

Appendix B. Elements and Element Compounds

Al	Aluminum	Ni	Nickel
Al ₂ O ₃	Aluminum-Oxide	O ₂	Oxygen
Au	Gold	Pt	Platinum
CF ₄	Carbon-tetraflouride	Si	Silicon
Cu	Copper	SiO ₂	Silicon-Dioxide
Cl	Chlorine	SF ₆	Sulfur-hexaflouride
GaAs	Gallium-Arsenide	Ti	Titanium
GaN	Gallium-Nitride	TiW	Titanium tungsten alloy (10-90)
H ₂	Hydrogen	W	Tungsten
HCl	Hydrochloric acid	ZnO	Zinc-oxide
IGZO	Induim-galluim-zinc-oxide		
N ₂	Nitrogen		

Appendix C: Unaxis 790 Series Plasma System Etch Recipes

C.1: CF₄/O₂ RIE Recipes

Etch Gas	Gas Flow Rate (sccm)	Chamber Pressure (mTorr)	Plasma RF Power (Watts)	*DC Bias (Volts)
CF ₄ /O ₂	40:2	40	200	465
CF ₄ /O ₂	40:2	40	150	223
CF ₄ /O ₂	40:2	40	100	184
CF ₄ /O ₂	40:2	40	50	111

C.2: SF₆ RIE Recipes

Etch Gas	Gas Flow Rate (sccm)	Chamber Pressure (mTorr)	Plasma RF Power (Watts)	*DC Bias (Volts)
SF ₆	40	40	200	205
SF ₆	40	40	150	130
SF ₆	40	40	100	85
SF ₆	40	40	50	40

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14. ABSTRACT Thin-Film-Transistors (TFTs) employing undoped zinc-oxide (ZnO) thin-films are currently being investigated by the Air Force for microwave switching applications. Since the on-resistance (R_{on}) of the device scales with channel length (L_C), ZnO TFT optimization should be focused on reducing L_C , therefore minimizing the associated insertion losses. In this research, deep sub-micron scaling of ZnO TFTs was undertaken using a subtractive reactive-ion-etch (RIE) process. Under optimum processing conditions, ZnO TFTs with L_C as small as 155 nm were successfully demonstrated. The active ZnO channels of the TFTs were patterned by selective SF_6 -RIE of a tungsten ohmic film through electron-beam defined openings in a polymethyl-methacrylate (PMMA) based resist. Through electrical testing, the width normalized R_{on} of ZnO TFTs with 155 nm channels was extracted as 3.6 Ω -mm and the devices were found to operate at drain current densities and transconductance values of 830 mA/mm and 121 mS/mm, respectively. Additionally, a total width-normalized source and drain parasitic resistance of 2.1 Ω -mm was observed using a gated transfer length method (TLM), indicating the tungsten-ZnO interface is low resistance. This demonstration of high performance and low R_{on} suggests the potential for ZnO TFTs in switching and microwave power applications.					
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