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**COGNITIVE RADIO LOW-ENERGY SIGNAL ANALYSIS  
SENSOR INTEGRATED CIRCUITS (CLASIC)**

**A Broadband Mixed-Signal Iterative Down Conversion  
Spectrum Analyzer For Signal Recognition Applications**

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14. ABSTRACT This research addressed the design of spectrum channelizers spanning a frequency range from baseband to several GHz. The work demonstrates power-efficient architectures that channelize the input spectrum in the analog or mixed-signal domain, in order to reduce the performance and dynamic range burden on the baseband processors that may be utilized for signal sensing or detection tasks in the digital domain. The approaches allow for full or partial spectrum analysis that can be adapted based on system requirement. Dynamic range enhancement based on active interference cancellation can be implemented. A key aspect to the channelizers is that they minimize the requirement for independent frequency synthesizers, and allow for spectrum decomposition based on the use of a single primary clock.						
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# 1 Summary

This report describes a University of Texas & Columbia University development project funded under the DARPA Cognitive radio Low-energy signal Analysis Sensor Integrated Circuits (CLASIC) program.

This research addressed the design of spectrum channelizers spanning a frequency range from baseband to several GHz. The work demonstrates power-efficient architectures that channelize the input spectrum in the analog or mixed-signal domain, in order to reduce the performance and dynamic range burden on the baseband processors that may be utilized for signal sensing or detection tasks in the digital domain. The approaches allow for full or partial spectrum analysis that can be adapted based on system requirement. Dynamic range enhancement based on active interference cancellation can be implemented. Critical challenges in the design and implementation of the channelizers were identified and addressed as part of this work. Design concepts were verified by means of integrated circuit implementations. A key aspect to the channelizers is that they minimize the requirement for independent frequency synthesizers, and allow for spectrum decomposition based on the use of a single primary clock.

## 2 Methods, Assumptions and Procedures

The proposed architecture was based on channelization of the RF input from 3-30 GHz in order to select a 500 MHz wide band. This 500 MHz band is applied to a baseband concurrent channelizer, which divides the band into 16-32 sub-bands that are simultaneously available. By pre-processing the signals in the analog domain, it is expected that the energy requirement of any signal detection scheme used at the outputs of the channelizer will be reduced, compared to a fully digital approach. A high-level architectural view of this approach is shown in Fig. 1. Frequency synthesis for the RF and baseband channelizers is indicated as well.

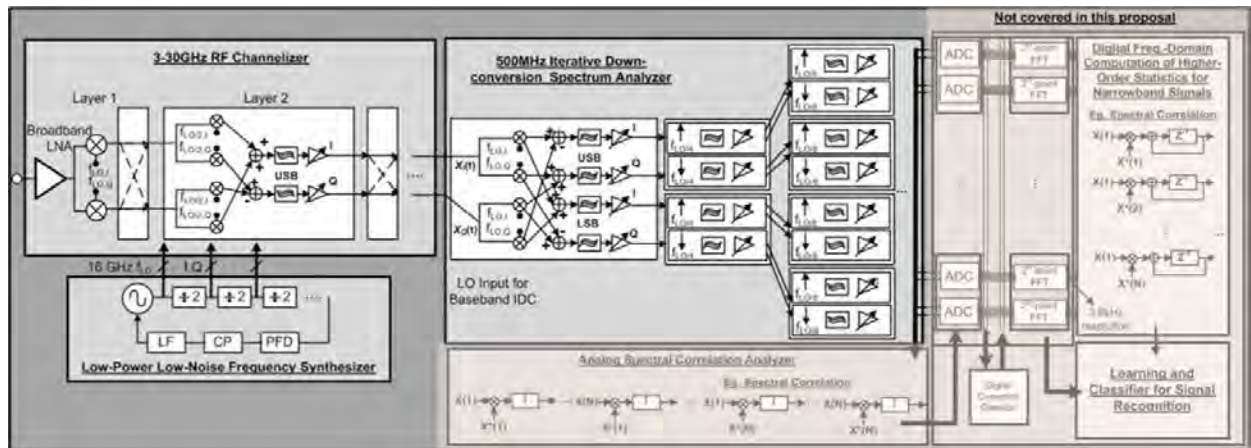


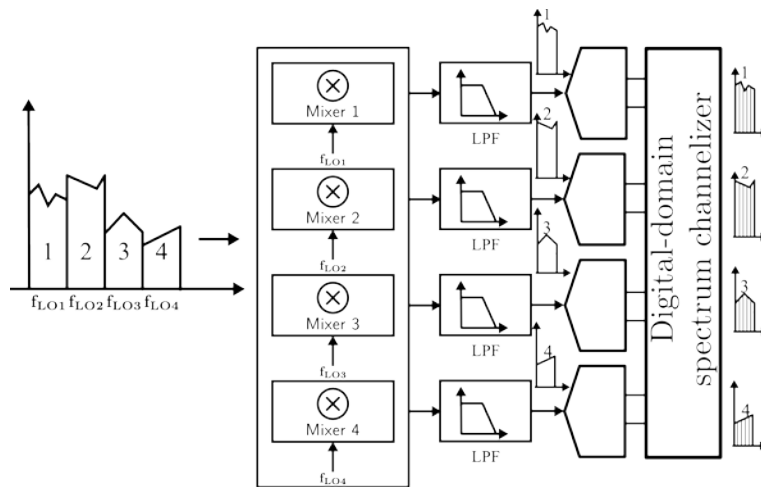
Figure 1: Top level architecture

### 3 Baseband-to-GHz Channelizers with Inherent Frequency Synthesis

The goal of the proposed research was to investigate efficient architectures for channelization of broadband analog signals, for signal-sensing applications. The team at UT focused on broadband baseband signals, with bandwidths up to several hundreds of MHz.

State-of-the-art spectrum channelizers employ broadband analog-to-digital converters, with digital-domain spectrum analysis. For bandwidths of the order of several hundreds of MHz, this requires the use of pipelined or time-interleaved analog-to-digital converters. A broadband ADC-based design faces several architectural and implementation challenges [A1]. Examples of architectural challenges include:

1. The requirement for full-spectrum digitization even if a limited portion of the spectrum is to be analyzed.
2. Self-jamming of portions of the spectrum with small signal strength, by those portions with relatively large signal content.

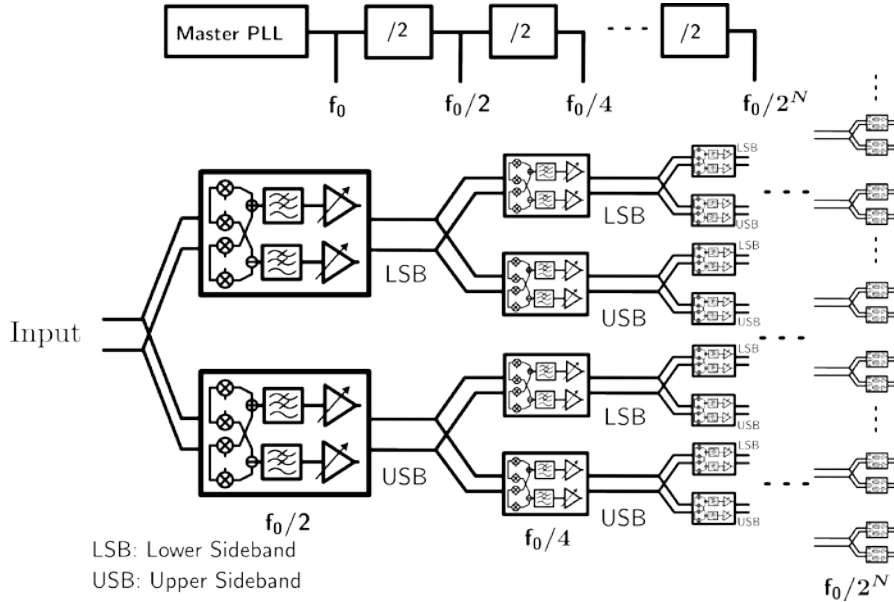


**Figure 2: Mixer-bank based channelizer**

Implementation challenges include the requirement for a broadband amplifier, with dynamic range in excess of the channelizer when small signals need to be analyzed which can be power-hungry, and the necessity for ADC sampler bandwidth in excess of the full bandwidth of the input signal. It has also been empirically observed that ADC power increases non-linearly with bandwidth, beyond a critical signal bandwidth in any given technology.

An architecture that performs coarse channelization in the analog domain and fine channelization in the digital domain addresses the above challenges. In such an approach, the broadband input is channelized into multiple sub-bands in the analog domain. Each of the sub-bands is then channelized further in the digital domain. This relaxes the sampling requirement on the ADCs in the signal path. Furthermore, the gains across the sub-bands can be equalized, thereby relaxing the problem of self-jamming. Finally, such a solution partitions the required gain across

frequencies, thus avoiding the need for a large gain preceding at the input itself.



**Figure 3: Architecture of IDC**

A mixer-bank e.g. [A2, A3] (figure 2) can be employed for such a design. A key challenge arises from the requirement for multiple LO sources in such an approach. If frequency synthesizers with independent oscillators are employed for generation of the LOs, IC implementation becomes difficult. This is the case since placing multiple concurrently operating oscillators on the same IC can lead to issues such as frequency-pulling, injection locking, and large spurious generation. Furthermore, it is also critical in such an approach to ensure that the harmonic response of the LOs is limited. Typically switching mixers are preferred over multipliers, since these are insensitive to amplitude noise on the LOs. However, the use of switching mixers also leads to large harmonic response, which can cause undesired portions of the input spectrum to be downconverted to a given sub-band, in addition to the desired signal.

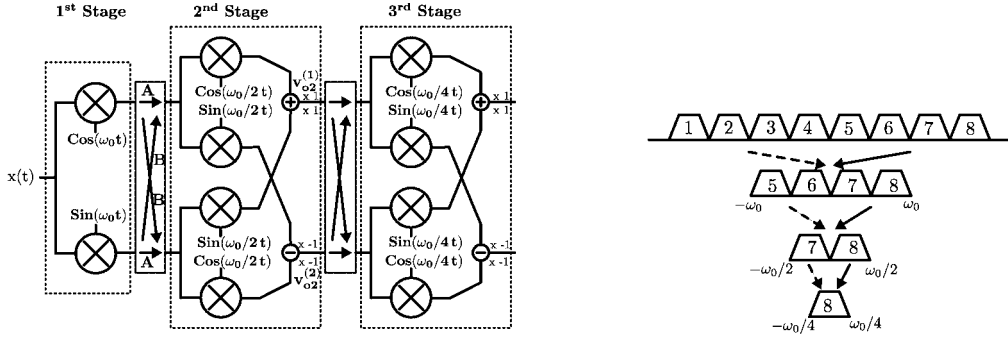
In the sections below, we describe the techniques and architectures that were demonstrated as part of the research, to address the above limitations of existing solutions.

### 3.1 Iterative Downconverter Architecture for channelization

An iterative downconverter (IDC) architecture was initially proposed to provide concurrent channelization of a broadband input spectrum (Fig. 3) [A4]. The architecture utilizes a cascade of  $N$  image-reject downconversion stages, to divide the incident spectrum into  $O(2^N)$  sub-bands. Each stage employs a local oscillator (LO) frequency that is half of that used in the previous stage.

The implementation of a single path within the IDC that describes this idea is shown in Fig. 4 below [A5]. The first stage of mixers in this cascade uses an LO of  $f_0 = \omega_0/2\pi$ , the second employs an LO of  $(1/2)(\omega_0/(2\pi))$  and the third an LO of  $(1/4)(\omega_0/(2\pi))$ . It can be shown that based on the configuration of the image-reject downconverters, which is determined by the connection of the switches indicated in the figure, the architecture can provide effective LOs of  $f_{LO,eff} = \{\omega_0 \pm \omega_0/2 \pm \omega_0/4\}/(2\pi)$ . This allows for the bifurcation and selection of sub-bands as shown in the inset of Fig. 4. Since the effective LO can be modified by simply

changing the setting of the interstage switches, rapid band-switching is feasible.



**Figure 4: Cascade of Image Reject Downconverters with Spectrum Bifurcation**

Parameter	Specification
Noise Figure	17 dB
IIP3 with 2 in-band interferers at -50 dB total SIR	2 dBm
IIP2 with 2 in-band interferers at -50 dB total SIR	40 dBm
Required Harmonic Rejection	60 dB
Required Image Rejection	60 dB
Phase Noise Floor of RF Synthesizer	-145 dBm/Hz

**Table 1: Specifications for the baseband 500 MHz concurrent channelizer**

The principle employed in this single path is extended in the IDC of Fig. 3 to divide the incident spectrum into  $2^N$  sub-bands. A major advantage of the IDC over mixer-bank based frequency domain channelizers (Fig. 2) is that the IDC generates all required frequencies from a single master LO, since all LO frequencies used in the cascaded image-reject downconverters are derived from divide-by-2 operations. This greatly simplifies the LO generation task. Additionally the IDC can provide all sub-bands simultaneously at baseband.

The mixers in this architecture must be able to reject harmonics of the LO and provide sufficient image rejection. A challenge in this approach arises from the use of multiple cascaded stages. Cascading downconversion stages can place significant noise and linearity requirements on the individual downconverters. Techniques for enhancing harmonic and image rejection in downconverters, and implementing channelization in a reduced number of stages are described below.

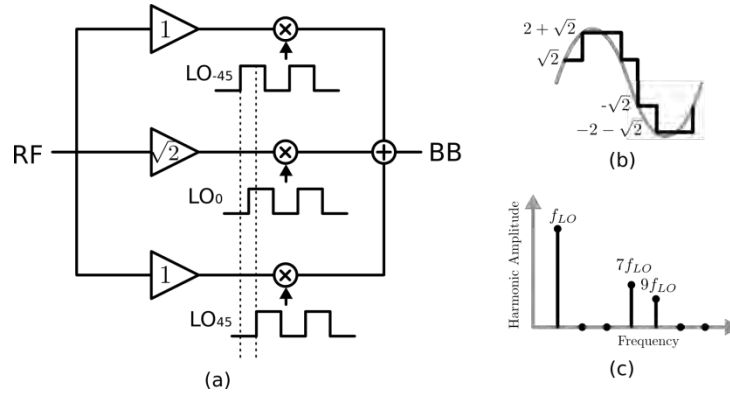
### 3.2 System specifications

Based on system specifications for the complete design, the minimum signal assumed at the input of the baseband channelizer was -75 dBm, with a signal-to-(noise+distortion) of 9 dB. The ratio of signal strength in the largest sub-band was assumed to be 50 dB larger than that in the smallest sub-band. The source resistance at the input of this section was assumed to be 50Ω. The input was assumed to be bandlimited to a 500 MHz RF bandwidth. The output signal-to-(noise+distortion) in any 15.625 MHz band was assumed to be 3 dB. This signal-to-(noise+distortion) metric is

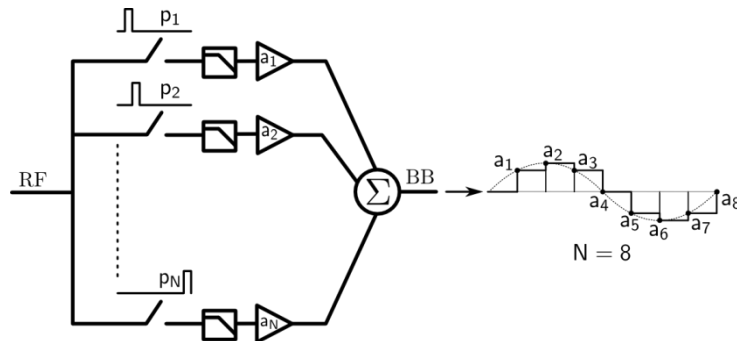
sufficient for several signal detection and identification tasks. Detailed channelizer metrics based on these assumptions are shown in Tab. 1.

## 4 Harmonic Rejection Mixer Topologies

As noted in the above sections the mixers used in the channelizers must provide adequate harmonic rejection. If a sub-band at  $f_{LO}$  is to be downconverted to baseband, it is critical that sub-bands located at  $k f_{LO}$  be rejected by the necessary amount. Based the specifications shown in Tab. 1, a harmonic rejection level of over 60 dB was required in the channelizer.



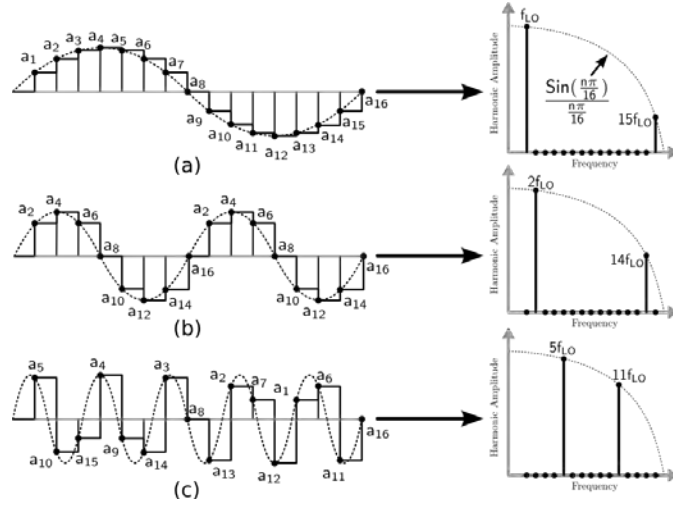
**Figure 5: (a) 50% duty cycle HRM, (b) the generated equivalent LO, and (c) the equivalent LO spectrum**



**Figure 6: HRM using  $1/N$  duty cycle clocks and baseband gain coefficients**

Harmonic rejection mixers (HRM) are commonly employed to limit spurious mixing in broadband receivers. The HRM as first proposed in [A6] consisted of three mixing paths in parallel with applied gain ratios of  $1 : \sqrt{2} : 1$ . The paths employed clocks with 50% duty cycle and fundamental frequency of  $f_{LO}$  that had relative phases of  $-45^\circ : 0^\circ : 45^\circ$  (Fig. 5). An equivalent LO which only contains the  $8m \pm 1$  harmonics of  $f_{LO}$ , where  $m$  is any integer, was derived from the summation of the three mixing paths. It is also possible to apply gains at baseband in an HRM, as shown in Fig. 6. Here phase-shifted clocks with duty cycle of  $1/N$  are used to apply the input to a set of gain coefficients  $[a_1 : a_N]$ . These coefficients are scaled samples of a sinusoid of frequency  $f_{LO}$  that is sampled  $N$  times per period, with time intervals  $1/(N f_{LO})$ , and sample clock of frequency  $N f_{LO}$ . The coefficients are given by

$$a_k = G \sin \left\{ \frac{2\pi k}{N} \right\} \quad (1)$$



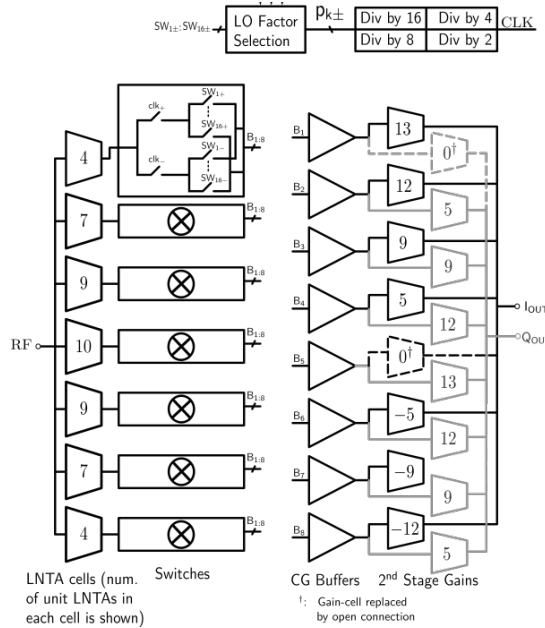
**Figure 7: Generation of (a)  $f_{LO}$ , (b)  $2f_{LO}$ , and (c)  $5f_{LO}$  by reordering HRM gain coefficients in time and the resulting LO spectrum**

where  $k \in [1 : N]$  and  $G$  is the largest scaling coefficient. In practice, the gain coefficients may be quantized versions of those in (1). By applying gains  $a_k$  to the input in a specific time-sequence, an effective downconversion frequency of  $f_{LO}$  is synthesized.

#### 4.1 Frequency-synthesis in HRMs

If the sampled sinusoid of (1) has a frequency of  $f_{LO}$ , consider the samples of a sinusoid with a frequency  $nf_{LO}$ , where  $n$  is an integer, when sampled by the same clock at frequency  $Nf_{LO}$ . It is easily shown that the set of gain coefficients  $[a_k^n]$  that result from sampling the sinusoid of frequency  $nf_{LO}$  are fully represented in the set  $[a_k]$  derived from the sampled sinusoid of frequency  $f_{LO}$ . For odd values of  $n$ ,  $[a_k^n]$  is a permutation of  $[a_k]$ . The difference in  $[a_k^n]$  compared to  $[a_k]$  is simply in the sequence of the coefficients. For even values of  $n$ ,  $a_k^n$  is a subset of  $[a_k]$ . Based on this observation, a single  $N$ -phase HRM can be used to synthesize all equivalent LO frequencies  $nf_{LO}$ ,

where  $n \in [1 : N/2]$ , if the gain coefficients already available within the HRM are appropriately reordered in time [A7]. Through an appropriate design, the modification of the LO frequency can have limited impact on conversion gain and HR. Fig. 7 shows the generation of  $f_{LO}$ ,  $2f_{LO}$ , and  $5f_{LO}$  by coefficient-reordering in time in a 16-phase HRM. It can be observed that  $f_{LO}$  and  $5f_{LO}$  utilize the same gain coefficients, while  $2f_{LO}$  employs a subset of those coefficients. The method allows for the generation of multiple downconversion frequencies for a fixed primary clock frequency at  $Nf_{LO}$  [A8]. As such a bank of HRMs can be configured to downconvert different parts of the input spectrum to baseband. This approach is utilized in the channelizer presented in Sec. 5.2.



**Figure 8: Block diagram of the frequency programmable 16-phase HRM (shown single-ended)**

## 4.2 Two-stage HRM with mitigation of gain and phase errors

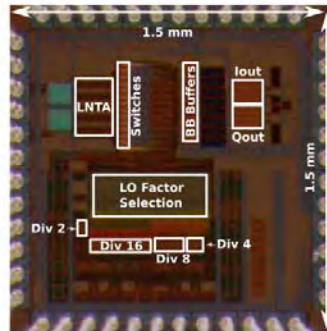
First-order HRMs of the form of Fig. 5 and Fig. 6 show sensitivity to gain and phase errors. Specifically, if the gains deviate from the ideal values shown in (1), then the harmonic rejection degrades linearly with the relative error in the gain coefficients. For example, if the desired gain ratios are of the form  $1:\sqrt{2}:1$  and the realized ratios are of the form  $1:\sqrt{2} + \delta:1$ , then the harmonics which should ideally be rejected, such as the third and the fifth harmonics in an 8-phase HRM, will show residual levels that are  $O(\delta)$ . Such gain errors can arise from two sources. The first error source is systematic. The gain ratios that result from (1) are irrational. It is not possible to implement such ratios in an IC, where gain ratios are typically implemented using device sizing. As such, an irrational gain ratio is typically approximated by an integer ratio. Thus  $1:\sqrt{2}:1$  or  $1:1.414 \dots:1$  may be implemented by devices with ratios such as  $5:7:5$  or  $2:3:2$ . The second source of error is random and arises from variations in the devices used to implement this approximate gain ratio, where, in practice, instead of an integer ratio such as  $5:7:5$ , one may realize a ratio  $5 + \delta_1:7 + \delta_2:5 + \delta_3$ . Another source of error arises from timing errors in the control signals that steer the input from one gain coefficient to the next, e.g.,  $p_1 - p_N$  in Fig. 6. A relative timing error of  $\Delta$  leads to a non-ideal harmonic response that is  $O(\Delta)$ .

A two-stage 16-phase HRM (Fig. 8) that was insensitive to both gain and phase errors was demonstrated in [A8]. The design used a cascade of two first-order HRMs, to provide second-order harmonic rejection capability [A9]. In such a design, if the first order has gain error of the order of  $\delta$  and the second-stage has gain error of the order of  $\gamma$ , then the net harmonic rejection error is  $O(\delta\gamma)$ . Typical CMOS processes can exhibit inherent gain errors that result in 30-40 dB of harmonic suppression without calibration. Thus a two-stage HRM can provide harmonic rejection of the order of 60 dB or better, without calibration, in the absence of timing errors. In addition to ensuring gain insensitivity, by employing retiming [A10, A11] in the gain steering clocks, the design was also made insensitive to timing errors. As was described in [A8], using

retiming in the two-stage HRM, also made the design insensitive to errors caused by delays in the master clock across the chip. If the relative timing error in master clock is of the order of  $\Delta$  and the gain error in the second HRM stage is  $\gamma$ , then the net non-ideal harmonic rejection resulting from timing error is  $O(\gamma\Delta)$ , which is significantly smaller than the  $O(\Delta)$  harmonic rejection that would be observed in a first-order HRM.

To verify the LO factor selection and harmonic rejection performance, a 16-phase frequency programmable HRM was implemented in a 130 nm CMOS process (Fig. 9). Ten IC samples were measured with  $f_{LO}$  of 50 MHz and 104 MHz to determine the HR ratio defined above, over process variation (Fig. 10a). No tuning or calibration was employed in the measurements and no low pass filter was used to enhance the HR performance. Worst-case HR for LO factors 1:6 is greater than 61 dB, while rejection for LO factor 7 exceeds 54 dB at  $f_{LO}=104$  MHz. At  $f_{LO}=50$  MHz, all LO factors except 5 show better HR. Results include both even and odd-order harmonic rejection, where even-order harmonics are seen to limit performance for LO factors 4:7 (Tab. 2). Fig. 10b shows the rejection of the 3<sup>rd</sup>, 5<sup>th</sup>, and 7<sup>th</sup> harmonics in mode  $f_{LO}$  at 104 MHz, with rejection in excess of 72 dB, 71 dB, and 67 dB respectively over all ten samples.

To verify the theory of LO factor selection, DSB NF and gain were measured at  $nf_{LO}=50$  MHz. The measured gain varied in the range from 8.8-11.9 dB. DSB NF ranges from 11.2-14.1 dB (Fig. 11). Fig. 11 shows measured and theoretically predicted noise figure. A two-tone test was used to measure the in-band IIP2 and IIP3. Tones were injected at 79 MHz and 80 MHz with an effective LO of  $nf_{LO}=75$  MHz for both tests, where the IM2 component was located at 1 MHz and the IM3 component at 3 MHz at BB. IIP2 was greater than 54 dBm over all ten IC samples in mode  $f_{LO}$ . IIP3 is shown in Fig. 12 for each LO factor and was in excess of +5.4 dBm for all LO factors.



**Figure 9: Die photo of the frequency programmable 16-phase HRM in 130 nm CMOS [A8].**

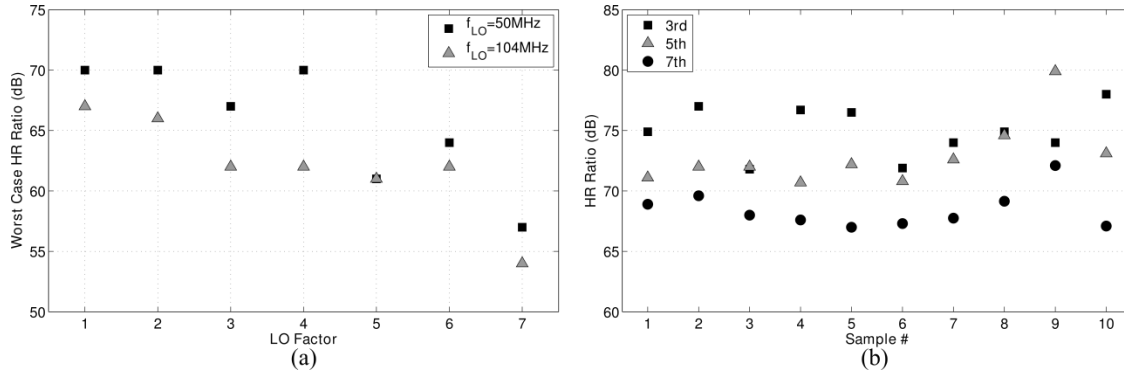


Figure 10: Harmonic rejection (HR) ratio (a) for each LO factor, and (b) HR3, HR5, and HR7 for each IC sample in mode  $f_{LO}$  at 104 MHz [A8]

LO Factor (n)	1	2	3	4	5	6	7
$n f_{LO}$ (MHz)	104	208	312	416	520	624	728
HR Ratio (dB)	67	66	62	62	61	62	54
Worst Harmonic ( $x f_{LO}$ )	7	6	5	8	6	4	8

Table 2: Harmonic Rejection (HR) ratio with  $f_{LO}=104$  MHz [A8]

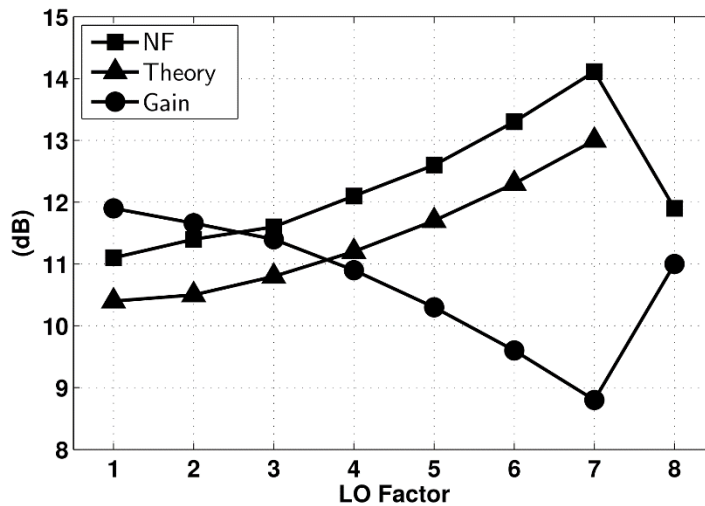


Figure 11: Noise figure and gain at  $n f_{LO}=50$  MHz [A8]

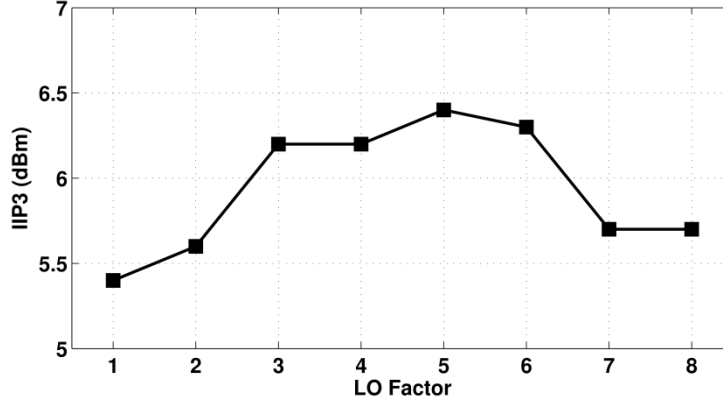


Figure 12: IIP3 versus LO factor at  $n f_{LO}=75\text{MHz}$  [A8]

### 4.3 Low-power bias-shared HRM

As described above, two-stage harmonic rejection mixers with retiming can provide excellent harmonic rejection performance [A8]. These HRMs use two single-stage HRMs, implemented using RF and baseband gain-coefficients, where each stage requires its own bias current. In this work, a new HRM topology was investigated where power saving was achieved by sharing the bias-current between the RF and baseband harmonic rejection stages [A12].

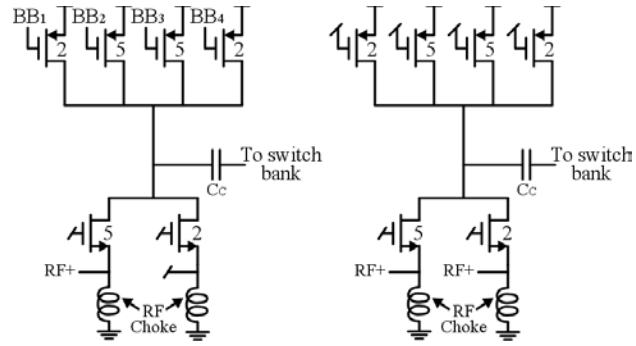
#### 4.3.1 Architecture

The basic building block of the bias-shared two-stage HRM design is a transconductance cell ( $G_m$ -cell) that is composed of fully-differential NMOS and PMOS transconductors (half-circuit is shown in Fig. 13a). Within each cell, NMOS transconductors convert RF voltage to current. The RF current is downconverted to baseband using passive switches. First-stage of harmonic rejection is achieved by combining phase-shifted currents from NMOS devices in three such cells as described below. This operation provides multiple phase-shifted baseband voltages. These voltage signals are then re-applied to the PMOS transconductors (Fig. 13b), that provide a second stage of harmonic rejection.

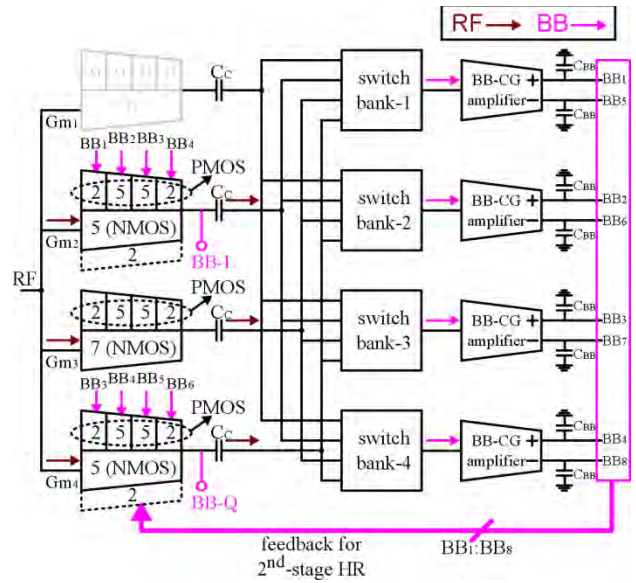
In a two-stage design without bias-sharing, e.g., [A8], the PMOS devices would be used simply to bias the NMOS transconductors. This design, on the other hand, is configured such that the PMOS stages appear as load current sources to the NMOS RF devices, and the NMOS RF devices appear as load stages to the PMOS baseband devices. This bias-current sharing is achieved without the requirement for increased voltage supply, and thus does not degrade dynamic range.

The outputs of the RF transconductors are capacitively coupled to the switch banks. These down-convert the RF transconductor currents to baseband, where they are connected to low-impedance source nodes of baseband common-gate (BB-CG) amplifiers (Fig. 13c). A 1<sup>st</sup> stage of harmonic suppression is achieved at nodes  $BB_1$  through  $BB_8$ . By phase-shifting the downconversion clocks, e.g., [A8], the relative phase shift between  $BB_1, BB_2 \dots BB_8$  is  $45^\circ$ .

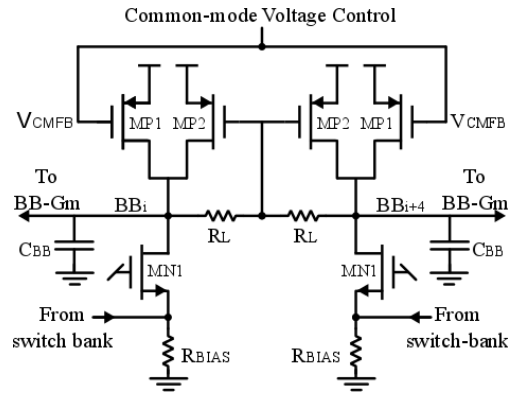
The outputs of the BB-CG amplifiers  $BB_1$  through  $BB_8$  are then applied to the baseband PMOS transconductors, which are configured as CS stages with gain ratios of  $2 : 5 : 5 : 2$ . These stages



(a)



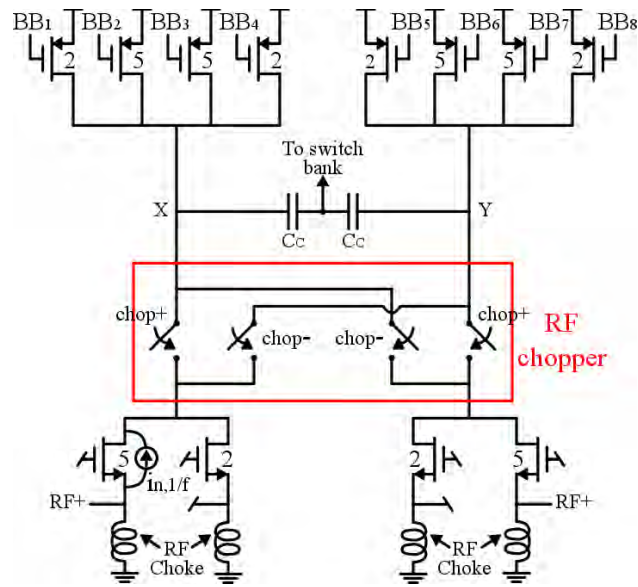
(b)



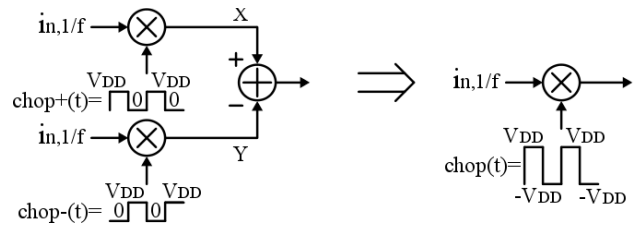
(c)

**Figure 13: (a) RF input cells with normalized Gm of 5 (left) and 7 (right) (b) Conceptual block diagram of the proposed bias-shared HRM (c) The BB-CG amplifier with common-mode voltage control**



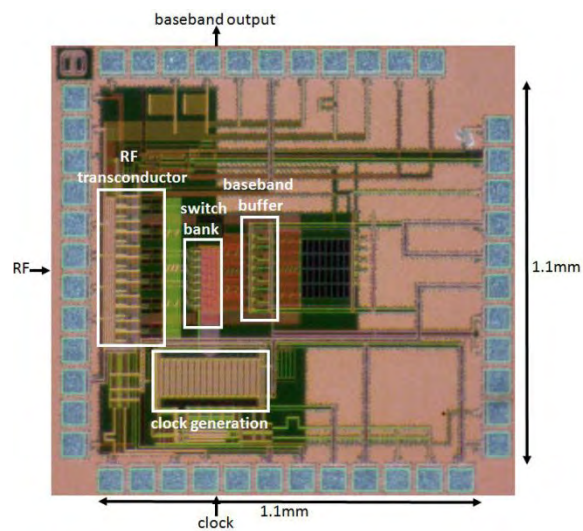


(a)



(b)

**Figure 15: (a) The proposed Gm-cell employing phase domain orthogonality and chopping (b) Effect of RF chopper on the flicker noise**



**Figure 16: Chip photo**

term  $i_{n,1/f}$ . This noise current is coupled to nodes X and Y as follows:

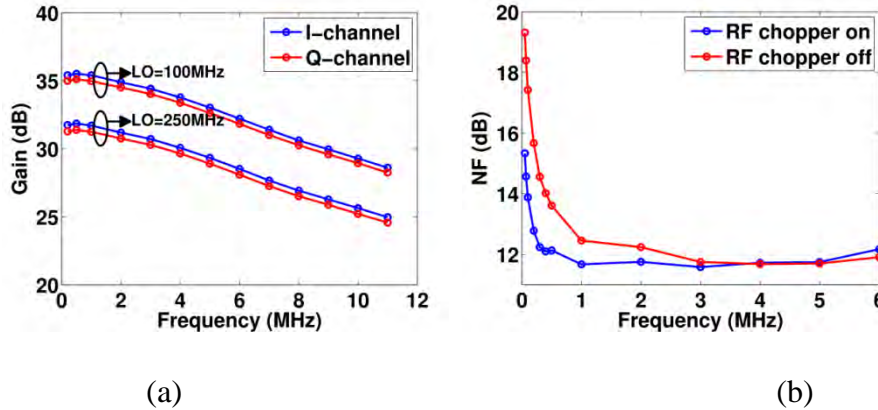
$$i_{n,1/f}^X = i_{n,1/f} \times chop^+(t) \quad (2)$$

$$i_{n,1/f}^Y = i_{n,1/f} \times chop^-(t) \quad (3)$$

Since the final baseband outputs is observed differentially across nodes X and Y,  $i_{n,1/f}$  is equivalently multiplied by  $chop(t) = chop^+(t) - chop^-(t)$  (Fig.15b). The RF chopper thus frequency translates  $i_{n,1/f}$  to the chopping frequency  $f_{chop}$  and its odd harmonics, since  $chop(t)$  does not contain any even harmonics. As a result, the flicker noise  $i_{n,1/f}$  will not appear at baseband. Through proper choice of  $f_{chop}$ , it can also be isolated from the RF signal. The chopper devices introduce small additional parasitic capacitance, however the RF current flows into a low-impedance node of the BB-CG stage and hence the extra parasitic does not have a significant impact on RF frequency response.

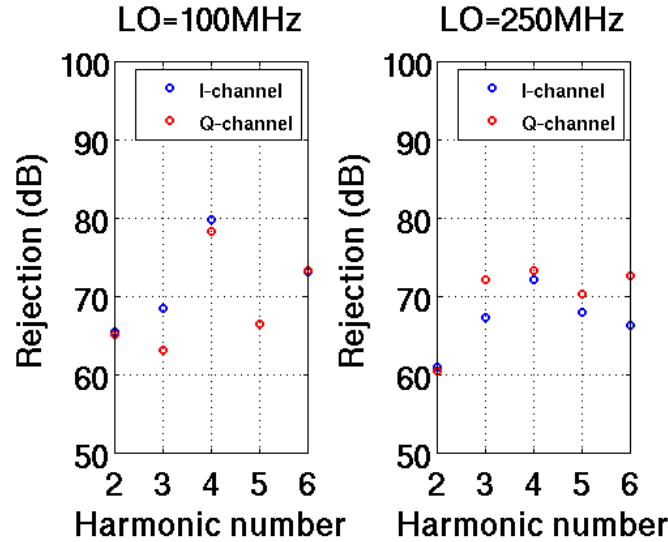
**Measurements** The bias-sharing HRM is implemented in a 130nm CMOS process. The master clock is derived from an externally applied sinusoidal signal, and has a frequency  $f_{CLK} = 8f_{LO}$ . An off-chip balun converts this to differential clocks and an on-chip clock buffer is used to generate 50% duty-cycle square waves, which are then used as the clocks for switching banks. The RF chopper also uses a chopping frequency of  $f_{chop} = 8f_{LO}$ .

The active chip area was approximately  $500 \times 700 \mu m^2$  (Fig. 16). The design was measured in a TQFP package on a PCB. The chip provided baseband differential I-Q outputs, which were converted to a single-ended output using an external differential-to-single-ended unity gain buffer. A conversion gain of 35.8 dB at  $f_{LO}$  of 100 MHz is measured with approximately  $\pm 0.5$  dB mismatch between the I and Q sides. For an  $f_{LO}$  of 250 MHz, the gain is approximately 32 dB (Fig. 17a). This gain decrease is because of a switched-capacitor ( $\propto 1/f_s C_{par}$ ) resistor that appears due to chopping across the loads of the PMOS devices. The noise figure was approximately 11.5 dB (Fig. 17b), and the flicker noise corner frequency with RF choppers enabled was observed to be nearly 82 kHz. Turning off the RF chopper yielded a flicker noise corner of 240 kHz. The  $S_{11}$  is measured to be better than -10dB up to 800MHz.



**Figure 17: (a) Measured conversion gain for  $f_{LO}=100\text{MHz}$  and  $f_{LO}=250\text{MHz}$  (b) Measured NF with and without RF chopper**

HRR was measured over 8 parts, and found to be consistently better than 60 dB, for harmonics  $2 f_{LO}$  to  $6 f_{LO}$ . A sample measurement is shown in Fig. 18. This performance is achieved without any calibration, and shows low sensitivity to the biasing state of the HRM. Out-of-band IIP3 was -3 dBm, and can be further improved by using capacitive loading at the BB-CG source nodes to provide additional filtering. This capacitor was not included in the design. By including this, an OOB-IIP3 enhancement of 12 dB, from -4 dBm to 8 dBm, was observed in simulation.



**Figure 18: A sample measurement of HRR for LO=100 MHz and LO=250 MHz**

The power dissipation in the RF stage was 11.7 mW, and 2.7 mW in the baseband CG stages. The power in the clock generator was 9.7 mW for  $f_{CLK}$  of 800 MHz. The RF chopper consumes around 6 mW and can be reduced by using a smaller driving buffer. Clock and RF chopper power are seen to scale linearly with  $f_{CLK}$ . Use of a faster technology, such as 65 nm CMOS, is expected to significantly reduce power dissipation, especially in the clock generator and the RF chopper. A comparison to other recently published HR-based receivers and mixers in similar technology nodes is shown in Table 3.

**Table 3: Performance comparison**

	This work	[A11]	[A16]	[A17]
$f_{LO}$ (MHz)	<b>100-250</b>	100-300	50-350	48-1000
Gain (dB)	<b>35.8-32</b>	19	3	15
DSB NF (dB)	<b>11.5</b>	11	13.5	12
OIP3 (dBV)	<b>22.8<sup>†</sup></b>	21	6	23
HRR3 (dB)	<b>&gt;61</b>	52	52	>60
HRR5 (dB)	<b>&gt;62</b>	54	-	>60
Power (mW)	<b>14.4(A) 15.7(D)</b>	91.8(A) 9.6(D)	34.8	93
Supply A/D (V)	<b>1.2/1.2</b>	2.7/1.3	1.2	1.5
Technology	<b>130nm</b>	110nm	130nm	130nm

<sup>†</sup>: Without load capacitor at CG input

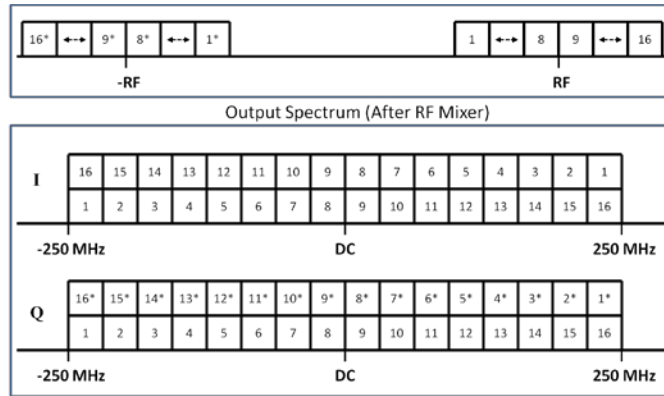
## 5 Research on Channelizer Topologies

### 5.1 Iterative Downconverter with reduced complexity

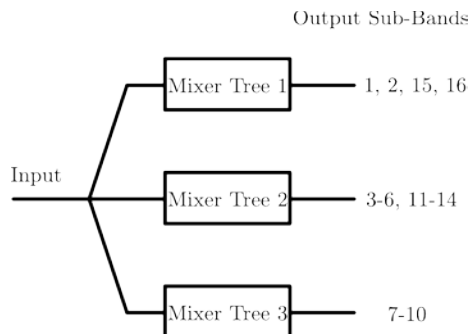
The IDC design of Fig. 3 employs a regular mixer tree that requires  $N$  downconversion stages to divide the input into  $2^N$  sub-bands. During the first reporting period, we showed the use of multiple mixer tree structures in parallel, instead of a single cascaded tree that allowed for reduced complexity. Compared to the full tree of Fig. 3, this approach allowed for fewer mixers compared to the original design, and was thus beneficial for reducing power dissipation.

This approach reduces the number of mixers by recognizing redundancies in the LO generation along any path of the tree. For example, consider a path along a tree that synthesizes an effective LO of  $f_{LO} - f_{LO}/2 - f_{LO}/4$ . In the full tree this needs a cascade of three mixing stages. However, this specific branch can be seen to use an effective LO of simply  $f_{LO}/4$ , which is already available. As such, the sub-band that is derived using these three mixers in cascade, can be also derived from using a single mixer, with an LO of  $f_{LO}/4$ .

The above reasoning was employed in the architecture of a 16 sub-band IDC. Assume that the input spectrum of the IDC is shown in Fig. 19. Each sub-band at baseband is  $250/16$  or 15.625 MHz wide. An RF IQ mixer is assumed to downconvert the incident spectrum to baseband.

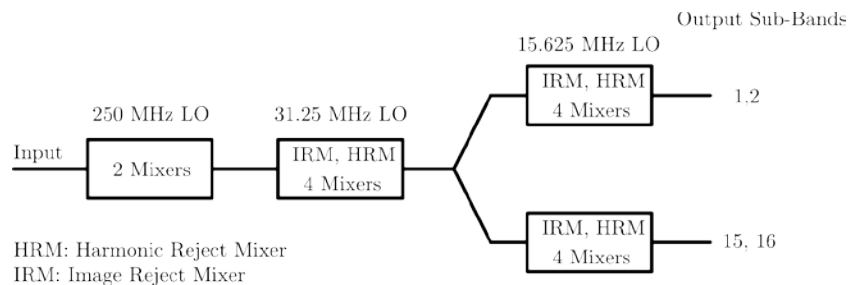


**Figure 19: IDC with 16 sub-bands**

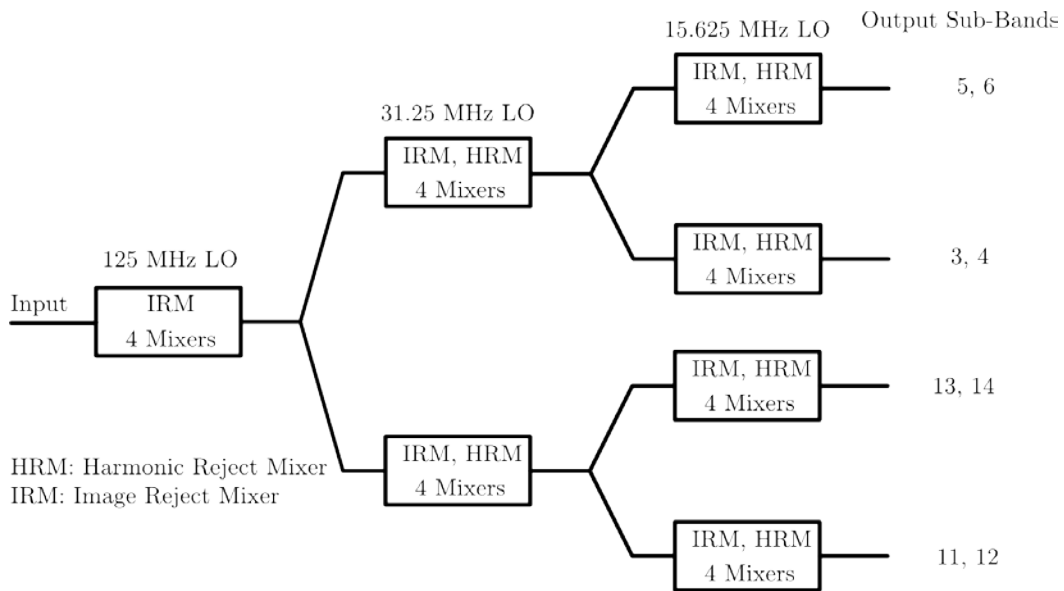


**Figure 20: Reduced order IDC**

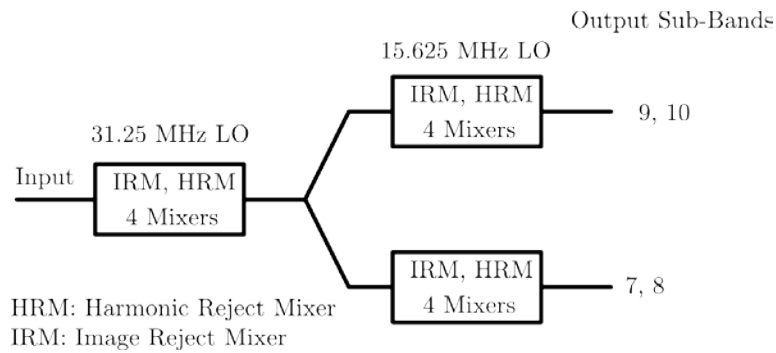
We show one potential reduced-order IDC in Fig. 20. This IDC utilizes three reduced-order downconversion trees instead of one. Each tree is designed to downconvert specific sub-bands that are mentioned in the figure. The architectures for the three trees are shown in Fig. 21, Fig. 22, and Fig. 23. These three mixer trees can be shown to synthesize all necessary frequencies required to downconvert the 16 sub-bands in Fig. 19. The reduced-order tree saves a total of 5 three path HRMs compared to the full tree.



**Figure 21: Mixer Tree 1**



**Figure 22: Mixer Tree 2**



**Figure 23: Mixer Tree 3**

## 5.2 Channelizer based on analog-frequency synthesis capable HRMs

While the above reduced IDC relaxes complexity compared to the IDC of Fig. 3, by using the analog frequency-synthesis capable HRMs of Sec. 4.1, the requirement for cascaded stages can be avoided entirely.

A channelizer based on the above mixer topology has been implemented and measured in a 65nm CMOS process [A18]. The channelizer divides a 500 MHz wide input spectrum at RF into 16 sub-bands. The band which is already at the baseband is not counted and also the actual bandwidth covered is slightly more than 500 MHz as shown in Fig. 24. The input to the channelizer assumes quadrature signal inputs with baseband bandwidths of approximately 250 MHz. Each mixer path employs quadrature mixers. Each pair of quadrature mixers is used to downconvert one specific sub-band and also isolate the sub-band from its image. For generation of all sub-bands, a total of 32 mixers of the form of Sec. 4.1 are implemented in the design.

The channelizer mixer bank consists of 8 I/Q downconverters that are implemented to receive 16 sub-bands (Fig. 24). Each downconversion path requires two pairs of quadrature HRMs, one each for baseband I and Q outputs. Two-stage 16-phase HRMs are used to provide downconversion from  $\pm f_{LO}$ ,  $\pm 3 f_{LO}$ ,  $\pm 5 f_{LO}$  and  $\pm 7 f_{LO}$ , where  $f_{LO} = 31.25$  MHz. Two-stage 8-phase HRMs are used to downconvert  $\pm 2 f_{LO}$  and  $\pm 6 f_{LO}$ . All 16-phase HRMs, and 8-phase HRMs at different LOs, are identical in design, and use appropriate gain sequencing for achieving the desired down-conversion frequency. A 4-phase HRM is used to downconvert  $4 f_{LO}$ . The primary clock in all these mixers is 500 MHz. A 4-phase HRM with a primary clock of 1 GHz is used to downconvert the band at  $8 f_{LO}$ .

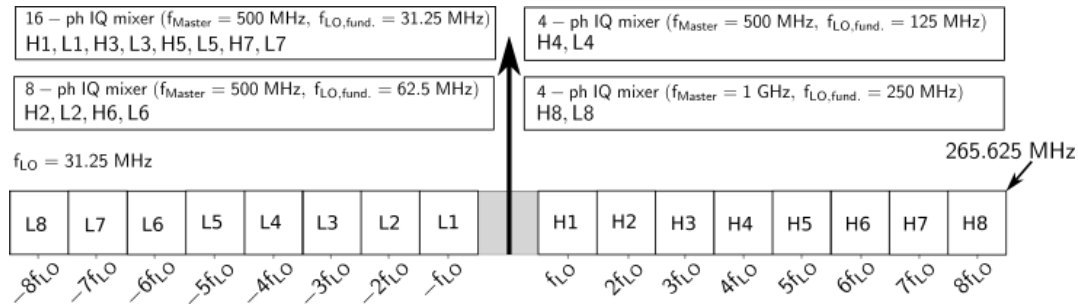


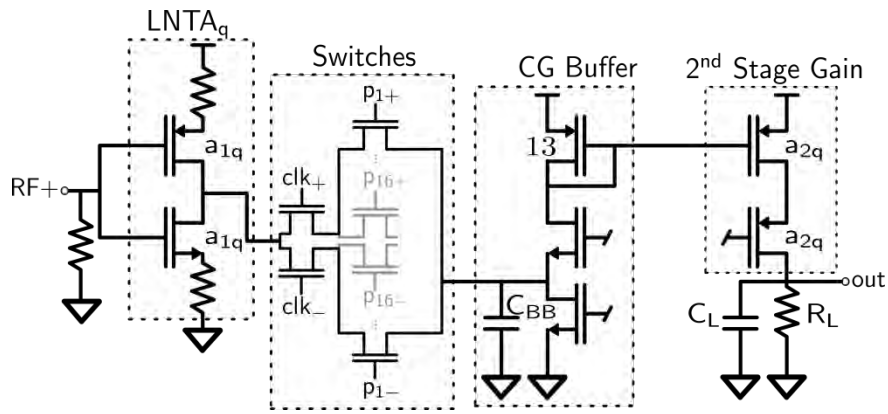
Figure 24: Channelization for 500MHz of RF bandwidth

Each quadrature mixer internally synthesizes local oscillator frequencies, corresponding to the center of the sub-band that is to be downconverted, using the analog frequency synthesis principle described in [A8]. The image reject principle is employed to downconvert upper and lower sidebands employing quadrature input signals. For quadrature inputs  $x_i(t)$  and  $x_q(t)$ , in the  $k^{th}$  sub-band, the quadrature downconverted outputs are given by  $x_i(t)\text{Cos}(k\omega_{LO}t) \pm x_q(t)\text{Sin}(k\omega_{LO}t)$  and  $-x_i(t)\text{Sin}(k\omega_{LO}t) \pm x_q(t)\text{Cos}(k\omega_{LO}t)$ . Image rejection is essential to ensure that the upper and lower sidebands do not interfere after downconversion. Thus if a quadrature mixer is required to provide baseband corresponding to sub-band H1 in Fig. 24, it must adequately suppress L1 and vice-versa.

### 5.2.1 Circuit description

A general circuit diagram for the mixer used for the channelizer is shown in Fig. 25 for one signal path. Inverter-based LNTAs are chosen to provide highly linear voltage-to-current conversion and

improve noise performance. Resistive degeneration is used in the input LNTA cells to enhance linearity performance. A replica bias scheme is used to set the DC bias within the LNTA. The architecture employed in the harmonic rejection mixers is similar to that described in [A8]. However for the task of channelization, three different types of mixers have been implemented, 16-phase, 8-phase and 4-phase. A key difference between these mixers and that described in [A8] is that the digital section in the mixer is programmable in [A8]. Thus a single signal path is employed for downconverting different portions of the input spectrum. However, in the above case at a given time only one specific LO is synthesized. In the current application however, since concurrent outputs are required, multiple HRMs with independent digital sections are designed. Clock generation for the HRMs is provided by D flip-flop rings driven by a master clock operating at frequency  $Nf_{LO}$  for an N phase HRM.



**Figure 25: Circuit diagram for one signal path of HRM with frequency synthesis capability**

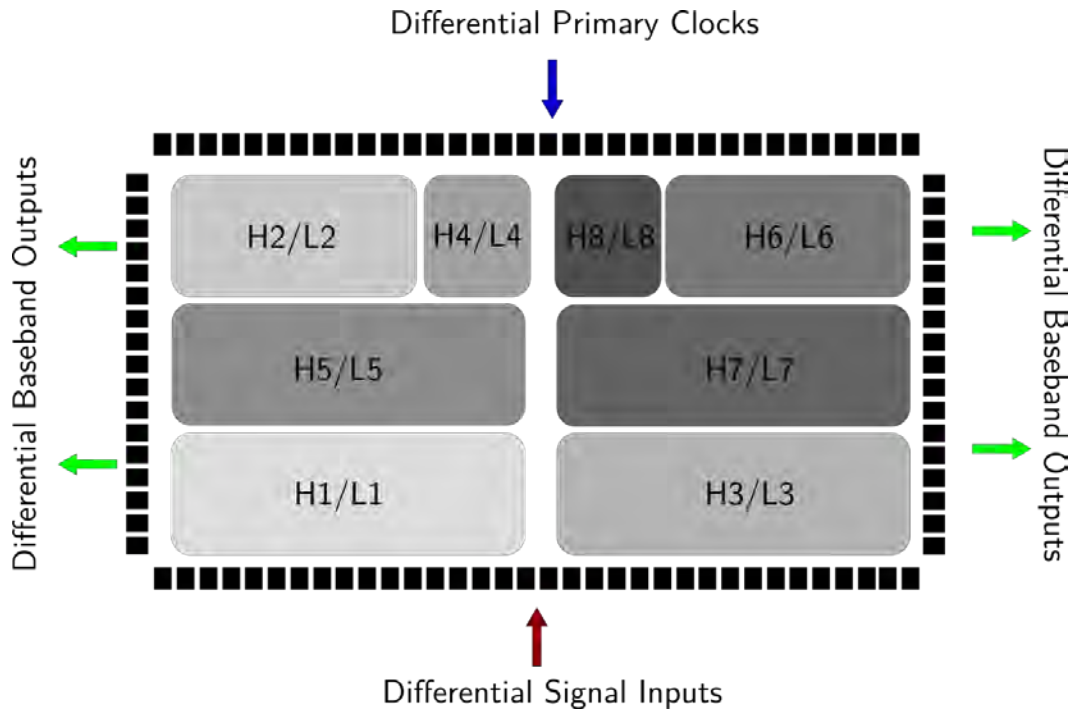
Band	Mixer Phase	First Unrejected Harmonic
H1,L1	16	$15 * f_{LO} = 468.75 \text{MHz}$
H2,L2	8	$7 * (2f_{LO}) = 437.5 \text{MHz}$
H3,L3	16	$13 * f_{LO} = 406.25 \text{MHz}$
H4,L4	4	$3 * (4f_{LO}) = 375 \text{MHz}$
H5,L5	16	$11 * f_{LO} = 343.75 \text{MHz}$
H6,L6	8	$5 * (2f_{LO}) = 312.5 \text{MHz}$
H7,L7	16	$9 * f_{LO} = 281.25 \text{MHz}$
H8,L8	4	$3 * (8f_{LO}) = 750 \text{MHz}$

**Table 4: Description of Bands,  $f_{LO} = 31.25 \text{MHz}$**

The primary frequency used to derive all the other frequencies is 500 MHz and different clock generation circuits are used for different mixers depending on if it is 16, 8 or 4 phase. For the test-chip, the downconversion of the highest band is achieved using a 4-phase mixer as well, except that its LO is at 1 GHz. All the downconverted bands have a baseband bandwidth of 15.625 MHz. The choice of different phase mixers and the first unrejected harmonic are shown in Table 4. A top-level mixer bank floorplan is shown in Fig. 26. The chip area is approximately  $3 \times 2 \text{ mm}^2$ . The die photograph is shown in Fig. 27.

As mentioned above, a two-stage architecture is employed in the mixers. The first stage is

implemented using inverter like LNTAs which convert the input to current and pass it to the switch bank. LNTA based input stage provides adequate overdrive margin and assists with linearity. After

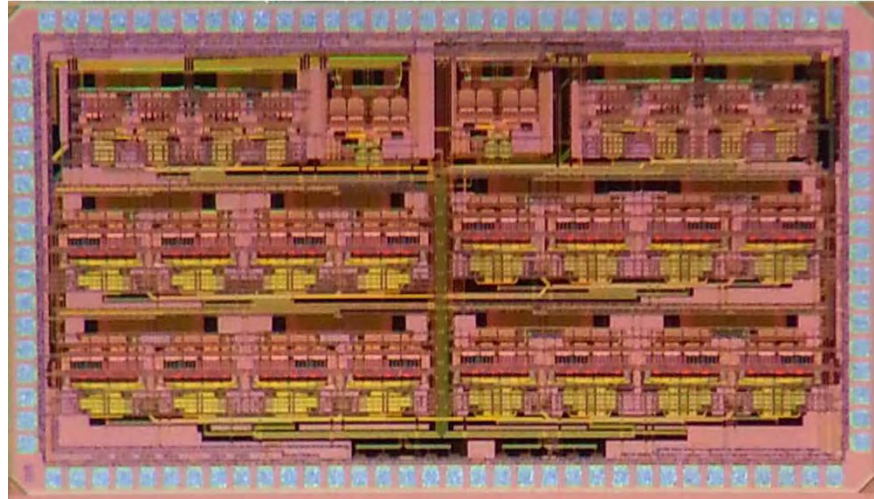


**Figure 26: Layout Floor Plan**

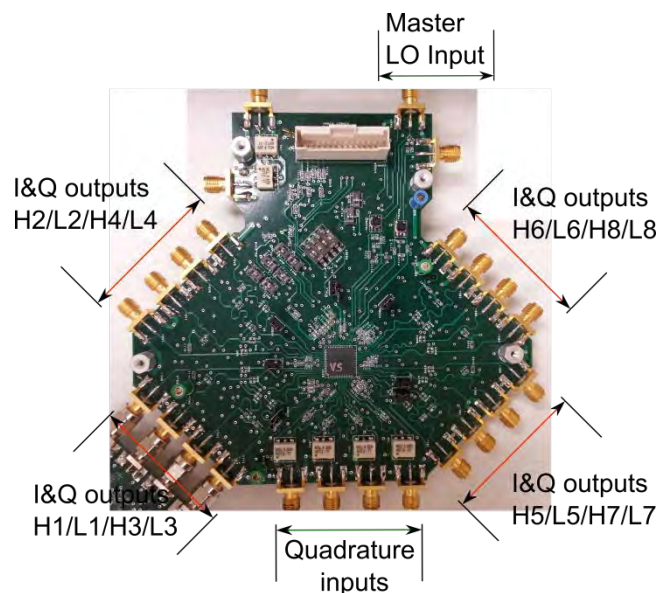
flowing through the switch bank the current is received in a common-gate input buffer. The current is mirrored and ratioed to another branch where it combines with other currents to give a voltage output across a resistive load. A single-path of a mixer is shown in Fig. 25.

### 5.2.2 Results from chip testing

Measurements on the IC based on the above design are described here. The test board is shown in Fig. 28. Each group of baseband outputs on the PCB has four bands multiplexed, with the four outputs in each group correspond to the differential I/Q outputs for one out of the four bands labeled in the Fig. 28 .



**Figure 27: Die photograph of 16-band channelizer**



**Figure 28: PCB designed to test 16-band channelizer**

A quadrature demodulator is used to generate inputs for the tests. The gains of the mixers are 13-17 dB and noise figure of 15-17 dB was achieved with an IIP3 of 3 dBm and P1dB of -10.5 dBm. The performance met the spectrum analysis requirement for which the channelizer was specified. Total power consumption of the chip was measured to be 269 mW. The digital power for the 16-phase image-reject mixer pairs was 9.5 mW each, for 8-phase mixers it was 5.5 mW, while for the 4-phase mixers it was 3 mW. The analog power dissipation was 29.5 mW for the  $\pm f_{LO}$  and  $\pm 3 f_{LO}$  IR mixer pairs (16-phase), 37.5 mW for the  $\pm 5 f_{LO}$  and  $\pm 7 f_{LO}$  IR mixer pairs (16-phase), 26.5 mW for the  $\pm 2 f_{LO}$  and  $\pm 6 f_{LO}$  mixers (8-phase), and 13.5 mW for the  $\pm 4 f_{LO}$  and  $\pm 8$

$f_{LO}$  mixers (4-phase). The power numbers were estimated based on the relative distribution of power across the mixers in simulation, while using the total measured power consumption. The worst case harmonic rejection across all mixers, and harmonics was observed to be in the range from 56.5-62 dB.

### 5.2.3 Techniques for enhancing image rejection in the design

A special design approach has been demonstrated as part of this work to enhance image rejection. This approach is described in [A18]. The effective downconversion frequencies are synthesized within the HRMs by applying the input to a sequence of gain coefficients, as discussed above. In order to provide baseband quadrature outputs, the input is downconverted using two HRMs that apply these gain coefficients with ideally a  $90^\circ$  phase offset.

Two sources of error can lead to quadrature error in this architecture. The first is an uncertainty in the time instants at which the gain coefficients are applied to the two mixers. In a single mixer this source of error leads to a degradation in phase error, while across two mixers this leads to a degradation in image rejection performance.

Error in the master clock timing can be mitigated by retiming the gain-sequencing clock with the master clock. This was demonstrated for enhancing harmonic rejection in [A11] for a single-stage active HRM and in [A8] for a two-stage passive HRM. The same technique is shown to desensitize image rejection performance to clock edge uncertainty.

A second source of degradation in image rejection performance arises from the mismatch in gain coefficients across the two HRMs. Consider downconversion by  $f_{LO}$ . The ideal gain sequence in one mixer should ideally be  $0, 1, \sqrt{2}, 1, 0, -1, -\sqrt{2}, -1$  and in the second mixer it should follow  $1, 0, -1, -\sqrt{2}, -1, 0, 1, \sqrt{2}$ , in order to provide perfect quadrature between the mixers. Assume that due to gain mismatches the gain coefficients are given by  $1 + \alpha_1, \sqrt{2}, 1 + \alpha_2, 0, -(1 + \alpha_1), -\sqrt{2}, -(1 + \alpha_2), 0$  in the I-path mixer, while the coefficients are  $1 + \beta_2, 0, -(1 + \beta_1), -\sqrt{2}, -(1 + \beta_2), 0, (1 + \beta_1), \sqrt{2}$  in the Q-path mixer, where each coefficient is applied for a time duration corresponding to two master clock pulse widths. This non-ideality leads to effective LOs in the two paths that are not in quadrature.

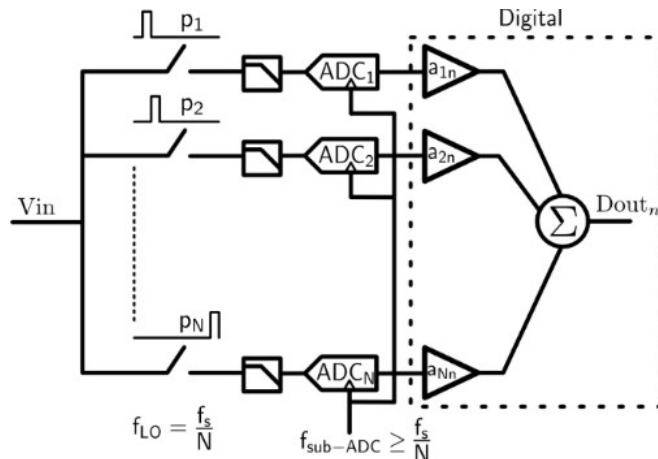
This issue can be solved by changing the sequence in which the gain coefficients are applied in each mixer, as described in [A18]. In the I-path for instance, the modified sequence is given by  $\{1+\alpha_1, 1+\alpha_2\}, \{\sqrt{2}, \sqrt{2}\}, \{1+\alpha_2, 1+\alpha_1\}, \{0, 0\}$  for the positive half cycle and  $\{-1+\alpha_1, 1+\alpha_2\}, \{-\sqrt{2}, \sqrt{2}\}, \{-1+\alpha_2, 1+\alpha_1\}, \{0, 0\}$  for the negative half cycle, where the time step corresponds to a single master clock pulse width. A similar scheme is applied in the Q-path. By using this approach, it can be shown that the phase error between the I and Q paths caused by the non-ideal gain coefficients is nullified.

Residual gain error mismatch between the I and Q paths can be enhanced using calibration. We note that calibration for image-rejection is typically considered a two-dimensional problem involving simultaneous gain and phase calibration. Using the above approach, the task is reduced to a single-dimensional gain calibration alone, which significantly lower complexity.

In the test for image rejection, amplitude calibration is performed at one frequency tone. The simultaneous image rejection achieved in the I and the Q bands is reported. This image rejection measurement is achieved after calibration of the phase mismatch added off-chip from the on-board traces or the quadrature demodulator, which is used to generate the quadrature inputs. Thus the measured image rejection is related to the difference in the phase mismatches in the I and the Q paths. Since both are zero-mean random variables, this can be treated as an upper bound on the phase mismatch in our design and any residual frequency dependent amplitude mismatch, since

Band	IR(dB) in I and Q outputs, chips 1-3	
	$f_{BB} = -14\text{MHz}$	$f_{BB} = 14\text{MHz}$
$\pm 1 * f_{lo}$	57-68	54-62
$\pm 2 * f_{lo}$	65-72	59-65
$\pm 3 * f_{lo}$	53-58	45-48.5
$\pm 4 * f_{lo}$	62-67	66-75
$\pm 5 * f_{lo}$	58-79	57-70
$\pm 6 * f_{lo}$	67-77	63.5-71
$\pm 7 * f_{lo}$	53.5-74	50-55
$\pm 8 * f_{lo}$	62-73	67-74

**Table 5: IR at band edge with calibrated amplitude**



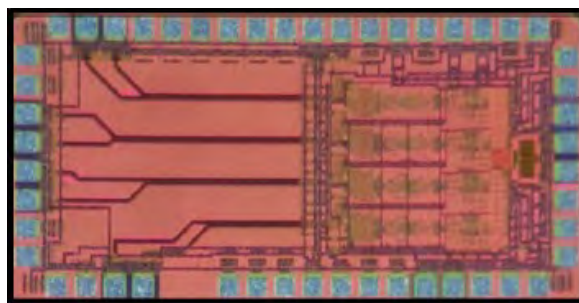
**Figure 29: Frequency-folder channelizing receiver [A19].**

we are performing an external amplitude calibration at a single tone for a mixer. Preliminary measurements from the first tested IC are reported in table 5.

### 5.3 Mixed-signal channelizer

This design operates as a frequency-folded channelizing receiver (Fig. 29). The design uses N-parallel paths with non-overlapping clocks with 1/N duty cycle, with frequency of  $f_{LO}$ . A broadband signal is downconverted to baseband. Signal components at N multiples of  $f_{LO}$  are aliased within the baseband bandwidth. These signals are separated employing harmonic rejection after baseband. This design is in essence a frequency-channelized analog-to-digital converter that offers the advantage of relaxed ADC clock timing when compared to a time-interleaved ADC [A19].

This design has been implemented in a 65nm CMOS process, and measured. The design uses a broadband input from 125MHz - 1GHz, and provides an effective 2 GS/s sampling rate. The analog path is integrated in the chip, which includes the input amplifier, downconversion switches, low-pass filters and baseband amplifiers. The first proof-of-concept channelizes the input into four 125MHz wide channels at baseband. Off-chip ADCs clocking at 500 MHz, that digitize each of the channels are employed. The chip layout is shown in Fig. 30. The design achieves a mean SNDR of 49-dB across the input bandwidth, while providing 38-43.3 dB of gain and a NF of 8.5-13.4 dB. Equalization-based calibration results in harmonic and image rejection greater than 59-dB and 58-dB, respectively, across the input bandwidth, while even better performance may be achieved for tonal interferers. The receiver consumes 104 mW from a dual 1.2/2.5-V supply.



**Figure 30: Layout of frequency-folded channelizer**

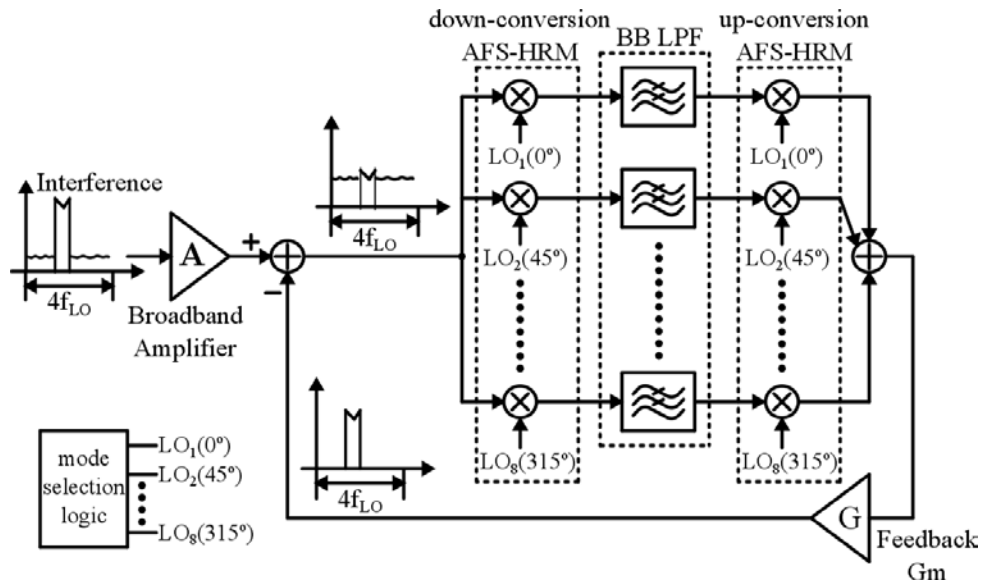
## 6 Research in Channelizer Linearization Techniques

An active interference canceler has been designed in silicon for use in a channelizer application [A20]. In the initial implementation, narrow-band cancellation is employed at the output of the transconductor that is used to drive the channelizer. The design utilizes a frequency-translated feedback loop with harmonic-rejection mixing in the down and up-conversion paths [A21]. The active interference canceler helps to enhance the blocker-limited dynamic range of the channelizer by attenuating a large blocker at its input.

The design includes two key features, both a consequence of using harmonic-rejection mixing in the canceler. The first is that harmonic responses are avoided. The second is that by using the frequency synthesis capability within the HRMs [A8], the frequency range of the synthesizer that is required to span the bandwidth of the input over which cancellation is needed, is significantly reduced compared to using the HRM in its fundamental mode.

### 6.1 Architecture

In the proposed scheme (Fig. 31), the input signal is amplified by a broadband amplifier **A**. An 8-path frequency-translated negative feedback loop is used to cancel the interference at the output of **A**. The interferer is downconverted to baseband within the loop, where it is selected by a baseband low-pass filter. The selected interferer is then up-converted, and subtracted from the output of the amplifier **A** in the current domain. This is equivalent to implementing a notch filter using a band-pass filter formed by  $N$ -path filters of the form introduced in [A22]. Instead of employing sinusoidal LOs and ideal multipliers, analog-frequency synthesis capable HRMs (AFS-HRMs) are used to reduce LO harmonics and provide frequency-synthesis in the down- and up-converters.



**Figure 31: Block diagram of the proposed interference cancellation technique**

Each of the 8 down-conversion and up-conversion LOs are phase shifted with respect to each other by  $45^\circ$ , and are synthesized from a master clock with frequency  $8 f_{LO}$  [A8][A9], for a

fundamental- mode notch response at  $f_{LO}$ . Depending on the location of the interference, mode selection logic is used to configure both the down-conversion and up-conversion AFS-HRM properly (Fig. 32a). With a master clock of  $8 f_{LO}$ , different LO waveforms can be synthesized similar to [A8] (Fig. 32). Synthesized LO waveform corresponding to  $k f_{LO}$  for  $k = 1 - 3$  are obtained by sampling an ideal sine wave of frequency  $k f_{LO}$  by  $8 f_{LO}$ , followed by zero-order hold (Fig. 32b-d). The spectrum of the sample-and-hold LO waveforms contains harmonics only at  $(8N \pm k) f_{LO}$ , where  $N$  is an integer greater than or equal to 0. The strength of the  $(8N \pm k)^{th}$  harmonic for the synthesized  $k f_{LO}$ ,  $a_k^{8N \pm k}$ , can be written as

$$a_k^{8N \pm k} = \text{sinc}\left(N \pm \frac{k}{8}\right) = \frac{\sin\left(\pi\left(N \pm \frac{k}{8}\right)\right)}{\pi\left(N \pm \frac{k}{8}\right)} \quad (4)$$

For example, if  $k = 3$ , then only harmonics around  $3 f_{LO}$  ( $a_3^3$ ),  $5 f_{LO}$  ( $a_3^5$ ),  $11 f_{LO}$  ( $a_3^{11}$ ), ... etc. will appear in the synthesized  $3 f_{LO}$  waveform.

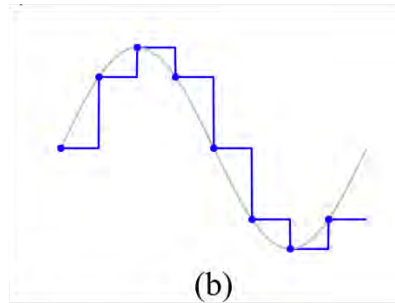
Two key issues need to be considered. The first is the maximum achievable rejection at the frequency band of interest, which is set by the harmonic response of the mixers. The second issue relates to folding of an interferer into adjacent channels owing to harmonic folding. These are discussed in Sec. 6.1.1 and Sec. 6.1.2 respectively.

### 6.1.1 Maximum achievable rejection

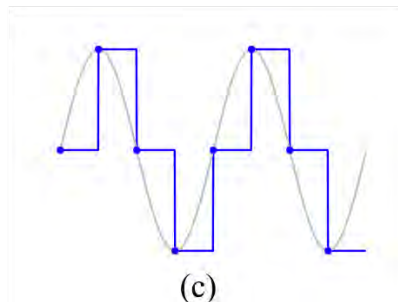
It can be shown that the output signal of the broadband amplifier  $X_o$  is related to its input  $X_i$  in the  $k f_{LO}$  mode through the following equation

Operation Mode	Interference Location	Master Clock
$f_{LO}$	$0 \sim 1.5 f_{LO}$	$0 \sim 12 f_{LO}$
$2 f_{LO}$	$1.5 \sim 2.5 f_{LO}$	$6 \sim 10 f_{LO}$
$3 f_{LO}$	$2.5 \sim 4 f_{LO}$	$6.7 \sim 10.7 f_{LO}$

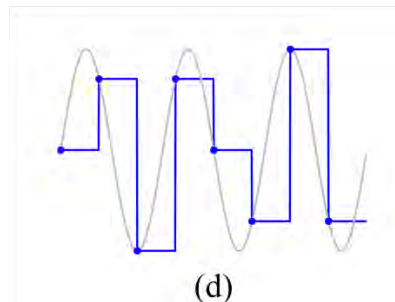
(a)



(b)



(c)



(d)

**Figure 32: (a) The interference location and the corresponding operation mode. Synthesized**

## LO waveforms for (b) $f_{LO}$ mode (c) $2f_{LO}$ mode and (d) $3f_{LO}$ mode

$$X_o(s) = \frac{1 + G \frac{\sum_{\ell \neq k} |a_k^\ell|^2}{|a_k^k|^2} Z(s - j2\pi k f_{LO})}{G \frac{\sum_{\ell} |a_k^\ell|^2}{|a_k^k|^2} Z(s - j2\pi k f_{LO})} X_i(s) \quad (5)$$

where  $Z(f)$  is the transfer function of the baseband low-pass filter, and  $a_k^i$ s are defined above (eq (4)).  $Z(f)$  is assumed to provide significant attenuation at  $f_{LO}$ .

If  $k = 1$ , i.e. the operation is in  $f_{LO}$  mode, the first large harmonic response of the synthesized LO will appear around  $7f_{LO}$ , which is outside the input bandwidth  $4f_{LO}$  (see Fig. 31). In the limiting case, for  $G \rightarrow \infty$ , the maximum rejection for  $f_{LO}$  mode can be written as

$$R_1 = \frac{|a_1^7|^2 + |a_1^9|^2 + \dots}{|a_1^1|^2 + |a_1^7|^2 + |a_1^9|^2 + \dots} \quad (6)$$

$R_1$  is determined by the strength of the synthesized  $f_{LO}$  in relation to its un-rejected harmonic responses at  $7f_{LO}$ ,  $9f_{LO}$ , ... etc. It can be shown that the maximum achievable rejection is around 26 dB.

In the  $3f_{LO}$  mode ( $k = 3$ ), the first large harmonic response appears around  $5f_{LO}$ . The in-band harmonic response is negligible similar to the reason in the  $f_{LO}$  mode. However, since the strength of un-rejected  $5f_{LO}$  harmonic is closer to that of  $3f_{LO}$ , the rejection

$$R_3 = \frac{|a_3^5|^2 + |a_3^{11}|^2 + \dots}{|a_3^3|^2 + |a_3^5|^2 + |a_3^{11}|^2 + \dots} \quad (7)$$

is degraded compared to the  $f_{LO}$  mode. A 2-stage up-conversion scheme proposed in [A21] can be used in this case to improve the rejection.

### 6.1.2 Harmonic folding

For an input frequency  $f_{in}$ , the first folded harmonic can be shown to be at  $f_{in} - 8f_{LO}$ . Thus if the bandwidth is limited to  $4f_{LO}$ , by using 8 paths, the unwanted harmonic folding will ideally all appear outside the input band. In practice, non-ideal matching between the 8 paths will result in non-zero harmonic folding.

## 6.2 Circuit implementation

### 6.2.1 Down-Conversion AFS-HRM

The down-conversion AFS-HRM (Fig. 33) is implemented by transconductors with ratios 5:7:5 to approximate  $1:\sqrt{2}:1$ . A switch bank similar to [A8] is used where a re-timing technique [A11] ensures that the phase shift between the 8 paths is  $45^\circ$ , even in the presence of mismatches between the re-timing switches and gain steering switches. The transconductance cell is implemented using CMOS transconductors. Source degeneration resistors are used to increase the

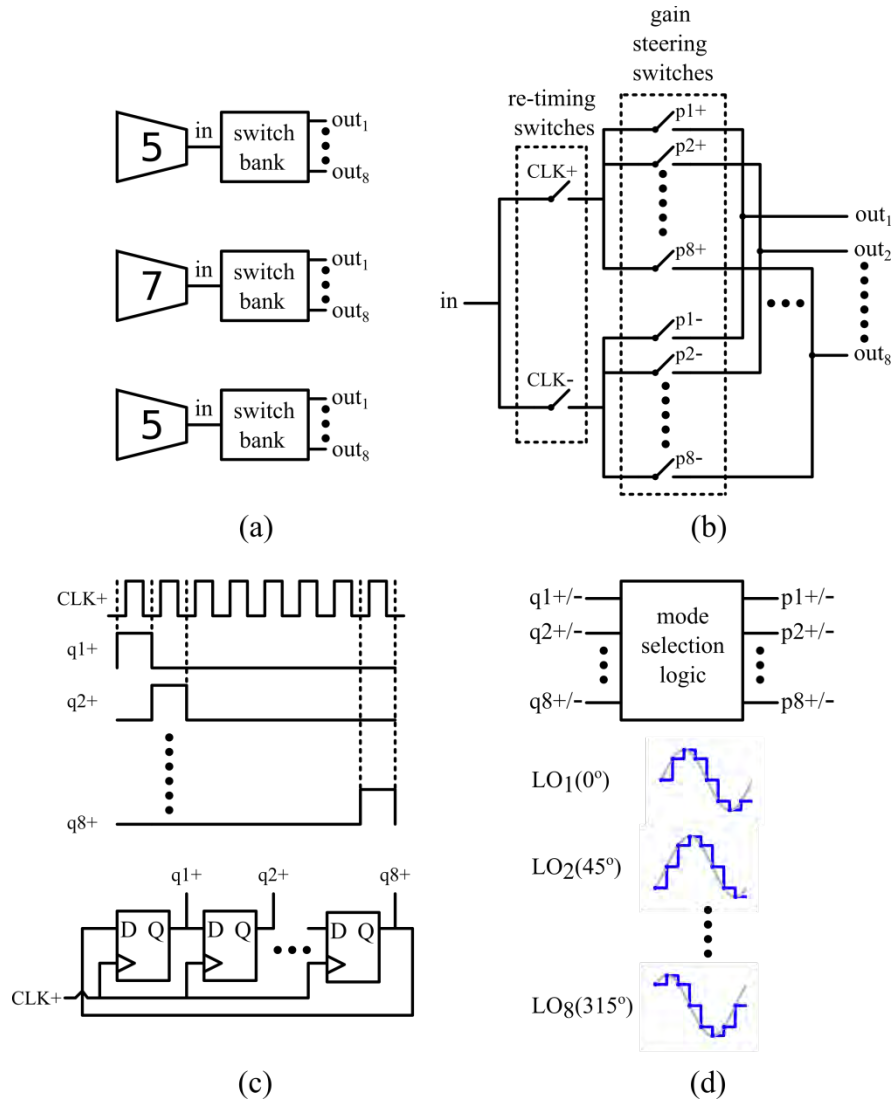
output impedance. The switch banks are implemented using NMOS switches. Gain steering switches are controlled by phase clocks p1+ to p8+, and p1- to p8-, with fundamental frequency  $f_{LO}$  and duty cycle 1/8. The phase clocks are generated from 8 flip-flops connected in a ring (Fig. 33c). Mode selection logic maps the ring flip-flop outputs (qi's) to proper phase clocks pi's, which determines the sequence in which gain coefficients are used, and hence the downconversion frequency. The equivalent synthesized LO waveform for  $k = 1$  along the 8 paths is shown in Fig. 33d. As noted in [A8], the  $3 f_{LO}$  mode can be obtained by re-ordering the gain coefficients accessed in time while the  $2 f_{LO}$  mode is obtained from a 4 flip-flop based ring.

### 6.2.2 Baseband filtering

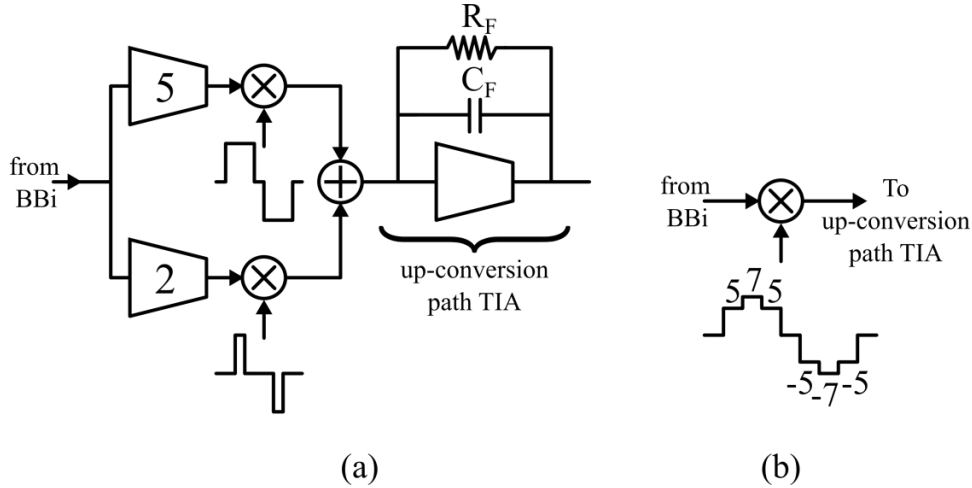
The outputs of the passive switches in the down-conversion AFS-HRMs are connected to low impedance common-gate amplifiers that provide  $I$ - $V$  conversion. The down-converted baseband current is then mirrored at the cascode output [A8], where it is applied to a single-pole RC low-pass filter.

### 6.2.3 Up-conversion AFS-HRM

The up-conversion AFS-HRM (Fig. 31) configured in the  $f_{LO}$  mode is shown in Fig. 34a. The ratio 0:5:7:5 is synthesized as  $5 \times [0 \ 1 \ 1 \ 1] + 2 \times [0 \ 0 \ 1 \ 0]$ . The equivalent synthesized up-conversion LO waveform is shown in Fig. 34b. A switch bank and selection logic similar to the down-conversion AFS-HRM is used to re-configure the up-conversion AFS-HRM to operate in different modes. A low-impedance TIA terminates the outputs of the up-conversion switches. The capacitor  $C_F$  in parallel with the shunt feedback resistance  $R_F$  is used to attenuate the harmonic response beyond the bandwidth  $4f_{LO}$ , which improves the achievable rejection (Eq. 6-7). Both the 5 and 2 cells are implemented as PMOS common-source amplifiers with resistive loads. This helps to mitigate the potential degradation due to up-converted flicker noise arising from non-ideal harmonic rejection.



**Figure 33: (a) Block diagram of the down-conversion AFS-HRM (b) Switch bank consisting of re-timing switches driven by master clocks, and gain-steering switches driven by phase clocks (c) The relative timing between the master clocks and phase clocks. (d) Synthesized LO waveform for  $k = 1$**



**Figure 34: (a) The up-conversion AFS-HRM (b) The equivalent synthesized up-conversion LO waveform**

The transconductance cell used in the up-conversion path TIA is implemented as a CMOS inverter.

#### 6.2.4 Feedback $G_M$ and LNA

The feedback  $G_M$  (Fig. 31) and the wideband input LNA are both implemented as self-biased inverting amplifiers. The ratio between them determines a tradeoff between the NF degradation caused by the loop and the large-signal blocker handling capability. A larger feedback  $G_M$  can handle large blockers, while at the cost of more degradation of NF, and power. A 2:1 ratio between the input LNA and the feedback  $G_M$  is used in this design.

### 6.3 Measurements

The design has been implemented in a 65nm CMOS process. The active chip area is approximately  $1000 \times 880 \mu\text{m}^2$  (Fig. 37). The design was measured in a QFN package on a PCB. An external differential-to-single-ended unity gain buffer was employed to interface the IC to the spectrum analyzer. The die-photograph of the chip is shown in Fig. 37.

The input bandwidth was chosen to be 250 MHz. The notch response of the proposed technique in various modes is shown in Fig. 36. Due to the use of AFS-HRMs in both down-conversion and up-conversion paths, there is no harmonic null response across the input band. The achieved small-signal rejection for  $f_{LO}$  and  $2f_{LO}$  modes is approximately 25 dB, and for  $3f_{LO}$  mode is approximately 15 dB. In-band harmonic folding is measured to be better than -40 dB (Sec. 6.1.2). The total external LO span for rejecting a blocker anywhere between 0-250 MHz is 750 MHz. Without the use of AFS-HRMs, the required span would be 2 GHz.

Linearity is measured with and without the interference cancellation technique (Fig. 35). The desired input signal is located 40 MHz away from the blocker and the notch response is tuned at the blocker frequency. An improvement of the blocker 1dB compression of 8-13 dB is observed. The IIP3 also shows 16 dB ( $f_{LO}$  mode) to 6 dB ( $3f_{LO}$  mode) improvement. The noise figure without

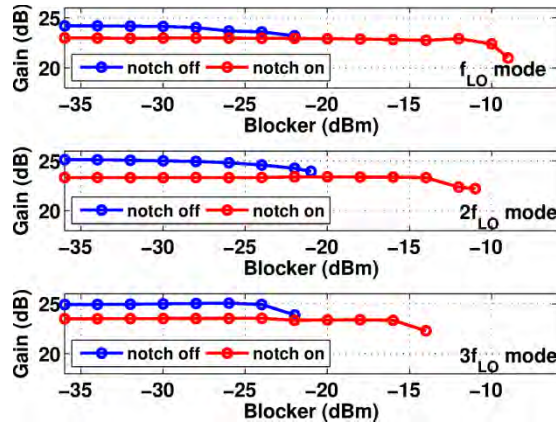


Figure 35: Blocker 1dB compression measurement with and without interference cancellation

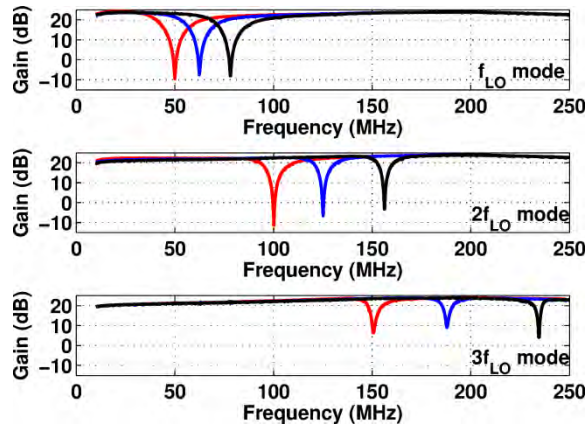


Figure 36: The notch response for various operation modes

and with the interference cancellation is 4.5 dB and 7 dB, respectively. The proposed technique consumes analog power of 33.8 mA, with nearly 60% used in the upconversion  $G_M$ , and digital power of 7.6 mA. The supply voltage is 1.4 V for the baseband section and the up-conversion AFS-HRM, while 1.2 V for all other analog and digital parts.

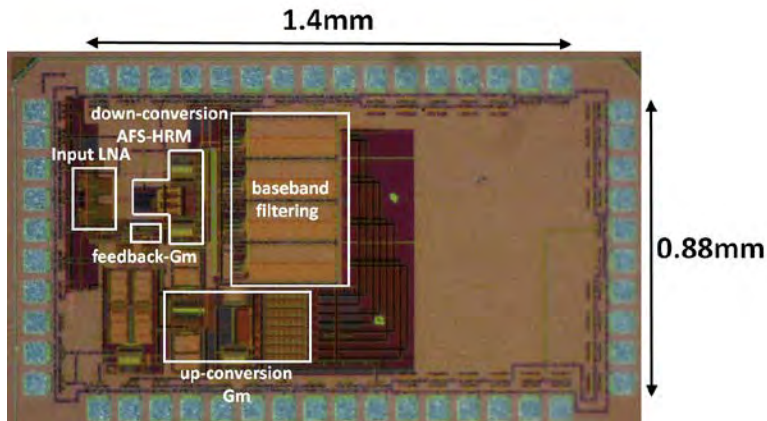


Figure 37: Chip photograph of AFS-HRM based linearization architecture

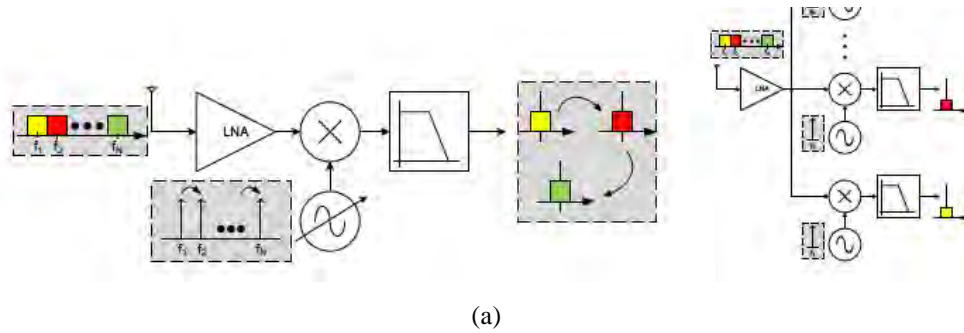
# 7 Single-Chip RF Channelizer Architectures using 3-Way Iterative Downconversion for Concurrent or Fast-Switching Spectrum Analysis

## Summary

*A single-chip, wideband RF channelizer architecture using the concept of 3-Way Iterative Down-Conversion (IDC) has been developed. The RF channelizer implementation splits the input spectrum of 0.6GHz-9GHz into 7 channels each with a 1.2GHz bandwidth. This RF channelizer implementation has the ability of concurrently down-converting 3 channels enabling multi-Gbps data reception. It further demonstrates the ability to rapidly switch from receiving one channel to another. A prototype of the RF channelizer has been fabricated in a 65nm standard CMOS process. A 400Mbps (BPSK) data transmission has been demonstrated by down-converting two channels concurrently. Channel switching can be as fast as 8ns and is always faster than 1 $\mu$ s. The chip occupies an area of 2mm x 1mm and consumes an average power of 435mW while offering a dynamic range between 58dB to 63dB.*

## 7.1 Introduction

Implementing low power, wideband RF spectrum analysis on a single chip is a very challenging problem. When the signal bandwidth covers several GHz, direct time-domain sampling and digitization for digital signal analysis with multiple incident blockers requires a high-speed, high- dynamic-range, and consequently power-hungry, Analog-to-Digital converter (ADC). Frequency channelization can alleviate the energy requirement for spectrum analysis, as it relaxes the sampling rate and dynamic range requirements of the ADCs that follow thanks to the filtering of out- of-band blockers for each channel by the channelizer.



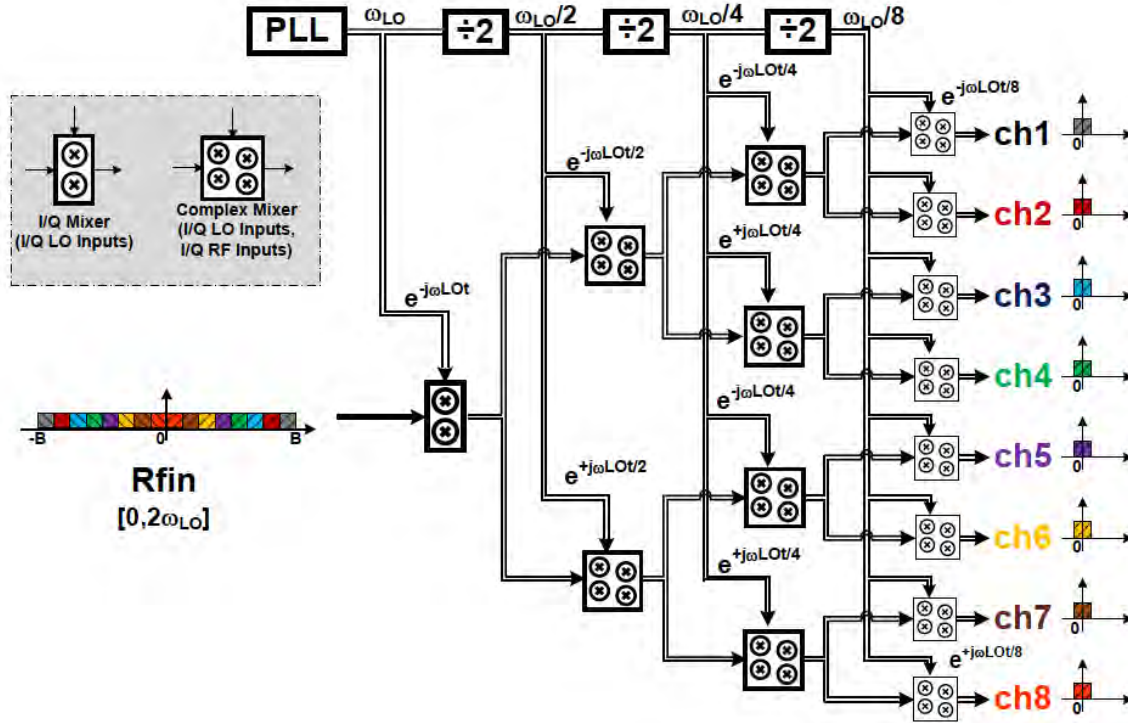
**Figure 38: Conventional approaches to RF channelization. (a) Sequential scanning of the spectrum. (b) Concurrent scanning using multiple parallel receivers.**

Active research is being conducted on broadband signal analysis and frequency channelization. In [B1], an up-downconversion architecture is utilized for DC-6GHz channelization with a fixed intermediate frequency (IF) of 6GHz. The up-downconversion architecture has benefits in terms of harmonic rejection, interference mitigation and local oscillator (LO) tuning range, but can be power hungry due to the larger number of blocks and the need for a higher-frequency LO signal. Furthermore, when switching channels, the LO phase locked loop (PLL) needs to re-settle which leads to slow channel switching so that fast hopping signals cannot be tracked. In [B2], multiple parallel receivers are used, each with their dedicated PLL. The LNA that splits the signal across multiple receivers is loaded with a large capacitance which limits the bandwidth and thus the number of parallel channels. Operating multiple PLLs on the same chip can further be power hungry and often leads to spurious coupling and unwanted spurs.

The concept of a bio-inspired active RF silicon cochlea for channelizing the RF spectrum was introduced in [B3]. The RF cochlea uses multiple stages of low-pass filters with progressively decreasing bandwidths. The higher parts of the incident RF spectrum is observed only on the outputs of earlier filter stages while the lower parts of the RF spectrum is observed until later stages. Further signal processing is needed before the RF Channelization is complete since the output signal of earlier filter stages contain the high frequency signals which need need to be separated from the low frequency signals. In addition the signals still have to be downconverted to baseband.

The iterative down-converter (IDC) concept has been introduced in [B4] and [B5] to overcome the problem of LO synthesis in broadband frequency channelizers. An IDC uses a cascade of image-rejection mixers to achieve LO synthesis from a fixed PLL frequency and its subharmonics. However, this architecture suffers from channel-to-channel signal leakage that is limited by the finite image rejection or harmonic rejection of individual mixers.

In this paper, a 3-way splitting IDC cell is introduced to improve the signal leakage performance. Using this 3-way IDC cell a concurrent channelizer can be realized to analyze multiple channels in parallel or a fast-switching channelizer can be realized that analyzes channels sequentially but with a very short switching time between channels. The circuit design of a 65nm CMOS RF channelizer [B6] using a partially-concurrent IDC architecture is described that concurrently down-converts a subset of the different channels as well as rapidly switches from one non-concurrent channel to another. It decomposes an input spectrum of 0.6GHz-9GHz into 7 channels, each of 1.2GHz bandwidth, and produces 3 concurrent outputs.



**Figure 39: RF channelization using Iterative Down-Conversion by cascading image-rejection mix- ers.**

## 7.2 Prior Work in RF Channelizers

A natural approach to RF channelization is to down-convert the desired channel to baseband using a sweeping LO as shown in Fig. 38. However, this would require a PLL capable of generating wide range<sup>2</sup> of LOs. Moreover, the time it takes the PLL to switch from one LO to the next would limit the spectrum analysis duration. The spectrum analysis time can be reduced by using multiple parallel receivers, each down-converting a separate channel. For N-concurrent outputs, N PLLs are needed. However, housing multiple PLLs on the same chip can pose serious frequency pulling challenges [B7].

The LO generation challenges can be overcome by using an IDC with a cascade of image reject mixers and merged LO synthesis (Fig. 39) [B4]. An LO of  $\omega_{LO,1} \pm \omega_{LO,2} \pm \omega_{LO,3}$  is artificially synthesized within the signal path by cascading two image-reject mixers operating with LOs of  $\omega_{LO,1}$  and  $\pm\omega_{LO,2}$ . However, signal leakage is associated with every stage of mixing due to finite image rejection and harmonic rejection.

The effect of finite harmonic rejection and image rejection is shown in Fig. 40. The image rejection (IR) in dB that can be achieved, is

$$IR \approx -10 \log \left( \frac{\Delta^2 + \phi^2}{4} \right) \quad (8)$$

where  $\Delta$  is the mismatch in the gain of I and Q paths and  $\phi$  is the phase error between the I

<sup>2</sup>At least  $f_0/2$  to  $f_0$  for down-converting a bandwidth of  $f_0$ .

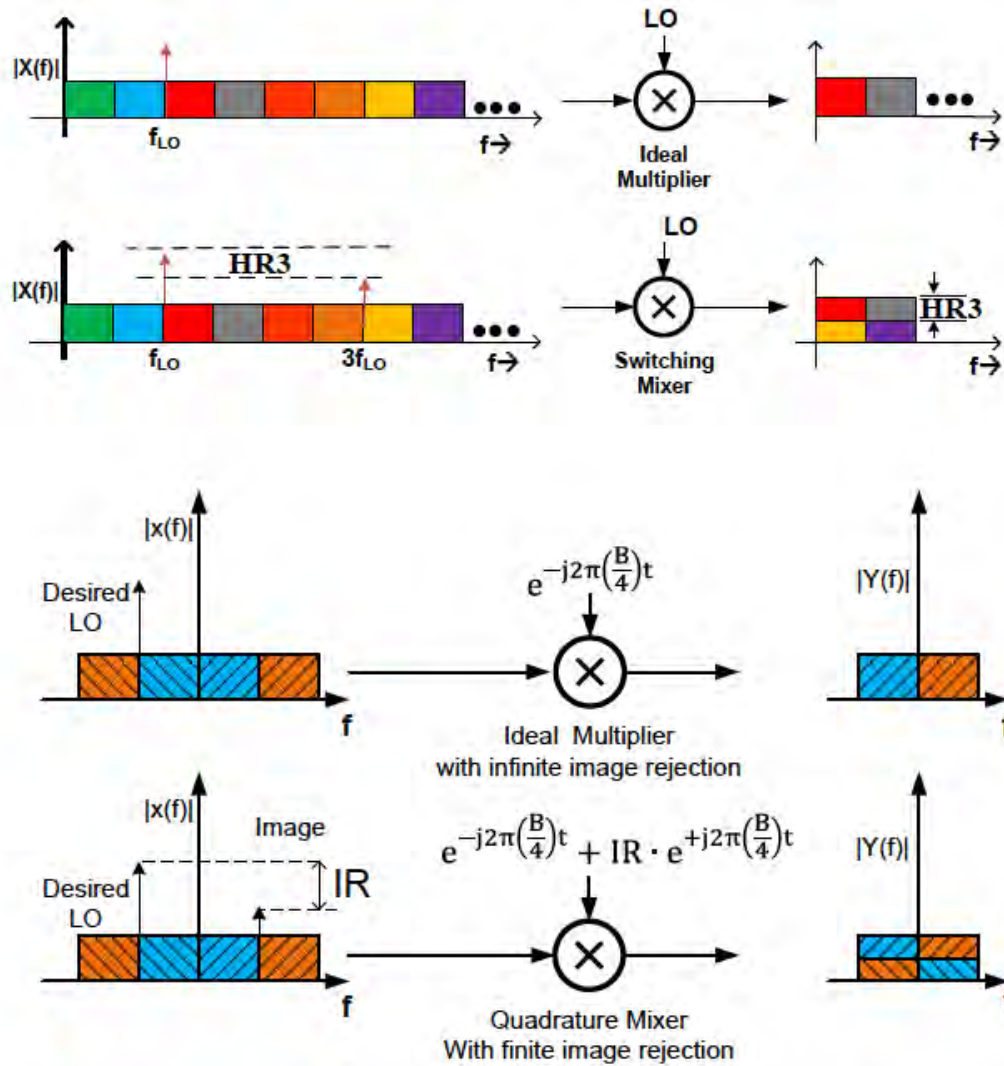


Figure 40: Mechanisms leading to signal leakage in a cascade of image reject mixers: (a) Finite harmonic rejection of switching mixers vs ideal multipliers, (b) Finite image rejection of practical quadrature mixers vs ideal quadrature multipliers.

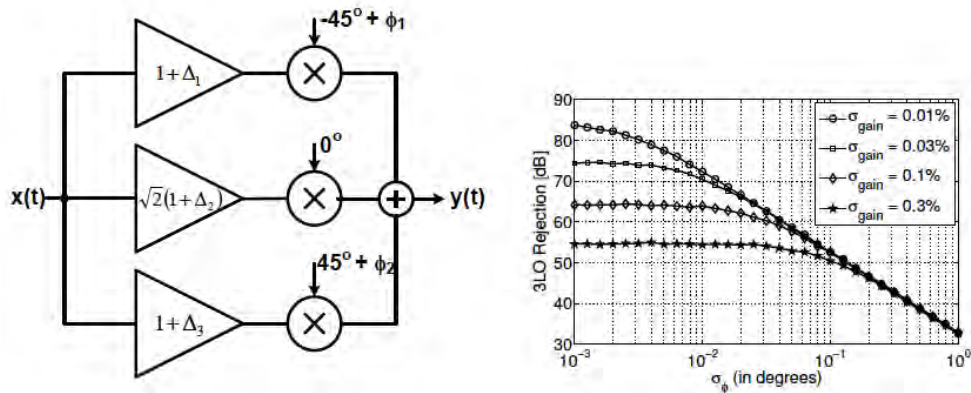


Figure 41: (a) Block diagram of a harmonic rejection mixer [B8] and (b) Achievable harmonic rejection ratio for various gain and phase mismatches.

**Table 6: A comparison of the PLL requirements and the scan time of different approaches for RF channelization into N channels.**

Architecture	$T_{scan}$	PLL Requirements
Sequential scanning (Fig. 38(a))	$N \cdot T_{analysis} + T_{hop}$	Wideband PLL
Parallel receivers (Fig. 38(b))	$T_{analysis}$	Multiple PLLs Single
IDC (Fig. 39)	$T_{analysis}$	fixed frequency PLL

and Q paths of the receiver [B9]. Typically achievable harmonic rejection is shown in Figure 41. Harmonic rejection is typically limited to 30-40dB, which places a fundamental limitation on the signal leakage. Although, the use of two-stage HRMs is possible to achieve higher harmonic rejection, using them in every mixer becomes a power hungry solution. This motivates the need for a new IDC architecture that can relax the requirements on harmonic rejection and image rejection. A comparison between various approaches for RF channelizers is presented in Table 6. The IDC architecture offers a very short scan time,  $T_{scan}$ , set by the analysis time,  $T_{analysis}$ , for one channel time while requiring only a single phase-locked loop. Sequential scanning approaches lead to  $N$  ( $N$  = the number of channels) times longer scan times and require PLLs that are tunable over a wide bandwidth; the time  $T_{hop}$  required for the PLL to jump from one channel to the next further increases the scan time. Parallel receivers have a fast scan time but require multiple PLLs on the same die which can lead to spurious coupling between the LO signals.

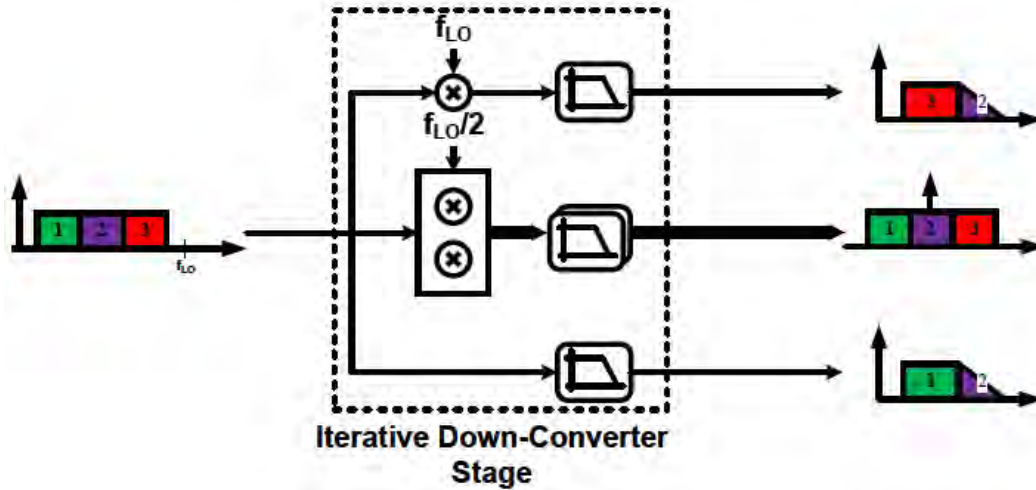
### 7.3 Proposed 3-way Splitting IDC for Concurrent RF Channelizers

IDC with a cascade of image-reject mixers (Fig. 39), signals in any part of the spectrum undergo the same number of frequency translations. Based on the signal leakage mechanisms described in the previous section, this would result in signal leakage for every band. We propose a 3-way IDC architecture (shown in Fig. 42 (a)) which reduces the number of mixers. The lower half of the input spectrum does not need to undergo any mixing<sup>3</sup>. A low pass filter is used to filter out interferers in the higher half of the input spectrum. The higher half of the input spectrum can be down-converted with a LO frequency= $f_{LO}$ . If the RF signal above  $f_{LO}$  is sufficiently attenuated, a simple switching mixer can be used; otherwise a quadrature (IQ) mixer needs to be used. The suppression of the signals beyond  $f_{LO}$  is a combination of the attenuation offered by all the preceding filters and the image rejection in the mixer. A third path is created to directly down-convert the signals around the mid-band which are in the transition band of the low-pass filters in the higher frequency and lower frequency paths. This ensures that the signals around the mid-band undergo only one down-conversion and that the low-pass filters can be designed with a lower order.

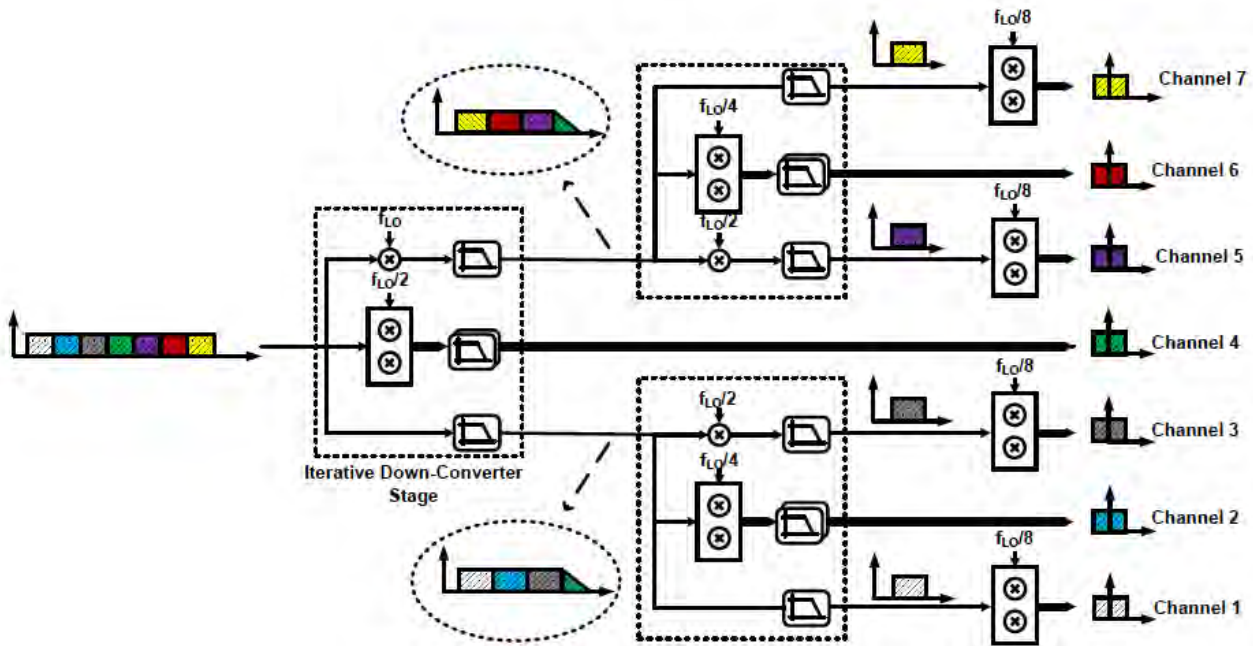
### 7.4 Analysis of Signal Leakage Mechanisms in 3-Way IDCs

The RF channelizer architecture based on the proposed 3-way IDC is shown in Fig. 42 (b). Channels 1, 2 and 4 have only one mixer in the signal path. This results in significant reduction in the signal leakage for these channels. Fig. 43 (a) shows the conversion gain of the RF Channelizer from input to Channel 1. In addition to the desired part of the input spectrum ( $f_{LO}/16$  to  $3f_{LO}/16$ ),

<sup>3</sup>The reduction of the number of mixers in an IDC was also proposed in [B10].

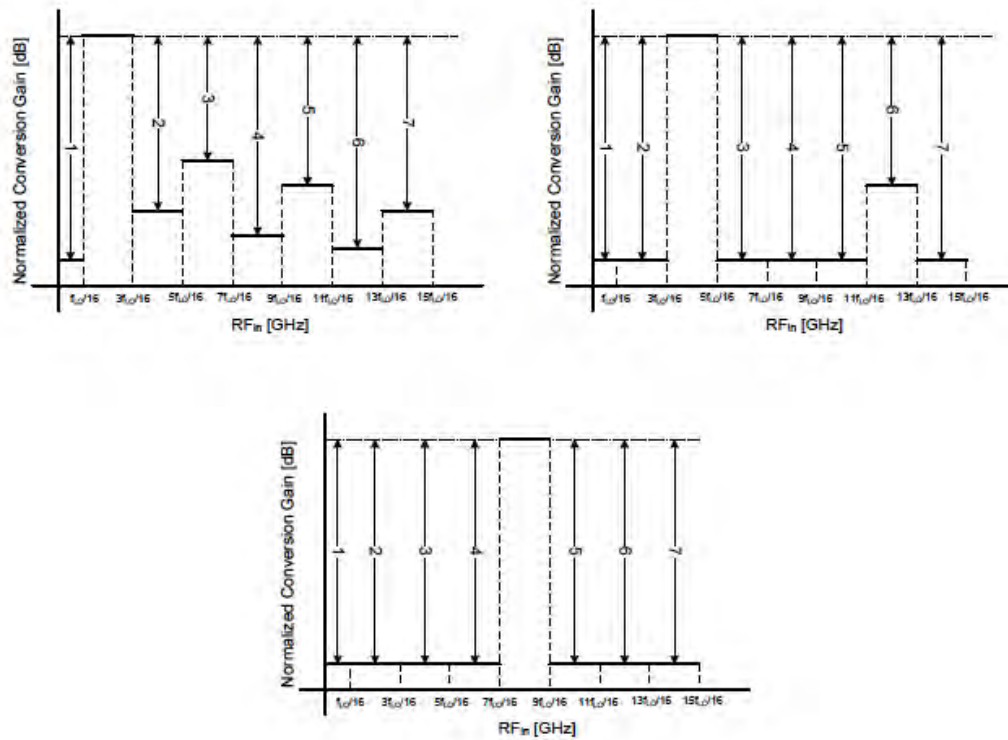


7.4.1 A single stage of the proposed 3-way IDC. There is no mixer in the low-frequency paths and a mid-frequency path is added to relax the specifications of the low-pass filters.



7.4.2 A concurrent RF channelizer using the proposed 3-way IDC. The number of mixers is reduced to one in Channels 1, 2 and 4.

**Figure 42: A RF Channelizer architecture using the proposed 3-way IDC with reduced number of mixers.**



**Figure 43: Expected conversion gain of the RF Channelizer when measured at various channels. (a) Measured at channel 1, (b) measured at channel 2, (c) measured at channel 4.**

signals from other parts of the input spectrum also get down-converted. The strength of the leaked signal is determined by the filter attenuation in the preceding stages and harmonic rejection of the  $f_{LO}/8$  mixer.

The typical conversion gain of the RF Channelizer from the input to Channel 2 and Channel 4 are shown in Fig. 43(b) and Fig. 43(c). The signal leakage for Channel 2 is limited by the sum of filter attenuation and the harmonic rejection of  $f_{LO}/4$  mixer. Signal leakage for Channel 4 is limited by the RF-to-IF leakage of the  $f_{LO}/2$  mixer.

Other channels have more mixers in the signal path resulting in multiple, more complex signal leakage mechanisms as shown in Fig. 44. The various signal leakage mechanism in the channelizer are indicated and estimates of the leakage levels are provided. The following features can be noted. The worst-case leakage is determined by a filtering + harmonic rejection or filtering + image rejection or RF-to-IF leakage in a mixer. With the proposed IDC, signal leakage improves significantly for the channels with lower number of mixers.

## 7.5 Partially Concurrent, Rapid-Switching RF Channelizer

The RF channelizer architecture presented in the previous section (Fig. 42) is a fully concurrent architecture; the input spectrum is frequency channelized into seven channels. This RF architecture can also be modified into a rapid-switching channelizer where all channels are available one by one at the same output port depending on the configuration of the channelizer. In order to demonstrate both the concurrency and rapid-switching capabilities of the RF channelizer architecture, a partially concurrent, rapid-channel-switching channelizer prototype is demonstrated in this work.

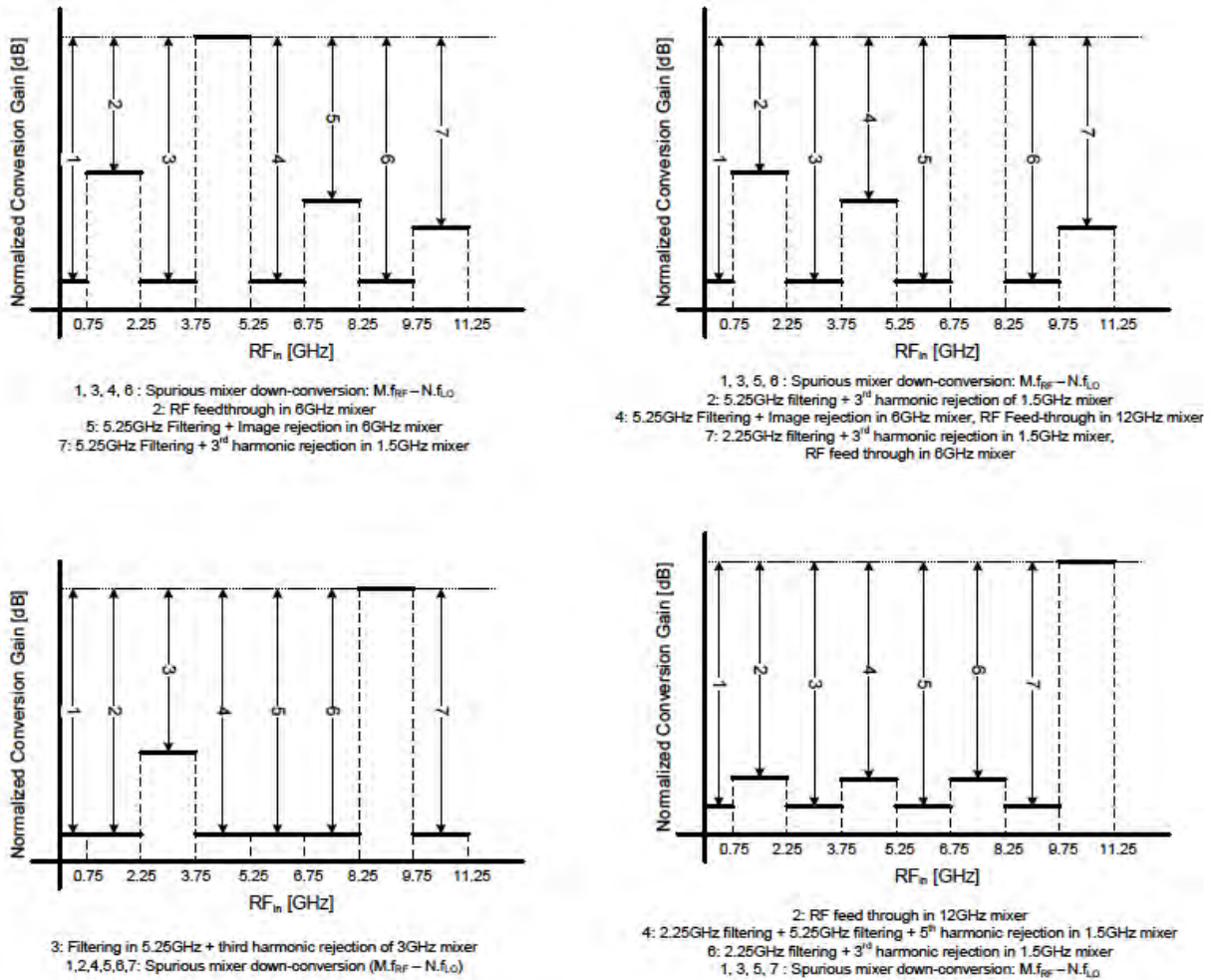


Figure 44: Signal leakage mechanisms for channels 3, and 5 through 7 of the RF channelizer.

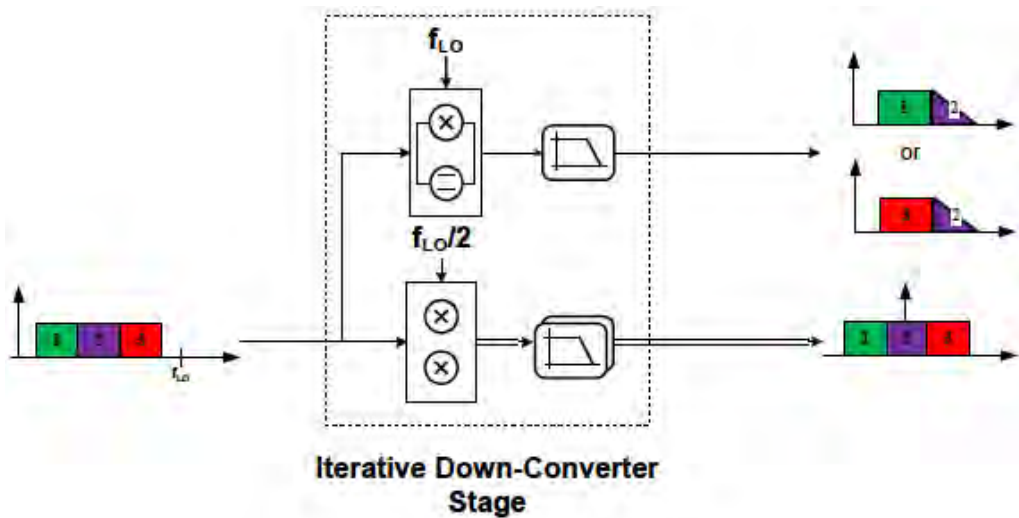
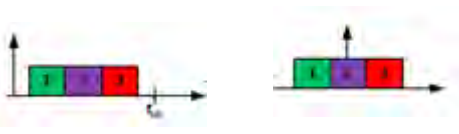


Figure 45: Block diagram of the partially concurrent implementation of the 3-way IDC stage from Fig. 42 (a). The paths delivering signal 1 and 3 are combined into one using a dual-mode mixer.



**Figure 46: Block diagram for the partially concurrent, fast switching RF channelizer prototype; it demonstrates the concurrency and fast switching features of the proposed RF iterative downconverter channelizer architecture.**

### 7.5.1 Partial Concurrency

The fully concurrent IDC shown in Fig. 42(a) can be reduced to a partially concurrent IDC as shown in Fig. 45. The paths delivering signal 1 and signal 3 are combined using a dual-mode mixer. The dual-mode mixer is capable of switching between a mixing mode or a transparent mode.

The block diagram of the prototype of the RF channelizer is shown in Fig. 46. It uses two stages of the proposed IDC (shown in Fig. 45). The prototype RF channelizer has 3 outputs instead of 7 outputs as in the case of a fully concurrent RF channelizer. Output 1 down-converts channels 1 or 3 or 5 or 7, with an ability to rapidly switch between them. Output 2 down-converts channels 2 or 6. Output 3 down-converts channel 4.

A limitation of the proposed partial concurrent prototype compared to a fully concurrency is that channel 6 and channel 1 (or 3) cannot be analyzed simultaneously. This is due to the configuration of the dual mode mixer in IDC stage 1.

**Rapid Channel Switching** In the RF channelizer prototype, output 1 delivers channels 1 or 3 or 5 or 7. Similar output 2 delivers channel 2 or 6. The time duration for switching an output of the RF channelizer from one channel to another is limited by (a) the bias settling in the dual-mode mixers, (b) the bias settling in current buffers and (c) the signal settling in filters. Of the three factors, the filter is expected to negligible (a few nano seconds) due to their wide bandwidth. The channel switching duration is limited by settling of bias voltages and currents in the mixers and current buffers.

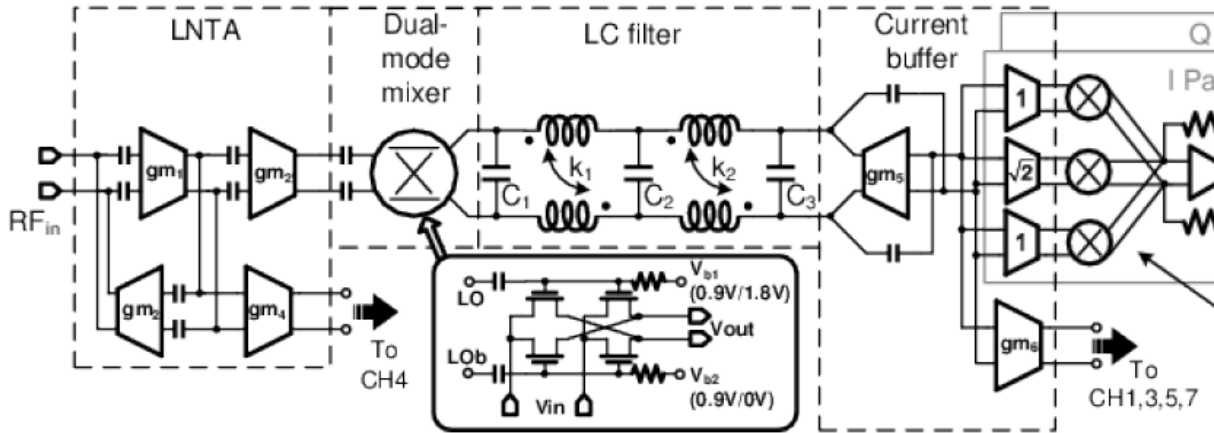
### 7.5.2 Circuit Implementation of the Partially Concurrent, Rapid-Switching RF Channelizer

Key circuit implementation details of the RF channelizer prototype are shown in Fig. 47. The RF input signal is amplified and converted to a current using a low-noise transconductance amplifier (LNTA). In the partially concurrent prototype, the LNTA has two outputs driving IDC stage 1: one driving the 4.8GHz I/Q mixer for channel 4 and the other driving the dual-mode mixer of IDC Stage 1.

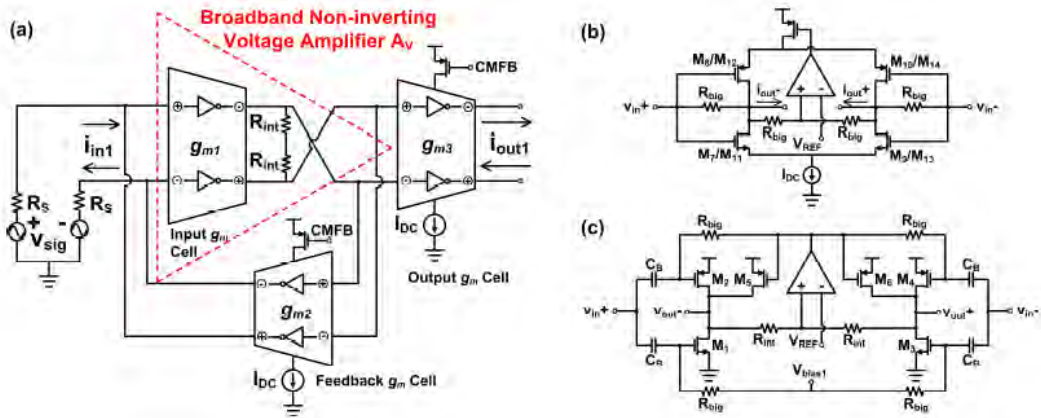
Following the dual-mode mixer, the signal is filtered with an on-chip LC filter and driven into a current buffer. The current buffer creates multiple copies of scaled currents for the mixers in the IDC stage 2. In Fig. 47 the harmonic rejection mixer and the transimpedance amplifier (TIA) for the path delivering output 2 (channel 2 or 6).

**Low-Noise Transconductance Amplifier** A multi-stage LNTA circuit based on a Gm-boosted current mirroring topology is chosen. The LNTA maintains high linearity through the inherent input match predistortion [B11]. Traditional single-stage LNTAs typically use common-source (CS)

stages to provide large transconductance ( $g_m$ ). The input parasitic capacitance of the CS stages



**Figure 47: Circuit implementation details for the signal paths to receive Channels 2 or 6 in the RF channelizer prototype of Fig. 45 (a) LNTA, (b) dual-mode mixer, (c) 5<sup>th</sup> order LC filter, (d) current buffer, (e) harmonic rejection mixer.**



**Figure 48: (a) Circuit implementation of the wideband LNTA. (b) Circuit diagram of the  $g_m$  cells  $g_{m2}$  and  $g_{m3}$ . (c) Circuit diagram of the voltage amplifier performing  $g_m$ -boosting.**

leads to an undesirable tradeoff between  $g_m$  and  $S_{11}$  bandwidth. To alleviate this tradeoff, a broadband voltage amplifier can be inserted before the CS stage ( $g_{m3}$  cell) to boost its  $g_m$ , leading to a smaller CS stage and therefore less capacitive loading, as shown in Fig. 48 (a). However, the large voltage swing brought by the voltage amplifier can degrade the linearity of the LNTA. Another  $g_m$  cell,  $g_{m2}$ , can be inserted as an active feedback for the broadband voltage amplifier. This  $g_m$  cell has the same structure as  $g_{m3}$  (Fig. 48 (b)). The  $g_m$  cell pair  $g_{m2}$  and  $g_{m3}$  forms a current mirror that provides a linear current gain despite the distortion brought by the voltage amplifier. The LNTA linearity is solely limited by the nonlinear current division between the source resistance and the input impedance of the LNTA.

The  $g_{m2}$  cell provides input matching. Since the broadband voltage amplifier boosts the  $g_m$  of  $g_{m3}$  as well as  $g_{m2}$ , the  $g_m$  required for input matching is reduced by the broadband amplifier voltage gain, leading to reduced noise contribution of  $g_{m2}$  as well. The feedback structure that consists of the broadband voltage amplifier and the  $g_{m2}$  cell acts like a gyrator and introduces a zero to the input impedance of the LNTA. By properly sizing all the  $g_m$  cells and the loading resistance

$R_{int}$ , the zero introduced can counter the pole caused by the LNTA input side capacitance and lead to extremely wide instantaneous  $S_{11}$  bandwidth.

The differential input LNTA is designed to provide a 100-ohm input impedance (differential) at the input interface of the chip and drives two amplified signals concurrently into the first stage of the IDC. One copy of the LNTA output is used for midband down-conversion using the 4.8GHz I/Q mixer to directly down-convert channel 4. The second copy drives the 9.6GHz dual-mode mixer.

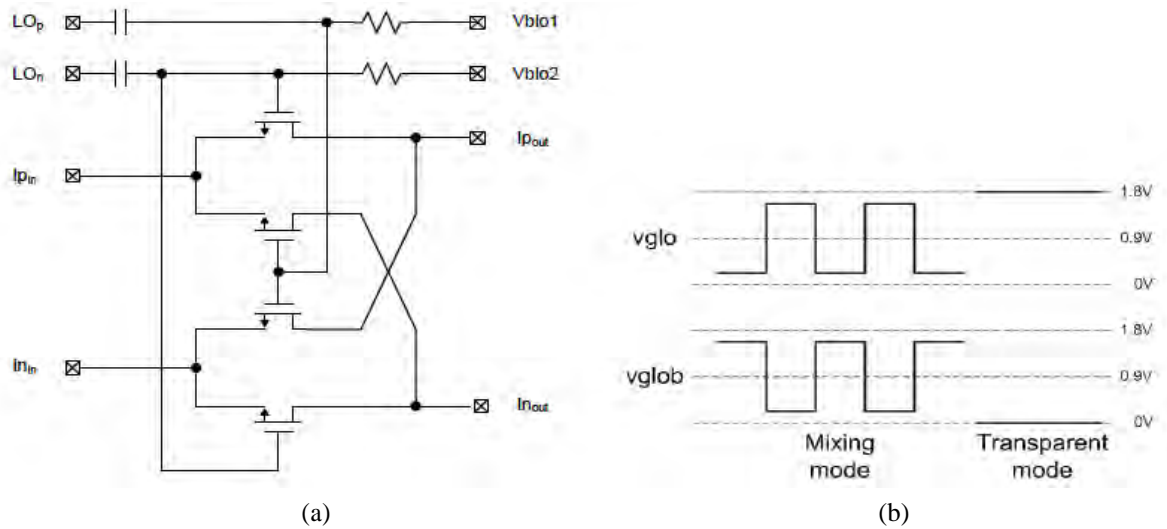
**Dual-Mode and Harmonic-Reject Mixers** The image and harmonic rejection requirements for the mixers are presented in Table 7. The dual-mode mixer in Fig. 47 needs the ability to operate either as a transparent block or as a mixer. The schematic of the dual-mode mixer circuit is shown in Fig. 49a. The source/drain voltage of the switches is set by the input stage common mode voltage of current buffer, which is approximately  $V_{dd}/2$ . The  $V_{GS}$  of the ON-switches is then limited to  $V_{dd}/2$  which increases their ON-resistance, which in turn increases the output voltage swing for the LNTA and degrades its linearity.

**Table 7: Image rejection and harmonic rejection requirements.**

		Requirements for Signal Leakage < -60dB
1 <sup>st</sup> stage 12G Mixer		No HR,IR requirements
1 <sup>st</sup> stage 6G Mixer: IR		60dB*
1 <sup>st</sup> stage LPF		5.25G, 5 <sup>th</sup> order
2 <sup>nd</sup> stage 6G mixer: IR		38dB
3G mixer	IR	60dB*
	HR3	14dB
2 <sup>nd</sup> stage LPF		5 <sup>th</sup> order
1.5G mixer	IR	60dB*
	HR3	18dB

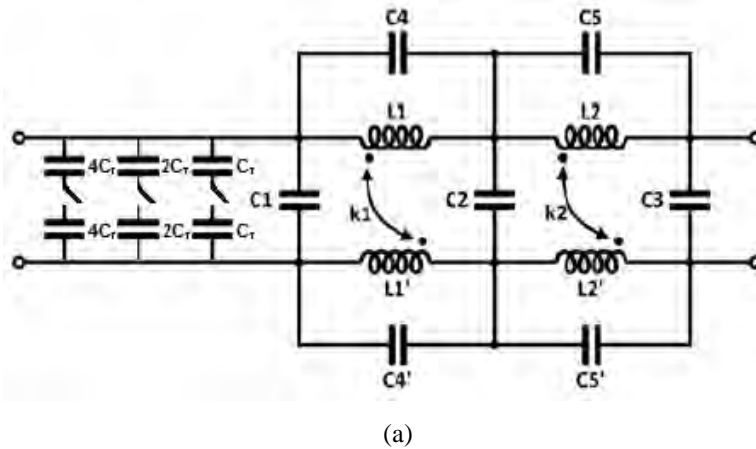
\*Off-chip I/Q calibration can improve the image rejection [B12].

In order to overcome this problem, LO signals are ac coupled to the gates of switches, and the gate bias voltages are set by  $V_{blo1}$  and  $V_{blo2}$ . In the mixing mode, the LO driver is turned on, and  $V_{blo1}$  and  $V_{blo2}$  are set to 0.9V. The bias voltage can be tuned with a bias circuit from 0.8V to 0.98V to tune the gain of the mixer and make sure the LO is non-overlapping. In the transparent mode, the LO driver is turned off,  $V_{blo1}$  is set to 0V, and  $V_{blo2}$  is set to  $3V_{dd}/2$  to only turn on one branch of the differential pair. The bodies of the switches are connected to their drain to make sure their  $V_{gb}$  will be not higher than VDD to avoid gate breaking down. All the switches are put into different deep-N-wells to separate the body from the substrate. The dual-mode mixer can be shut-off by grounding the gates of all the switches.



**Figure 49: (a) Schematic of dual mode mixer. (b) Ideal LO waveforms for the dual mode mixer**

Multiple techniques for harmonic rejection mixers (HRMs) have been demonstrated [B8, B13, B14, B15, B16]. The HRM architecture demonstrated in [B8] was chosen for the HRM used in the RF channelizer given its ability to extend to high frequencies of operation. The requirements from various harmonic rejection mixers are tabulated in Table 7.



	Filter 1	Filter 2
C1	480fF	2.1pF
C2	1.8pF	5.2pF
C3	320fF	1.7pF
C4	1.7pF	2.3pF
C5	1pF	1pF
C <sub>T</sub>	260fF	340fF
L1	260pH	640pH
L2	290pH	650pH
k <sub>1</sub> ,k <sub>2</sub>	0.55	0.55

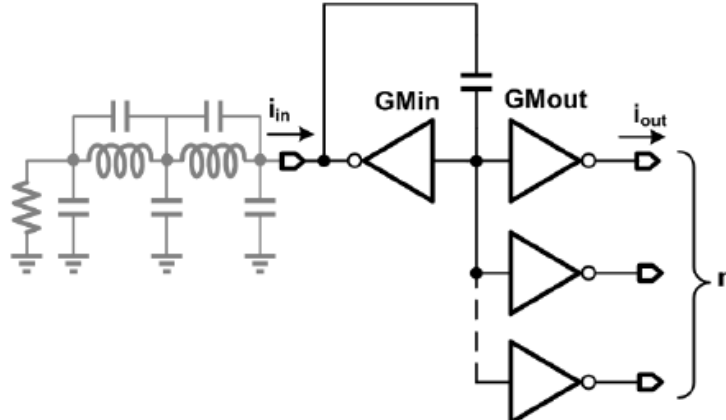
(b)

**Figure 50: (a) Circuit diagram of the LC low pass filters (b) Component values for the filters.**

**On-Chip Low-Pass LC Filters** Passive LC filters were chosen given the required high frequency of operation and superior linearity properties of LC filters. Signal leakage is determined by the suppression of out-of-band blockers and the harmonic/ image rejection of the following mixers. In order to simplify the mixer requirements, a 5<sup>th</sup> order elliptic filter [B17] with a 4dB passband ripple was designed. The filter is driven by a high output impedance current source and loaded by a 25Ω differential current buffer. The filter design is shown in Fig. 50a, and values are specified in Fig. 50b. The area of Filters 1 and 2 are 372μm x 225μm and 615μm x 210μm respectively.

**RF Current Buffers with Scaled Outputs** A current buffer provides the appropriate load for the filters and produces copies of the RF current signal for the following stages of mixing (see Fig. 47). The simplified current buffer circuit schematic is shown in Fig. 51. It consists of one input gm cell and several output gm cells. The input and output terminals of GMin are AC shorted to make a low input impedance of 12.5 Ω as the loading of 5.25GHz ladder type filter. If the input impedance is lower the linearity is better, but the power consumption is higher. Transistor parasitic capacitors will generate an equivalent input capacitor. That capacitor can be absorbed into the last capacitor of passive filter, thus, so that the bandwidth is not limited by the transistor  $f_T$ . The GMin and GMout are matched to cancel the non-linearity of the Gms to the first order.

GMout provides multiple current copies of signal for the subsequent harmonic reject mixers (both I & Q paths). The current ratio required by the HRM is  $1:\sqrt{2}$  which is implemented by

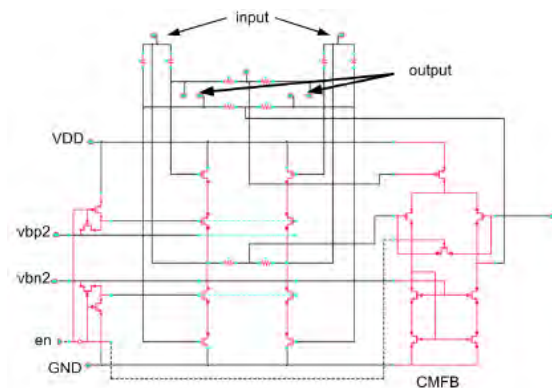


**Figure 51: Simplified schematic of RF current buffer with one input and multiple outputs**

rationing the number of transistor fingers. Since the number of fingers are integers, 29:41 is used as an approximation for the ideal  $1:\sqrt{2}$  ratio, which is sufficiently accurate for up to 60dB harmonic rejection ratio. The current buffer further provides a branch for the I/Q mixer in the next stage. The branches fed into dual-mode mixer and HRM can be turned off separately. The current buffer can be fast switched between its two output branches, or can have all its output branches turned on to support partial concurrency.

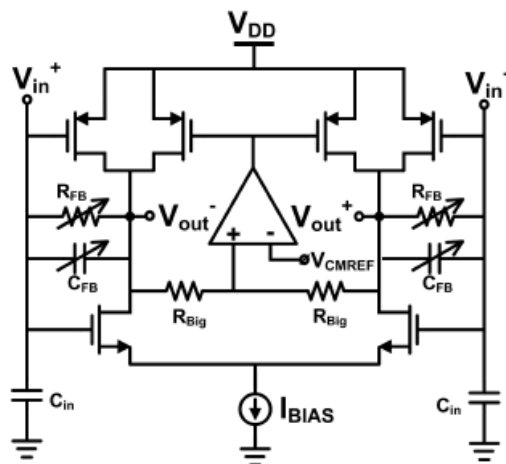
Fig. 52 shows the transistor implementation of input RF gm cell. The core of gm cell is a pseudo-differential pair, which has good linearity compared to a differential pair. A current-reuse topology is used to decrease the power consumption for a given transconductance. Cascode transistors are used to increase the output impedance of the gm cell. gm cell can be turned off by switching the gate voltage of the PMOS cascode transistor to VDD and switching the gate voltage

of the NMOS cascode transistor to GND. Since there are no decoupling capacitors between the switch and the gate of cascode transistor, the gm cell can be turned on and off very quickly.



**Figure 52: Transistor schematic of the RF current buffer input gmstage.**

**Trans-Impedance Amplifiers** To meet the high bandwidth requirement (3-dB bandwidth greater than 600MHz) of the transimpedance amplifier (TIA), a single stage wideband  $g_m$  cell is used instead of the traditional two-stage OTA (Fig. 53). Switchable feedback resistors and capacitors allow the tuning of the TIA transimpedance gain and bandwidth. At the differential input nodes



**Figure 53: Schematic diagram of the Transimpedance Amplifier (TIA).**

**Table 8: Measured P1dB, IIP3, Noise Figure and computed Noise Floor, SFDR for the RF Channelizer in the different channels.**

Channel	1	2	3	4	5	6	7
P1dB [dB]	-30.6	-21.7	-16.7	-21.3	-13.0	-13.8	-18.0
IIP3 [dBm]	-19.9	-12.4	-8.8	-12.5	-3.4	-5.5	-8.5
NF [dB]	6.8	7.7	14.3	7.2	22.6	18.1	16.6
Noise Floor <sup>1</sup> [dBm]	-107.2	-106.3	-99.7	-106.8	-91.4	-95.9	-97.4
SFDR [dB]	58.4	62.6	60.6	62.9	58.7	60.2	59.3

<sup>1</sup> Noise bandwidth is assumed to be 1MHz.

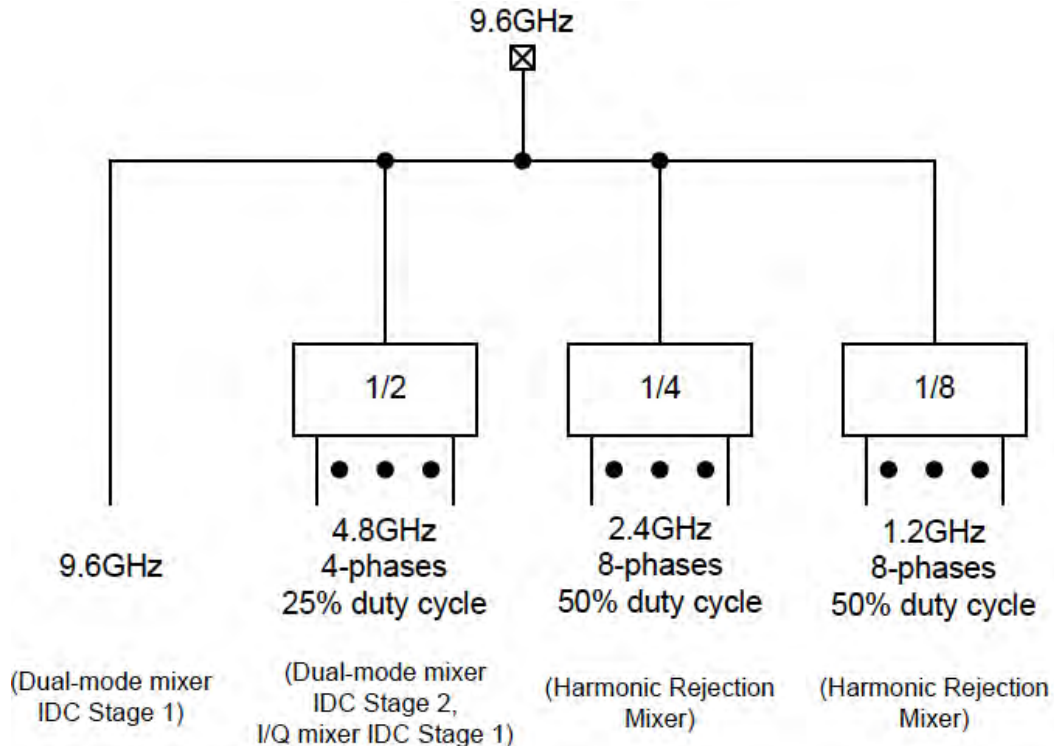
grounded capacitors are added to ensure the low input impedance at frequencies out of the  $g_m$  cell bandwidth.

**LO Generation and Distribution** The LO signal for the channelizer is generated by a fast switching PLL described in Part 10. The block diagram of the RF channelizer’s LO distribution network is shown in Fig. 54. The LO path is designed to receive an external 9.6GHz differential LO signal. The differential signals are distributed across the chip after conversion to rail-to-rail CMOS signals. The 9.6GHz LO is then locally frequency-divided to generate the phases required by the various mixers.

**Frequency Dividers** For dividing the input clock of 9.6GHz, D-Latch blocks are concatenated in a feedback loop. Current mode logic (CML) is used for designing D-Latches. Figure 55 describes the D-Latch schematic based on the CML approach. The differential input data ( $in$  and  $\bar{in}$ ) are fed into the inputs of the differential amplifier ( $M_1$  and  $M_2$ ) with pull up resistor of  $R_1 = 1.2K\Omega$ . The tail current,  $I_{tail}$  is steered between the differential stage and the latch stage ( $M_3$  and  $M_4$ ), using the differential input clock phase,  $LO$  and  $\bar{LO}$ .

## 7.6 Experimental Results

The chip was designed and fabricated in a standard 65nm CMOS process and packaged in 6mm-x-6mm 48-pin QFN package. Fig. 56 shows the die photo of the chip.



**Figure 54: Block Diagram of the LO distribution network.**

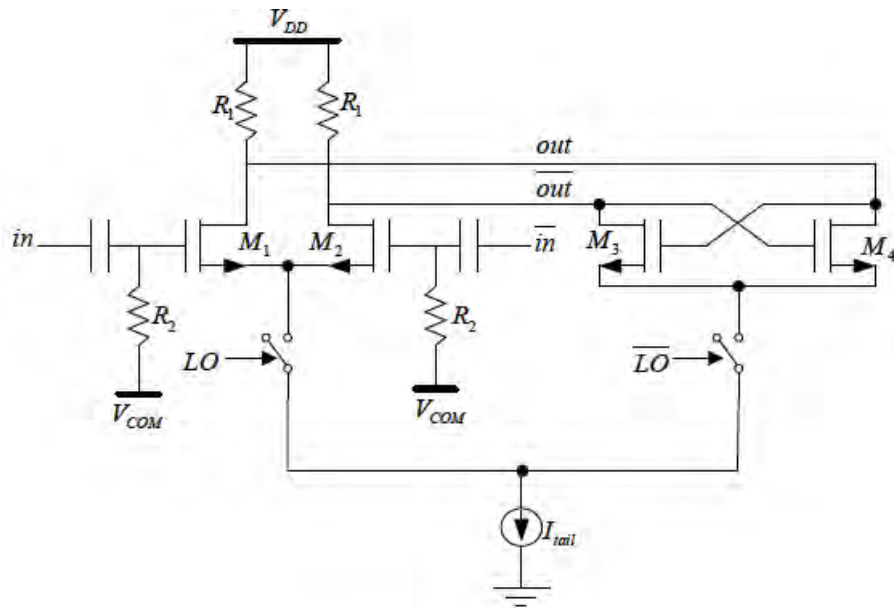


Figure 55:  
D-Latch.

CML

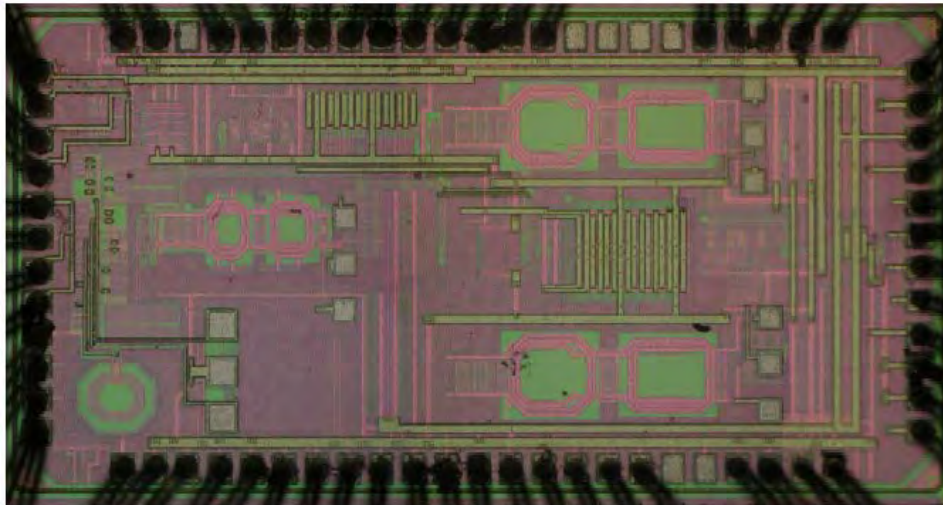


Figure 56: Die photo of the prototype chip.

Table 9: Duration for various modes of switching of the RF Channelizer.

Switch	Duration	Switch	Duration
Ch 1 to Ch 3	390ns	Ch 3 to Ch 1	821ns
Ch 1 to Ch 5	437ns	Ch 5 to Ch 1	881ns
Ch 1 to Ch 7	13ns	Ch 7 to Ch 1	50ns
Ch 3 to Ch 5	10ns	Ch 5 to Ch 3	59ns
Ch 3 to Ch 7	778ns	Ch 7 to Ch 3	480ns
Ch 5 to Ch 7	920ns	Ch 7 to Ch 5	513ns
Ch 2 to Ch 6	8ns	Ch 6 to Ch 2	8ns

A summary of the measured IIP3, P1dB, Noise figure, Noise Floor ( $P_{\text{Noise}}$ ) are presented in Table. 8. The spurious free dynamic range (SFDR) is calculated as:

$$SFDR = 2/3 \times (IIP3 - P_{\text{Noise}}) \quad - \quad (9)$$

### 7.6.1 Concurrency

Concurrent signal channelization by the RF channelizer was demonstrated by simultaneously receiving a signal in Channel 1 and Channel 2. Fig. 57 shows the measured BER vs incident desired signal power for various power levels of signal in the adjacent channel. A 200Mbps BPSK signal was used in each channel resulting in an aggregate data rate of 0.4Gbps for two channels. The aggregation of the three concurrent outputs along with the use of higher-order QAM modulations will result in multi-Gbps data rates.

### 7.6.2 Fast Channel Switching

Since it avoids PLL frequency switching and the associated settling time, the presented RF channelizer is capable of rapidly switching from one channel to another. The switching time is now limited by the turn-ON/OFF times of the bias circuits in the signal path blocks which include mixers and current buffers.

Channel switching measurements were performance between a large set of channel combination and are summarized in Table 9; the switching can be as fast as 8ns and is always faster than  $1\mu\text{s}$ . This is significant in applications where tracking a 77kHz FHSS signal is a requirement. A further improvement in switching speed is possible by increasing the power consumption in the bias circuits. Fig. 58 shows the scope measurement demonstrating 2MHz channel hopping between switching between Channel 2 and Channel 6.

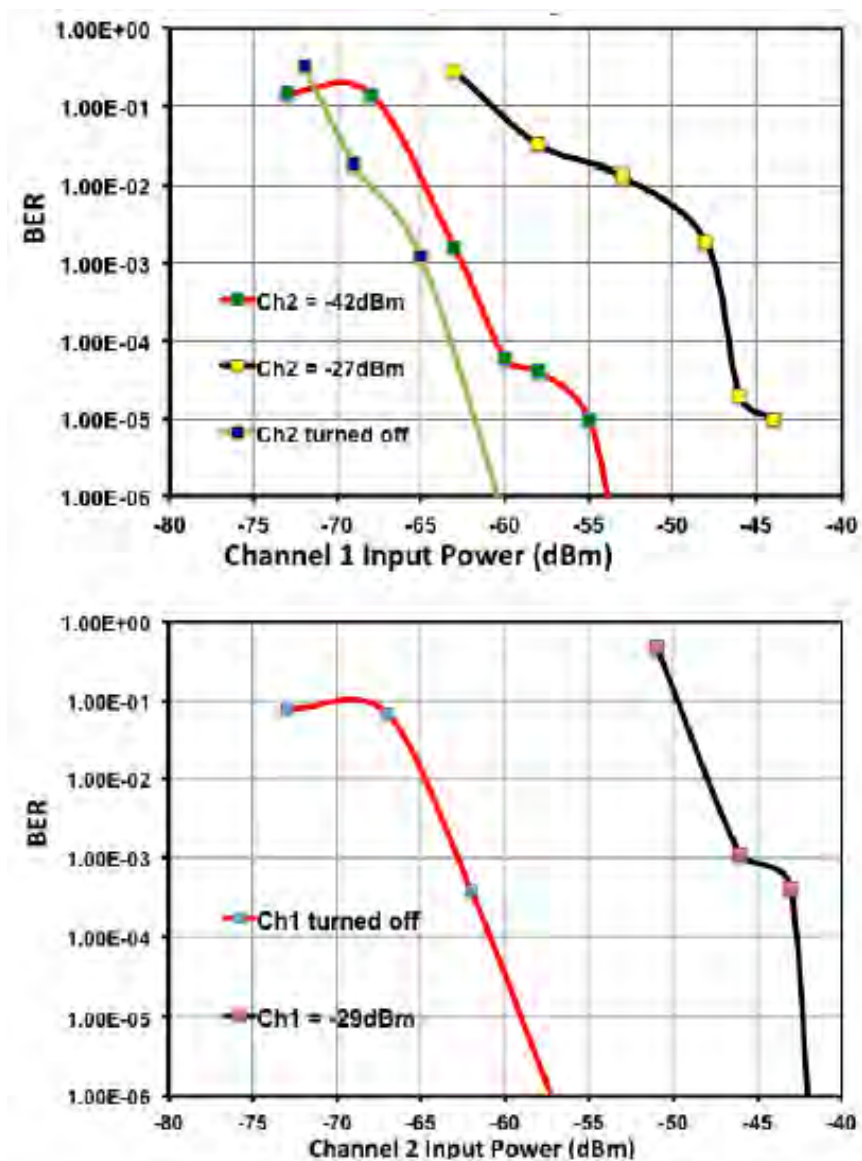


Figure 57: (a) Measured BER of the RF channelizer receiving channel 1, while simultaneously receiving channel 2. (b) Measured BER of the RF channelizer receiving channel 2, while simultaneously receiving channel 1.



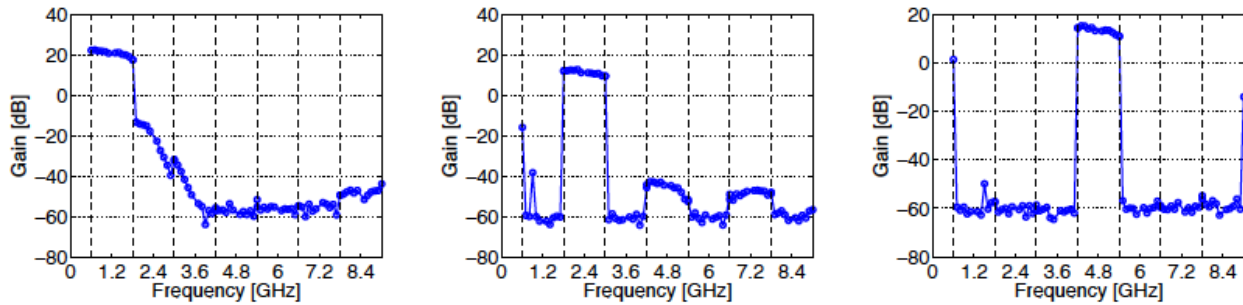
**Figure 58: (a) Measured 2MHz hopping between Channel 2 and 6 at output 2. (b) A closer look at the transition from channel 2 to channel 6. (c) A closer look at the transition from channel 6 to channel 2.**

### 7.6.3 Signal Leakage Among Channels

The conversion gain of the RF Channelizer in its various configuration is shown in Fig. 59 and Fig. 60. The channelizer provides higher gain to a signal in desired channel while attenuating the signals outside the desired channel.

The 3-way splitting iterative down-converter architecture reduces the number of stages of down-conversion in certain configurations of the RF Channelizer while retaining that number for the rest. The effect of this can be observed in the superior signal leakage performance in channel 1, 2 and 4 as shown in Fig. 59.

The measured signal leakage between a few specific channels is worse than the desired 60dB because of two primary reasons. Firstly, The RF channelizer was designed for receiving a 0.75-11.25GHz bandwidth using a fixed 12GHz LO. The LC filters were designed for 5.25GHz band-



**Figure 59: Measured conversion gain as a function of RF input frequency for (a) RF Channelizer configured to receive Channel 1, (b) RF Channelizer configured to receive Channel 2 and (c) RF Channelizer configured to receive Channel 4. These configurations have just one mixer in the signal path.**

width and 2.25GHz bandwidth. However due to the limitations from PCB transmission line and LO input matching circuits, LO frequency was restricted to 9.6GHz, thereby forcing a 80% scaling in the frequency plan. However, the frequency scaling could not be applied to the LC filter. LC filters of bandwidth 4.2GHz and 1.8GHz instead of 5.25GHz and 2.25GHz would provide additional suppression (around 15dB) of the undesired signals.

RF-to-IF leakage in mixers cause specific signal leakages. This mechanism was overlooked at the time of design. A re-design of the mixer will reduce RF-to-IF leakage and improve the signal leakages. The following signal leakages could be attributed to RF-to-IF leakage in 9.6GHz and 4.8GHz mixers:

**7.6.3.1** Leakage from channel 1 to channel 7 (as shown in Fig. 60 (d)), leakage from channel 2 to channel 6 (as shown in Fig. 60 (c)), Leakage from channel 1 and 3 to channel 5 (as shown in Fig. 60 (b)) are due to RF-to-IF leakages in 9.6GHz mixer.

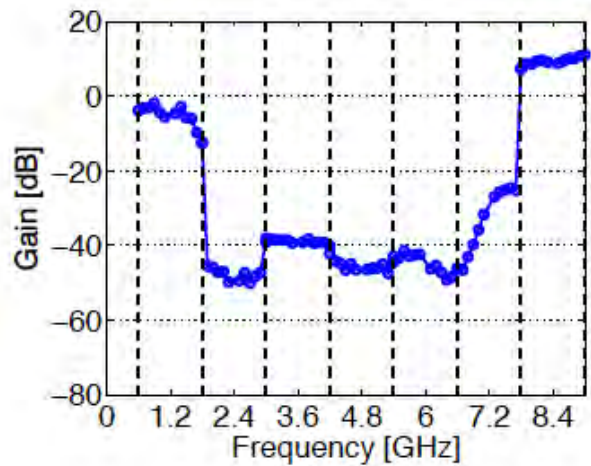
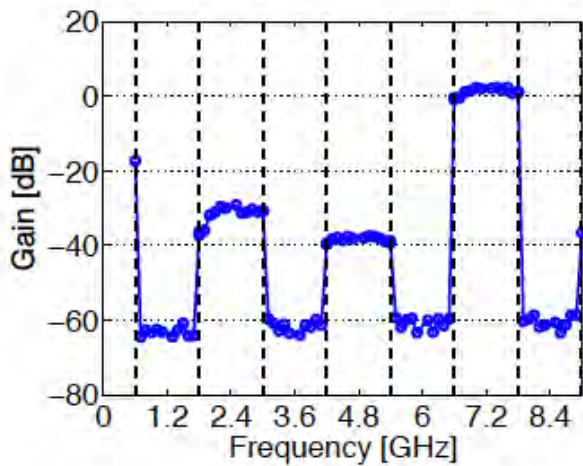
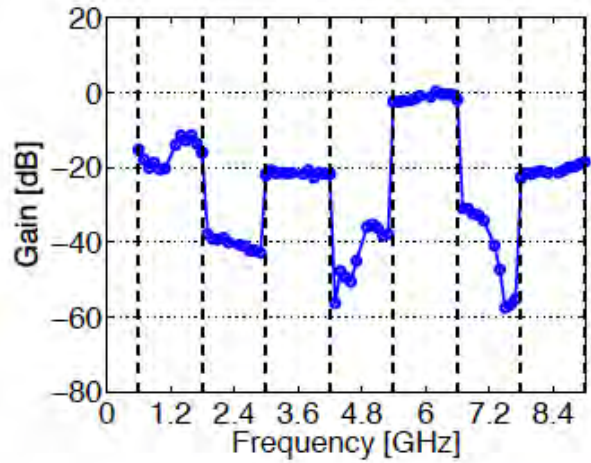
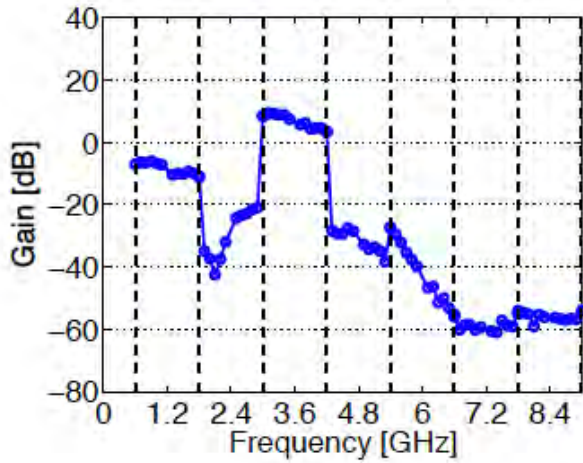
**7.6.3.2** Leakage from channel 1 while receiving channel 3 (as shown in Fig. 60 (a)) and leakage from channel 7 while receiving channel 5 is due to RF-to-IF leakage in 4.8GHz mixer.

#### 7.6.4 Comparison with State-of-Art RF Channelizers

Table 10 compares our RF channelizer with the state-of-art approaches to frequency channelization. In comparison with other implementations, our RF channelizer processes a significantly wider bandwidth while demonstrating concurrency as well as the ability to rapidly switch channels.

### 7.7 Conclusions

A novel 3-way iterative downconversion (IDC) architecture has been proposed. The signal leakage for channels in lower half of input spectrum is significantly improved compared to cascade of image reject mixers, because of lower number of frequency translations. The IDC architecture is amenable to concurrency as well as rapid-switching implementation. A prototype semi-concurrent, rapid-switching RF channelizer has been fabricated in 65nm technology to demonstrate concurrency and rapid switching. The RF channelizer has been experimentally demonstrated to have switching times of less than  $1\mu s$  and for certain cases as quick as 8ns. By using two concurrent



**Figure 60: Measured conversion gain as a function of RF input frequency for (a) RF Channelizer configured to receive Channel 3, (b) RF Channelizer configured to receive Channel 5, (c) RF Channelizer configured to receive Channel 6 and (d) RF Channelizer configured to receive Channel 6. These configurations have more than one mixer in the signal path.**

**Table 10: Comparison of State-of-Art RF Channelizers**

	[B1]	[B2]	[B5]	This work
Feature	Scanning, Two-stage conversion	7 parallel receivers	Cascaded image reject mixers	Semi- concurrent, fast- switching
Input BW [GHz]	0-6	3.1-10.6	1.75-8.75	0.6-9
Power [mW]	678 <sup>2</sup>	342 <sup>2</sup>	41	435
T <sub>hop</sub> [ $\mu$ s]	10	0.2 <sup>3</sup>	few ns <sup>4</sup>	0.008-0.92
Concurrent O/Ps	1	7	1	3
No. of LO sources	2	7	1	1
IIP3 [dBm]	10	-5/-9	Not available	-3.4/-19.9
NF [dB]	Not available	2.5/14	Not available	6.8/22.6
Signal Leakage [dB]	Not applicable	36-70	11-37	11-63
Technology	130nm	130nm	130nm	65nm
Area [mmxmm]	3.7x3.9	1.3x2.7	0.8x1.1	1x2

<sup>2</sup> Includes PLL power. <sup>3</sup> Estimated settling time using  $\frac{1}{PLL \cdot BW}$ . <sup>4</sup> Data not available, estimate made from figures.

channels and BPSK modulation, the RF channelizer has been demonstrated to support 400Mbps data rate. By using more concurrent channels and complex modulation schemes, multi-Gbps data rate can be supported.

# 8 Switched-Capacitor RF Filtering for RF Channelizers

## 8.1 Introduction

From the results presented in earlier sections in this report on RF channelization, it is clear that a key challenge is the realization of on-chip band-select filters. In this section we report on our work on demonstrating how to use switched-capacitor techniques to implement those filters.

For the conventional filter implementation, the LC filter needs large inductors and has small tuning range, the active RC filter cannot work at high center frequency due to finite GBW of the opamp, and the Gm-C filter has the poor linearity drawback. The switched-capacitor technique can implement high center frequency bandpass filter [B18], and it also can implement integrated complex-bandpass filter in super-heterodyne receivers [B19]. The switched-capacitor techniques have an advantage in process scalability, since with new process the switches can be faster, and the LO generator circuits can be faster and consume less power. The passive switched-capacitor circuit is very linear, the linearity of the filter is only limited by the Gms. We report on an RF front end with embedded bandpass filtering. It consists of switches, capacitors and Gms.

## 8.2 Basic concept

In a conventional RF front end (Fig. 61(a)), the passive off-chip RF band-select filter rejects the OB blockers, the active LNA provides impedance matching and signal amplification, and after down-conversion, active high-order lowpass filtering needs to be implemented to further attenuate OB signals. In the SC front end presented here (Fig. 61(b)), impedance matching, blocker rejection, down-conversion and high-order filtering are performed with passive SC circuits. The switches are driven by an 8-phase non-overlapping clock signal  $p(i)$ . Capacitors  $C_{h1}(i)$  with the  $s_0(i)$  switches in all 8 banks realize an RF N-path bandpass filter. The RF signal is sampled and down-converted to capacitors  $C_s(i)$ . The impedance matching is achieved by dumping the charges on  $C_s(i)$  with switches  $s_6(i)$ . After sampling, history capacitors  $C_{h2}(i)$ - $C_{h4}(i)$  and the relevant switches realize a high order DT IIR filter [B19]. Switches  $s_5(i)$  propagate the signal from the  $C_s(i)$  to the next stage. The subsequent low-noise active Gm-TIA circuits amplify the signals and combine them for harmonic rejection [B20].

The SC front end achieves different circuit functions in sequential time intervals as shown in Fig. 61(c). bank #1, the RF signal is sampled from node  $v_{in}$  to  $v_s$  in sampling phase  $p_1$ , propagated to next stage in output phase  $p_5$ , and dumped from  $C_s$  in  $p_7$ . From  $p_2$  to  $p_4$ , the signal is filtered at node  $v_s$  with increasing order. The blank time intervals relax the timing constraints. The 8 banks operate in a time-interleaved fashion.

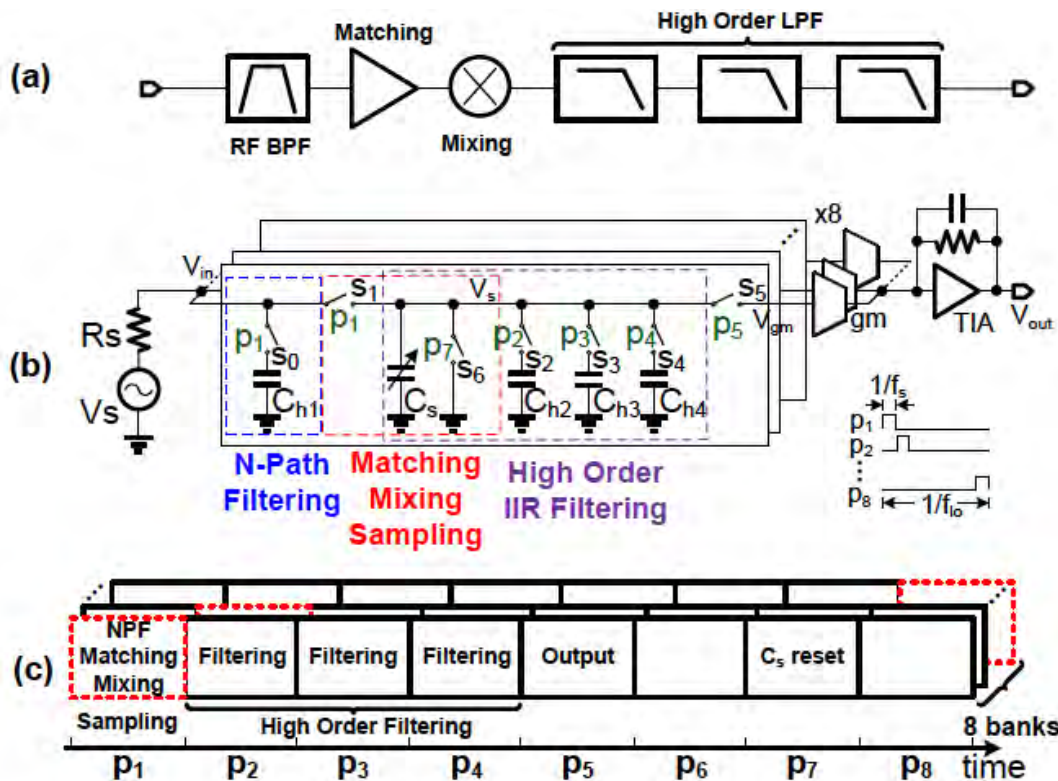


Figure 61: (a) Conventional RF front end architecture; (b) Proposed switched-capacitor (SC) RF front end (single-ended circuits and only one path is shown for simplicity); (c) Operation of the RF SC front end.

### 8.3 Switched-Capacitor RF Front-End with Filtering Implementation

The architecture of the RF front end is shown in Fig. 62(a). It is composed of the SC circuits, baseband Gm cells and a clock generator. When using a fully differential architecture, two  $C_s$ s with opposite phases can share the same  $C_h$  which eliminates the even-order LO harmonic down-conversion; two banks in Fig. 61(a) are merged into one bank in Fig. 62(a); as a result we need 8 capacitors for  $C_s$  and 4 capacitors for each  $C_h$ . The switches are implemented with CMOS transmission gates. The NMOS and PMOS are sized equally to reduce the charge injection and clock feedthrough. Compared to an NMOS switch, CMOS switches can tolerate larger blockers. The  $R_{on}$  of the sampling switches  $s_1$  and the output switches  $s_5$  is  $14\Omega$ , while the other switches are sized for  $20\Omega$ . The  $C_s$  is implemented with a MoM capacitor bank with switches to ground. The  $C_s$  tuning range is 1-16pF with a 1pF/step. All the  $C_h$ s are the same with an effective single-ended 50pF capacitance and are realized with differential MoM capacitors and MOS capacitors to ground.

The clock divider generates the 8-phase non-overlapping clock and drives the switch drivers. The switch drivers for the switches in the IIR filter can be turned off to lower the filter order and save power. The switch drivers are DC coupled to the switches. Since the  $V_{cm}$  of the front end is 0.8V, the VDD and VSS of the clock generator are 1.4V and 0.2V respectively to make sure  $V_{cm}=(VDD-VSS)/2$  and to limit the rail-to-rail voltage to 1.2V.

The Gm cells combine the 4-phase output signals from the SC circuits and are realized by simple CMOS inverters with tail current (Fig. 62(a)) operating from a 1.6V supply. The Gm input-

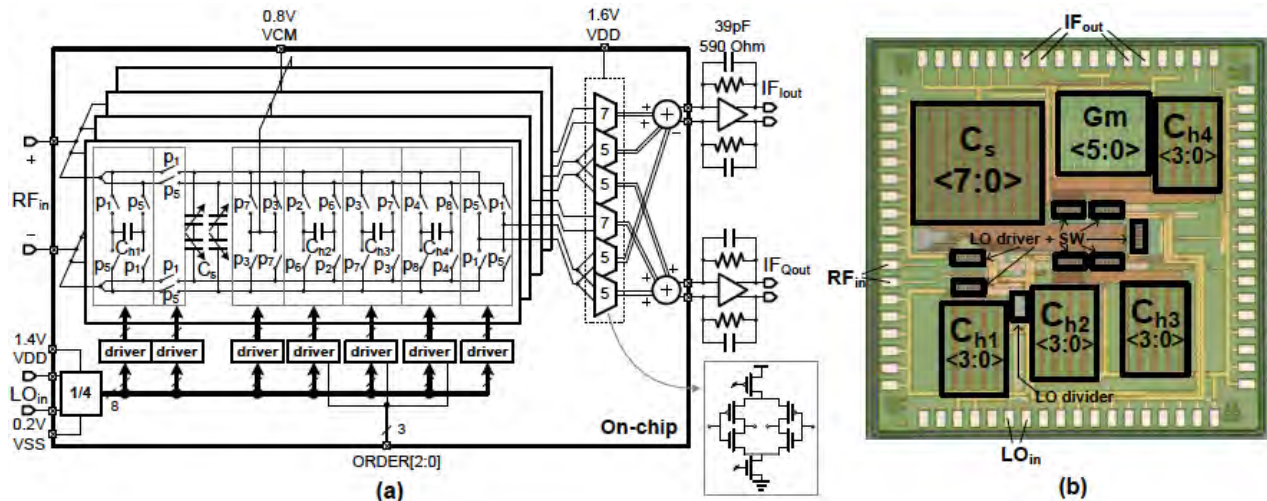


Figure 62: (a) Architecture of the switched-capacitor RF front end; (b) Chip photo.

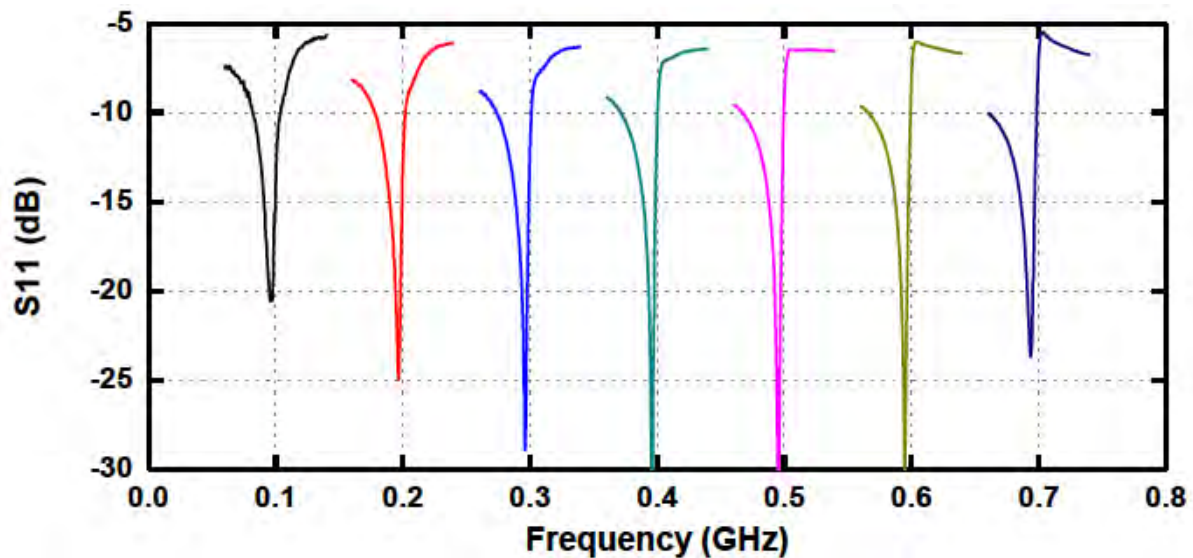


Figure 63: Measured differential-mode S11 for LO frequencies from 0.1 to 0.7GHz with a 0.1GHz step.

common-mode voltage is set by  $V_{cm}$  in the reset phase. Common-mode feedback circuits set the output common-mode voltage to 0.8V. The harmonic recombination transconductor architecture eliminates the harmonic down-conversion from third and fifth LO harmonics. The 5:7 size ratio is used to approximate  $1 : \sqrt{2}$ . Dummy Gms are used to balance the load of previous stage. The transconductance of the size-5 Gm cell is 40mS. Each Gm cell can be tuned with a 9-bit control code to calibrate harmonic rejection ratio (HRR) as in [B20].

## 8.4 Measurement Results

The chip prototype was fabricated in a 40nm LP CMOS process and the die size is  $1.8 \times 1.8 \text{mm}^2$  (Fig. 62(b)). The chip area is dominated by MoM capacitors. In this prototype the MoM capacitor has only 4 metal layers. The availability of more metal layers or higher capacitance density would directly reduce the chip size. In the measurements, an off-chip  $180^\circ$  hybrid drives the differential

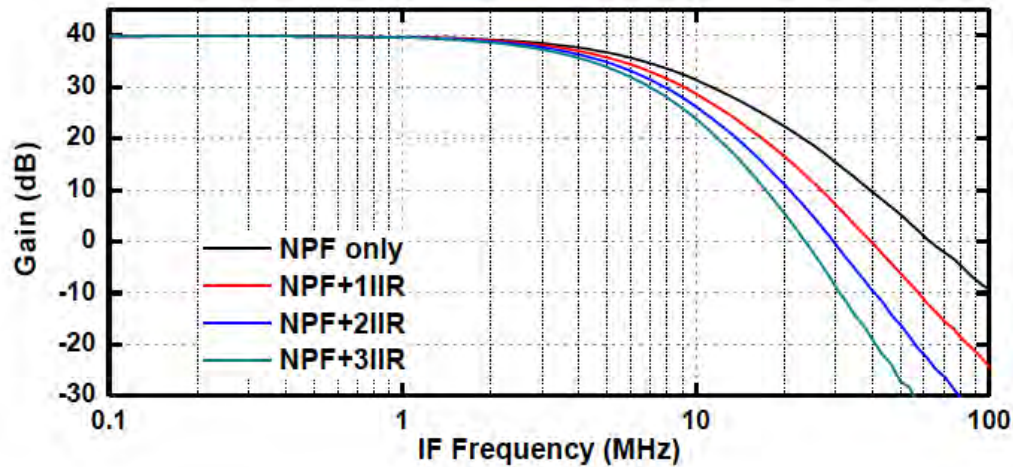


Figure 64: Measured conversion gain of different filter orders for an LO frequency of 0.2GHz.

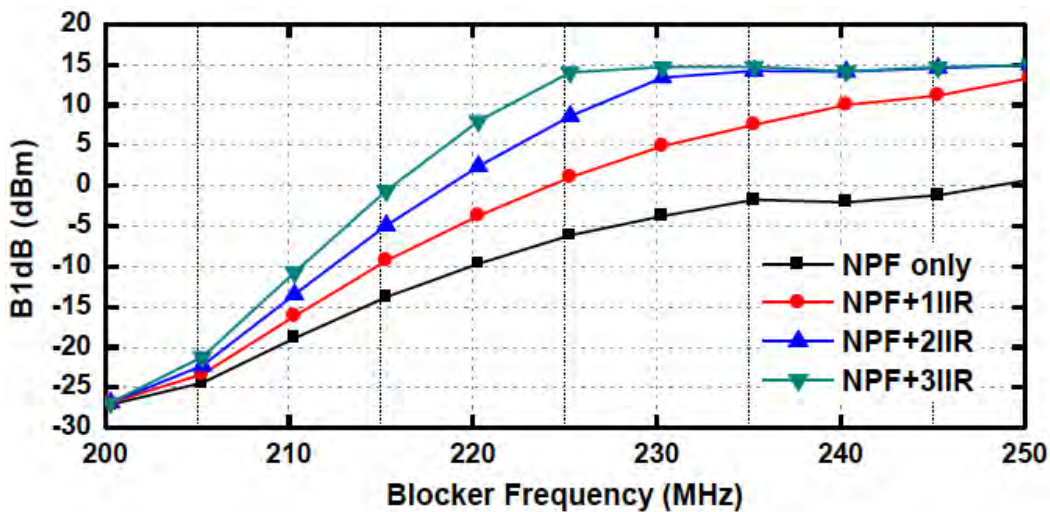


Figure 65: Measured blocker 1dB compression point versus blocker frequency for an LO frequency of 0.2GHz.

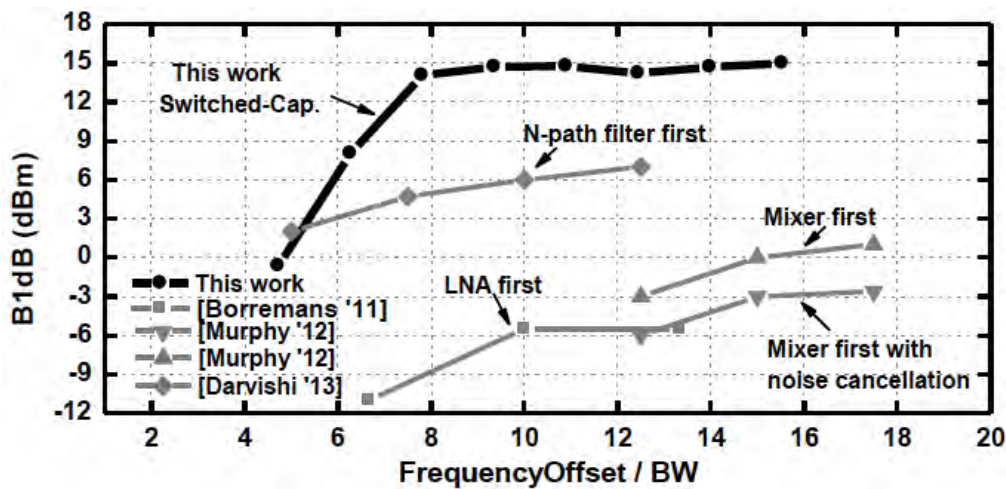


Figure 66: Comparison of the B1dB versus relative blocker frequency offset with other blocker tolerant RF front ends.

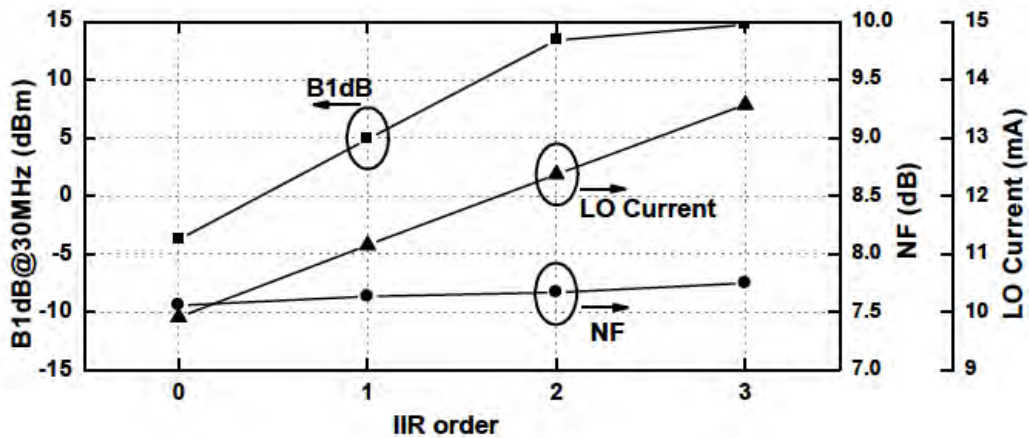


Figure 67: Measured B1dB@30MHz frequency offset, noise figure, LO current consumption versus filter order for an LO frequency of 0.2GHz.

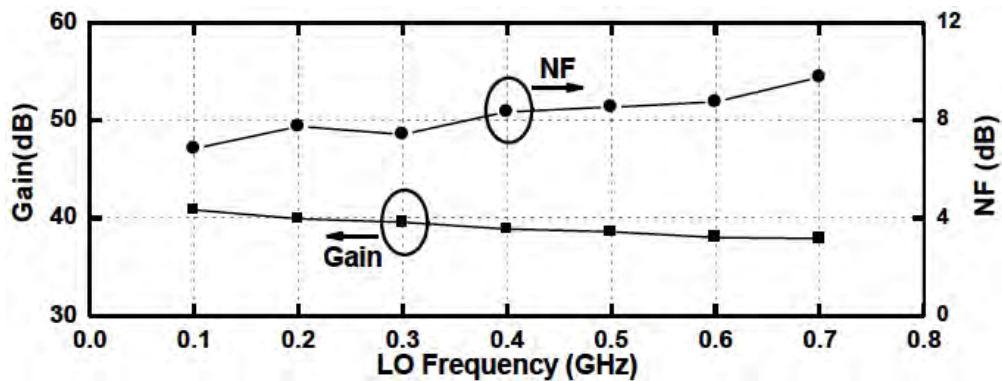


Figure 68: Measured conversion gain and noise figure versus LO frequency.

RF inputs and the hybrid loss was calibrated out. The differential S11s for LOs from 0.1 to 0.7GHz (Fig. 63) are calculated from the measured 2-port S parameters of differential RF inputs, and the shape doesn't change with the order of IIR filter; the front end matches to 50Ω in band (around the LO frequency) while OB the S11 is higher due to the low OB NPF impedance. The slight deviation of the S11 notch and the LO frequency is caused by parasitic capacitances at the RF input. Measured LO leakage to the RF input is lower than -60dBm across LO frequencies.

The conversion gain from the RF input to TIA output with different filter orders is measured for an LO frequency of 0.2GHz in Fig. 64. The roll-off increases with higher filter order. The bandwidth changes from 4.8 to 3.2MHz when the filter order increases. In Fig. 65 the B1dB versus blocker offset frequency is measured for a 0.2GHz LO frequency and an in-band signal of 201MHz. The blocker tolerance increases with filter order. With a third order IIR filter the B1dB is as high as 14.7dBm at a 30MHz frequency offset. The OB-IIP3 with 3rd-order IIR filtering is 24dBm with an LO frequency of 0.2GHz and the two tones at 0.231 and 0.261GHz.

The B1dB versus relative blocker frequency offset is compared with other blocker tolerant RF front ends [B21][B22][B18] in Fig. 66. To normalize the comparison (frequency offset)/BW is used as the x-axis. For [B18] the bandwidth of a single sideband is used since it is a RF bandpass filter. With third order filtering, this work achieves a higher maximum B1dB while the slope is also larger than other work thanks to the high order filtering.

**Table 11: Comparison with the state of the art**

	<b>This work</b>	Borremans JSSC '11	Andrews JSSC '10	Murphy JSSC '12	Darvishi JSSC '13
Technology	40nm	40nm	65nm	40nm	65nm
Type	Switched-Cap.	LNA+NPF	Mixer first	FTNC	NPF
Filter order before active circuits	<b>1-4</b>	0	1	1	1
Frequency range (GHz)	0.1-0.7	0.4-6	0.1-2.4	0.08-2.7	0.1-1.2
Gain (dB)	40	70	70	72	25
BW (MHz)	3.2-4.8	0.4-30	<20	2	4 <sup>2</sup>
NF (dB)	6.8-9.7	3-7	3-5	1.5-2.4 <sup>1</sup> , 3.5-5	2.8
OB-IIP3 (dBm)	24@30MHz	10	25 @20MHz	13@20MHz <sup>1</sup> 17@20MHz	26 @50MHz
Max. B1dB (dBm)	<b>15</b>	<-5	<6	<0 <sup>1</sup> , <5	7
HR3/5 (dB)	>38/>35 >66/>73 (cal.)	NR	35.5/42.6	>42/>45	NA
Power (mW)	Ana : 51(32.5mA) LO: 7-53(6-44mA)	30-55	30-70	35-78	18-57.4

**8.4.1** with noise cancellation 2. single sideband

Fig. 67 shows the B1dB at a 30MHz frequency offset, the noise figure and the LO current consumption for different IIR filter orders. With higher order filtering, the B1dB is improved but with a higher LO current, while the noise figure only increases by 0.2dB.

The gain and noise figure versus LO frequency are shown in Fig. 68. The gain is 41dB at 0.1GHz and 38dB at 0.7GHz. The noise figure of the whole front end is 6.8dB at 0.1GHz and increases to 9.7dB at 0.7GHz.

## 8.5 Comparison to State of the Art

The performance summary and comparison with the state of the art is shown in Table. 11. This work has higher order filtering before active circuits and achieves the highest B1dB. The OB-IIP3 is as high as other work since the high order filtering improves the large blocker tolerance more than the small-signal non-linearity. The calibrated HR3 and HR5 are better than 66dB and 73dB respectively, but they cannot be achieved with same calibration code as explained in [B20].

## 9 RF “Instantaneous-Hop” PLL

### 9.1 Introduction

Fast-hopping frequency synthesizers are useful in several applications. As mentioned earlier, a fast-hopping synthesizer enables rapid and energy-efficient spectrum analysis in emerging cognitive radios [B23], and are particularly useful in the context of the iterative downconversion RF channelizer described earlier. Military receivers employ fast frequency-hopping as an electronic protection against jammers [B24]. Multiband orthogonal frequency division multiplexing (MB-OFDM) communication systems have been proposed for high data-rate wireless communication in the 3-10GHz ultra-wide-band(UWB) spectrum[B25]. OFDM and fast frequency hopping together provide interference immunity, reduced multi-path fading and multiple access.

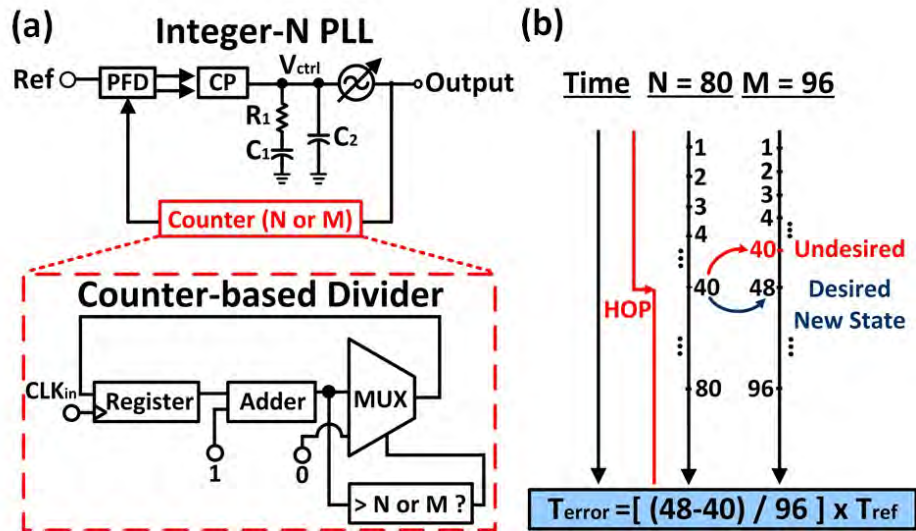
Conventional phase-locked-loop (PLL) based frequency synthesizers trade-off loop bandwidth, settling time, noise, spurs and frequency resolution [B26]. Prior works seek to expedite the locking process of the PLL. The works in [B27], [B28], [B29] effectively vary bandwidth, mode, and type of PLL respectively between transient locking and steady-state operation to mitigate the bandwidth versus settling time trade-off in type-II integer-N PLLs. [B30] utilizes a pre-determined look-up table (LUT) to preset the digital control word (DCW) of the VCO in the PLL. This reduces the initial VCO frequency error, but the potentially harmful initial phase error induced by the divider is not addressed.

We propose a PLL where initial frequency and phase error at the hop instant are eliminated through digitally-intensive initial-condition control. This eliminates acquisition and enables “instantaneous hops” to within a frequency error limited only by the DCW resolution.

### 9.2 Zero-Initial-Phase-Error Multi-Modulus Divider

The conventional integer-N charge-pump PLL (shown in Fig. 69(a)) is a nonlinear dynamical feedback system characterized by its state variables. Specifying the values of all state variables completely defines the system’s state. An LC-VCO based charge-pump PLL is a mixed-mode system whose state variables include inductor current and capacitor voltage in the VCO, the control voltage across the loop filter’s capacitor, and the state of the digital divider (which is essentially a digital finite-state-machine (FSM) counter). Initial conditions are critical in the transient response of such systems. *We propose the assignment of initial conditions to each state variable in the system at the hop instant through extensive digital control and calibration to essentially hop to a locked state.*

The digital divider is essentially a counter with a programmable terminal count. Fig. 69(b) shows the transient behavior of a conventional binary-sequence counter-based divider at the frequency hop instant. If the terminal count is set to either  $M = 80$  or  $N = 96$  at the hop instant, the counter induces an initial phase error to the reference signal if its original state (count 40 here) is maintained. Typical multi-modulus dividers use pulse-swallow counters or cascaded divide-by-2/3 structures, which have their own state-machine descriptions and so, initial-phase-error mechanisms. These initial phase errors can be eliminated by reconfiguring the state of the FSM at the hop instant.



**Figure 69: (a) PLL with a binary-sequence counter-based divider. (b) Mechanism of initial phase error in the counter-based divider.**

To implement a divider with initial-state control, two aspects must be addressed. First, as in Fig. 70, assuming the divider chain has multi-modulus and fixed-ratio dividers, one aspect is if the multi-modulus divider should be at the input or at the output of the divider chain. If zero initial phase error is achieved, this means that after reconfiguration of the divider modulus at the hop instant, the divider output is unchanged and perfectly aligned to the reference. Placing the multi-modulus divider at the front of the chain implies no initial-state control is necessary in the fixed ratio dividers that follow (Fig. 70(a)), easing the digital control that is exercised at the hop instant. A second aspect is if the front-side multi-modulus divider should be synchronous or asynchronous. Asynchronous dividers are generally used as reduction in clock frequency down the chain reduces dynamic power consumption. In such chains the sub-dividers at different clock frequencies are mutually skewed due to divider delays. This makes initial-state control and even defining a state fundamentally problematic. Thus, to enable instantaneous hops, the multi-modulus divider must be synchronous at the cost of slightly higher power consumption. The following fixed-ratio divider can be asynchronous.

With these considerations, we propose a zero-initial-phase-error divider shown in Fig. 71 with a synchronous divide-by-20/22/24 Johnson-counter divider followed by asynchronous flip-flop-based divide-by-2 dividers. The multi-modulus nature of the Johnson-counter dividers is from the 3-1 multiplexer (MUX) that controls feedback. As shown in Fig. 72, in the absence of state reconfiguration at the hop instant, the initial phase error accumulates throughout the period of the synchronous divider output and resets to zero at each rising/falling edge. Thus, if the hop instant is synchronized with the rising edge of the synchronous divider output, initial phase error is eliminated without extensive digital controls. The delay induced by this synchronization will be less than one period of synchronous divider output ( $\sim 4.7\text{ns}$  in this prototype).

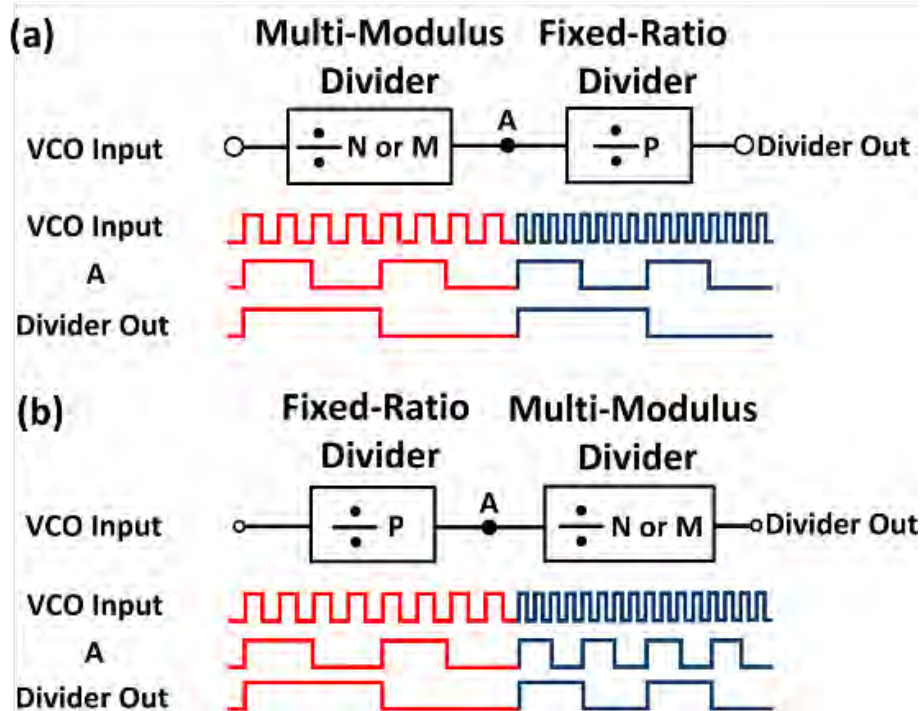


Figure 70: (a) Multi-modulus divider first: no initial state control is necessary in the fixed-ratio divider that follows. (b) Fixed-ratio divider first: initial state control is required throughout the chain.

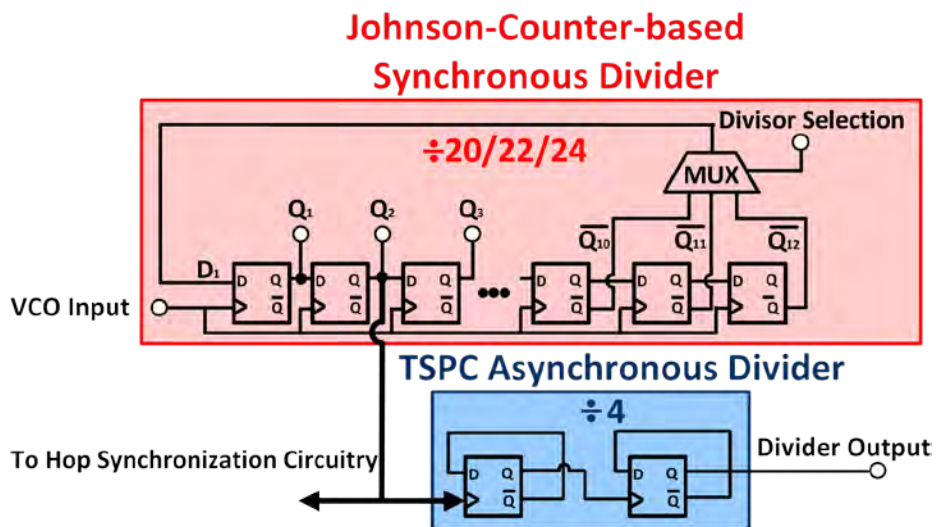


Figure 71: Proposed zero-initial-phase-error divider structure.

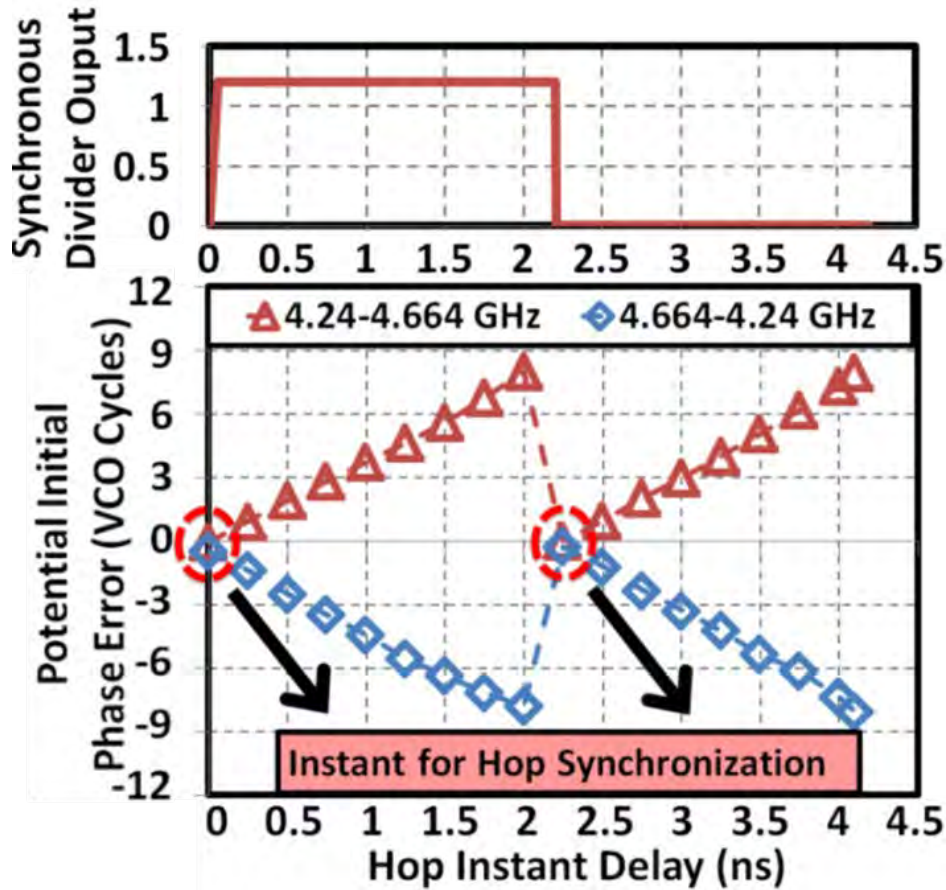


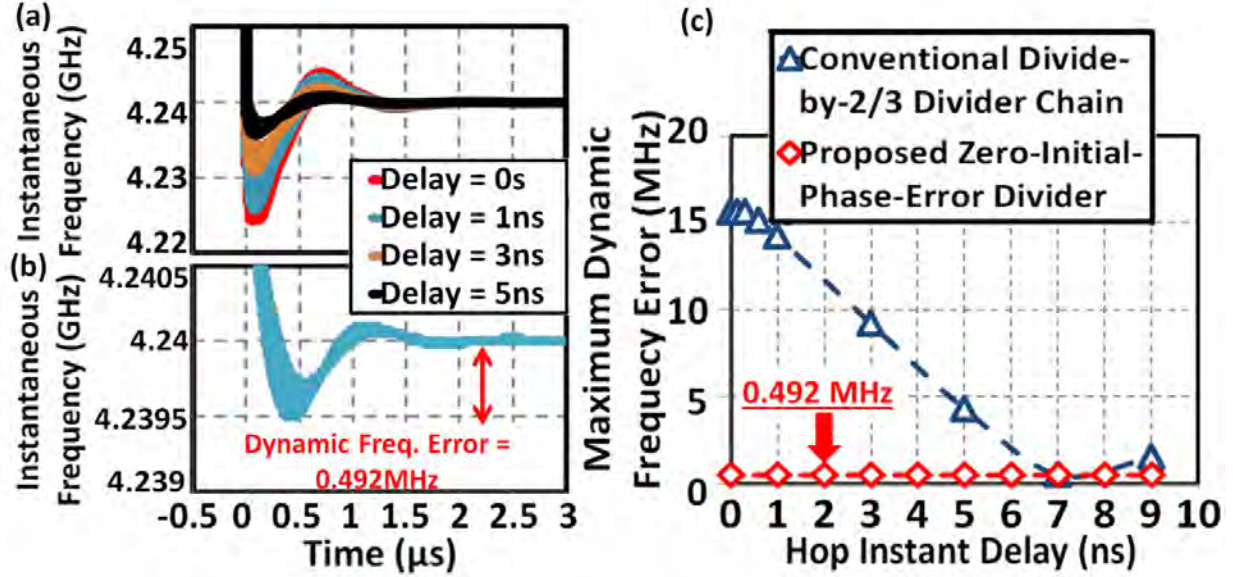
Figure 72: Potential initial phase error in the proposed divider structure for upward and downward hops.

### 9.34.0-5.84 GHz Instantaneous-Hop PLL

A type-II third-order charge-pump PLL (Fig. 73) forms the core of the proposed synthesizer. The PLL has an LC-VCO operating over 4.0-5.84 GHz which is tuned with an accumulation-mode varactor and a high-resolution 9-bit DCW (Fig. 75), and the programmable 80/88/96 divider chain described earlier (Fig. 71). A 53 MHz off-chip crystal oscillator enables locking of the PLL to 4.24, 4.664 and 5.088 GHz with division ratios of 80, 88 and 96 respectively. A conventional tri-state phase-frequency detector (PFD) and passive loop filter are integrated on chip. The loop parameters are designed for a bandwidth of 800 kHz and phase margin of  $45^\circ$ . Loop filter capacitor  $C_1$ ,  $C_2$  are 35 and 5 pF respectively,  $R_1$  is 6k $\Omega$ .

As described earlier, for zero initial phase error, the hop instant must be synchronized with the rising edge of the synchronous divider output. In addition to state variables, the charge pump current is also reprogrammed at the hop instant to maintain constant loop bandwidth due to varying  $K_{VCO}$  gain. Note that the charge pump current is not a PLL state variable and does not contribute to initial condition errors. In this prototype, an on-chip state register stores the DCW of 9-bit VCO, divider ratio control and charge pump current control. A second on-chip memory with a serial interface (SPI) stores the settings for the different frequencies between which the PLL hops (limited to two in this prototype). The externally-applied hop signal clocks a flip-flop that registers





**Figure 74: Instantaneous frequency versus time for different hop instants in (a) a conventional PLL using divide-by-2/3 asynchronous dividers, (b) proposed instantaneous-hop PLL. (c) Maximum dynamic frequency error versus hop instant in both cases.**

PFD is modeled in Verilog-AMS while charge-pump is at the transistor-level. Fig. 74 shows the simulated settling behavior for a hop from 4.664 to 4.24 GHz. Frequency pre-setting is done in both cases while the external hop signal is varied in time over one reference cycle. The proposed divider eliminates initial phase error, and thus minimizes  $V_{ctrl}$  overshoots and dynamic phase error by 1-2 orders of magnitude during settling.

## 9.4 Measurement Results

A 65nm CMOS prototype was fabricated with  $0.95 \text{ mm}^2$  chip-area (Fig. 75(b)). It draws 14 mA current from a 1.2V supply. The measured tuning range of the VCO is 4.0-5.84 GHz. Fig. 76(a)-(d) shows the VCO's frequency,  $K_{VCO}$ , frequency-difference between two successive DCW values at mid- $V_{ctrl}$  (0.6V), and single-band frequency tuning range across all DCW. With these, a DCW for any desired output frequency placing the required  $V_{ctrl}$  near mid-VDD with residual initial frequency error less than 3.64 MHz on an average can be found.

Fig. 77 shows the hopping behavior. To monitor hopping, the  $V_{ctrl}$  node is noted with a unity-gain buffer. The PLL output is also quadrature-downconverted and captured on an oscilloscope to determine the instantaneous frequency. Fig. 77(a) shows  $V_{ctrl}$  in a hop from 4.664 to 4.24 GHz as divider ratio changes from 88 to 80. The PLL settles within  $4\mu\text{s}$  with minimum overshoot. Fig. 77(b) shows the instantaneous frequency during this period. The dynamic frequency error never exceeds 850 kHz. Fig. 77(c) shows  $V_{ctrl}$  in a hop from 4.136 to 4.512 GHz with divider ratio programmed from 88 to 96. Fig. 77(d) shows  $V_{ctrl}$  in a hop between 4.24 and 4.644 GHz. In all cases, a very small dynamic frequency error is maintained.

Measured phase noise for 4.24, 4.664 and 5.088 GHz carriers at 1MHz-offset are -115.2, -114.4 and -112.1 dBc/Hz respectively.

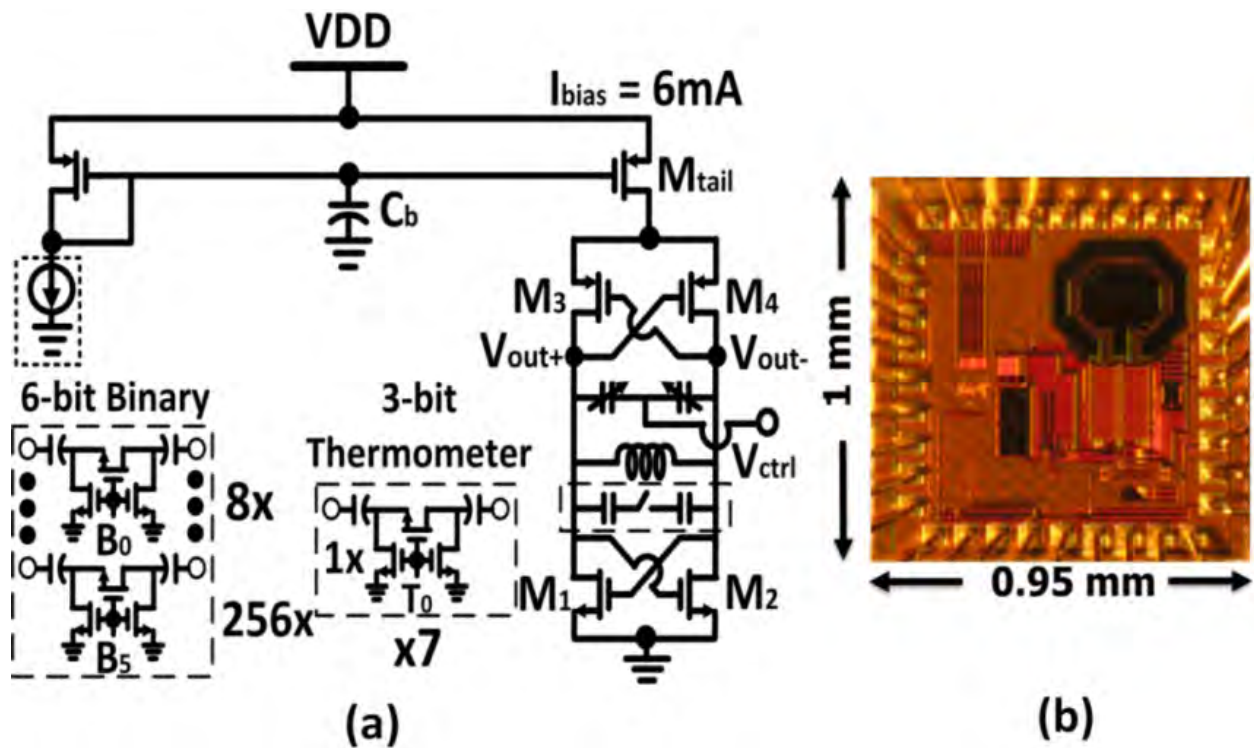


Figure 75: (a) 4.0-5.84 GHz 9-bit digitally-controlled LC-VCO with analog varactor tuning. (b) Chip microphotograph.

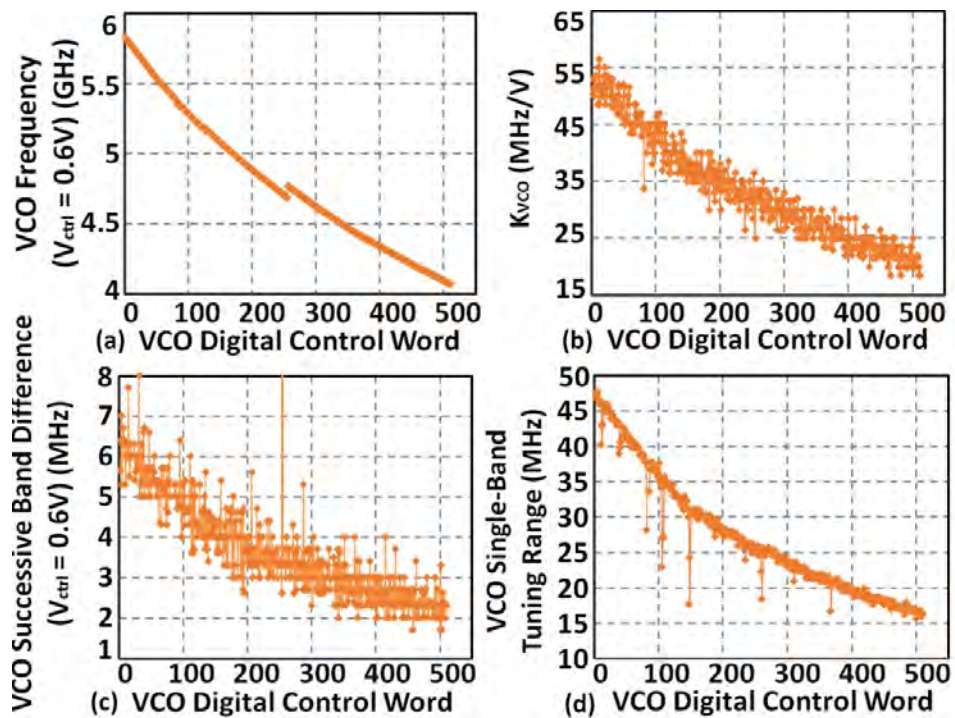


Figure 76: Measured 4.0-5.84 GHz 9-bit LC-VCO performance at  $V_{ctrl} = 0.6\text{ V}$  versus DCW: (a) frequency (b)  $K_{VCO}$  (c) frequency difference between two successive DCW (d) single-band frequency coverage as  $V_{ctrl}$  is varied from 0-1.2V.

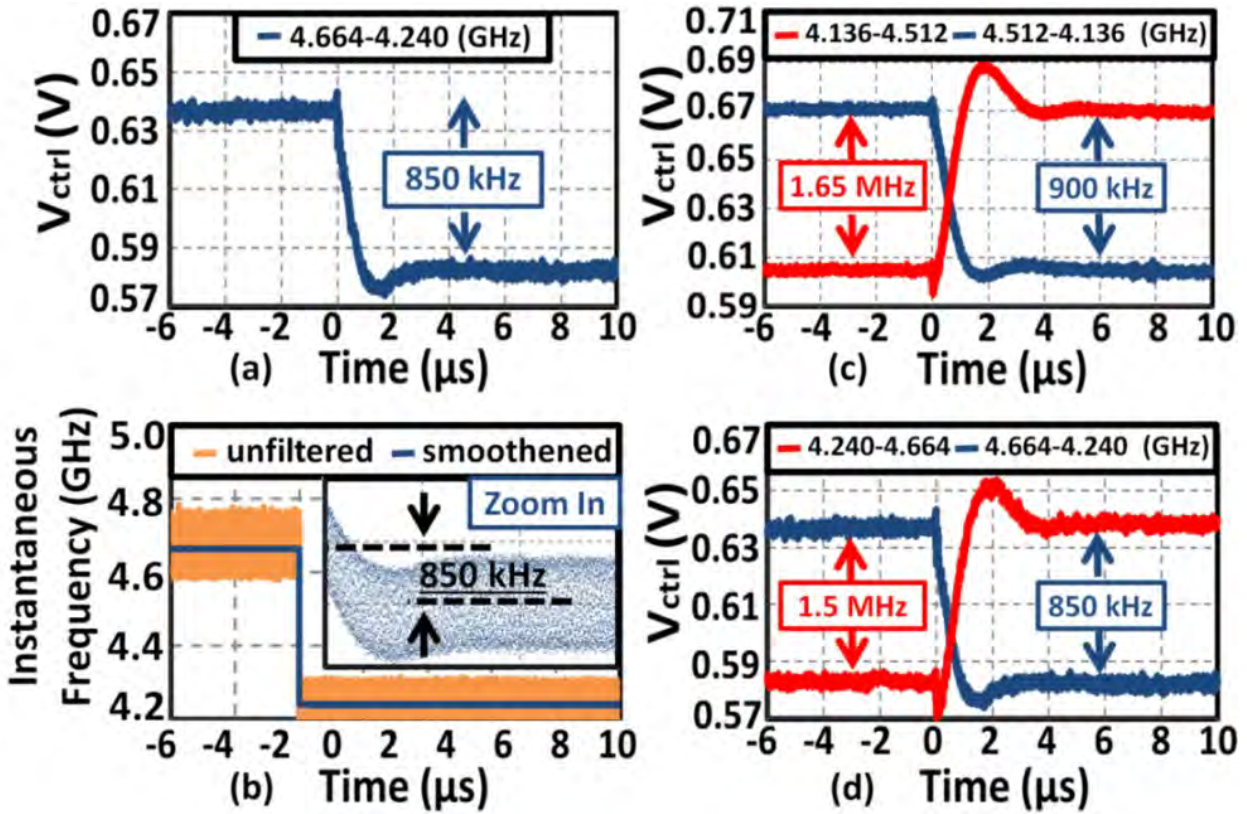


Figure 77: Measured (a) control voltage and (b) instantaneous output frequency for a hop from 4.644 GHz to 4.24 GHz showing a maximum dynamic frequency error of 850 kHz. Measured control voltage for upward and downward hops (maximum upward/downward dynamic frequency error) between (c) 4.136 GHz and 4.512 GHz (1.65MHz, 900kHz) (d) 4.24 GHz and 4.644 GHz (1.5MHz, 850kHz). The 4.664 to 4.24 GHz downward hop is a repeat of (a).

## 9.5 Conclusion

An instantaneous-hop frequency synthesizer based on a zero-initial-phase-error multi-modulus divider that breaks the fundamental trade-off between hopping time, spectral purity and frequency resolution is shown. Topics for future research include techniques to achieve instantaneous-hop functionality within multi-modulus dividers with a wide programmable modulus range and the combination of the proposed techniques with existing techniques that expedite the locking process by varying the bandwidth, mode, and type of PLL in the transient locking period.

## 10 Publications

- [1] W.-G. Ho, T. Forbes, and R. Gharpurey, “A low-power two-stage harmonic rejection quadrature mixer employing bias-current reuse,” in *IEEE 58th Int. Midwest Symposium on Circuits and Systems*, 2015, Accepted for Publication.
- [2] T. Forbes, W.-G. Ho, and R. Gharpurey, “Design and analysis of harmonic rejection mixers with programmable LO frequency,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2363–2374, Oct. 2013.
- [3] W.-G. Ho, V. Singh, T. Forbes, and R. Gharpurey, “An active interference canceler with reduced harmonic response and synthesizer tuning range,” in *IEEE Radio Frequency Integrated Circuits Symp.*, 2015, accepted for Publication.
- [4] W.-G. Ho, T. Forbes, V. Singh, and R. Gharpurey, “An active interference cancellation technique with harmonic rejection for a broadband channelizer,” in *IEEE 56th International Midwest Symposium on Circuits and Systems*, Aug. 2013.
- [5] V. Singh, T. Forbes, W.-G. Ho, J. Ko, and R. Gharpurey, “A 16-band channelizer employing harmonic rejection mixers with enhanced image rejection,” in *IEEE Custom Integrated Circuits Conference (CICC)*, 2014, accepted for publication.
- [6] T. Forbes and R. Gharpurey, “A 2 GS/s frequency-folded ADC-based broadband sampling receiver,” *IEEE Journal of Solid-State Circuits*, vol. 49, no. 9, pp. 1971–1983, 2014.
- [7] J. Zhu, H. Krishnaswamy, and P. Kinget, “A DC-9.5GHz Noise-Canceling Distributed LNA in 65nm CMOS,” *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2013.
- [8] T. Yang, K. Tripurari, H. Krishnaswamy and P. R. Kinget, “A 0.5GHz-1.5GHz Order Scalable Harmonic Rejection Mixer,” *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2013.
- [9] Y. Xu, J. Zhu, and P.R. Kinget, “A Blocker-Tolerant RF Front End with Harmonic-Rejecting N-Path Filtering,” *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2014.
- [10] H. Krishnaswamy, K. Tripurari, Y. Xu, L. Zhang, D. Gidony, B. Jovanovic, and P. R. Kinget, “RF Channelizer Architectures using Iterative Downconversion for Concurrent or Fast-Switching Spectrum Analysis,” **invited talk**, *International Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2014.
- [11] L. Zhang, Y. Xu, K. Tripurari, P. R. Kinget, H. Krishnaswamy, “Analysis and Design of a 0.6-10.5GHz LNTA for Wideband Receivers,” *IEEE Transactions on Circuits and Systems II*, 2014
- [12] Y. Xu and P. R. Kinget, “A Switched-Capacitor RF Front End with Embedded Programmable High Order Filtering and a +15dBm OB-B1dB,” *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2015. **Best Student Paper Award – Second Place.**

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## 12 Symbols, Abbreviations and Acronyms

<b>Acronym</b>	<b>Description</b>
ADC	Analog to Digital Converter
AFRL	Air Force Research Laboratory
BB-CG	Base Band Common Gate
B1dB	1-dB Blocker Induced Gain Compression Point
CML	Current Mode Logic
CMOS	Complimentary Metal-Oxide Semiconductor
DC	Direct Current
DSB NF	Double Side Band Noise Frequency
HRM	Harmonic Rejection Mixer
IC	Integrated Circuit
IDC	Iterative Down Converter
IF	Intermediate Frequency
IIR	Infinite Impulse Response
I/Q	In-Phase/Quadrature Components
LC	Inductor Capacitor Circuit
LNA	Low-noise Amplifier
LNTA	Low-noise Transconductance Amplifier
LO	Local Oscillator
MoM	Moment of Method
MUX	Multiplexer
NF	Noise Figure
NMOS	Negative Metal-Oxide Semiconductor
OFDM	Orthogonal Frequency Domain Multiplexing
P1dB	1-dB Gain Compression Point
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PLL	Phase-locked Loop
PMOS	Positive Metal-Oxide Semiconductor
RF	Radio Frequency
SFDR	Spurious Free Dynamic Range
TIA	Trans-Impedance Amplifier
TQFP	Thin Quad Flap Pack
TSPC	To-hop Synchronization Circuitry
UT	University of Texas