

CHARACTERIZATION AND PHYSICS-BASED MODELING OF ELECTROCHEMICAL MEMRISTORS

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14. ABSTRACT We have developed and validated models device- and circuit-level models that describe the underlying physics governing the electrical behavior of electrochemical memristors (PMCs). Devices are modeled through numerical solutions to equations that capture charge transport and reaction properties in solid state electrolyte materials. Numerical simulations enable a physics-based characterization of the dynamics of filament formation and dissolution in ion conducting films that result from electrical or optical stress. Model parameters and electrical characteristics were obtained from and validated with experiments on test structures designed and fabricated during the program. Circuit applications that use memristors in a conventional integrated circuit framework have been designed and simulated with derived compact models. The program has led to significant advances in our understanding of the physics of memristor operation, expanded our understanding of the application space for the technology, and supported the identification of potential radiation threats, of which there seem to be few except for some single event effect susceptibility.					
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1 SUMMARY

This two year program will focus on developing and validating models that describe the underlying physics governing the electrical behavior of electrochemical memristors. Analytical models capturing charge transport and ion reaction properties in solid state electrolyte materials used for these devices will be developed and implemented in finite element, i.e., TCAD, solvers. Numerical simulations will enable a physics-based characterization of the dynamics of filament formation and dissolution in ion conducting films. Model parameters and electrical characteristics will be obtained from and validated with experiments on test structures designed and fabricated during the program. The project will lead to significant advances in our understanding of the physics of electrochemical memristor operation, support the identification of potential radiation threats and strategies for improving radiation hardness, and quantify the impact of thermal stress on these technologies.

In this program, the mechanisms of Ag transport and reactions have been experimentally characterized and modeled using device and circuits simulation. Over the past two years the key questions we have addressed are:

1. What is the nature of bulk glass and the metal-glass interface and how is active metal incorporated?
2. How is charge transport modeled and to what extent can standard flux-based functions such as drift-diffusion, Poisson, and continuity be used to describe memristor operation?
3. What is the physics of metallic filament formation and dissolution?
4. How does radiation and temperature impact the operation of ChG-based memristors?

By addressing these questions, we have advanced our understanding of the physics of resistive switching. An experimental effort for the program is conducted to verify theoretical calculations and to articulate new physics. The program has been divided into five tasks. In the first task we successfully designed and fabricated several types of test structures (lateral and vertical chalcogenide and vertical silicon-dioxide devices). These devices were tested extensively in the second task to characterize material parameters, operation in static and dynamic modes, and radiation effects. The results of the experiments were used to validate numerical finite element models for the third program task. With the use of numerical simulation, the processes of oxidation, auto-ionization, field-induced ion transport, electro-deposition, and ion trapping were accurately modeled for the first time. The modeled characteristics included electrical behaviors and optically stimulated processes. In the fourth task the results of the numerical modeling effort on devices and experimental data were also used to develop the first comprehensive compact model for chalcogenide and SiO₂ electrochemical devices. The compact model was exercised in both digital and neuromorphic design as well in this fourth task. In the fifth task, the devices' response to cumulative total ionizing dose damage and transient single event radiation effect were modeled and experimentally characterized. The results showed that the technology is highly tolerant to the effect of all forms of ionizing radiation.

The program has led to significant advances in our understanding of the physics of electrochemical memristor operation, expanded our understanding of the application space for the technology, and supported the identification of potential radiation threats..

2 INTRODUCTION

Subject - Silver-based electrochemical memories show enormous potential for applications in non-volatile memory, as well as in more challenging, mixed signal applications, including neuromorphic computing. These devices are fabricated with thin films of chalcogenide glass (ChG) ion conductors sandwiched between active and inert metallic electrodes. Through a combination of reduction/oxidation (ReOx) and silver ion (Ag^+) transport processes, conducting filaments in the ChG film may be grown or dissolved as a function of bias, thereby enabling resistive switching between the two terminals. While several groups have made significant strides in device development, and in process integration, to the point where this technology is approaching readiness in non-volatile memory applications, significant challenges remain to improve cell function, reliability, and cycling endurance, as well as to facilitate their practical use in analog applications. The central problem is the large variability, even within the same device, of operational parameters and programmed resistance.

A recent International Technology Roadmap for Semiconductors (ITRS) report has determined that memristive memory is one of the most promising new memory technologies due to its scalability, speed, pJ/bit switching energy, and retention, and has recommended that it receive increased research focus [1]. This technology has also generated considerable interest as a potential rad-hard non-volatile memory. Furthermore, high speed and endurance indicate that memristive memory can replace DRAM and possibly SRAM – eliminating a number of radiation sensitivity mechanisms. The combination of low power, high performance, and high density along with the potential for radiation hardness suggest electrochemical memristors are viable candidates for the next generation of memory technologies and are therefore of significance to industries developing robust non-volatile memory for space flight. These devices can also be utilized in memristive realizations of existing circuits with potentially dramatic reductions in power-delay product. This will be of great interest in commercial space systems with constrained power budgets. Moreover, the resistive switching property and seamless integration into the IC back-end-of-line metal stack suggests that ChG-based memristors may be adapted for FPGA, structured ASIC, and other reconfigurable architectures. Finally, in the long term, memristors are expected to play a central role in development of high-performance, neuromorphic applications in intelligent, survivable systems. The program's focus on technology modeling will accelerate the refinement of the ChG-based memristor technology, facilitate the development of accurate models for commercial space-based applications, and support the evaluation of technology readiness for robust system integration.

Purpose - To understand variabilities associated with the performance of electrochemical memristors, we need to understand and model: 1) the solid state characteristics of the ChG film and the metal-glass interface (e.g. band offsets and work functions); 2) charge transport and reaction properties in the ChG bulk and interfaces (e.g., metal diffusivities and charge carrier reaction rates); and 3) the physics of conducting filament formation and dissolution. While continued engineering approaches could lead to technological breakthroughs, we contend that this problem would be better solved with a balanced approach that includes model-based theory with experimental studies on both isolated materials, and device structures. We already know that memristive action in these electrochemical devices is a function of ChG stoichiometry and of transition metals doped into the glass. However, at present there are no physical models that

capture the process of resistive switching in a chemically specific way, and the experiments are controversial. We anticipate that the filament growth depends on the composition of the bottom electrode and properties of the glass film, but there is, to date, neither quantitative measurements nor detailed finite element simulations that capture this. In this program we have applied published results from molecular dynamics (MD) and first principles quantum mechanical defect studies [2] of the active device materials to build models that incorporate detailed physics and simulate how these devices work electrically, how they age, and how they respond in radiation and extreme temperature environments.

Scope – In this program, the mechanisms of Ag transport and reactions in ChG are modeled using device and circuit simulation. For the numerical simulations, the processes of oxidation, auto-ionization, field-induced ion transport, electro-deposition, and ion trapping have been modeled with a flux-based, drift-diffusion numerical solver that simulates the transport and reactions of ionic species in ChG solid state materials. For circuit simulations, the physics of memristor operations are reduced to analytical circuit-based compact models. Key questions that are addressed in the program are:

1. What is the nature of bulk glass and the metal-glass interface? Specifically, can we quantify solid state parameters such as permittivity, affinity, density of states, and band-gap and can we determine how ion concentration (e.g., Ag) impacts these parameters. Moreover, what is the nature of the Ag-ChG interface and the glass interface and what roles do the metal work-functions and ChG material parameters play in the equilibrium on- and off-state of the electrolyte and on ionic and electron/hole transport?
2. How is charge transport modeled and to what extent can standard flux-based functions such as drift-diffusion, Poisson, and continuity be used to describe memristor operation? What are the mechanisms Ag⁺ ion, neutral Ag, and charged carrier (electrons and holes) transport in ChG? Can we quantify parameters such as diffusivity and mobility of all charged species? Lastly, can the interaction of mobile ionic species with the host material be captured in continuity equations, relating recombination and generation to energy dependent reaction rates and flux gradients to ion and electron/hole transport properties?
3. What is the physics of metallic filament formation and dissolution? What is the static nature of Ag, in low and high impedance states? How do growth and dissolution processes map to device operation, reliability, and radiation effects? How does Ag concentration impact the equivalent impedance of the system?
4. How can the physics of memristor operation be captured as closed form compact (analytical) models that can be used small scale memory, digital logic circuit (i.e., threshold logic), and neuromorphic system simulations?

By addressing these questions, this program has advanced our understanding of the physics of resistive switching. This physics-based approach supports the characterization of reliability and radiation threats to these technologies. We complement the modeling effort with an experimental effort that includes material and device fabrication and chip design to verify theoretical calculations and to articulate new physics and identify application. Electrical characterization of

simple devices comprised of the $\text{Ag-Ge}_x\text{Se}_y$ as well as an alternative Cu-SiO_2 systems are useful in understanding mobile species interaction. Electrical characterization experiments include steady state current-voltage, capacitance-voltage, transient, opto-electronic, and frequency response measurements which allows us to probe the release, movement, and capture of mobile species within the glass matrix during and after programming.

The effort has been performed over a two year period. The program focused specifically on the following tasks:

Task 1 – Chalcogenide Glass Material and Memristor Fabrication

Task 2 – Electrical and Material Characterization

Task 3 - Physics-based Modeling of Electrochemical Memristors

Task 4 - Development of an Analytical (Compact) Modeling Framework

Task 5 – Radiation and Temperature Effect Testing and Modeling

3 TASK 1 – CHALCOGENIDE GLASS MATERIAL AND MEMRISTOR FABRICATION

3.1 Methods, Assumptions, and Procedures

ChG (including $\text{Ge}_x\text{Se}_{1-x}$ and SiO_2 films) material, lateral structures, and vertical memristors, based on the Programmable Metallization Cell (PMC) technology platform developed at ASU [3, 4], have been designed and fabricated in the ISO Class 3 cleanroom in the ASU Center for Solid State Electronics Research (CSSER) and in the associated laboratory of the ASU Center for Applied Nanoionics (CANi). Two variations of the technology have been evaluated to optimize performance and reliability, assess compatibility the Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits (ICs), and support the modeling effort.

3.2 Results and Discussion

3.2.1 $\text{Ge}_x\text{Se}_{1-x}$ Chalcogenide Glass Technology

Two variants of $\text{Ge}_x\text{Se}_{1-x}$ ChG devices were fabricated for analysis and characterization in this program: lateral test structure and vertical programmable metallization cells

3.2.1.1 Lateral Test Structures

Lateral test devices are extremely simple to make as the fabrication process involves only two main steps: (1) deposition of a thin ChG film on a substrate and (2) formation of electrodes on the ChG. The electrodes supply the metal for photodoping as well as the terminals for resistance measurement. The substrate may be insulating or conductive, depending on the device configuration, and may also be flexible.

The lateral device exploits the mechanism of radiation-induced diffusion of the surface electrode metal. Which enables a detailed characterization of photo- and high-energy-radiation-induced transport of active metal ions (Ag) into the ChG matrix. The ChG film resistance is measured between two electrodes on its surface. The materials selected were $\text{Ge}_{20}\text{Se}_{80}$ and $\text{Ge}_{30}\text{Se}_{70}$ glasses and Ag electrodes. In general, Ag has high diffusion ability in Ge-Se films and many tens of atomic percent of Ag can be incorporated in them. These particular Ge-Se compositions were chosen to assess the effect of chalcogen content on device response since it is known that Ag diffusivity is higher in more chalcogen rich material. Several Ge-Se thicknesses were also used to determine the effect of this parameter on device behavior.

The processing steps involved in the fabrication of the lateral devices are shown in Figure 1. Blanket $\text{Ge}_{20}\text{Se}_{80}$ and $\text{Ge}_{30}\text{Se}_{70}$ films, 5 nm, 10 nm and 20 nm thick, were evaporated onto cleaned microscope glass slides in a Cressington 308 thermal evaporator at a deposition rate of 0.1 nm/s. Then 35 nm of Ag was evaporated at 0.1 nm/s through a shadow mask on top of the deposited ChG film in the thermal evaporator in order to form the Ag electrodes on the Ge-Se film surface. Figures. 2a and 2b shows the cross-sectional view and top-view of the lateral devices, respectively. The Ag dots are 2 mm diameter, with a spacing of 1 mm between them.

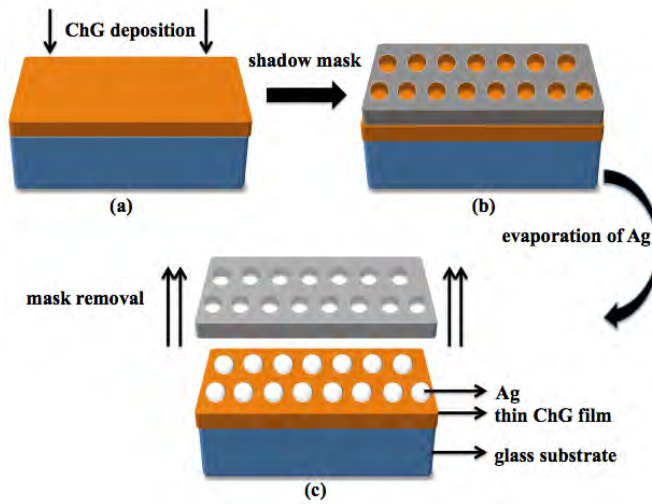


Figure 1. Lateral device: Sensor fabrication process sequence

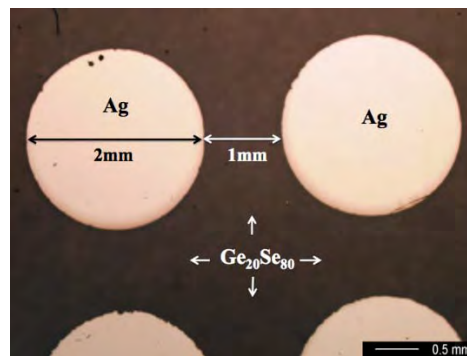
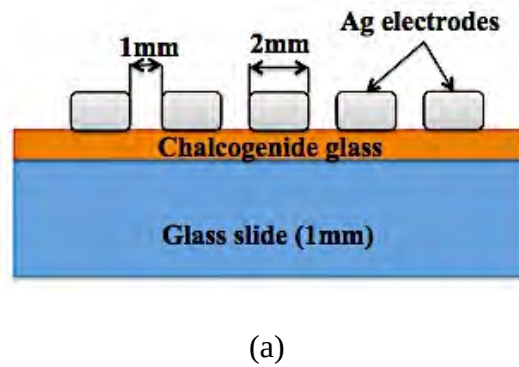


Figure 2. Lateral device: (a) Cross-section view and (b) top view

3.2.1.2 Vertical Programmable Metalization Cells (PMCs)

Vertical PMCs can be described as having a metal–electrolyte–metal or metal-insulator-metal (MEM/MIM) structures. The cells achieve resistive switching through the formation and dissolution of nano-sized metallic conductive filaments within a solid-state electrolyte material. Electric field assisted transport of ions, and electrochemical reduction-oxidation (redox) reactions at the electrodes allow for the filaments to be grown and dissolved. These devices have been demonstrated to be compatible with standard CMOS, readily integrated into the back-end-of-line (BEOL) process. Like other resistive random access memory (RRAM) devices, the PMC is a two terminal element capable of resistance change when a voltage, above or below specified thresholds, is applied across its terminals. In PMCs, under the application of positive bias at the anode, the Ag atoms are oxidized and move towards the cathode as cations under the influence of electric field. Ion hopping has been proposed as the primary mechanism of cation transport [5, 6]. At the cathode, the cations are reduced and electrodeposited, forming a conducting filament that grows towards the anode. Upon reaching the anode, the filament provides a low resistance path through the film. This constitutes a change from a high resistance state (HRS) to a low resistance state (LRS). Under reverse electrical bias, the filament undergoes dissolution and eventually the device returns to its HRS condition. A typical PMC I-V characteristic is shown in Figure 3(a), which represents a typical resistance switching characteristic for the PMC devices. The figure shows a write voltage threshold (HRS to LRS switching) between 200 mV and 300 mV. The erase voltage threshold (LRS to HRS switching) was less than -100 mV. Similar write/erase thresholds were obtained for all devices tested, regardless of device area. The maximum current allowed to flow through the devices during characterization, i.e., the compliance or programming current, was set to 10 μ A for the DC response shown in Figure 3(a). Previous studies have determined that the LRS resistance shows an inverse power law dependence on the magnitude of the programming current compliance [5]. Similar LRS resistance vs. compliance current characteristics was observed for the PMCs examined in here as well, as shown in Figure 3(b).

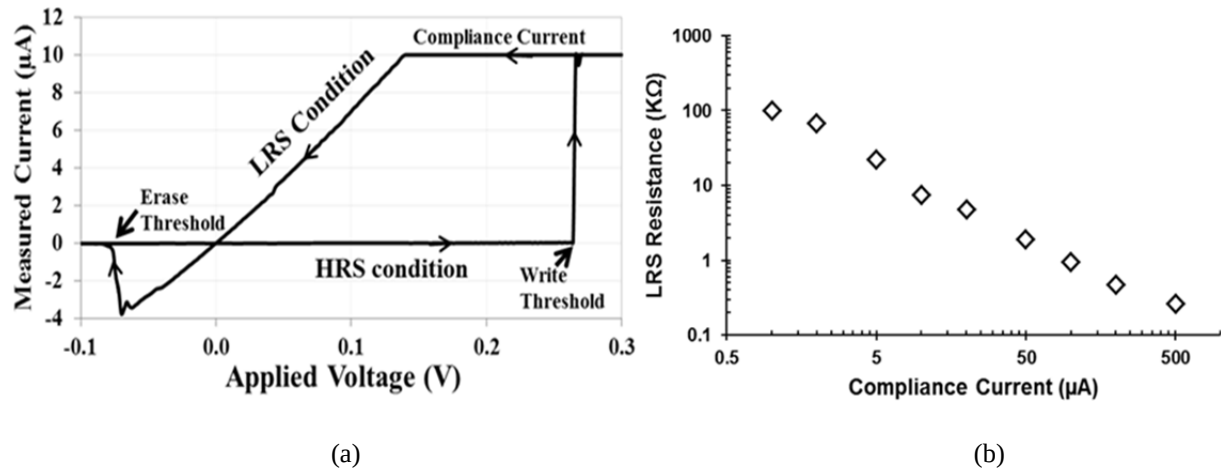


Figure 3. (a) DC I-V characteristics of a PMC device and (b) experimentally obtained inverse power law dependence

3.2.1.2.1 Single Device Design

Test chips containing several single PMC device variants arranged in an array were fabricated at ASU. PMC devices are fabricated on a 100mm (diameter) 0.5mm (thick) p-type Silicon wafer. First, the wafer goes through standard cleaning processes (Acetone and IPA rinse followed by dehydration bake at 120C for 5 minutes). Then, it is loaded into an e-beam evaporator tool (Lesker PVD75 E-beam Evaporator) for deposition of oxide and metal stack (100nm of SiO₂, 100nm of Ni and again 100nm of SiO₂).

The intermediate Ni layer acts as device cathode and the top SiO₂ layer is used for isolation. Then, a photolithography step is performed to pattern the substrate for forming device via(s) on the top SiO₂ isolation layer. It then goes through a wet etch step to expose the Ni layer in the via regions. The vias are used either as contact holes to the Ni electrode, i.e., cathode vias, or as “device” vias which define the active area of the PMC. After etching, a second photolithography step is performed to pattern the substrate for deposition of 60 nm Ge₃₀Se₇₀ and 30 nm Ag films. These films are deposited on the vias using a thermal evaporator (Cressington). The wafer is then exposed to UV light ($\lambda = 324$ nm, $E = 3.82$ eV) for 1 hour at a power density of 10 mW/cm² in order to allow Ag photo-doping of the chalcogenide film. Photodiffusion of silver is one of the most interesting effects that occur in chalcogenide glass films as it dramatically changes the properties of the starting material. Exposing PMCs to UV light causes Ag incorporation from the anode into the chalcogenide glass. This photo-induced doping changes the electric properties of the glass from dielectric to solid-state electrolyte and ensures repeatable switching behavior [7, 8]. An additional 35 nm of Ag is then deposited on top of the silver-doped Ge₃₀Se₇₀ layer to create the device anode. A lift off and the third photolithography step follows to pattern the substrate for final metal pad depositions. For the current devices, a stack of 800nm Al, 10nm of Cr and 150nm of Au is used to form the metal pads. The metal pad formation step completes with a final lift off step which prepares the device for a post processing annealing step at 120° C for 60 minutes. Figure 4(a) illustrates a cross section of the PMC device. Figure 4(b) shows the top-view photo-micrograph of a PMC fabricated with a 500 μ m by 500 μ m via dimension.

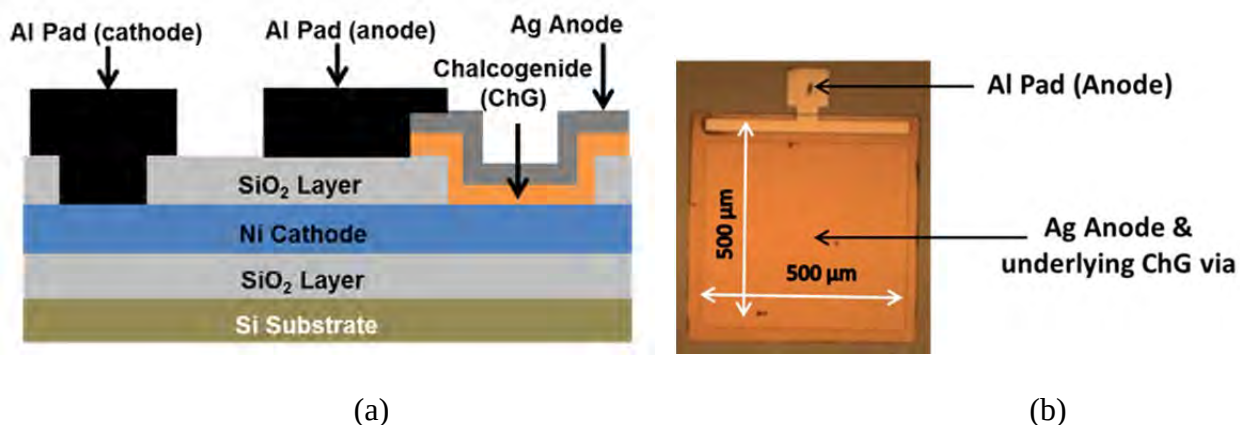


Figure 4. (a) Illustration of PMC cross-section and (b) photo-micrograph showing top (planar) view of a PMC device

Bias-dependent transport of Ag (or Cu) ions, via the application of a voltage or current across the electrodes, and electrochemical reduction-oxidation (redox) reactions allow Ag- or Cu-rich filaments to be grown or dissolved in the active film where ions conduct. In order to reduce the energy needed for filament growth or dissolution, electrochemically active metal is typically introduced into the film during fabrication when a metal/glass bilayer is exposed to light in a process known as photo-doping. Exposure to photons of ultra-violet (UV) light causes metal to diffuse into the film and form ternary phases that extend into the film from the active metal side. Within this photo-doped, metal-rich region, the film resistivity is many orders of magnitude less than undoped glass]. However, even with metal concentrations as high as tens of atomic percent, these metal doped chalcogenide films have resistivities that are still many orders of magnitude higher than the metallic filaments [7].

After a typical photo-doping process involving Ag and a ChG, the resulting structure comprises an Ag-rich ternary layer extending from the active Ag anode and a region of relatively undoped (high resistivity) glass. Photo-doping can be used in PMC processing to produce such a layered structure and thereby reduce the span of undoped material over which a filament must be grown. Reducing the thickness of material to be bridged decreases the switching voltage and filament formation time.

3.2.1.2.2 Cross-bar Array

The full fabrication process for the cross-bar array, which is similar to the process for the single device chip is highlighted in Figures 5 to 15. A four inch diameter, 525 μm thick Si p-type wafer was placed inside a Lesker PVD75 electron-beam evaporator. After reaching a vacuum of approximately 3×10^{-6} torr, a 100 nm layer of SiO_2 was deposited at 0.9°A/s to provide insulation between the Si substrate and the device structures (Figure 5). Without breaking vacuum, a 100 nm layer of Ni was deposited at 0.9°A/s on top of the SiO_2 insulating layer, shown in Figure 6. After Ni deposition, the vacuum chamber was brought back up to atmosphere and the wafer removed. To create the nickel (Ni) contact patterning, hexamethyldisilazane (HMDS) was first spun onto the nickel surface to promote adhesion of the resist. HMDS was always applied before spinning on resist, though this step will not be mentioned in further lithography steps. A 1 μm layer of AZ3312 photoresist was spun onto the treated nickel surface at 3500 RPM for 30 seconds. The resist covered wafer was then soft baked at 100 C for 60 seconds. Lithography exposure was performed using an EVG 620 set to 45 mJ/cm^2 UV exposure.

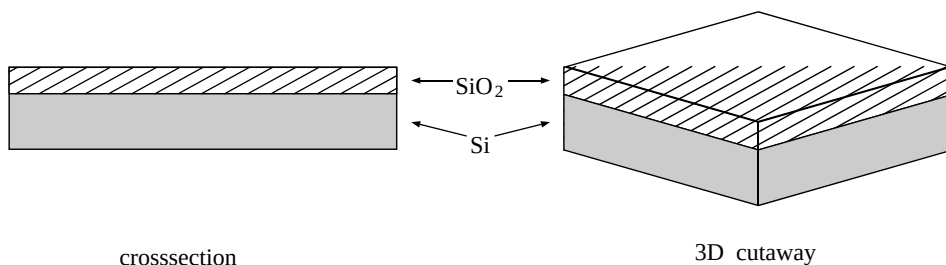


Figure 5. Deposition of 100 nm SiO_2

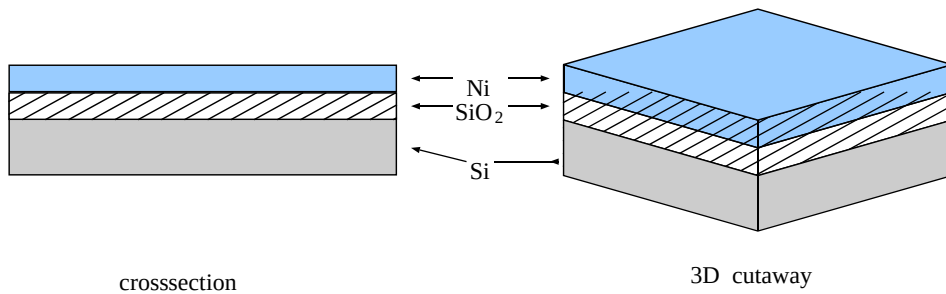


Figure 6. Deposition of 100 nm Ni

Mask #1 was used to create the Ni cathode bar positive image in the resist (Figure 7). After exposure, the resist was developed for 80 seconds using AZ 300 MIF developer. Preparation of the resist layer for wet etching was concluded by hard baking the wafer for three minutes at 110 C. The Ni left exposed after lithography was etched away after ten minutes, using 100 mL of Nickel Etchant TFB (Nitric Acid). A representation of the etched feature is shown in the right hand side of Figure 8.

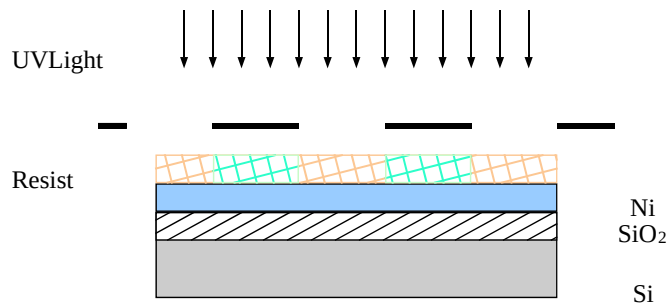


Figure 7. First lithography mask exposure to create cathode bar.

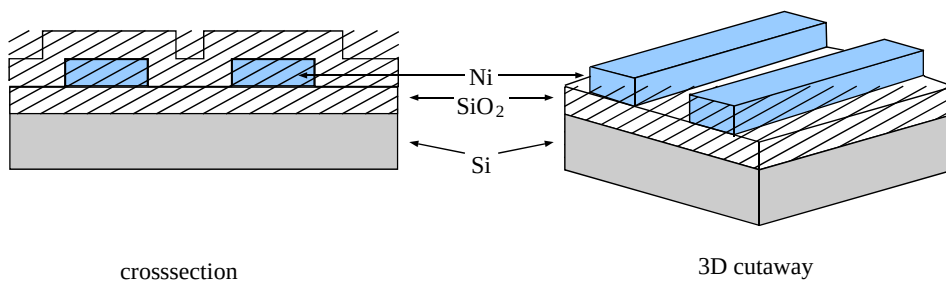


Figure 8. Ni layer wet etched to create cathode bar followed by deposition of SiO₂.

Several steps were used to form the active layer of the PMC. The protective layer of resist was removed by soaking the wafer in acetone followed by a rinsing of isopropyl alcohol (IPA). After the resist was removed, the wafer was placed back into the Lesker PVD75 electron beam evaporator, pumped down to high vacuum, and a 100 nm layer of SiO₂ deposited at 0.9 °A/s. The wafer was removed from the vacuum chamber and another layer of AZ3312 resist spun on with the same recipe as described previously.

Crossbar mask #2 was used to pattern (Figure 9) the resist, this time with vias used for holding the active device layer. The vias shown in Figure 10 were etched through the SiO₂ layer with 100 mL buffered oxide etch (BOE) solution after ten minutes. The resist for the etch mask was removed with acetone and another layer of resist, this time AZ4330, was spun on at 2000 RPM for 30 seconds. The resist was soft baked at 100 C before undergoing lithography with crossbar mask #3 in the EVG to a 300 mJ/cm² UV exposure. This lithography step is depicted in Figure 11. The resist was developed for two minutes using AZ 300 MIF. The wafer was placed into a Cressington 308R thermal evaporator where, as shown in Figure 12, 60 nm of Ge₃₀Se₇₀ was deposited followed by

30 nm Ag. As shown in Figure 13, the Ge₃₀Se₇₀ layer was photo-doped with the Ag by exposing the device side (top) of the wafer to UV ($\lambda = 324$ nm) light for one hour. After the photo-doping process, the wafer was place back into the Cressington evaporator where 35 nm of additional Ag was deposited to form the top active metal anode. Figure 14 shows the device structure after the resist is dissolved, lifting off the chalcogenide and electrode layers around the individual device vias.

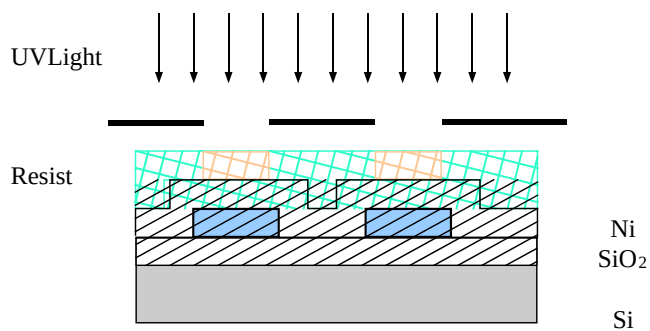


Figure 9. Second lithography mask to etch via through SiO₂

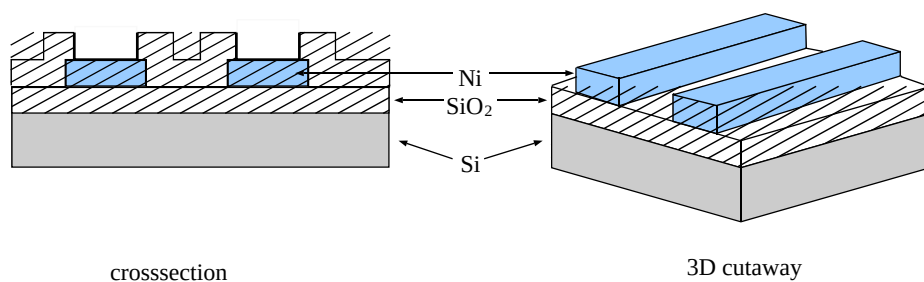


Figure 10. Vias wet etched through SiO₂ to Ni layer

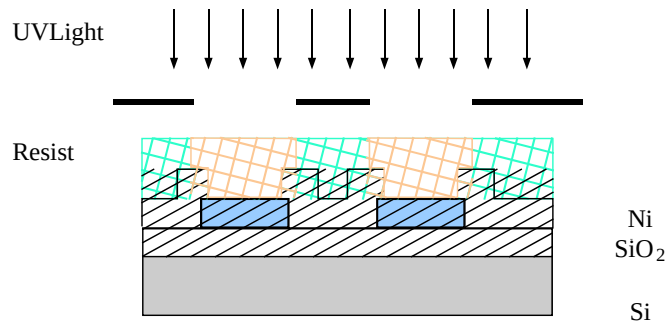


Figure 11. Third lithography mask for device layer lift-off

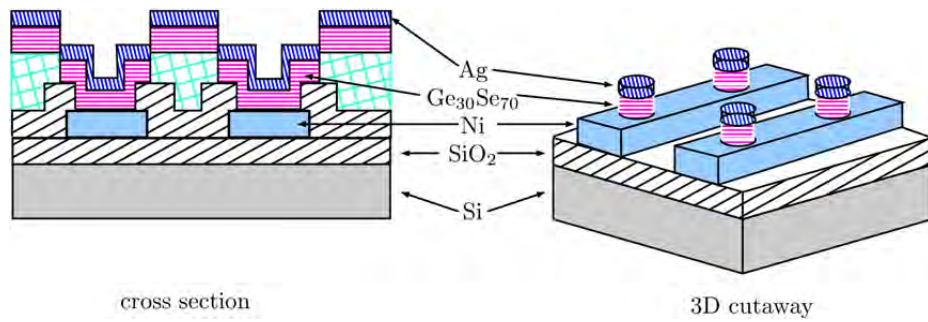


Figure 12. Ge₃₀Se₇₀ is deposited followed by Ag

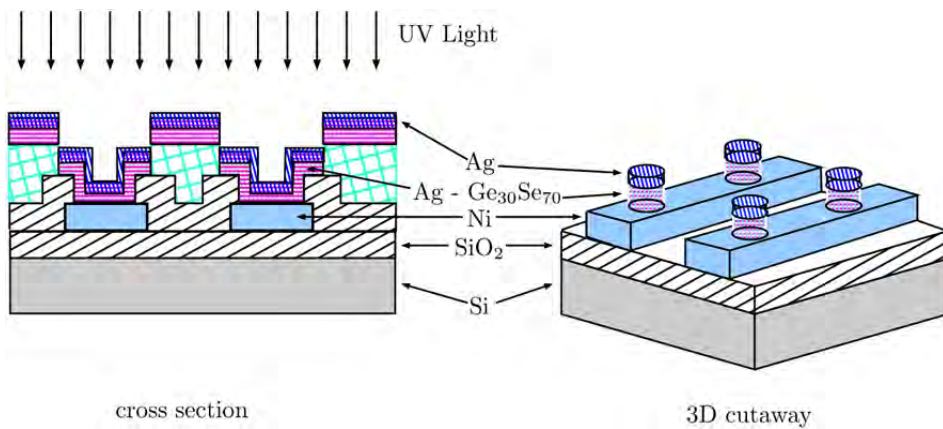


Figure 13. Ge₃₀Se₇₀ is photo-doped with Ag by exposing to UV light

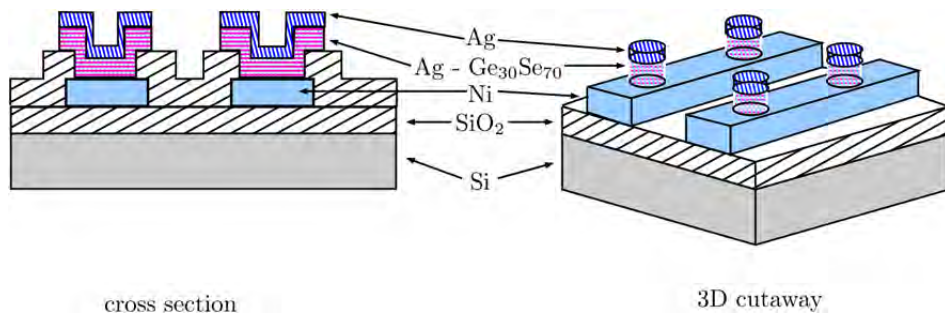


Figure 14. Additional Ag is deposited then the wafer is soaked in acetone to remove the resist and lift off the excess material

The final steps create the Al crossbar contacts across the anode of the devices. The wafer was again coated in AZ4330, spun on at 2000 RPM for 30 seconds. The resist was soft baked at 100 C for 60 seconds. Crossbar mask #4 was used to image a lift-off layer for the Al contacts, using the EVG for a UV exposure to 300 mJ/cm². The wafer was placed in the Lesker electron beam evaporator where 400 nm of Al was deposited at 1 A/s. The resist layer was dissolved in acetone to lift-off the excess Al, leaving behind dog bone style contacts. Another layer of AZ4330 resist was laid down in the manner described for the Al lift-off layer. The final mask #5 was used to image contact pads over both ends of the dog bone electrodes (both anode and cathode contacts). The purpose of this layer was to apply a thicker layer of metal where probing and wire bonding may take place. The wafer was placed back into the Lesker one final time, to deposit an additional 400 nm of Al at 1.5 °A/s. After deposition, the resist was removed with acetone to lift-off the Al. To finish the devices, the wafer was annealed at 120 C for 20 minutes. Figure 15 depicts the complete layer stack of the PMC. A picture of the finished crossbar structure is shown in Figure 16.

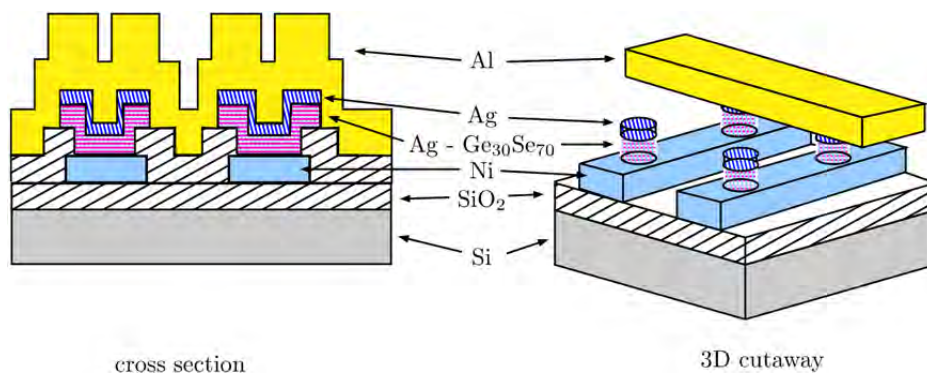


Figure 15. Al is deposited and lifted off to create top anode crossbar

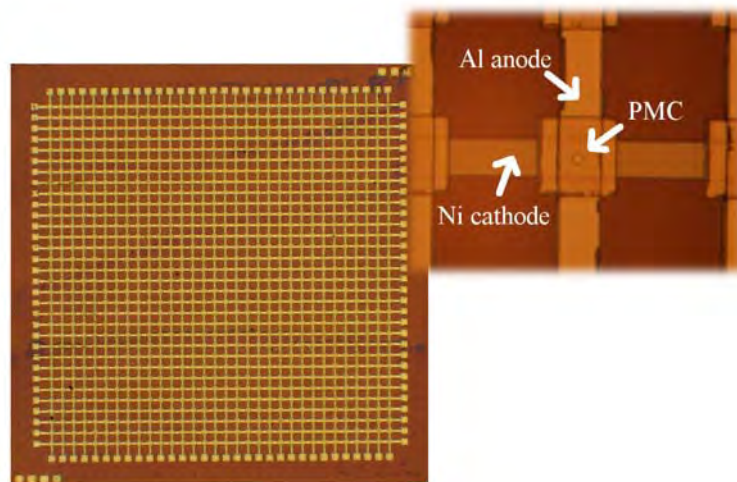


Figure 16. Fabricated crossbar tile. Zoomed image highlights the device contacts and active device region

3.2.2 Cu-SiO₂ Programmable Metallization Cells

In this sub-effort of the fabrication task, PMCs with a copper (70nm), silicon dioxide (13nm), and tungsten (100nm) vertical stack were manufactured at ASU. The copper acts as the active anode and tungsten works as the inert cathode. A thin layer of evaporated SiO₂ is sandwiched between these two metal electrodes. Figure 17(a) shows cross-section illustration of a Cu-SiO₂ PMC device fabricated at Arizona State University.

Starting from an RCA cleaned 4 inch silicon wafer, a 300 nm SiO₂ insulation layer was thermally grown using wet oxidation at 1050°C. A 100 nm thick tungsten film was sputtered on top by a Lesker PVD75 magnetron sputtering system. A layer of 100 nm thick SiO₂ was deposited on top of tungsten film by plasma-enhanced chemical vapor deposition (PECVD) at 350°C with SiH₄ and N₂O gas. This PECVD SiO₂ was photolithographically patterned and the exposed parts were wet etched by buffered oxide etch (BOE) to create vias. Photolithography was performed again on top of vias to define anode patterns. The patterned wafer was transferred to a Lesker PVD75 electron beam evaporator, and 13 nm SiO₂ and 70 nm copper films were e-beam evaporated at room temperature without breaking the vacuum. Fabrication of the Cu-based PMC devices was finalized after a standard lift-off process. The actual device size was determined by the size of via.

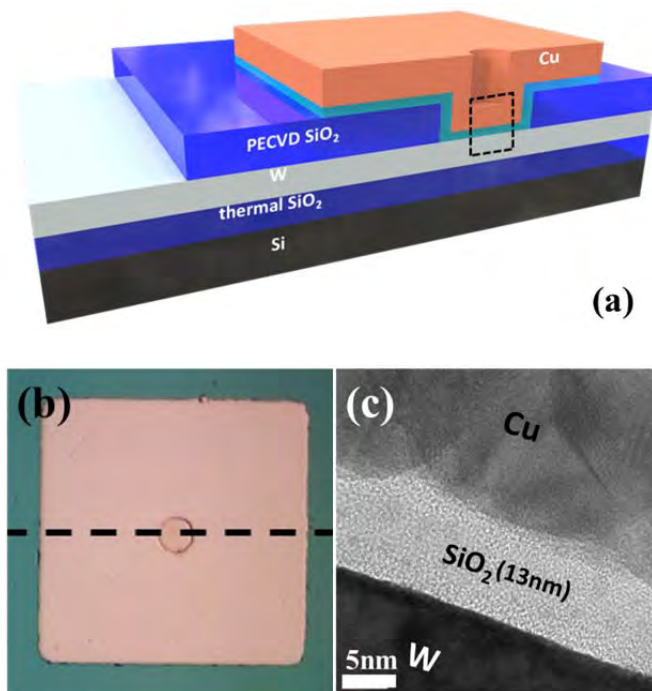


Figure 17. (a) 3D cross-section of PMC, (b) optical image of the top view of PMC, and (c) TEM image of Cu/SiO₂/W stack

Figure 17(b) shows the optical image of the top of the PMC. The circle in the center is the 10 μm via. Figure 17(c) is the actual cross-section, obtained with the use of focused ion beam (FIB) cutting and transmission electron microscopy (TEM), along the dotted box marked in Figure 17(a) and line in Figure 17(b).

3.3 Conclusions

Proper, controlled fabrication of test structures was critical to the various studies performed for this program. Lateral structures were used primarily to characterize for model validation that processes of both photo- and radiation-induced transport of active metal ions into the ChG materials. Single device vertical ChG PMCs were constructed to support impedance vs. frequency, DC current and capacitance-voltage measurements, and current vs. time characterizations for static device TCAD simulation and compact model development. Similar ChG PMC structures in cross-bar configurations were fabricated to enable better part packages for *in-situ* bias testing from radiation experiments and evaluate the yields in these higher density architectures. Lastly, we added new PMC structures composed of Cu-SiO₂ in order to evaluate alternative materials with greater CMOS compatibility.

With this comprehensive set of solid electrolyte structures, we were able to perform a variety of experiments to support program tasks 2 through 5.

4 TASK 2 – ELECTRICAL AND MATERIAL CHARACTERIZATION

4.1 Methods, Assumptions, and Procedures

Material analysis is performed on lateral and vertical test structures using optical and energy dispersive X-rays scattering (EDS) measurements. Materials characterization was ASU's LeRoy Eyring Center of Solid State Science (LE-CSSS). The results provide information on the rate and distribution of metal ions into the insulating electrolyte matrix. Electrical tests on lateral ChG structures, Ag-ChG-based and Cu-SiO₂-based memristors include DC current-voltage (and resistance) measurements, impedance vs. frequency, and current vs. time. Tests were performed in the ASU's Wireless Communication Circuits Measurement Laboratory (WCCML). Relevant measurement equipment in WCCML includes: HP4284 LCR meter, HP4156 Parameter Analyzer (PA), and a customized transient pulse measurement system (pulse generator and oscilloscope). Wire-bonding for die packaging and a Cascade Summit 11560 Probe Station equipped with an Attoguard chamber probe station for on-wafer and bare die measurements were also used to conduct the electrical measurements.

4.2 Results and Discussion

4.2.1 Characterization of Ge_xSe_{1-x} Chalcogenide Glass Technology

4.2.1.1 Lateral Test Structure Characterization

Although some ChG technologies utilize photo-induced doping in their manufacturing process or even in their application, several questions regarding the physics of photodoping in ChG materials remain unsolved. For example, the electro-chemistry of photodoping is still not fully understood and accurate physically-based models for the process remain illusive. One of the goals of the program is to analyze and model this process as well as the simple process of unstimulated Ag incorporation into the materials. To experimentally characterize the processes associated with metal incorporation into ChG, both with and without light stimulus, Ag distributions within a ChG film are measured on devices that are either un-doped or photo-doped. The two device types are lateral variants of the standard PMC technology, similar to those shown in Figure 2, except one terminal is an inert metal Nickel (Ni) contact. The only difference between the two device types is an extra processing sequence added to the photodoped structures.

In order to investigate the active metal (Ag) composition of the ChG layer prior to and after photodoping, energy dispersive X-rays scattering (EDS) measurements were performed to extract the Ag profile between the anode and cathode terminals. The electron beam used to generate the scattering response was used to extract Ag concentrations on both un-doped and photo-doped devices along the cutline shown in Fig. 3 (top view of lateral device). The characteristic X-ray emission spectrum was retrieved at each point on the scanned e-beam line. Figure 18(b) shows clear evidence that for the doped devices, a dendritic region is forming near the Ni contact and that no such pattern is observable in Figure 18(a), the undoped structure. Therefore, photodoping induces more ionic transport from Ag contact toward Ni contact by overcoming the potential barrier and Ag atoms accumulate near the Ni cathode.

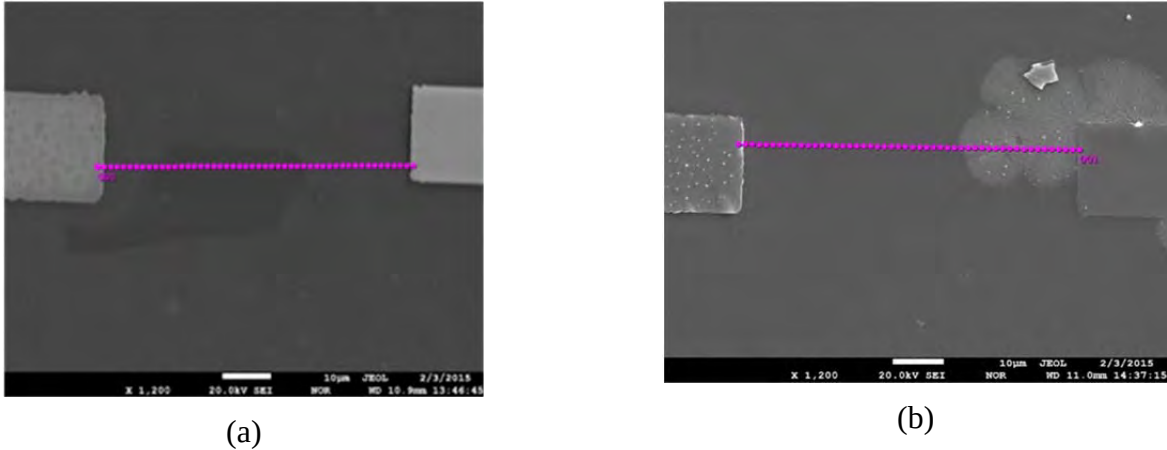


Figure 18. The SEM image for (a) the unphotodoped PMC device, and (b) the photodoped PMC device

The concentration of Ag in both device types was quantified with EDS using a JEOL JXA-8530F Hyperprobe. A 15kV accelerating voltage was applied during the measurement and Ge, Se, Ag and Ni elements were selected for detection. The counts per second of Ag's characteristic x-ray emissions are shown in Figure 19. The lateral axis in Figure 19 is the distance from the Ag anode edge. The Ag concentration in the undoped device is approximately uniform. For the photodoped device, the Ag concentration is similar to that of the undoped within 30 μm of the anode, but shows an abrupt increase within 20 μm of the Ni cathode. These results are consistent with the dendritic plume observable in Figure 18(b). These measurements indicate that in response to light exposure, Ag atoms transport towards and accumulate near the inert cathode. The physics of these processes are reproduced with the numerical model, presented in the modeling task 3.

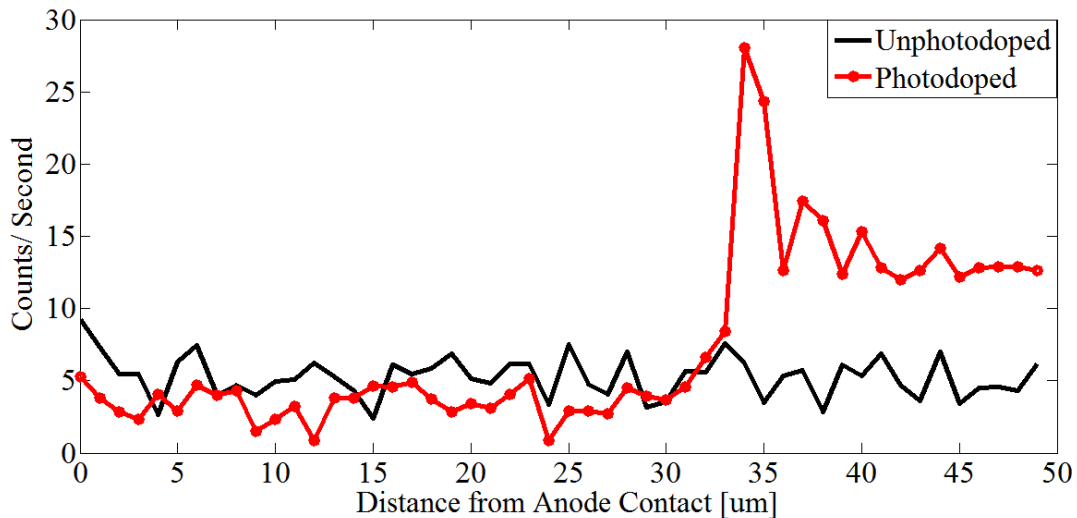


Figure 19. EDS results show Ag profile across both unphotodoped and photodoped devices

Further optical and resistance measurements were performed on lateral structures (with two Ag contacts) in order to optically and electrically measure the process of photo-induced Ag incorporation into ChG films.

Figure 20 shows the evolution of Ag lateral diffusion in $\text{Ge}_{20}\text{Se}_{80}$ with respect to UV exposure time. Figure 20(a) shows two Ag electrodes on top of 5 nm thick $\text{Ge}_{20}\text{Se}_{80}$. These two electrodes are used as contact pads for electrical measurements as well as providing the Ag for incorporation into the ChG layer. Before UV exposure, the device exhibits a very high resistance state (OFF state). This OFF state resistance cannot be determined precisely using the PA, as the current is below the measurement limit of the instrument, but is in the order of $10^{12} \Omega$.

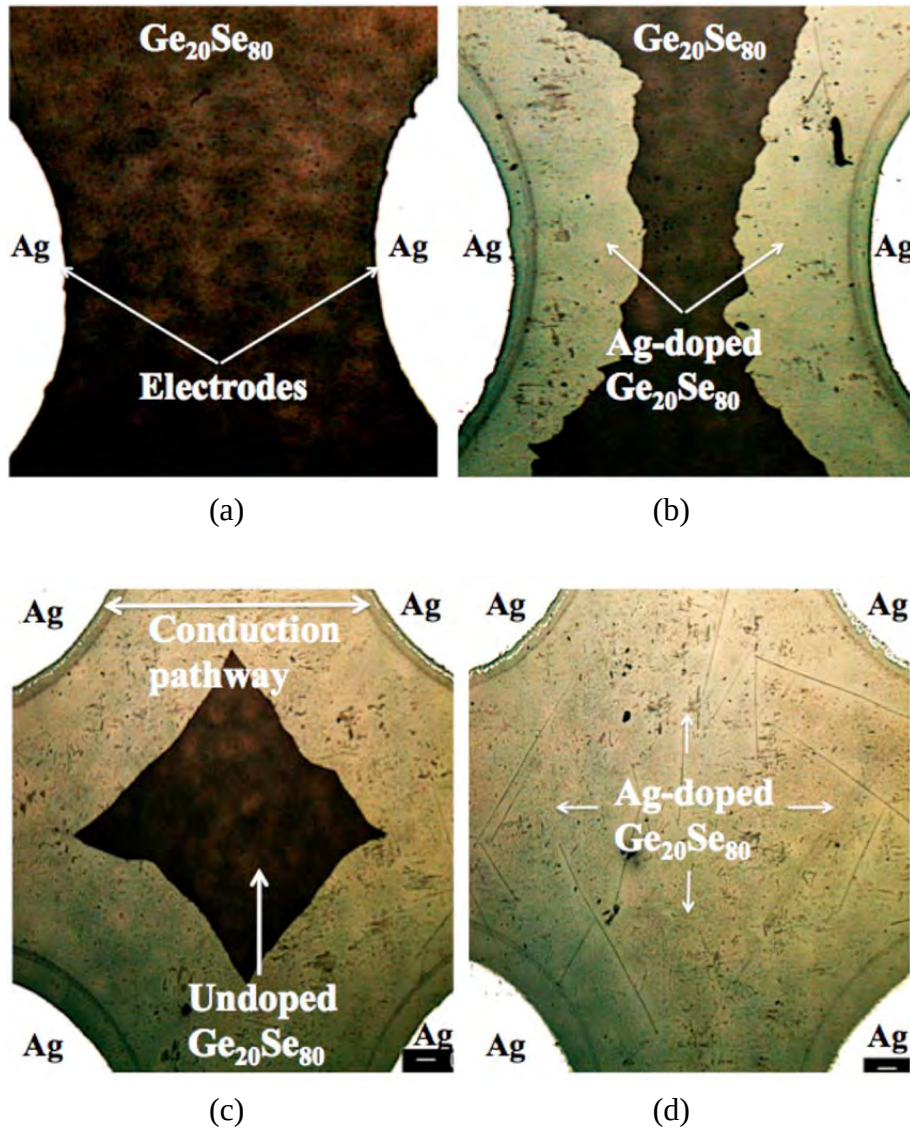


Figure 20. Evolution of UV light induced Ag lateral diffusion in a 5 nm thick $\text{Ge}_{20}\text{Se}_{80}$ film

After 19.22 J/cm^2 of UV exposures, as shown in Figure 20(b), Ag has diffused laterally by more than 0.5mm between the two electrodes. At this stage, the device is still in the OFF-state, as there remains a region of undoped ChG between the measurement electrodes. As shown in Figure 20(c), after 33.64 J/cm^2 of UV exposures, the ChG layer between the electrodes has been bridged by Ag-Ge-Se (doped) material. At this stage, the device is in a low-resistance 'ON-state'. After 43.25 J/cm^2 of UV dose, the image shows complete saturation of the ChG film with Ag.

The average resistance with respect to total UV dose was measured on a minimum of 20 devices. The devices were exposed to a total UV dose of 124.93 J/cm^2 . The resistance of each device was monitored for 500 s and Figure 21 shows the average resistance with respect to measurement time, at various total UV dose levels.

Figure 21 shows that the resistance of the devices decreases and saturates in response to the total UV dose. The high OFF-state resistance (approximately $10^{12} \Omega$) is not plotted, since it is beyond the instrument range. After a dose of 43.25 J/cm^2 , the resistance of the device was $2.5 \text{ k}\Omega$ (R_{sat}) and shows no significant change beyond this, even after 124.93 J/cm^2 of UV exposures. The average resistance also shows no significant change during the measurement time (i.e. 500 s) at room temperature, therefore suggesting that the application of bias (at 10 mV) during measurements may not cause Ag diffusion and disturb the state of the device. The decrease in resistance at incremental UV doses is mainly due to UV induced photodoping of Ag into the ChG and not due to measurement bias. The OFF-state resistance is not plotted since it is beyond the instrument range.

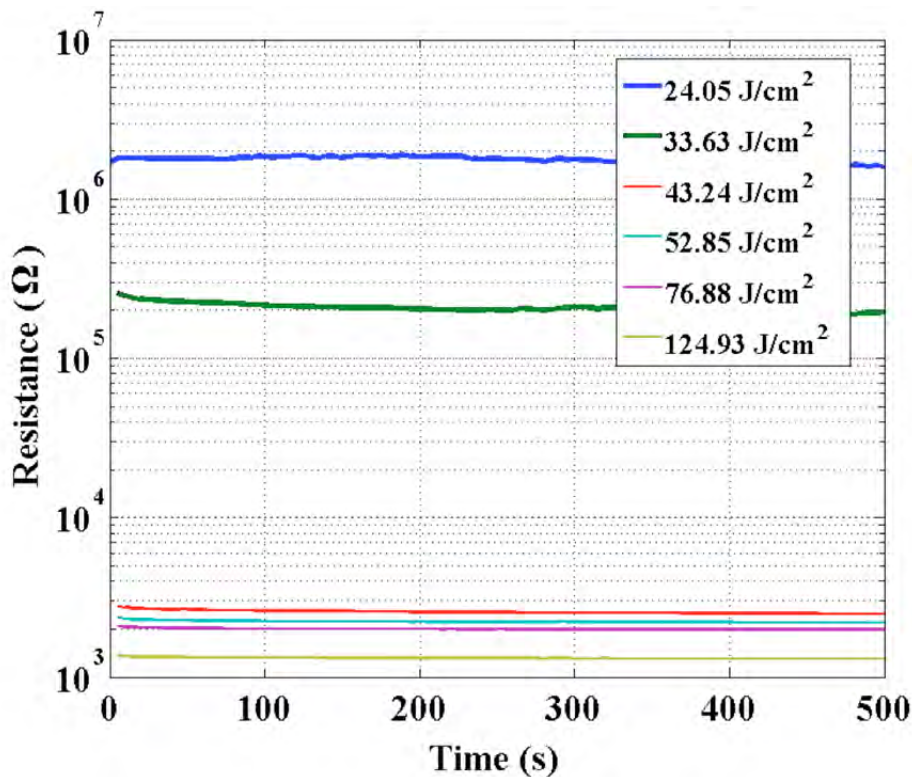


Figure 21. Resistance as a function of time of 5 nm $\text{Ge}_{20}\text{Se}_{80}$ lateral devices

Two different thicknesses of $\text{Ge}_{20}\text{Se}_{80}$ (5 nm and 20 nm) and $\text{Ge}_{30}\text{Se}_{70}$ (5 nm and 20 nm) samples were fabricated in order to differentiate the effect of ChG thickness and composition on structure performance. Figure 22 plots of average resistance with respect to UV dose for four different samples and Table I shows the effect of composition and thicknesses on D_{th} and D_{sat} . These results demonstrate that regardless of device type, the sensors show a rapid reduction in resistance followed by saturation in response, when exposed to UV irradiation.

As shown in Figure 22, the devices with greatest sensitivity are 5 nm thick $\text{Ge}_{20}\text{Se}_{80}$ devices and the second most are 5 nm thick $\text{Ge}_{30}\text{Se}_{70}$ devices. From Table 1, the threshold UV dose (D_{th}) of 5 nm and 20 nm $\text{Ge}_{20}\text{Se}_{80}$ are 24.0 and 48.1 J/cm^2 respectively, and for 5 nm and 20 nm $\text{Ge}_{30}\text{Se}_{70}$ are 33.6 and 67.3 J/cm^2 , which shows that the D_{th} of the device can be increased by increasing the thickness of ChG layer. At D_{th} , the resistivity of 5 nm $\text{Ge}_{20}\text{Se}_{80}$ is calculated as $7.5 \times 10^{-3} \Omega \cdot \text{m}$ and of 5 nm $\text{Ge}_{30}\text{Se}_{70}$ is $3.75 \times 10^{-2} \Omega \cdot \text{m}$. It is also evident that the composition of ChG can also influence the D_{th} of the device. Also the difference, $D_{\text{sat}} - D_{\text{th}}$, is smaller in $\text{Ge}_{20}\text{Se}_{80}$ compared to $\text{Ge}_{30}\text{Se}_{70}$ devices, indicating that $\text{Ge}_{20}\text{Se}_{80}$ devices might have greater radiation sensitivity due to more rapid achievement of the threshold condition. This is likely due to the greater Ag diffusivity in more chalcogen rich materials.

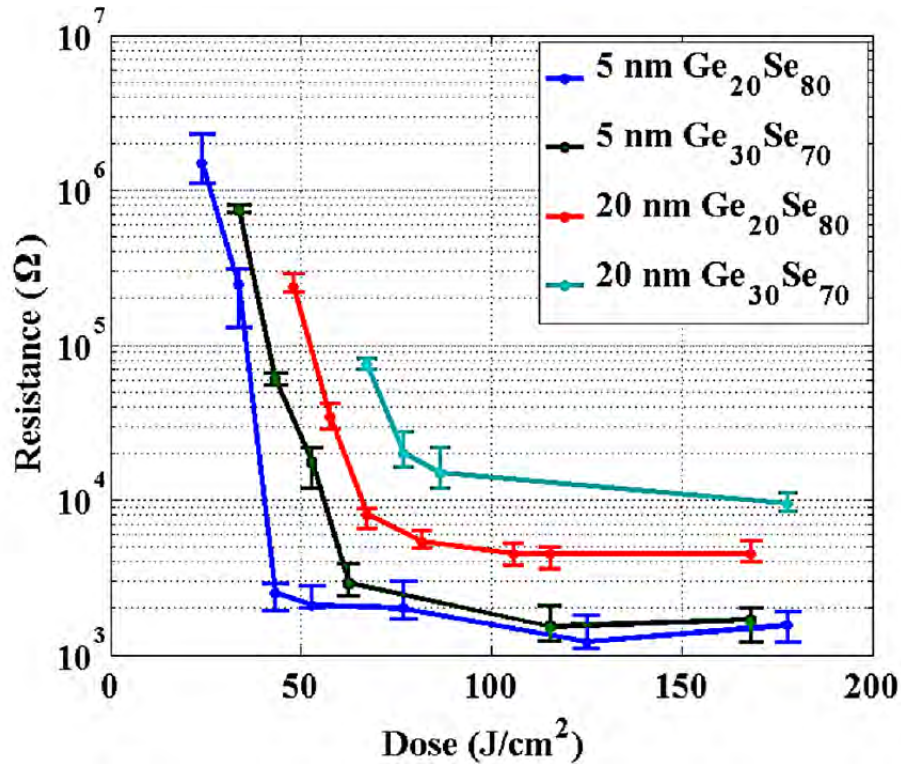


Figure 22. UV dose response curve of lateral devices

Table 1. UV Performance

Devices	D_{th} (J/cm ²)	R_{th} (Ω)	D_{sat} (J/cm ²)	R_{sat} (Ω)	$D_{sat}-D_{th}$ (J/cm ²)
5 nm Ge ₂₀ Se ₈₀	24.03	1.5×10^{06}	43.25	1.6×10^{03}	19.22
5 nm Ge ₃₀ Se ₇₀	33.64	7.5×10^{05}	62.47	1.8×10^{03}	28.83
20 nm Ge ₂₀ Se ₈₀	48.06	2.3×10^{05}	67.28	8.0×10^{03}	19.22
20 nm Ge ₃₀ Se ₇₀	67.28	7.5×10^{05}	96.12	1.6×10^{04}	28.83

4.2.1.2 Vertical PMC Characterization

Material analysis and both DC and AC frequency response measurements were performed on the PMCs with different via areas: 100 μm by 100 μm , 250 μm by 250 μm , 400 μm by 400 μm and 500 μm by 500 μm . The resistance switching characteristics were obtained by sweeping the voltage from -0.5V to 0.5V with an Agilent 4156C PA. Impedance measurements were performed with an Agilent 4284A LCR meter on PMCs in both HRS and LRS. Impedance spectra were obtained between 20 Hz and 1 MHz with a small signal AC voltage (10 mV_{RMS}) applied across the device. Since this applied voltage is much below the device switching threshold voltage, the state of the device is not disturbed during the small signal measurement.

4.2.1.2.1 Material Characterization

Transmission Electron Microscopy (TEM) was performed on a HRS PMC to investigate the device cross section. TEM was conducted with a JEOL ARM200 microscope and images were acquired for a magnification of 2×10^6 with 200keV electron and a beam current of 14 pA. Figure 23(a) shows the cross section of a device in the HRS using high angular dark field. All the major layers are identified, including the Ag anode, Ni cathode, chalcogenide active via and the SiO₂ isolation layer. The Ag and Ni layers show crystalline granularity, while the chalcogenide layer is amorphous and formed by two different layers within via – a photo-doped Ag-rich layer (lighter in color) and an Ag-poor region (darker). This is seen in Figure 23(b) which is a magnified view of the ChG-Ni interface.

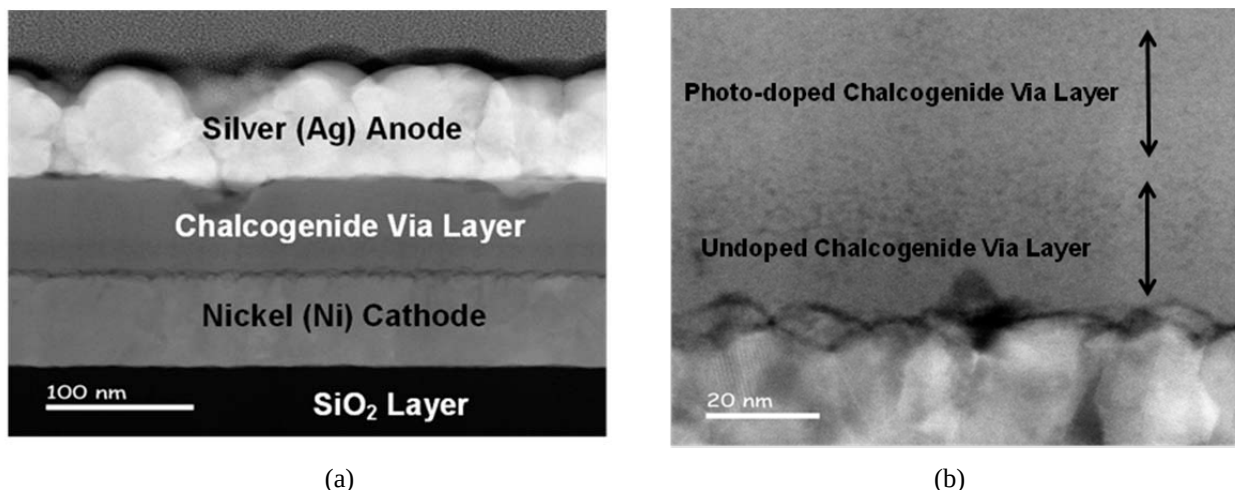


Figure 23. (a) TEM image of PMC cross section and (b) magnified view

To estimate the composition of the layers within the PMC via, energy dispersive x-ray scattering (EDS) was used to obtain profiles of species present in the device via. The electron beam was scanned along a line in the plane of device via and a characteristic emission x-ray spectrum was retrieved at each point of the scanned line. The profiles obtained for the PMC are shown in Figure 24. From the obtained atomic profiles along the device, it can be seen that the Ge and Se profiles are almost identical and indicate the ChG film thickness. The Ag profile is high and constant in the beginning, indicating the Ag anode layer, and then drops to a lower value which stays at more or less the same level, indicating the presence of a photo-doped Ag rich layer within the via. The sharp fall in Ag profile near the Ni cathode indicates the boundary with a second layer, which has considerably less Ag-incorporation.

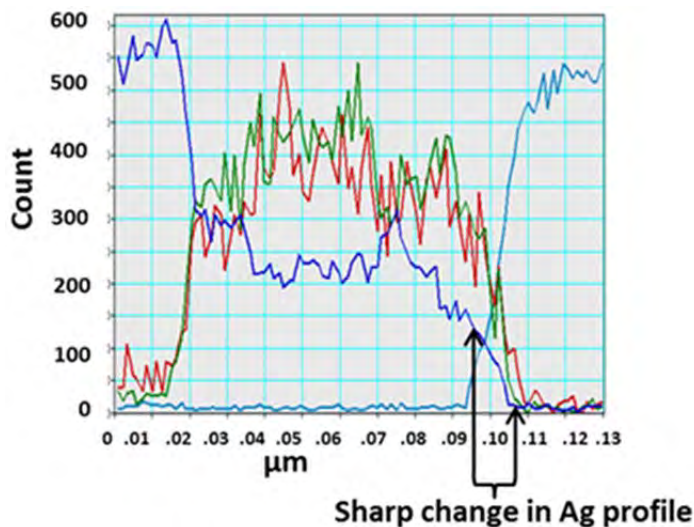


Figure 24. Atomic profiles of Ge (red), Se (green), Ag (dark blue) and Ni (light blue) along the PMC device

4.2.1.2.2 HRS Equivalent Circuit Parameterization

It is known that device illumination with UV light causes Ag to diffuse into the chalcogenide (ChG) via layer and form a solid-state electrolyte. During this process, Silver diffuses from the top Ag electrode towards the bottom Ni electrode, reacting with the ChG to form different phases within the film. After annealing, which is the final processing step used on the devices studied in this work, binary phase like Ag_2Se may appear. After processing, the PMC via may be described as a non-uniformly doped electrolyte with a significantly reduced Ag doping concentration close to the bottom Ni electrode. Measured spectra of all the HRS PMC devices across via areas demonstrated similar characteristics that indicate presence of two regions within the chalcogenide via with different electrical characteristics. Based on the experimental impedance spectra and the physical characterization results discussed earlier, an equivalent circuit consisting of a contact resistance (R_{cont}) in series with two separate parallel RC configurations is extracted.

Figure 25 plots the imaginary components of complex impedance ($-Z''(\omega)$) (Figure 25(a)) and of its corresponding electric modulus ($M''(\omega)$) (Figure 25(b)) vs. their respective real components $Z'(\omega)$ and $M'(\omega)$ for a $100\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ PMC in HRS. The plots indicate two separate regions, each with separate RC time constants, corresponding to the equivalent circuit model in Figure 25(a).

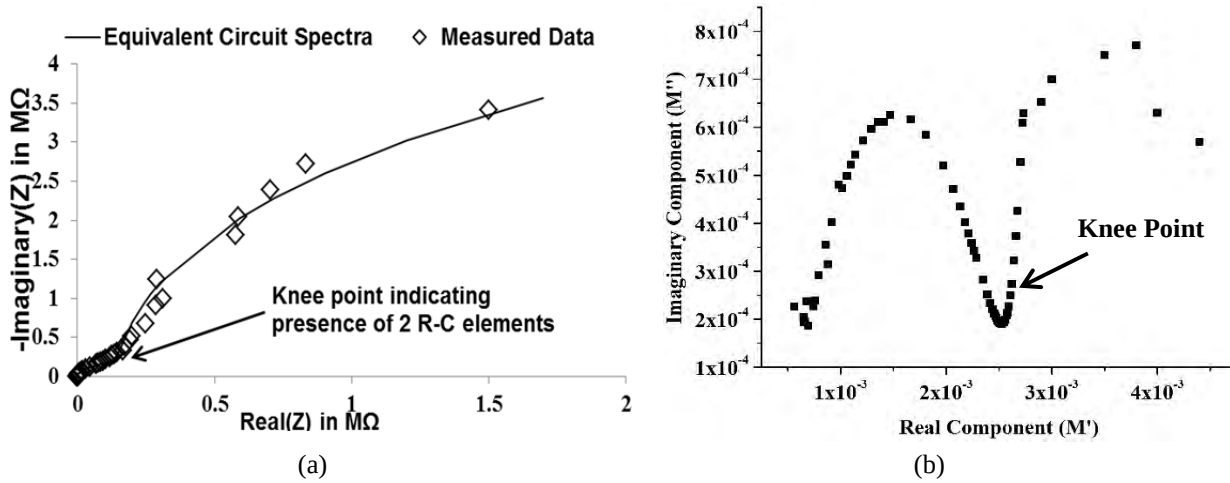


Figure 25. (a) HRS impedance spectra of a PMC device and (b) imaginary component vs. real component of electric modulus

Figure 26 illustrates a cross-section of a vertical ChG PMC in a high resistance state. The top RC configuration, composed of R_1 and C_1 , determines the impedance of the photo-doped portion of the ChG film and the second RC configuration, composed of R_2 and C_2 , is associated with the un-doped (Ag-poor) chalcogenide (ChG). Each of the parallel RC elements produces a semicircle in the complex impedance plane.

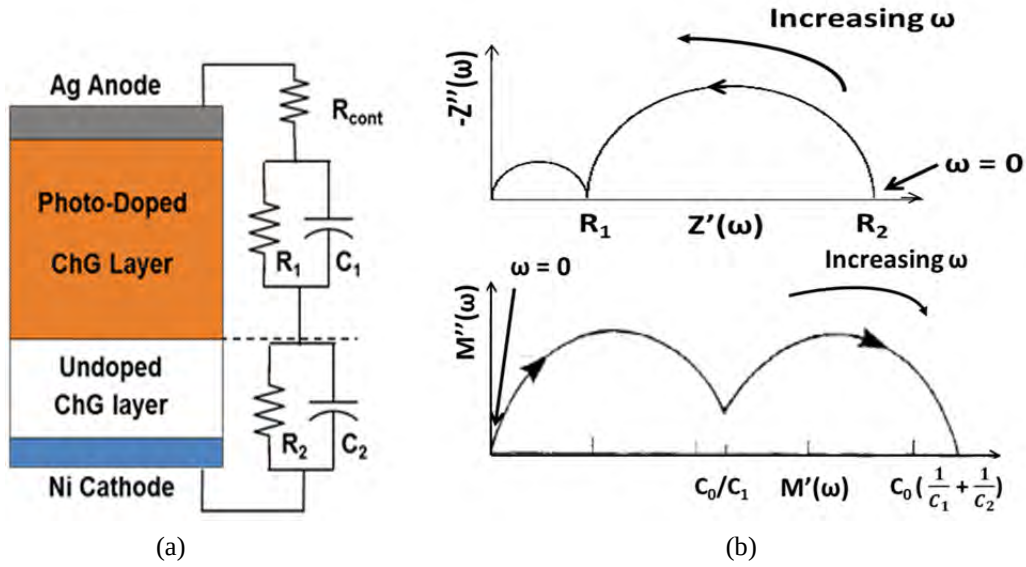


Figure 26. (a) HRS PMC RC equivalent circuit and (b) complex plane representation

Mathematically, the HRS PMC complex impedance is given by,

$$Z(\omega) = (R_1 \parallel \frac{1}{j\omega C_1}) + (R_2 \parallel \frac{1}{j\omega C_2}), \quad (1)$$

Using (1), the real and imaginary components of impedance can be derived (ignoring the small R_{cont}) as,

$$Z'(\omega) = \frac{R_1}{1 + (\omega R_1 C_1)^2} + \frac{R_2}{1 + (\omega R_2 C_2)^2}, \quad (2)$$

$$Z''(\omega) = \frac{R_1(\omega R_1 C_1)}{1 + (\omega R_1 C_1)^2} + \frac{R_2 \omega R_2 C_2}{1 + (\omega R_2 C_2)^2}, \quad (3)$$

Corresponding real and imaginary components of $M(\omega)$ can be derived as,

$$M'(\omega) = \left(\frac{(\omega R_1 C_1)^2}{1 + (\omega R_1 C_1)^2} \right) \cdot \frac{C_0}{C_1} + \left(\frac{(\omega R_2 C_2)^2}{1 + (\omega R_2 C_2)^2} \right) \cdot \frac{C_0}{C_2} \quad (4)$$

$$M''(\omega) = \left(\frac{\omega R_1 C_1}{1 + (\omega R_1 C_1)^2} \right) \cdot \frac{C_0}{C_1} + \left(\frac{\omega R_2 C_2}{1 + (\omega R_2 C_2)^2} \right) \cdot \frac{C_0}{C_2} \quad (5)$$

Figure 26(b) shows the complex plane plots using the analytical equations derived above.

The extracted value for R_{cont} , which primarily represents the resistance of the probe contact, was less than 100 Ω and is independent of via size. Figure 27 plots the average values for R_1 and R_2 as a function of via area, respectively. It can be seen that both R_1 and R_2 vary inversely with via area as expected. It can also be observed that R_2 (the resistance of the un-doped layer) is nearly

100 times greater than the resistance of the photo-doped layer, R_1 . Since the resistances are in series, it is the un-doped layer resistance that determines the DC HRS impedance. The HRS resistance ranges from approximately 10 M Ω for the smallest via area to approximately 200 k Ω for the largest.

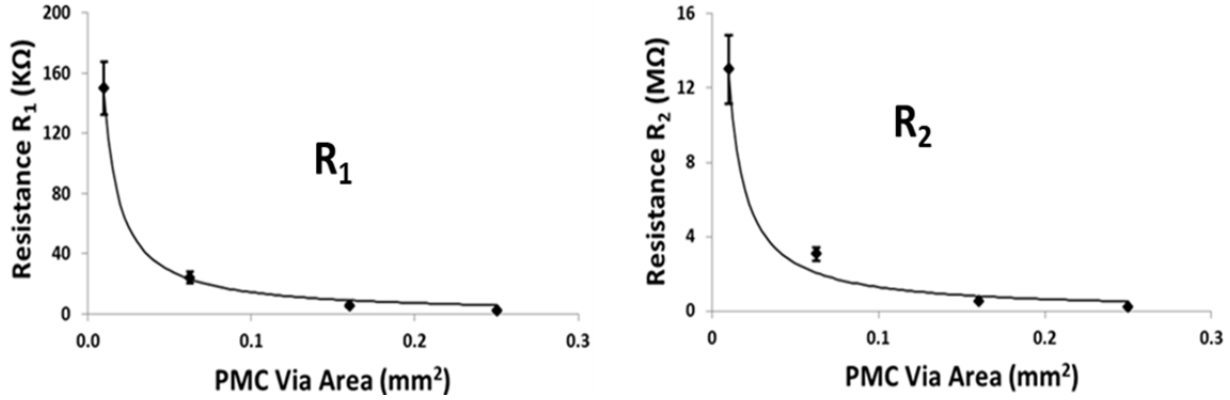


Figure 27. Plots showing scaling of HRS resistance parameters R_1 and R_2 with via area

Figure 28 plots the dependence of C_1 and C_2 on PMC via area. The capacitance of the photo-doped region (C_1) exhibits a higher-order, non-linear dependence on via area. This may be due to variations in the dielectric properties of Ag-doped GeSe caused by non-uniform incorporation of Silver into the material. As the Figure 28 (b) shows, unlike the capacitance of the doped chalcogenide material, the capacitance in the undoped layer (C_2) scales linearly with via area.

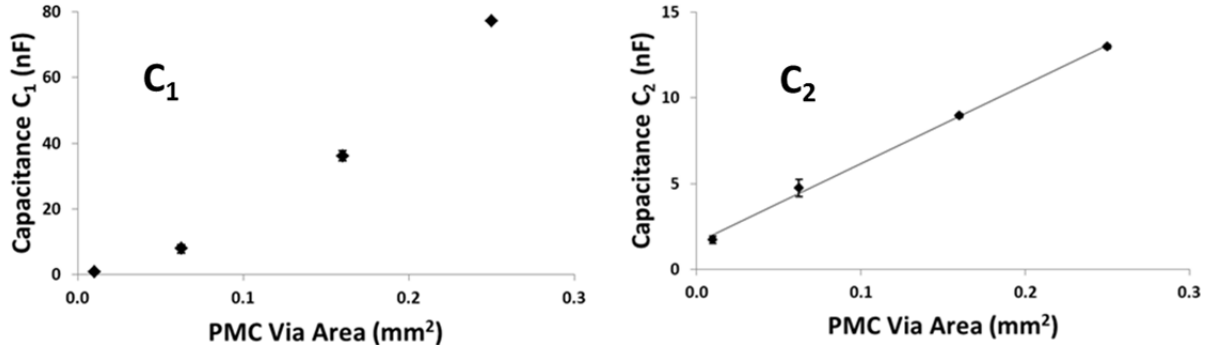


Figure 28. Scaling of HRS PMC capacitance parameters

4.2.1.2.3 LRS Impedance Spectra

During the write process (HRS to LRS switching), Ag^+ ions from the Ag-rich photo-doped layer drift towards the cathode, eventually creating a conductive Ag filament across the entire via. In this condition, the device is in LRS. The resistance across the chalcogenide film can now be assumed to be dominated by the resistance of the conductive filament and thus the LRS PMC can

be modeled as a contact resistance in series with one parallel RC element. The impedance of this configuration can be represented on the complex plane with a single semicircle.

Prior to small signal impedance measurement, a positive dc voltage sweep at a compliance (limiting) current of 10 μA was used to set each PMC device into a fixed low resistance state (LRS). The LRS device equivalent circuit shown in Figure 29 (a) is associated with a contact resistance R_{cont} , the on-state resistance, R_{on} , and the LRS device capacitance, C_{on} . A typical complex impedance Cole-Cole plot of a 100 $\mu\text{m} \times 100 \mu\text{m}$ device obtained experimentally is shown in Figure 29 (b).

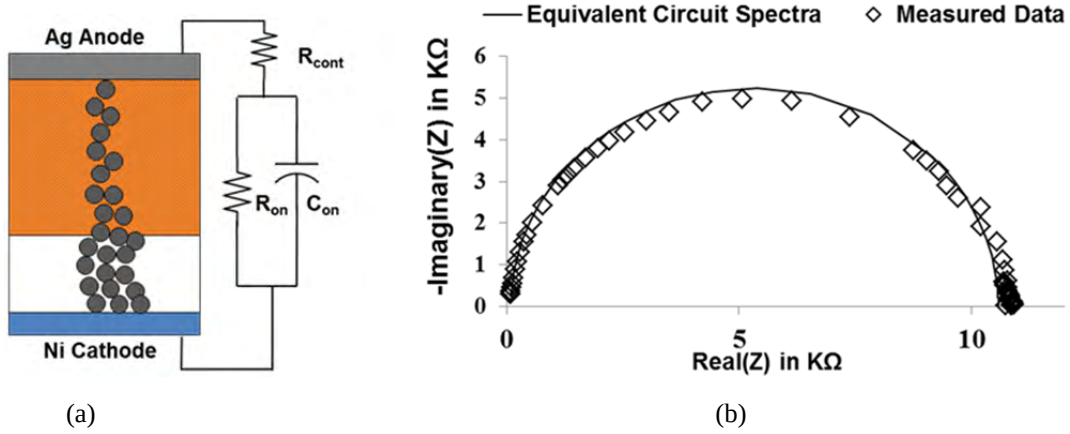


Figure 29. (a) LRS PMC equivalent circuit and (b) impedance spectra of a PMC device

Figure 30(a) plots average values of R_{on} vs. via area. As the figure shows, the on-state resistance is less than 10 $\text{k}\Omega$ and does not seem to depend on via size. This non-scalability can be attributed to the fact that R_{on} is determined by the resistance of the conductive Ag-filament formed across the film, which is probably independent of the device area. Finally, we observe the ratio of HRS to LRS resistance (R_2/R_{on}) ranges from approximately 2,000 for the smallest area device to 40 for the largest. Figure 30 (b) plots the dependence of the LRS capacitance, C_{on} , on PMC via area. As with the HRS capacitance in the un-doped layer, the capacitance, C_{on} , scales linearly with via area. When the device switches into the LRS condition, the filament creates a low resistance pathway between the anode and cathode terminals while the LRS capacitance C_{on} is then in effect, the series combination of HRS capacitances C_1 and C_2 , i.e.,

$$C_{\text{on}} = \frac{C_1 C_2}{C_1 + C_2} \quad (6)$$

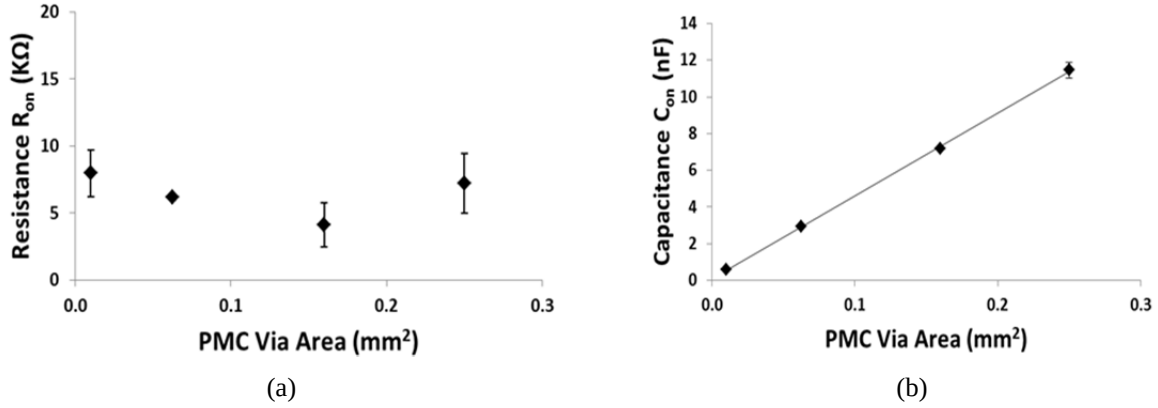


Figure 30. (a) LRS resistance parameter R_{on} vs. area and (b) LRS capacitance parameter C_{on} vs. area

Figure 31 plots the extracted C_{on} as well as its value, using the values for C_1 and C_2 obtained for the HRS fit. The good agreement between the two sets of values for C_{on} suggests that the application of a HRS to LRS switching bias has not appreciably altered the Ag concentrations across most of the doped and un-doped regions layers. Since the conductive filament formed in LRS is only a few tens of nm in diameter, a significant change in Ag concentration throughout the rest of the film is unlikely, especially considering the large dimensions of the devices (≥ 100 μ m) characterized. Therefore, in LRS the Ag concentration, aside from the filament, has not changed, and thus capacitances in the doped region, C_1 , and un-doped region, C_2 , have not been measurably altered.

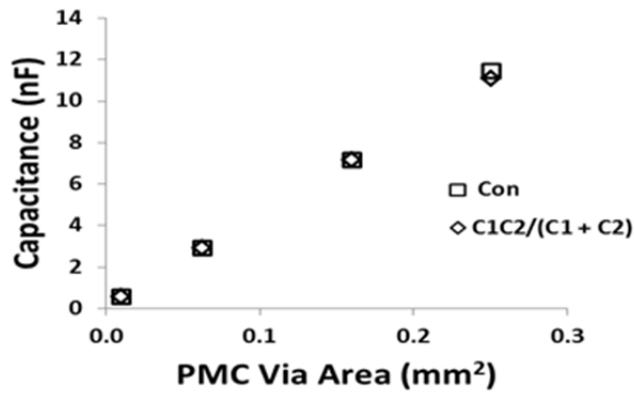


Figure 31. Capacitance vs. area showing close match between C_{on} and series combination of C_1 and C_2

Based on the linear scaling of extracted capacitance parameters C_2 and C_{on} , the capacitance per unit area of the PMC devices is calculated to be approximately 4.6 μ F/cm². The dielectric constant (ϵ_r) of the undoped chalcogenide layer can be calculated from the HRS capacitance (C_2)

per unit area (A) and the estimated thickness of the Ag layer (d) (which can be obtained from Ag profile measurement via EDS as shown in Figure 24) as,

$$\epsilon_r = \left(\frac{C_2}{A} \right) \cdot d / \epsilon_0 \quad (7)$$

Using an estimated Ag layer thickness of 5 nm as observed in the EDS measurements, the value of ϵ_r is calculated to be approximately 26.

4.2.1.2.4 Quasi-Static Switching Behavior Characterization

The characteristic switching behavior of PMC devices was experimentally measured using the standard voltage double sweep using an Agilent 4156C semiconductor parameter analyzer. Figure 32 (a) shows typical measured I-V characteristics, while Figure 32 (b) identifies the key electrical parameters that can be extracted from such a plot.

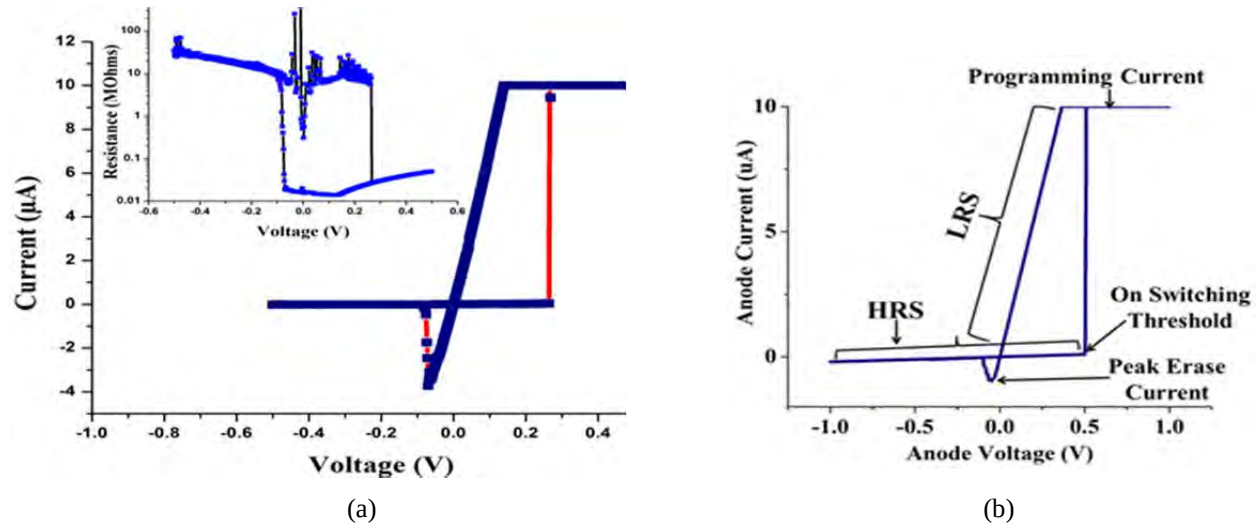


Figure 32. (a) DC I-V characteristics of a PMC and (b) with key parameters identified

PMC devices, like many other resistive memory technologies, demonstrate multi-level resistance programmability in its LRS state [9]. The most common demonstration of this property is performed by controlling the current through the device during programming, either using the in-built compliance current function of the 4156C instrument, or at circuit level by controlling the saturation drain current of the access transistor in a 1T-1R PMC element. The higher the programming current used, the lower is the final programmed LRS level. This is believed to be due to greater charge flow allowed at higher compliance leading to a thicker conductive filament (CF) in the LRS.

Switching behavior of Ag-GeSe PMC devices (5 μm x 5 μm cross section) was recorded over several cycles (≥ 25) for a wide range of compliance current levels.

Experimental I-V characteristics at 100 μA compliance current over 20 write-erase cycles are shown in Figure 33(a). Figure 33 (b) shows the decrease in LRS with increasing compliance current. Figures 33 (c) and 33(d) show the dependence of LRS and peak erase current respectively on compliance current. As shown in Figure 33 (c) that LRS (R_{on}) is dependent on the compliance current ($I_{\text{compliance}}$) as,

$$R_{\text{on}} = \frac{0.363}{I_{\text{compliance}}^{1.14}} . \quad (8)$$

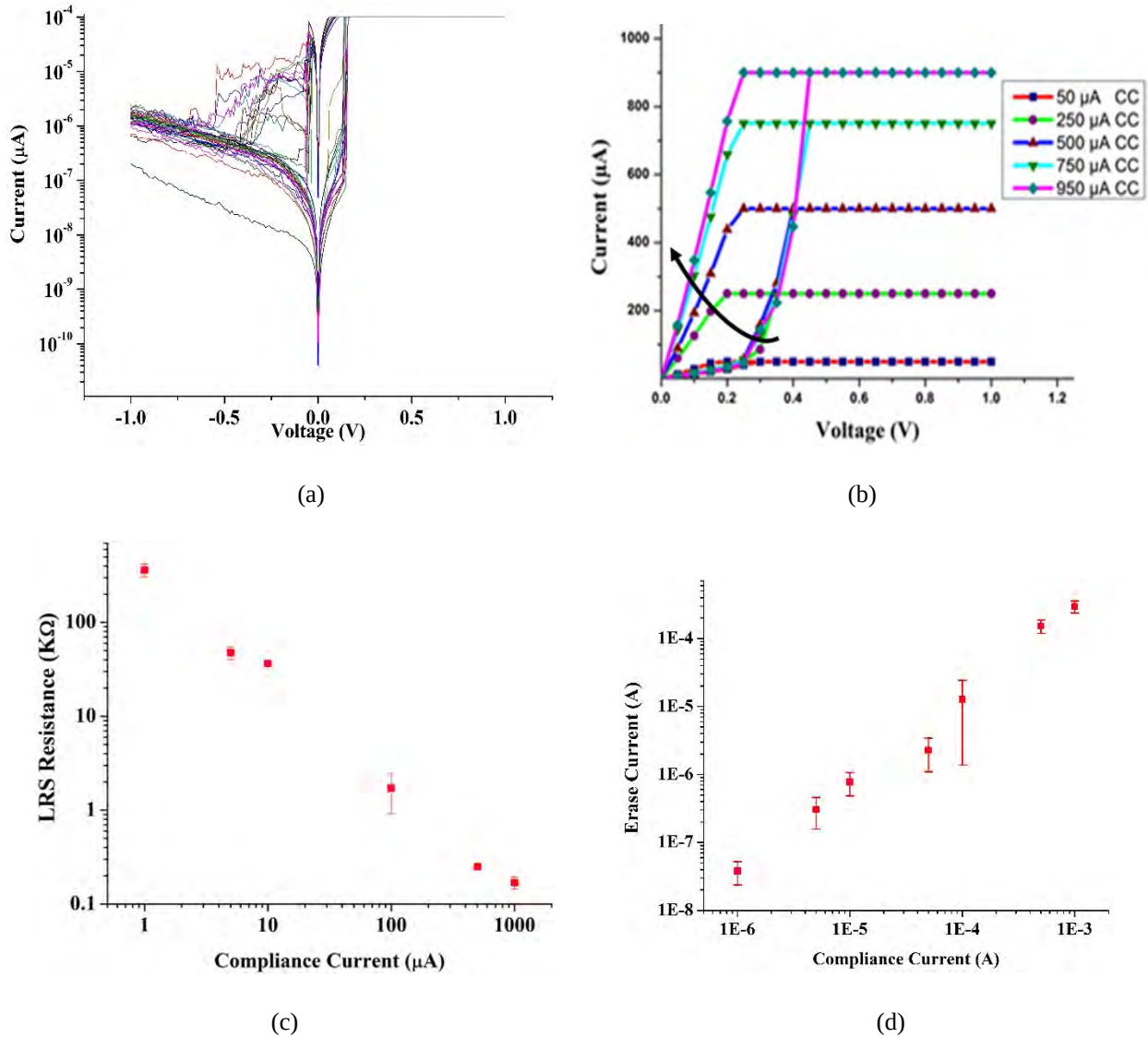


Figure 33. (a) Quasi-static I-V, (b) I-V for positive voltage sweep, (c) dependence of LRS resistance on compliance current and (d) dependence of peak erase current on compliance

Another test involved repeated DC sweeps performed at successively higher stop voltages so as to induce gradual change in resistance. The compliance current was not reached during these sweeps. A series of positive voltage double sweeps starting from 0 V with successively increasing stop voltages (from 65mV to 120mV) on an already ‘On’ device made it possible to observe gradual decrease in resistance, likely due to increase in CF diameter. Such a set of positive sweeps is shown in Figure 34(a). For each successive sweep, the device starts from the resistive state defined by the previous sweep. An identical test was then performed for performing gradual erase. A gradual increase in resistance was obtained by applying a series of negative voltage double sweeps with successively increasing stop voltages (from -0.5V to -1.5V for each successive sweep, as shown in Figure 34 (b). This is most likely due to a gradual decrease in the CF diameter.

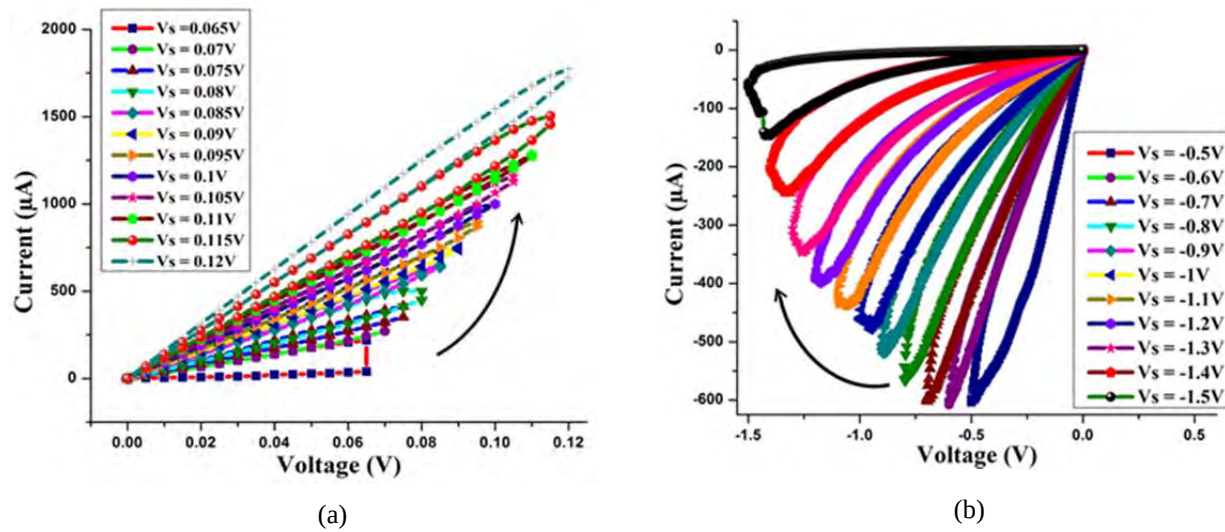


Figure 34. (a) Resistance decrease under positive dc bias and (b) resistance increase under negative bias

4.2.1.2.5 Resistance programming in transient (pulsed) mode

Transient characterization of the PMC involved applying positive and negative “write/erase” voltage pulses to decrease or increase the resistance of the device, respectively. The transient test setup is shown in Figure 35 (a). An arbitrary waveform generator (Tektronix AWG520) is used to generate voltage pulses of either polarity and of different magnitudes and pulse widths. The waveform generator output is applied to a PMC device in series with a current limiting resistor, R_L . In order to “read” the PMC resistance, a low voltage pulse is applied after each write/erase pulse. During the read operation, the voltage measured across the limiting resistor is used to sample the PMC resistance. The value of the limiting resistance is important. As mentioned previously, the change in PMC resistance is a function of current flowing through the cell. A lower value of resistance will allow a larger voltage drop across the PMC as well as greater current flow through the device. Thus the limiting resistor is one of the factors controlling the amount of change in PMC resistance in this setup. The “read” pulse magnitude is set low so as not to disturb the resistive state. For this purpose, a read pulse not greater than 200 mV

magnitude was used. Figure 35 (b) and Figure 35 (c) demonstrate a ‘hard’ write-erase operation whereby the PMC device is programmed to a LRS by a single positive pulse and then into a HRS by a single negative pulse. It is worth noting that the minimum voltage required to change the resistive state of the device is dependent on the voltage sweep rate. Hence minimum voltage required to switch the device is greater for pulsed voltage (with much faster sweep rates) compared to DC or quasi-static voltage.,

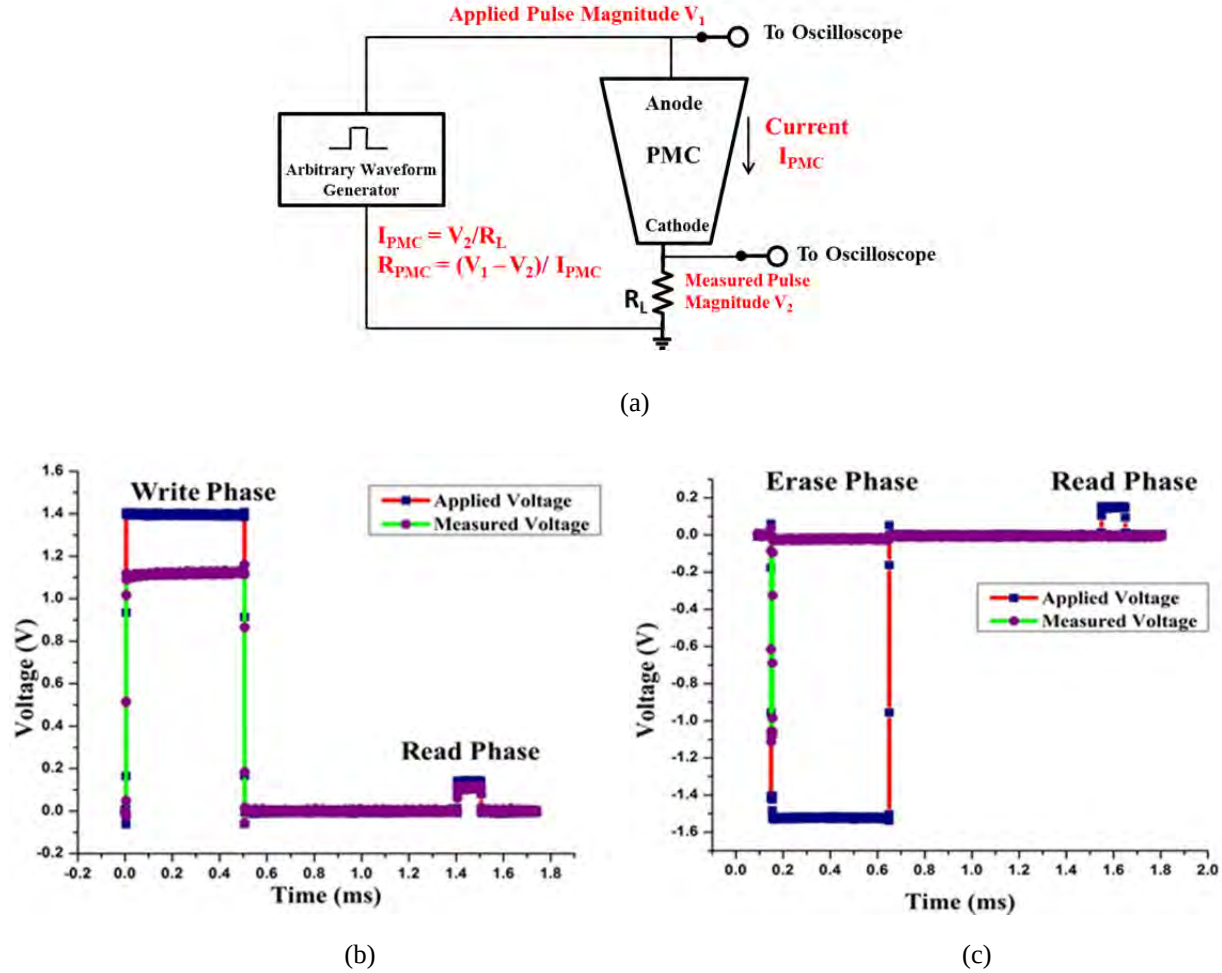


Figure 35. (a) experimental test setup, (b) PMC write and read voltage transients and (c) PMC erase and read transients

By varying the applied voltage magnitude and pulse width, the conductive filament lateral dimension and consequently the amount of resistance change in the device, can be controlled. So it is possible to set the device into different LRS by applying voltage pulses of same pulse duration but of different amplitudes. Figure 36(a) shows a typical write-erase operation used to demonstrate this behavior [10]. Figure 36 (b) shows distribution of experimentally measured LRS for voltage pulses of amplitudes between 1.4V and 2V and 25 μ s width. Multiple write operations (≥ 20) were performed starting from an initial HRS (≥ 0.5 M Ω). Figure 36(c) shows the mean and standard deviation of the LRS data presented in (b).

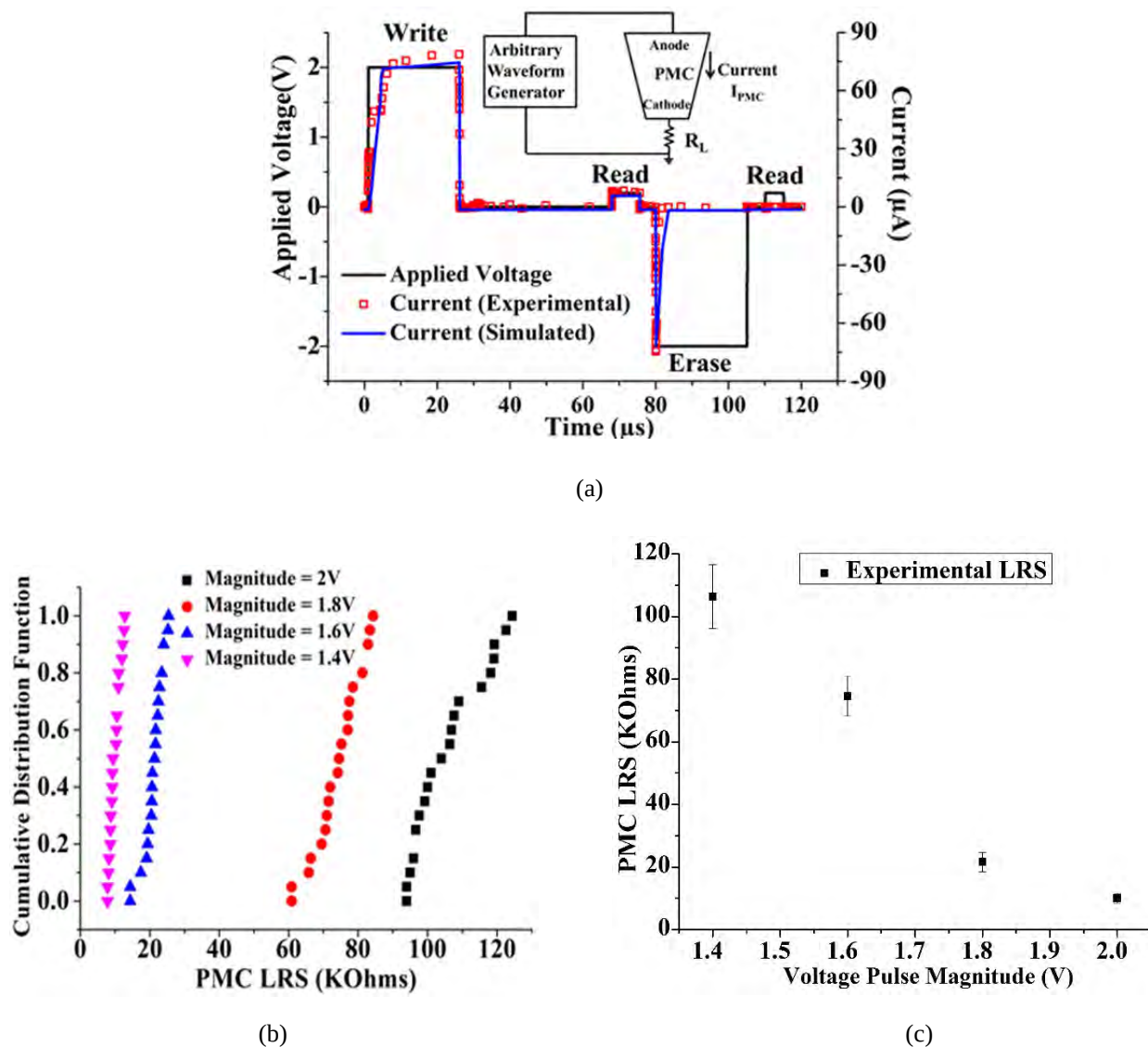


Figure 36. (a) Write-erase operation, (b) data showing multiple LRS and (c) LRS obtained from data of (b)

A potential application of the multi-level programmability of PMC devices and other resistive memory devices is in neuromorphic circuit applications where they can provide a compact single device implementation of the synaptic conductance modulation observed in biological neurons (analogous to numerical weight change in artificial neural networks). For an electronic synapse, its resistance should be capable of changing gradually with the application of a voltage pulse (each pulse being analogous to the voltage spikes generated by biological neurons for conductance modulation of synaptic pathways). Controlling the magnitude and pulse width will determine the amount of resistance change after each step. Figure 37 shows a typical experimental result obtained for incremental resistance programming using the current limiting resistor setup described earlier. The resistance of a PMC device was first gradually decreased to a low value and then gradually increased to restore the initial high resistance value. PMC

resistance values were calculated based on measured output voltage during read pulse applied after each step. These results are obtained for constant magnitude positive and negative voltage pulses for program and erase, respectively. $\pm 1.5\text{V}$ magnitude pulses were used of width $100\text{ }\mu\text{s}$ width for gradual programming and $200\text{ }\mu\text{s}$ width for gradual erase. From the measured resistance values, each program/erase operation can be estimated to cause an average change of approximately 3% of the initial and final PMC resistance before and after the program and erase sequence.

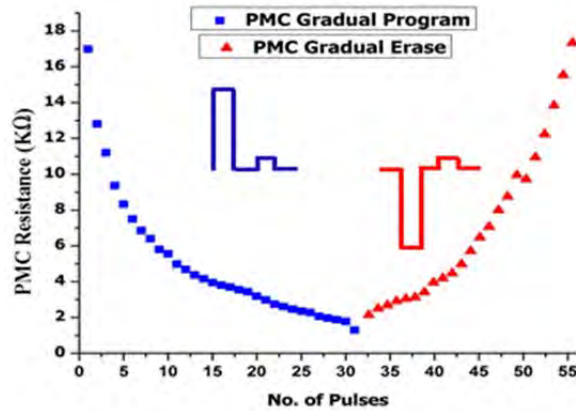


Figure 37. Incremental resistance programming of a PMC

To demonstrate the effect of applied voltage pulse width on the change in resistance, a sequence of programming voltage pulses with increasing magnitudes and fixed pulse width were applied to the PMC device as shown in Figure 38(a). Three different pulse widths of $100\text{ }\mu\text{s}$, $500\text{ }\mu\text{s}$ and 1 ms were used. The results are shown in Figure 38(b). It can be seen that the change in PMC resistance is accelerated by using longer pulse width, as the largest change in PMC resistance occurs for 1ms pulse width sequence followed by the sequence with $500\text{ }\mu\text{s}$ and lastly $100\text{ }\mu\text{s}$ widths. This behavior is expected, as longer pulse widths allow more radial CF growth.

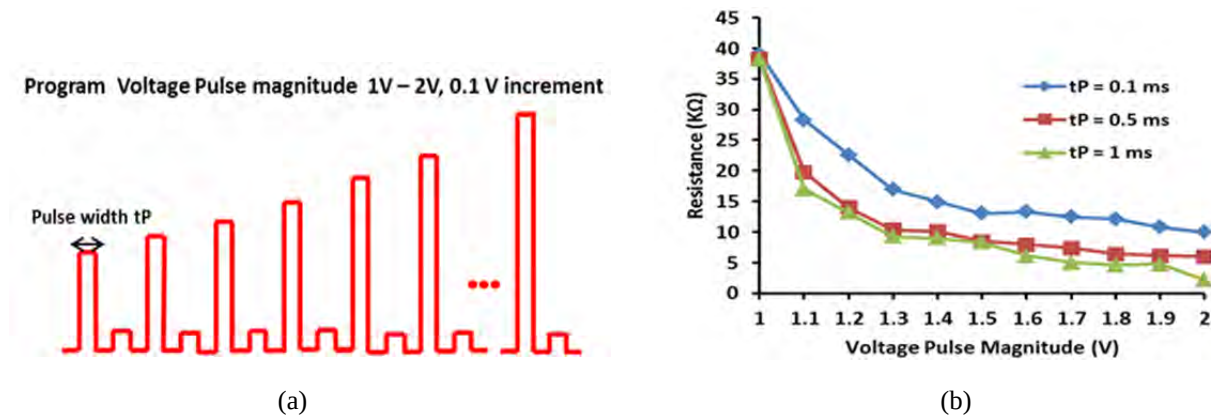


Figure 38. (a) Sequence of programming voltage pulses and (b) resistance vs. voltage pulse

4.2.2 Characterization of Vertical Cu-SiO₂ Programmable Metallization Cells

For Cu-SiO₂ PMCs, before any resistive switching occurs in a device, an activation process, also called electroforming, is usually needed to condition the SiO₂ layer. The electroforming voltage is generally greater than the set voltage for conventional resistive switching because a higher voltage is needed to alter the virgin SiO₂ matrix. Electroforming creates ‘channels’ in the dielectric which support cation transport. The electroforming step is also needed to ionize Cu and drive the metal ions into SiO₂ layer. Electroforming is necessary since the amount of copper in the as-fabricated SiO₂ is not enough to sustain proper resistive switching.

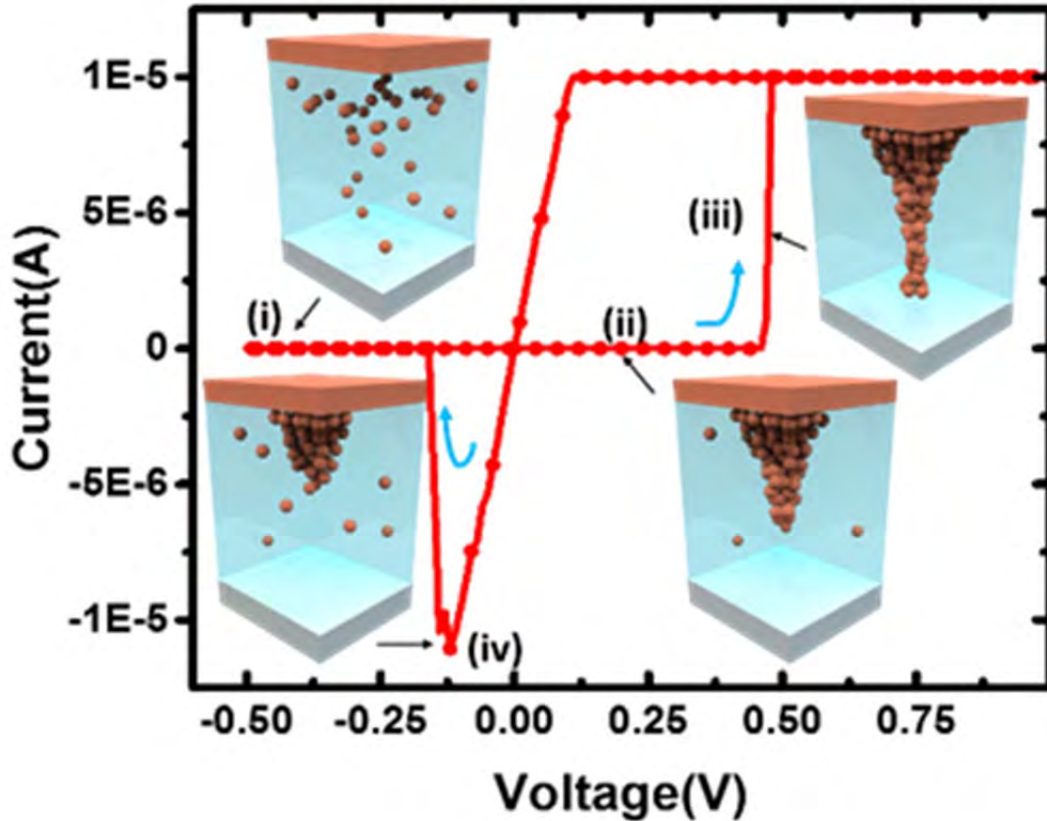


Figure 39. Schematic of SET and RESET operation of Cu-SiO₂ PMC

After electroforming, the Cu-SiO₂ device can be switched on and off, a typical resistive switching curve is shown in Figure 39. DC resistance switching can be described starting from a high-resistance state (OFF-state), where there is no electrodeposit of anode metal on the cathode (i). The device will change to a low-resistance state (ON-state) if the anode bias is increased to a positive set voltage (V_{set}) which is ~ 0.5 V for this technology. This transition involves three steps: step 1, the Cu anode is oxidized ($\text{Cu} \rightarrow \text{Cu}^{2+} + 2e^-$); step 2, Cu^{2+} cations drift away from the anode into the thin SiO₂ film; and step 3, the Cu^{2+} is reduced and nucleates (ii) according to reaction ($\text{Cu}^{2+} + 2e^- \rightarrow \text{Cu}$). In steps 1 and 2, the operation of the oxide-based PMC is similar to ChG PMC, but step 3 is somewhat different because, in the Cu-oxide system, reduction occurs

before the ion reaches the cathode. This is because cation mobility in oxides are lower than in chalcogenide glasses and, as will be shown later in this text, copper ions quickly neutralize because of their energy state in SiO₂. These differences reverse the direction of filament growth in Cu-SiO₂ PMCs. The device is switched to a low resistance state when the metal filament reaches the cathode and bridges the oxide (iii). At this point, the current increases dramatically until limited by the programed current compliance. The transition from the low-resistance state back to a high-resistance state is essentially the reverse of the set process, i.e., when a negative voltage bias is applied to the copper electrode, the metallic filament will be oxidized and dissolve into the SiO₂ (iv). As the copper anode is swept to a more negative bias, Cu²⁺ cations migrate back to the anode, where they are reduced. For anode voltages below the negative reset potential ($V_{\text{reset}} < -200$ mV) the device switches back to its high-resistance state (i).

Another important characteristic of Cu-SiO₂ PMCs is the multilevel switching ability. Like the ChG PMC the resistance value of low-resistance state, R_{on} , can be modulated by programming current (I_{prog} , or current compliance). The change of the low-resistance state can be explained by lateral filament growth. Once a copper filament is formed, further reduction causes a growth in filament radius. For higher programming currents, more Cu ions are generated and electrodeposited, resulting in a thicker filament. Figure 40(a) plots the multilevel switching curves of Cu-SiO₂ PMCs. The x-axis is voltage plotted in linear scale and y-axis is current plotted in logarithmic scale. The ON-state and OFF-state can be differentiated by programming currents as low as 50 nA.

We can also observe from Figure 40(b) that R_{on} decreases monotonically with the increasing of programming current following the power-law

$$R_{\text{ON}} = \frac{A}{I_{\text{prog}}^n}, \quad (9)$$

where A is a constant with unit of voltage, and n is a dimensionless number close to 1. In Figure 40 (b), I_{prog} and R_{on} are plotted on a log-log scale. Eight programming currents were used; and for each current, three 10um devices were tested and each device was swept for 10 cycles. All resistance values were read out at 100mV as marked in Figure 40 (a). As shown in the figure, the Cu/SiO₂/W PMCs can be repeatedly cycled over a wide range of ON-states, with switching current as low as 50 nA. Operating at such low current helps reduce the programming power consumed and extends battery life in remote systems.

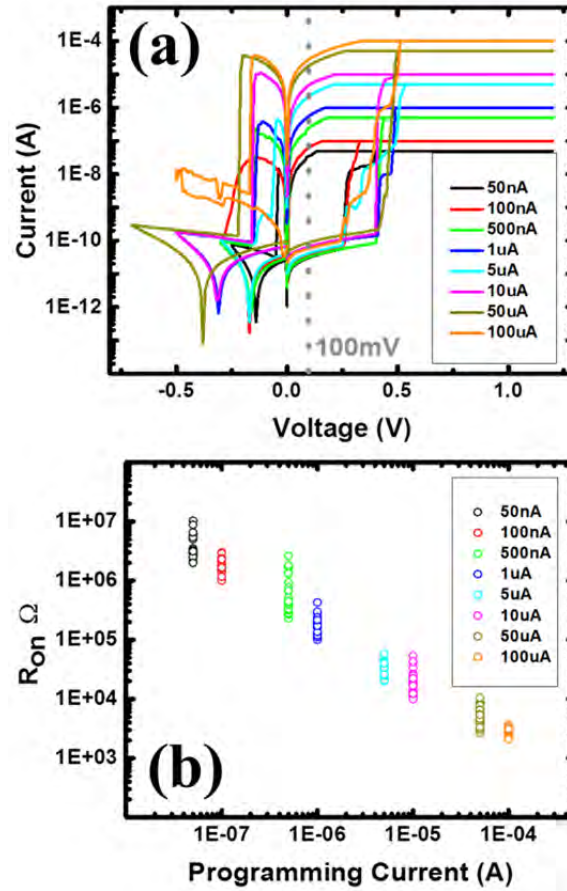


Figure 40. (a) I-V characteristics of multilevel switching, (b) R_{on} as a function of programming current

4.3 Conclusions

Material and electrical measurement performed on ChG and SiO₂ test structures have enabled a demonstration of device performance and produced data critical for the characterization of physical mechanisms. The use of lateral test structures has allowed us to characterize the process of active metal incorporation into ChG films through both optical and with EDS measurements. These data are necessary for validation of models developed in task 3. EDS measurements on vertical structures has also produced data describing the distribution of silver into ChG films after photodoping. These results combined with current-voltage and impedance spectroscopy, have enabled us, for the first time, to develop a passive equivalent circuit description of the devices in both high resistance and low resistance states. Parameters extracted from these data are critical to the construction of the numerical models developed in task 3. Time dependent pulsed measurement have demonstrated incremental resistance change, which is a capability necessary for the use of these devices in neuromorphic computing applications. Lastly, during this program, under this task, we have demonstrated for the first time a Cu-SiO₂ PMC device. Due to its inherent CMOS technology capability, the Cu-SiO₂ devices provides a new foundry ready alternative to the current ChG PMC.

The following list represents publications and conference presentations that were the outcome of work in this task:

1. D. Mahalanabis, Y. Gonzalez-Velo, H. J. Barnaby, M. N. Kozicki, P. Dandamudi, and S. Vrudhula, "Impedance Measurement and Characterization of Ag-Ge₃₀Se₇₀-Based Programmable Metallization Cells," *IEEE Transactions on Electron Devices*, vol. 61, pp. 3723-3730, 2014.
2. D. Mahalanabis, H. J. Barnaby, Y. Gonzalez-Velo, M. N. Kozicki, S. Vrudhula, and P. Dandamudi, "Incremental resistance programming of programmable metallization cells for use as electronic synapses," *Solid-State Electronics*, vol. 100, pp. 39-44, 2014.
3. W. Chen, H. J. Barnaby, M. N. Kozicki, Y. Gonzalez-Velo, R. Fang, W. Yu, S. Yu, K. Holbert, "A Study of Gamma-ray Exposure of Cu-SiO₂ Programmable Metallization Cells," IEEE Nuclear and Space Radiation Effects Conf., Boston, MA., July 2015.

5 TASK 3 – PHYSICS-BASED MODELING OF ELECTROCHEMICAL MEMRISTORS

5.1 Methods, Assumptions, and Procedures

Data, obtained from electrical and material characterizations, described in the previous task (2), support model development, validation and refinements. Material parameters associated with both the Ag-rich (photo-doped) and Ag-poor (unphoto-doped) layers in the ChG film are not well known. A precise physical model that captures the electrical behavior of the static PMC in both its low-resistance on-state (LRS) and high resistance off-state (HRS) has not developed. Neither computer models that characterize the dynamics of resistance switching, which informs the development of the compact model (task 4), nor the photo-doping process been produced.

The primary objective of this task is to model the PMC to simulate:

1. the electrical characteristic of a PMC in static HRS and LRS states and material parameters associated with the ChG film,
2. the dynamics of filament growth and resistance switching as a function of electrical stimulus,
3. ChG film electrostatics from electrochemical reactions,
4. the dynamics of active metal incorporation in ChG and SiO₂ films during the photo-doping process.

Density functional theory is used for modeling effort. These parameters include material bandgaps, band offsets, dielectric constants, effective carrier mobilities, defect levels, diffusion constants for Ag and other extrinsic species, and energies required for chemical reactions. ASU is working closely with software developers at Silvaco to enhance the capability of its simulation tool, ATLAS, to model the physics and electrochemistry of ChG-based memristors.

5.2 Results and Discussion

5.2.1 Static PMC model

The objective of this subtask is to model the ChG PMC with a device simulator and extract material parameters associated with the film when the device is in static HRS and LRS.

Parameter extraction is performed by adjusting material parameters, which include material bandgaps, affinities, dielectric constants, carrier mobilities and effective state densities, in order to fit simulation results to electrical data on actual PMC devices. These extracted values are compared to first principles calculations on GeSe films, as well as results reported in literature. Obtaining an accurate set of material parameters for both Ag-rich and Ag-poor ChG systems enables greater fidelity in PMC device simulation, which significantly enhances our ability to understand the underlying physics of ChG-based resistive switching memory.

5.2.1.1 Parameter Extraction Approach

After processing, the PMC structure may be described as a non-uniformly doped electrolyte with a significantly reduced Ag doping concentration close to the bottom Ni electrode. As can be seen from the Ag atomic profile shown in Figure 24, the Ag concentration in the $\text{Ge}_{30}\text{Se}_{70}$ is relatively low up to 5 nm from the cathode contact. This low Ag concentration will result in a high resistivity layer which will dominate the off state resistance of the PMC. During the write process (HRS to LRS switching), Ag^+ ions from the anode and from the Ag-rich photo-doped layer contribute to the formation of the metal filament along the length of the device, included in the lightly-doped region.

In order to extract parameters for the film in both its HRS and LRS, the ATLAS device simulator from the Silvaco suite of simulation tools is used to perform three-dimensional finite difference modeling on the structures. For the HRS case, two layers are defined, one Ag-rich region (Ag- $\text{Ge}_{30}\text{Se}_{70}$) with 55 nm thickness and one Ag-poor (un-photodoped $\text{Ge}_{30}\text{Se}_{70}$) with a thickness of 5 nm. For the LRS model, the structure must be modified to include another region as a grown conductive Ag filament across both layers in the electrolyte. The diameter of this filament in the model is estimated at 5 nm from the on-state resistance data and conductivity values obtained for Ag filaments at room temperature from previous works [11].

The cylindrical TCAD structures used for the HRS and LRS models are shown in Figures 41 and 42

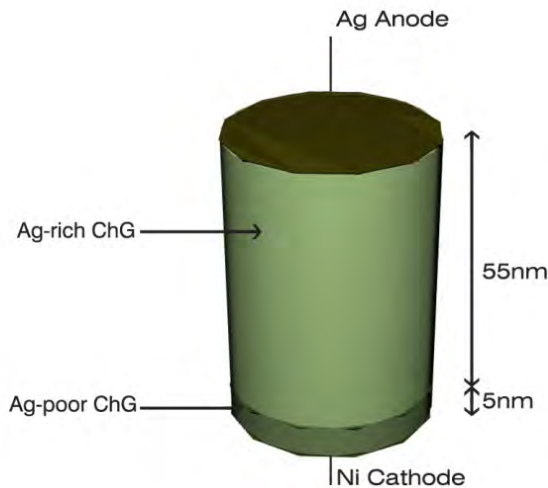


Figure 41. The PMC off-state (HRS) model

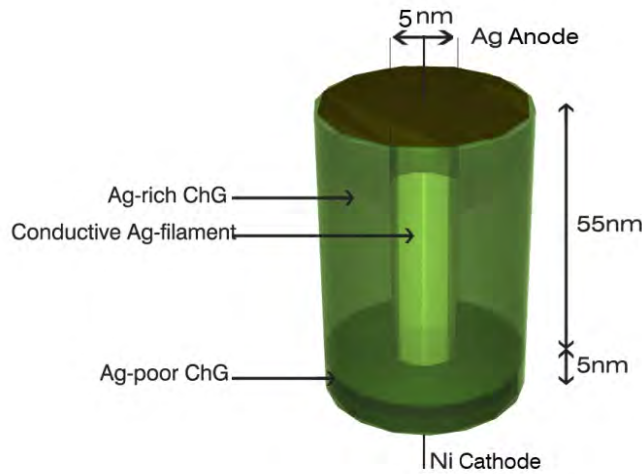


Figure 42. The PMC on-state (LRS) model

Finally, in order to complete parameterization, both HRS and LRS device conditions are modeled with the RC networks (Figure 43). Figure 43(a) shows that when the PMC is in the HRS, it can be modeled as a passive RC network composed of two parallel RC configurations. The HRS RC configuration composed of R_1 and C_1 determines the impedance of the photo-doped layer of the chalcogenide film. The R_2 and C_2 configuration is related to the un-photodoped chalcogenide layer. In the LRS, the resistance across the chalcogenide film can be assumed to be dominated by the resistance of the conductive filament and thus the LRS PMC can be modeled as one parallel RC circuit as it is shown in Figure 43(b).

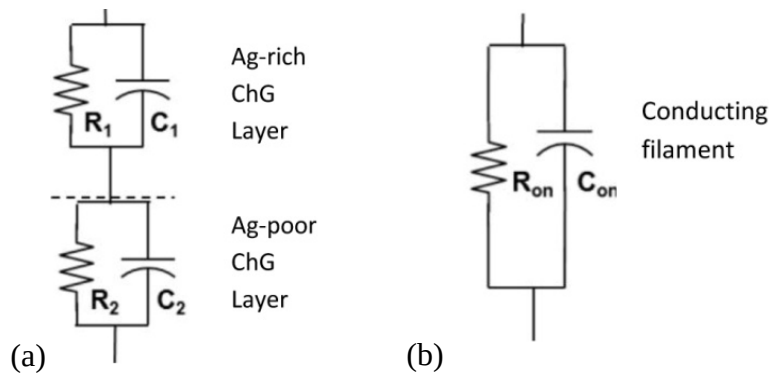


Figure 43. (a) HRS PMC and (b) LRS PMC

By fitting the HRS and LRS equivalent circuit impedance formulas to the experimental data, all resistance and capacitance values related to the Ag-poor, Ag-rich and conducting filament regions can be extracted. After extraction of the equivalent RC network parameters in both HRS and LRS, parameters for doped and un-doped ChG films are determined by adjusting material constants used by the simulator in order to fit the extracted resistance and capacitance values.

These constants include bandgap, density of states in conduction and valence bands, electron affinity, intrinsic carrier concentration, electron and hole mobility and dielectric constant for the Ag-rich and Ag-poor regions as well as the filament parameters in the LRS case.

5.2.1.2 Results

All the resistance and capacitance values related to the Ag-poor chalcogenide, Ag-rich chalcogenide, and conducting filament layer for PMCs with via diameters of 250 μm , 400 μm and 500 μm are obtained from the data and reported in Table 2.

Table 2. HRS and LRS states for equivalent RC circuit model

Via Diameter Size	250 μm	400 μm	500 μm
$R_1(\Omega)$	5	4.8×10^3	2.1×10^3
$R_2(\Omega)$	2	1.8×10^5	1.2×10^5
$C_1(F)$	2×10^{-8}	3.5×10^{-8}	7.7×10^{-8}
$C_2(F)$	3.6×10^{-9}	9.1×10^{-9}	1.3×10^{-8}
$R_{on}(\Omega)$	9.8×10^3	6.4×10^3	5.3×10^3
$C_{on}(F)$	2.9×10^{-9}	7.2×10^{-9}	1.1×10^{-8}

From capacitance values, the dielectric constant of each photo-doped (Ag-rich) ChG layer and unphotodoped (Ag-poor) ChG layer can be obtained using the Eq. (10)

$$C = \frac{k\epsilon_0 A}{t_l} \quad , \quad (10)$$

where, A is the via/device area, t_l is the thickness of that layer, and k is the semiconductor dielectric constant used in that layer.

The on-state resistance for all the PMCs with three different via sizes does not seem to be strongly dependent on via size. This non-scalability can be attributed to the fact that R_{on} is determined by the resistance of the conductive Ag-filament formed across the film, which is likely independent of the device area. So in our simulation an Ag metallic filament with 5 nm diameter and conductivity of $5 \times 10^3 \Omega^{-1}\text{cm}^{-1}$ [11, 12] is used to model the LRS resistance across the chalcogenide film.

The filament diameter is calculated from Eq. (11)

$$d = 2 \sqrt{\frac{\rho \cdot l}{\pi \cdot R_{\text{on}}}} \quad , \quad (11)$$

where, ρ is the filament resistivity, l is length of the filament, and R_{on} is the on-state resistance.

By adjusting the material parameters used by the ATLAS simulator to fit the experimental data, parameters for the Ag-rich and Ag-poor regions have been extracted and reported in Table 3. These values are in good agreement with those from previous works. For example, the bandgap and affinity difference between Ag-poor $\text{Ge}_{30}\text{Se}_{70}$ and Ag-rich $\text{Ge}_{30}\text{Se}_{70}$ regions is 0.3 eV which is similar to values reported in [13].

Effective densities of states were obtained from density functional theory (DFT) calculations, in the generalized gradient approximation, applied to crystalline GeSe_2 . We used QUEST, a local orbital code that uses double-zeta-quality basis functions plus polarization basis elements. We also used the Perdew-Burke-Ernzerhoff (PBE) exchange-correlation functional, Hamann pseudopotentials, and Monkhorst-Pack k-space gridding.

The effective density of states was obtained from equations in standard semiconductor theory starting from Eq. (12) which is valid in the conduction band,

$$n = \int_{E_c}^{\infty} n(E) \cdot f(E) d(E) \quad . \quad (12)$$

Here $n(E)$ is the density of states in the conduction band, $f(E)$ is the probability of occupation, i. e. the Fermi-Dirac distribution function, and E_c is the energy at the conduction band edge. The standard analysis then assumes parabolic band structure, so that Eq. (13) can be written

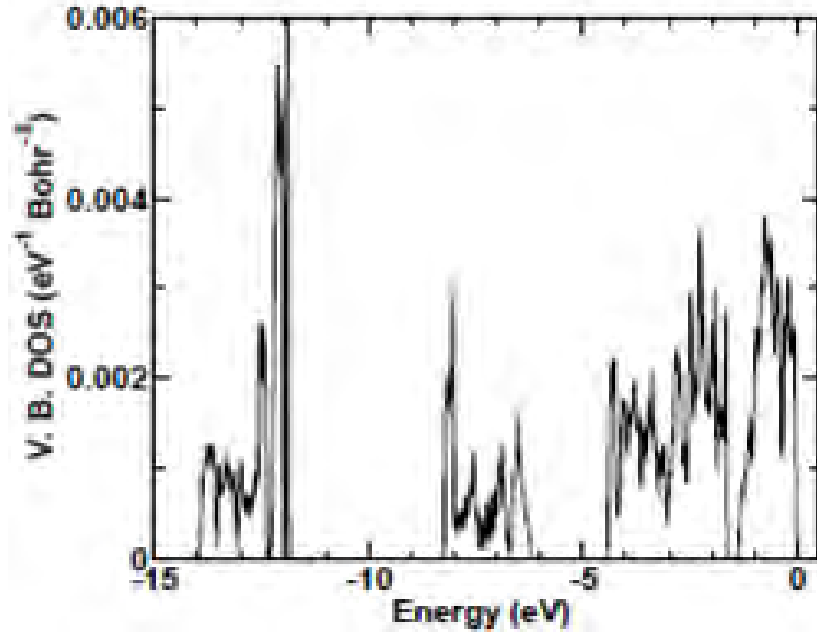
$$n = \frac{2 N_c}{\sqrt{\pi}} F_{\frac{1}{2}}(\eta_c) \quad , \quad (13)$$

where N_c is an effective density of states, $F_{\frac{1}{2}}(\eta_c)$ is the order $\frac{1}{2}$ of Fermi-Dirac integral, η_c is $(\varepsilon_F - E_c)/k_B T$, ε_F is the Fermi level, E_c is the energy at the conduction band edge, k_B is Boltzmann's constant, and T is the absolute temperature.

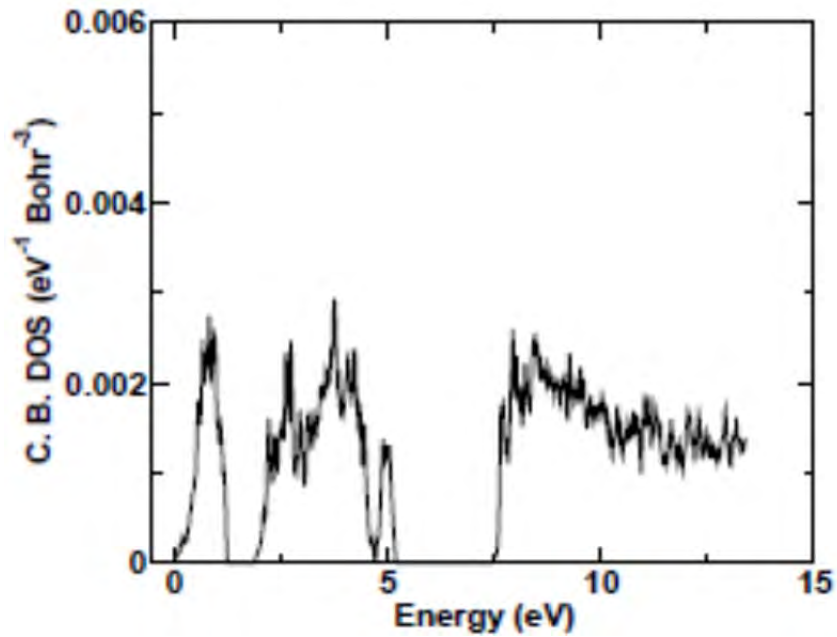
For non-degenerate semiconductors, Eq. (14) reduces to

$$n = N_c \exp\left(\frac{\varepsilon_F - E_c}{k_B T}\right) \quad . \quad (14)$$

There is an analogous expression for N_v , the effective density of states in the valence band. Because the band structure in Ge-Se compounds can be non-parabolic, we evaluated Eq. (12) using the calculated, DFT density of states (DOS), and then took advantage of Eq. (14) to evaluate N_c . Reliable values of N_c and N_v required a dense Monkhorst-Pack grid (2034 k-points in a 48-atom unit cell). The calculated DOS in the valence and conduction bands are shown in Figure 44.



(a)



(b)

Figure 44. (a) Calculated DOS for GeSe₂ in valence band and (b) conduction band

The values used for N_C and N_V in the simulations reflect the slopes of each DOS function, which, in turn, reflect the curvatures at the respective band edges, shown in Figure 45. As expected, the

effective density of states in the valence band is much larger ($\sim 10X$), reflecting the nearly flat valence band edge.

The intrinsic electron concentration reported in Table 3 is calculated using the obtained values for N_c and N_v as

$$n_i = \sqrt{N_c N_v} \exp\left(\frac{-E_G}{2KT}\right) \quad (15)$$

The charge carrier drift mobility values in low conductivity materials of disordered structure are independent of technology. In our model we assumed very low mobility for the electrons and a hole mobility of $100 \text{ cm}^2/\text{Vs}$ at room temperature. Figure 46(a-f) shows the real and imaginary parts of the impedances versus frequency (from 10Hz to 1MHz) for both HRS and LRS of the simulated PMC devices with via diameters of $250 \mu\text{m}$, $400 \mu\text{m}$ and $500 \mu\text{m}$. To see how well the simulation results are correlated with the impedance spectra data, the measured data are also shown on the same figures. At low frequencies from real part $R_1 + R_2$ for the off state and R_{on} for the on state can be extracted. Since we know in a parallel RC circuit the maximum for the imaginary part happens at $\omega = \frac{1}{\sqrt{RC}}$, C_1 , C_2 and also C_{on} can be estimated. The excellent fit between simulation and impedance experiment data shows the accuracy of our model in parametrizing the Ag-rich and Ag-poor $\text{Ge}_{30}\text{Se}_{70}$ material for next PMC static behavior studies.

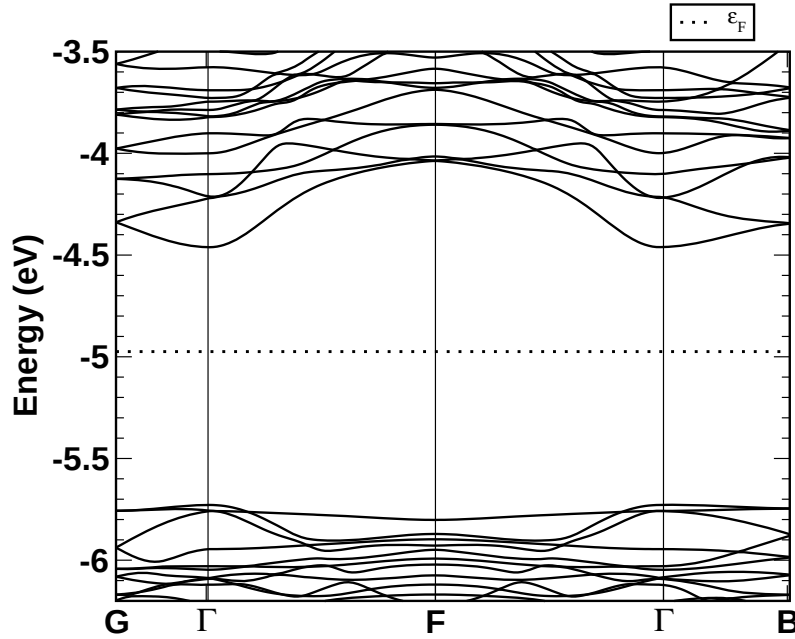
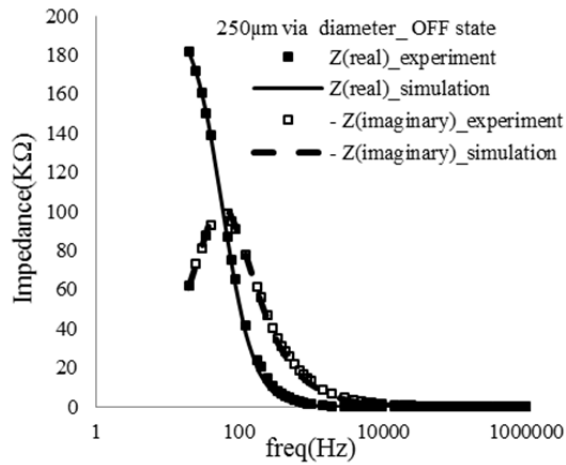


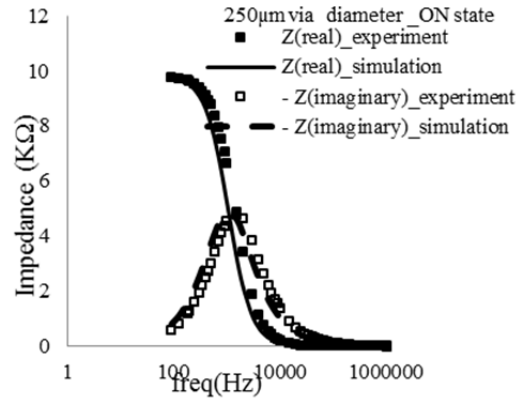
Figure 45. DFT band structure for crystalline GeSe_2

Table 3. The static parametric model for Ge₃₀Se₇₀

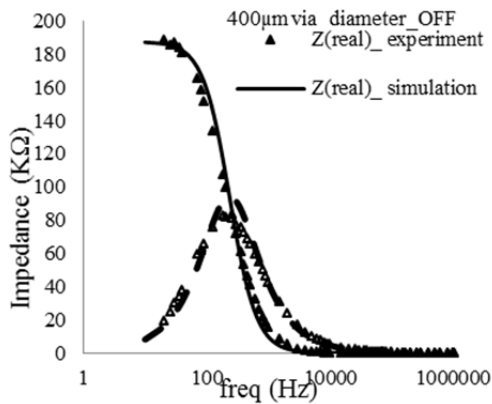
	Ag-poor Ge ₃₀ Se ₇₀	Ag-rich Ge ₃₀ Se ₇₀	Ag metallic filament
Bandgap (eV)	1.86	1.56	–
Affinity (eV)	3.05	3.35	–
Density of States in Conduction Band (per cc)	1	1	–
Density of States in Valence Band (per cc)	1	1	–
Intrinsic Carrier Concentration (per cc)	2.52×10^6	7.61×10^3	–
Electron Mobility (cm ² /Vs) ^c	1×10^{-5}	1×10^{-5}	–
Hole Mobility (cm ² /Vs)	10	10	–
Dielectric Constant	40.9	1.7	–
Conductivity ($\Omega^{-1} \cdot \text{cm}^{-1}$)	–	–	5



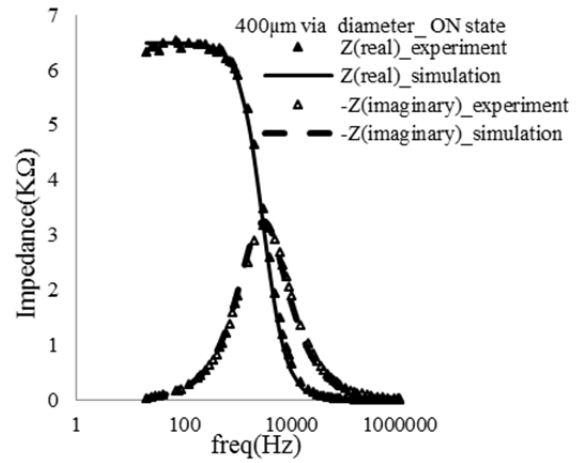
(a)



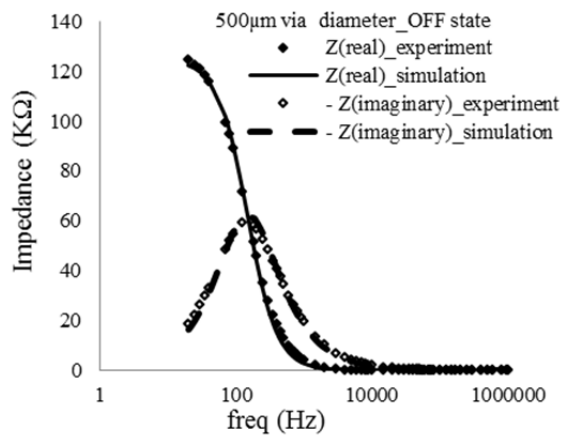
(d)



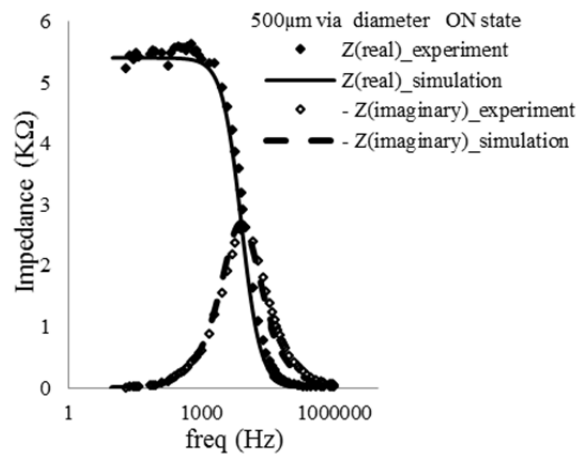
(b)



(e)



(c)



(f)

Figure 46. The PMC simulated impedance

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5.2.2 Dyanamic TCAD model for PMC operation

5.2.2.1 Model Equations

Finite element simulations are performed with Silvaco Atlas on a cylindrical structure representative of a three layer PMC. Figure 47 shows the structure with the anode, electrolyte and cathode layers from top to bottom. The ChG film electrolyte is modeled as a wide bandgap semiconductor. Table 4 reports the material constants used for the electrolyte and electrodes, which were extracted above and reported in [14] and obtained from density functional theory (DFT) calculations.

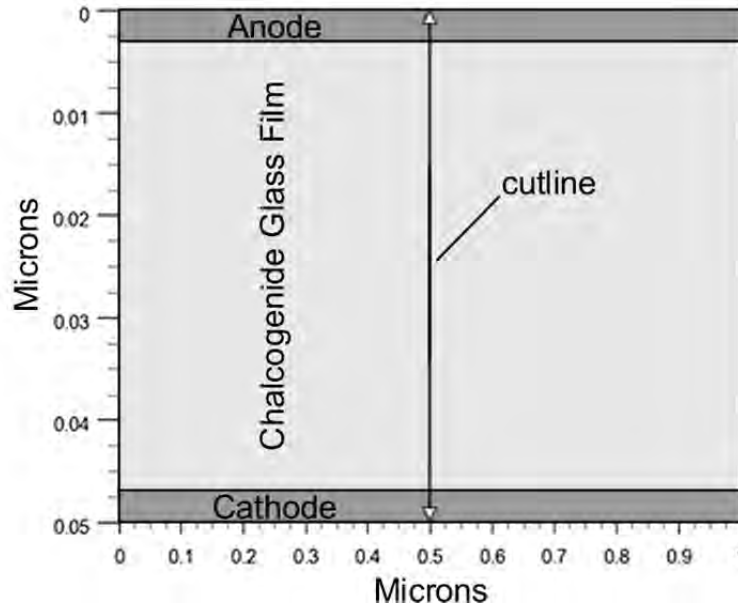


Figure 47. Two dimensional FE simulation structure

Table 4. Material constants used in Atlas simulation

ChG bandgap	1.86 eV
Dielectric Constant	40.9
ChG affinity	3.05 eV
Anode work function	4.6 eV
Cathode work function	4.2 eV

Atlas solves standard carrier statistics and transport equations for semiconductors. Additional models are utilized to simultaneously perform ion transport and reaction calculations on the structure. Continuity equations for the model are expressed analytically as

$$\frac{dN_{Ag^+}}{dt} = -(\nabla F_{Ag^+}) - (R_{Ag^+}) + (G_{Ag^+}) \quad (16)$$

$$\frac{dN_{Ag}}{dt} = -\nabla F_{Ag} - R_{Ag} + G_{Ag} \quad (17)$$

$$\frac{dn}{dt} = -\nabla F_n - R_n - G_n \quad (18)$$

where N_{Ag}^+ , N_{Ag} , and n are the concentrations of Ag^+ , neutralized Ag, and electrons, respectively. The flux for each species, i.e., parameter F_X in Eqs. 16-18, is obtained from the drift-diffusion equations

$$F_{Ag^+} = -(D_{Ag^+}) \left(\frac{q\nabla\Psi}{kT} + \nabla N_{Ag^+} \right) \quad (19)$$

$$F_{Ag} = -D_{Ag} \nabla N_{Ag} \quad (20)$$

$$F_n = -D_n \left(-\frac{q\nabla\Psi}{kT} + \nabla n \right) \quad (21)$$

where D_{Ag^+} , D_{Ag} , and D_n are the diffusion constants for Ag^+ , neutralized Ag, and electrons, respectively, and Ψ is the potential within the simulated electrolyte. The Ag^+ diffusion constant is estimated from first principles calculations using the diffusivity approximation

$$D = a^2 f \exp\left(\frac{-E_A}{kT}\right) \quad (22)$$

where a is the average hopping distance of the particle, f is the attempt to escape frequency, and E_A is the activation energy for hopping. E_A comes directly from atomistic calculations using the nudged elastic band method. Preliminary investigations of interstitial Ag^+ in a crystalline model of Ge_2Se_3 indicates activation energies greater than 2.5 eV within the layer while transport along the layer surfaces has much lower activation energy of approximately 0.5 eV. The attempt-to-escape frequency is taken from vibrational calculations showing $\sim 5 \times 10^{11} \text{ s}^{-1}$. The hopping distance is approximately 7 Å. Plugged into Eq. 22, these predict a diffusivity of about $1.0 \times 10^{-11} \text{ cm}^2/\text{s}$ at room temperature. The recombination and generation terms in equations Eqs. 16-18 capture the kinetics of the forward and reverse chemical reactions expressed as



The forward and reverse reactions are described by Eq. 24 and 25, respectively.

$$R_{Ag^+} = R_n = G_{Ag} = k_{Fwd} \exp\left(\frac{-E_{AFwd}}{kT}\right) (N_{Ag^+})(n) \quad (24)$$

$$G_{Ag^+} = G_n = R_{Ag} = k_{Rev} \exp\left(\frac{-E_{AREv}}{kT}\right) (N_{Ag}) \quad (25)$$

The forward and reverse reaction rate coefficients, k_{Fwd} and k_{Rev} , and forward and reverse activation energies, W_{AFwd} and W_{AREv} , are also estimated using the first principles, DFT calculations.

5.2.2.2 Generic Ion Model Explained

Atlas allows for doping profiles of species to be defined for the generic ion transport and reaction models where the species are neutral and charged particles that can react with each other and free carriers. For a PMC, a neutral species (sp0) could represent Ag, and a +1 charged species (sp1) could represent Ag^+ . To serve as the source of Ag^+ , the structure is initially doped with sp1. A built-in electric field due to the electrode work function difference forces sp1 toward the anode in equilibrium. Initial equilibrium yields a high gradient in the sp1 doping profile within the electrolyte with greatest concentration next to the anode as shown in Figure 48.

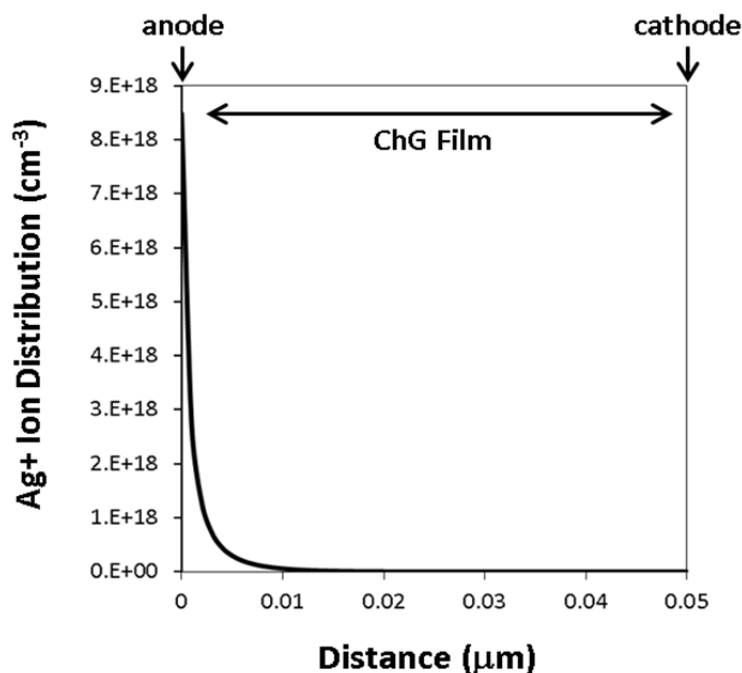


Figure 48. Distribution of Ag^+ in equilibrium along vertical, center cutline (Figure 47)

Upon applying a voltage greater than the write threshold voltage to the anode, sp1 begins to transport toward the cathode. The required process from there is to have sp1 meet an electron at the cathode to recombine with and form sp0, representative of neutral Ag. Subsequent sp1 should then be able to recombine upon reaching the newly formed sp0. That process should repeat thereby forming a bridge of sp0 from the cathode back to the anode.

Unfortunately, the species cannot behave as required to simulate PMC operation. The species can only transport, react with other species and free carriers, and simply exist as arbitrary neutral or charged dimensionless particles. The species exist in concentration rather than as individual particles that fill discrete spaces and the species cannot react with the device materials. Therefore, the species are not capable of forming any type of phase, conductive or not, which is required for the filament.

There is another problem even if the species could form regions of greater conductance. The long-range disorder in ChG solid-electrolyte provides fast transport channels for Ag^+ [15]. Those channels would determine the possible routes of Ag^+ and, consequently, possible shapes of the filaments. Atlas cannot simulate those channels for the species to navigate and fill. Unlike Ag in nano-voids, the species move unrestricted in location, and their concentration gradients are relatively gradual.

Atlas performs some computational physics that need to be applied to the PMC such as standard carrier statistics and carrier transport; however, its generic ion transport and reaction model currently has shortfalls making it incapable of simulating a PMC. Atlas is not made to simulate electrochemical devices, such as the PMC, in which metal is rearranged. No FEA software suitable for a PMC has been reportedly developed as of yet.

5.2.2.3 Generic Ion Model Workaround

A workaround was devised to address the non-conductance of sp0, which is the neutral species representing neutral Ag in the electrolyte. First, a bit more explanation of the simulation in Atlas is necessary. Atlas has a transient solution mode which is used to simulate the quasi-DC measurement. Like the quasi-DC measurement, a transient simulation is a series of small voltage steps over time. The transient setup is defined by the initial and ending voltage, total ramp time, and a maximum time step between voltage steps. A solution is calculated at each voltage-time step. The voltage increment between solutions is not explicitly defined. The time step (and voltage step) may be dynamically reduced if the solution does not converge with the maximum step. If the generic ion model could produce a conductive filament, then simulation of the PMC switching on would consist of a single voltage-time sweep. Because sp0 is not conductive, a workaround is necessary to add something conductive in place of sp0 as it occurs. The conductance of the filament is important even before the electrodes are bridged, because as the filament shrinks the distance between the electrodes the electric field increases even with a constant voltage applied. In turn, the growth rate and selectivity of the filament is expected to increase.

The idea of the workaround is to split the single transient simulation into many transient simulations. Then, n-type dopants (donors), serving as the conductive material, can be added to match the doping profile of sp0. The result is that a bridge of donors is grown across the electrolyte. While this is not equivalent to the precise nature of neutral Ag in the film, the conversion does effectively reduce the resistance across the film as sp0 grows with increasing anode voltage. Inserting metal instead of donors would seem like a better option, but that is not an option in Atlas. All metal is simulated as ideal metal, which means it has no resistance. While that could possibly work during vertical filament growth, the simulation would prematurely cease upon bridging. Only one electrode would exist at that time, and Atlas requires two or more electrodes. There are several pieces required for this multipart simulation including, an initial input deck, a running input deck, a Python script to generate doping profiles from the output structure files, an AWK script to update the running deck, and another Python script to bring these pieces together for an automated multipart simulation.

The finite element model multipart transient simulation is performed by increasing the voltage on the anode in 0.1V increments up to 0.9V while the cathode is fixed at 0V. The voltage ramps up in 1 μs and is held at each increment for 10 μs . The sp1 (Ag^+) concentration at voltages of 0V, 0.2V, 0.4V, 0.6V, and 0.8V along the vertical, center cutline are plotted in Figure 49. The ions drift away from the anode with increasing voltage and begin to accumulate at the cathode interface between 0.2 and 0.4V. An additional simulation ramping down the voltage to 0V shows that the ions return to their equilibrium distribution within 100 μs . It should be noted that the transport times are highly dependent on the diffusion constants. Refinements on the first principles calculations and parametric extraction from experimental data may lead to adjustments of the diffusivity values.

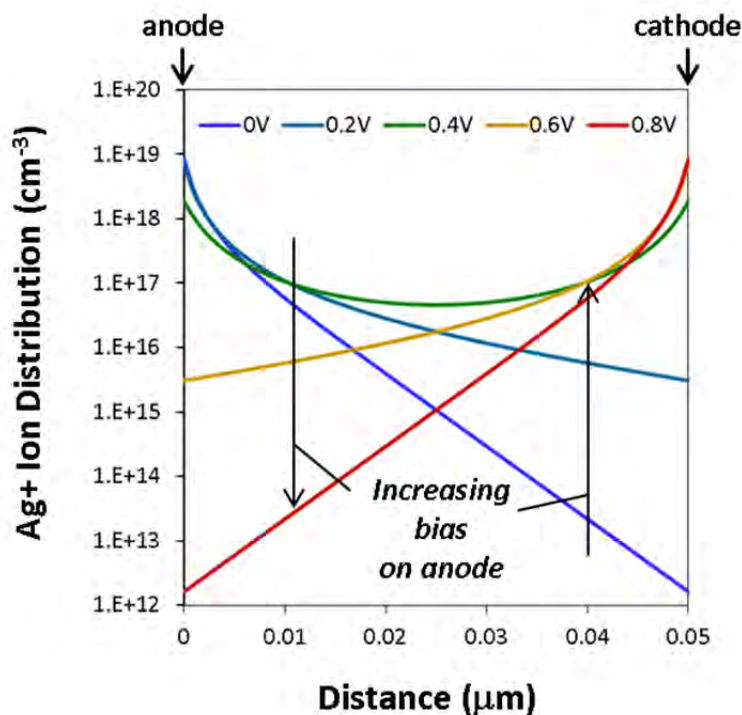


Figure 49. Ag^+ distribution with increasing anode voltage and cathode fixed at 0V

The evolution of sp0 and donor (neutral Ag) concentration versus anode voltage is plotted in Figure 50. The figure shows a significant rise in the concentration and evidence of species accumulation at the cathode interface for voltages above 0.4V. Note that the concentrations are uniform across the width of the structure instead of forming a thin filament. As explained above, the FEA software is not able to accurately model the filamentary bridging mechanism.

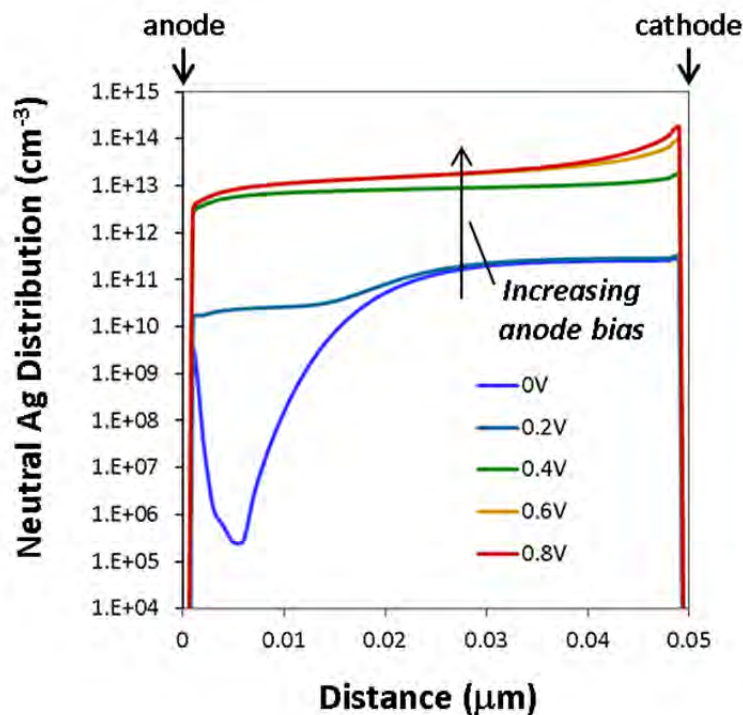


Figure 50. Ag distribution with increasing anode voltage and cathode fixed at 0V

Figure 51 plots the resistance versus anode voltage during the simulated voltage sweep. The resistance before programming is greater than 1 GΩ. The resistance exhibits an exponential decrease during the voltage sweep up to 0.4V. Above 0.4V, the change in resistance becomes linear and reaches approximately 300 kΩ at 0.9V. Further simulation reveals that this low resistance level is maintained when the anode is returned to 0V. Although the resistance does decrease orders of magnitude, comparison with the measured data reveals the difference in bridging kinetics. The ASU PMC has a discontinuous change in resistance while the finite element model has a continuous change in resistance. A discontinuous change in resistance indicates a low resistance filament forming through a high resistance film. The large, discontinuous step in resistance occurs when the filament connects or disconnects the anode and cathode. A continuous change in resistance indicates that the film is changing from anode to cathode all together; i.e. there is no filament growing from one electrode to the other.

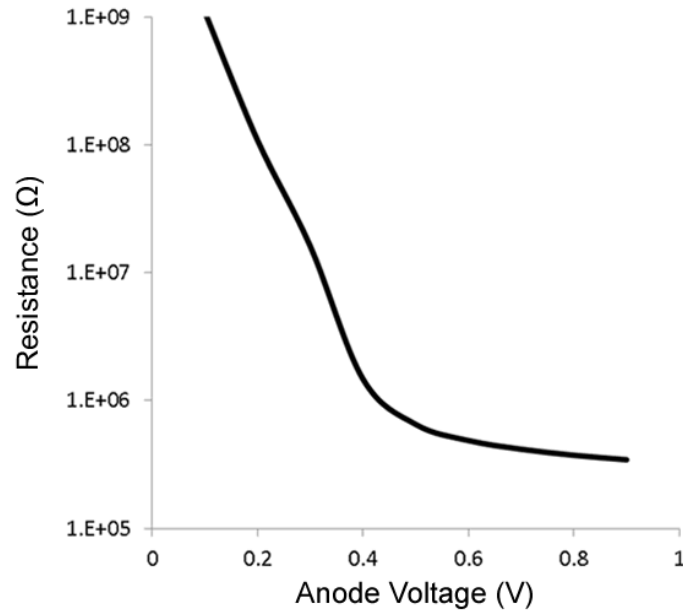


Figure 51. R-V characteristic of finite element model

Figure 52 plots the anode I-V as the anode voltage increases from 0V to 0.9V and then returns to 0V. The I-V response of the structure shows that the simulation models the hysteresis characteristic of resistive NVM. These results show that during the upward “write” sweep, the resistance changes from a high to low state (i.e., low to high current), and when the anode is returned to 0V the low resistance state is saved. Unlike the measured I-V data in 32, there is no current limit in the finite element model. Even with limited current, the finite element model’s I-V characteristic would remain inconsistent with that of the ASU PMC due to the aforementioned difference in bridging kinetics. The current would not discontinuously jump up to the current limit. The resistance upon entering current limiting would remain approximately constant, and the current would come down from the limit at about the same point it entered.

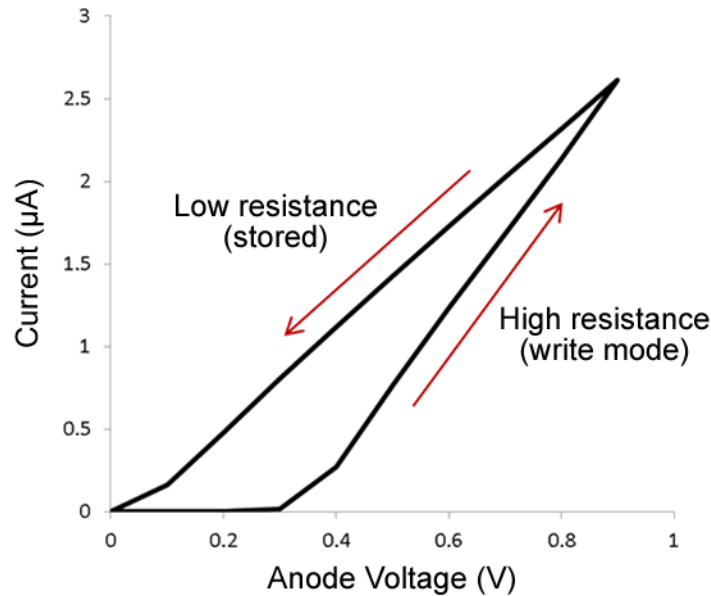


Figure 52. I-V characteristic of finite element model

The simulation results of the finite element model with generic ion transport and reactions in conjunction with the workaround and standard carrier statistics and transport equations are shown to effectively model some type of resistance change NVM, but the model is somewhat inconsistent with the switching behavior of the ASU ChG PMC. Because of this discrepancy we have also developed a resistance switching model implemented in MATLAB.

5.2.3 Dynamic MATLAB model for PMC resistance switching

5.2.3.1 Numerical Method

A physics-based numerical model has been developed specifically for the PMC. A numerical model is required to simulate with arbitrary voltage inputs because the PMC has a complex hysteresis. Development of this model began as a reproduction of the model above and was then significantly improved upon. The model is written in m-code for Octave or MATLAB and uses a time-stepping procedure with analytical equations to obtain the model's behavior over time. The Mott and Gurney ionic hopping current is assumed to be the rate limiting process in the PMC. All of the ionic flux is assumed to reduce on the filament, which is modeled as a cylinder with adjustable height and radius. The filament height is adjusted each time step in proportion to the ions accumulated during the step and the concentration of neutralized ions in the filament. The radius can change once the filament has connected the anode and cathode. The operating mechanism of the PMC model is visualized in Figure 53. The filament height and radius along with material properties are used to calculate the non-ohmic resistance of the cell at each time step. A single equation is used to calculate the resistance independent of OFF/ON state. Current limiting is implemented in the model to simulate standard testing as with the Agilent PA. The numerical routine checks for errors within each time step, such as current compliance or filament overgrowth, and dynamically adjusts the time step for precise and quick solutions.

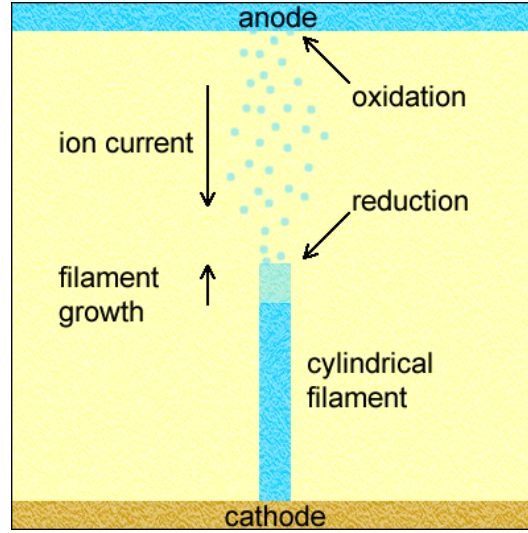


Figure 53. Operating mechanism of PMC model

5.2.3.2 Structure and Resistance Model

The resistance model calculates the total resistance of the PMC given the dimensions and material properties of the cell and filament. The simulation structure is modeled after an ASU PMC that is a cylindrical cell with a diameter of 5 μm and a ChG electrolyte thickness of 60 nm. The height and radius of the filament are variables during the simulation. The electrolyte and filament are modeled as separate diodes in parallel. The resistances of the diodes are calculated using the Shockley ideal diode equation with quality factor and added series resistance. The electrolyte series resistance is given by

$$R_{se} = \rho_e \cdot L / (\pi \cdot (r_{cell}^2 - r^2)) \quad (26)$$

where ρ_e is the resistivity of the electrolyte, L is the electrolyte thickness, r_{cell} is the radius of the PMC, and r is the radius of the filament. The series resistance of the filament is calculated as two resistors in series – the resistance of the neutralized ion portion of the filament and the resistance of the electrolyte in the cylindrical space remaining between the filament and the anode.

$$R_{sf} = (\rho_f \cdot h + \rho_e \cdot (L - h)) / (\pi \cdot r^2) \quad (27)$$

where ρ_f is the resistivity of the filament and h is the height of the filament. The resistances of the electrolyte and filament diodes are given by Eq. 28 and 29, respectively, where V is the applied anode voltage. An insignificant value, 10^{-16} , is added to the diode current to avoid a division by zero error.

$$R_f = V \cdot \left[I_{sf} \cdot \left(\exp\left(\frac{V}{n_f kT}\right) - 1 \right) + 10^{-16} \right]^{-1} + R_{sf} \quad (28)$$

$$R_e = V \cdot \left[I_{se} \cdot \left(\exp \left(\frac{V}{n_e k T} \right) - 1 \right) + 10^{-16} \right]^{-1} + R_{se} \quad (29)$$

The total resistance of the PMC (see Figure 53) is the parallel combination of Eqs. 28 and 29.

$$R = (R_f^{-1} + R_e^{-1})^{-1} \quad (30)$$

Table 5 summarizes the parameter values used in these equations.

Table 5. Parameters for structure and resistance

Parameter	Value	Unit	Description
ρ_f	7.0E-4	$\Omega \cdot \text{cm}$	Filament resistivity
ρ_e	8.0E4	$\Omega \cdot \text{cm}$	Electrolyte resistivity
L	6.0E-6	cm	Electrolyte thickness
r_{cell}	2.5E-4	cm	Cell radius
I_{sf}	1.8E-6	A	Reverse saturation current
I_{se}	1.4E-9	A	Reverse saturation current
n_f	1	none	Diode quality factor
n_e	2	none	Diode quality factor

The filament grows and dissolves according to the flux of Ag^+ (j_{hop}) given by Eq. 19 and the concentration of Ag in the filament. However, polarity dependent activation energy is used to account for the asymmetric OFF/ON switching voltages. An asymmetric energy barrier is suggested as a possible cause for this behavior. The electric field is given by Eq. 31.

$$E = V / (L + h \cdot (\rho_f / \rho_e - 1)) \quad (31)$$

The temperature of the cell is

$$T = T_0 + V^2 R_{th} / R, \quad (32)$$

where T_0 is the equilibrium temperature, V is the applied anode voltage, R_{th} is the equivalent thermal resistance and R is the total cell resistance. The concentration of Ag in the filament is given by

$$N_{Ag} = 2N_A \cdot \rho_{Ag_2Se} / m_{Ag_2Se}, \quad (33)$$

where N_A is the Avogadro constant, and ρ_{Ag_2Se} and m_{Ag_2Se} are the density and molar mass of Ag_2Se , respectively. When the PMC is non-bridged, the growth velocity of the cylindrical filament height is given by

$$v_h = j_{hop} / (zqN_{Ag}) \quad (34)$$

When the PMC is bridged, the electric field is replaced by the applied anode voltage multiplied by a fitting parameter, because there are no longer gaps between the electrodes with which to calculate electric field. An electric field must still exist in order to grow and dissolve the filament radius. The ionic hopping current density for the on-state is

$$j_{hop_on} = 2zecaf(-\frac{W_a}{kT})\sinh(\frac{V \cdot \beta \cdot ze \cdot a}{2kT}) \quad (35)$$

where β is the electric field fitting parameter with units of cm^{-1} . In the on-state, the filament radius after a time step, dt , is given by

$$r_{n+1} = r_n \sqrt{\frac{dt \cdot j_{hop_on}}{(LzqN_{Ag})} + 1} \quad (36)$$

where r_{n+1} is the radius after dt , and r_n is the radius before dt . The model assumes an initial radius of 2 nm. Once the filament bridges, the radius quickly grows until the resistance is reduced to where the current becomes limited and the voltage drops below the threshold for electrodeposition. A larger current limit allows the resistance to drop lower since the threshold for electrodeposition is fixed. This is why the ON resistance varies inversely with the compliance current limit. While the Butler-Volmer equation is actually responsible for electrodeposition and electrodisolution, the model implements those thresholds in a much simpler and direct way. The ionic hopping current is only allowed when the applied voltage is above the set electrodeposition threshold (V_{fwd}) or below the set electrodisolution threshold (V_{rev}). The parameters used in the filament growth equations and the electro-deposition/dissolution thresholds are reported in Table 6.

Table 6. Parameters for filament growth

Parameter	Value	Unit	Description
k	8.617E-5	eV/K	Boltzmann constant
ze	1.602E-19	C	Charge per ion
$2zeca_f$	5.379E3	A/cm ²	Mott-Gurney lumped coefficient
a	6E-8	cm	Effective hopping distance
W_{a_fwd}	0.310	eV	Forward hopping activation energy
W_{a_rev}	0.206	eV	Reverse hopping activation energy
T_0	295	K	Equilibrium temperature
R_{th}	1.0E5	K/W	Thermal resistance
N_A	6.022E23	mol ⁻¹	Avogadro constant
ρ_{Ag_2Se}	8.216	g/cm ³	Ag ₂ Se density
m_{Ag_2Se}	294.7	g/mol	Ag ₂ Se molar mass
N_{Ag}	3.358E22	cm ⁻³	Ag concentration in filament
β	0.6	cm ⁻¹	E-field fitting parameter
V_{fwd}	0.1	V	Electrodeposition threshold
V_{rev}	-0.05	V	Electrodisolution threshold

Compliance current is the maximum allowable electrical current to a device under test. The Agilent PA has a compliance current setting to limit the current supplied to the device under test. A PMC is usually tested with compliance current to prevent overheating and to set different values of resistance. That same type of current limiting is needed in the numerical model so the same tests can be simulated. Current is limited by reducing the applied voltage. In the numerical model, the voltage is constant during each time step. The model performs compliance checks and adjustments at the beginning and end of each time step. If the current exceeds compliance at the beginning of the step, then the reduced voltage is calculated to yield compliance by

$$V = I_{comp} \cdot R \cdot \text{sgn}(V_{in}), \quad (37)$$

where I_{comp} is the compliance current and V_{in} is the unadjusted input voltage used to get the sign of the voltage. The filament can grow during the time step thereby decreasing the resistance and possibly causing the current to exceed the limit by the end of the step. Therefore, the current cannot be maintained exactly at the limit. A tolerance of 1% of the compliance current is allowed in the model. If the current exceeds compliance plus tolerance at the end of the step, then the time step, dt , is halved until the current remains in compliance at the end of the step.

The simulated input, Figure 54, is a triangle wave function that performs the double voltage sweep starting at 0V with a ramp rate of ± 1 V/s with a maximum time step of 2 ms. V_{in} is the user-defined input function and V is the compliance adjusted function.

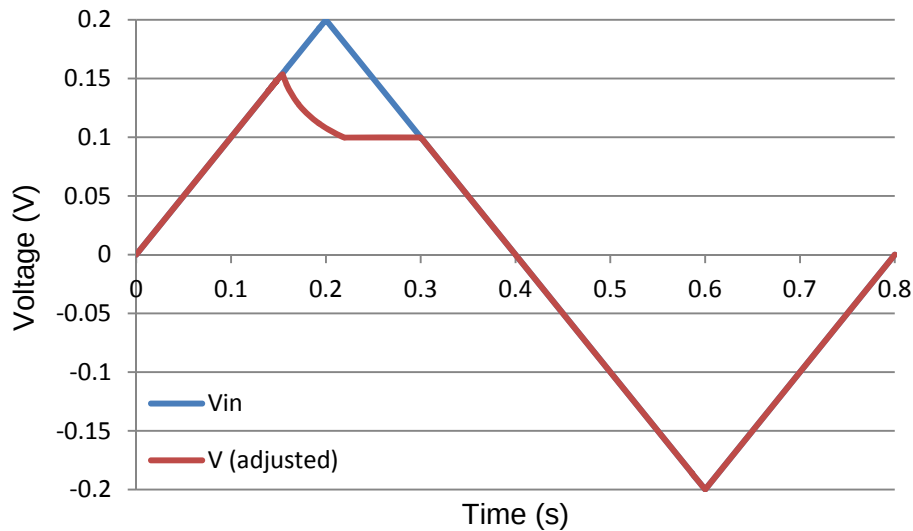


Figure 54. Simulated piecewise linear function voltage input

The I-V characteristic is plotted on a linear y-scale in Figure 55 and overlaid on ASU PMC data. These plots show an excellent match between the model and entire data curve. Notice that the curve has a kink in the programming switch as is sometimes observed in measured data. The first jump in the current occurs when a filament bridges the electrodes, but the resistance is not small enough to maximize the current. From there, the diameter of the filament increases until the

resistance drops enough to maximize the current. Once the current is limited, the voltage will drop below the minimum for electrodeposition and the filament will cease growth.

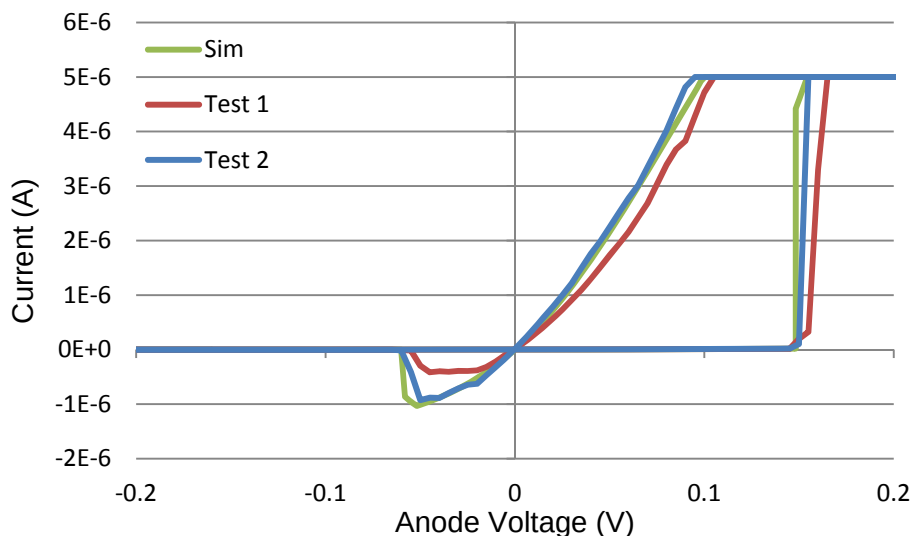


Figure 55. Linear I-V numerical model data overlaid on ASU PMC data

The I-V characteristic is plotted on a logarithmic y-scale in Figure 56 and overlaid on the ASU PMC data. These plots show an excellent match of the current at orders of magnitude.

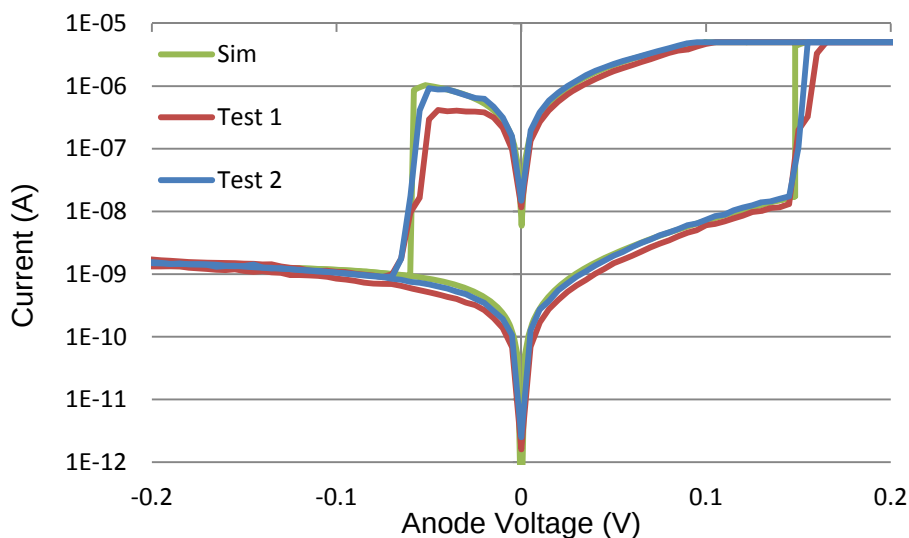


Figure 56. Logarithmic I-V numerical model data overlaid on ASU PMC data

The R-V characteristic is plotted in Figure 57 and overlaid on the ASU PMC data. These plots show a very good match of the resistance at all levels. The model is now able to show the real R-V characteristic even where the current is limited.

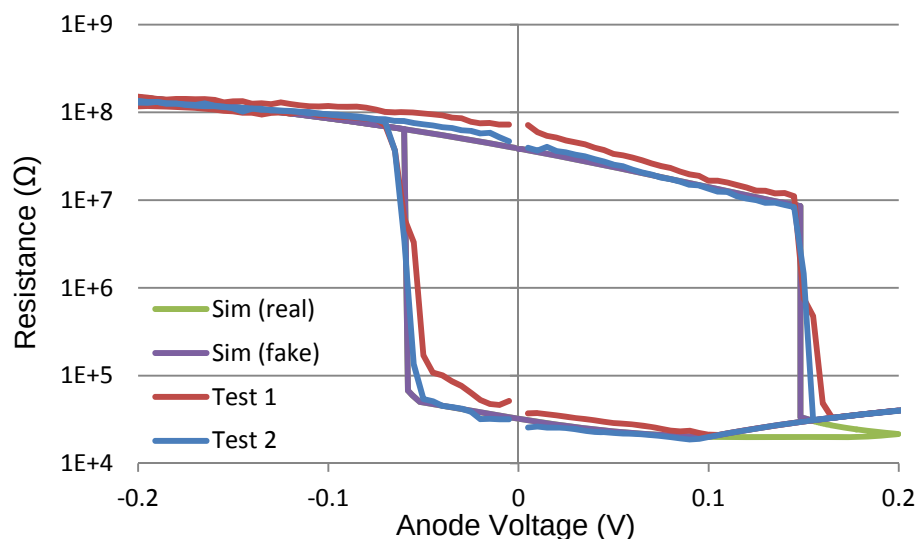


Figure 57. R-V numerical model data overlaid on ASU PMC data

Table 7 provides a quantitative comparison of key I-V characteristics between the ASU PMC Test 2 data and the numerical model. The percentage errors are fairly small, and they could be further reduced with better parameter fitting. The parameters of the numerical model were quickly adjusted for an approximate match by visual comparison of the plotted I-V data on a logarithmic scale. However, PMCs are currently not precision devices. These values vary between PMC devices of the same design and even between measurements of a single device. Therefore, fitting the model nearly exactly with data from a single measurement may be of little importance.

Table 7. Quantitative comparison of ASU PMC and numerical model

	$R_{\text{OFF}} (\Omega)$ @ 10 mV	$R_{\text{ON}} (\Omega)$ @ 10 mV		$V_{\text{write}} (\text{mV})$	$V_{\text{erase}} (\text{mV})$
ASU PMC Test 2	3.664E+07	2.622E+04		150.0	-60.00
Numerical Model	3.530E+07	2.975E+04		148.3	-60.10
Percent Error	-3.657	13.46		-1.13	0.17

A parametric simulation was also performed where only the compliance current limit was varied. Figure 58 plots the I-V curves with compliance currents of 1 μA , 5 μA and 10 μA . Figure 59 plots the corresponding R-V curves. These results demonstrate the multilevel programmability of the numerical model. A greater compliance current allows the filament radius to increase more and the resistance to decrease more until the minimum electrodeposition voltage divided by the resistance equals the greater compliance current. Notice that all three curves drop out of the limited current regime at 0.1V, because that is the electrodeposition threshold which determines

the set resistance. The results also show that larger filaments require more negative voltage-time to dissolve.

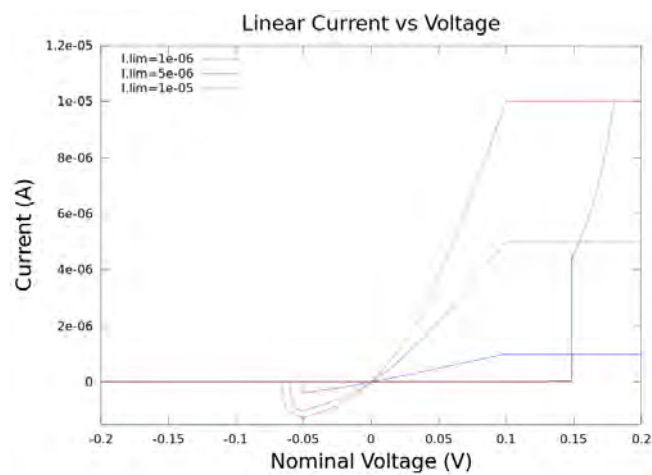


Figure 58. I-V simulation with parametric compliance current

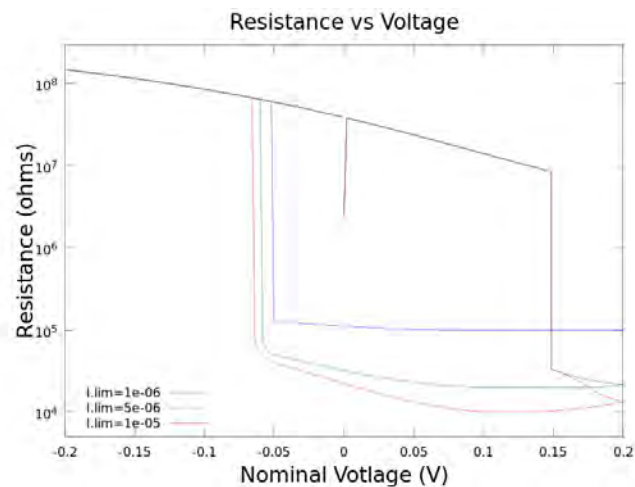


Figure 59. R-V simulation with parametric compliance current

5.2.4 ChG Film Electrostatics

5.2.4.1 Overview

One important, although often overlooked, aspect of modern solid state materials and devices is the relationship between electrical and chemical effects [16]. In solid state electrolytes, for example, when electrons are released from an atom, the resulting positively charged ions can transport under an electric field. The process of oxidation can be reversed when an ion captures an electron through reduction. Through these reduction-oxidation (RedOx) processes, atoms

converted to ions at one location can be deposited at another. The ion-conducting materials are often compounds of oxygen (O), sulfur (S), and selenium (Se) characterized by their relatively high ion mobility.

As discussed above, during photodoping the negatively charged chalcogen atoms and positively charged metallic ions form intrinsic electric fields that can be sufficient for the metallic ions to overcome the barrier energy at the interface. The difference in electrochemical potentials facilitates the penetration of ions into ChG materials during exposure. The relatively rigid covalent bonds mixed with soft van der Waals interconnections enable the ChG materials to form traps where electrons, generated by light or ionizing radiation, are absorbed. As shown in Eq. 38, an initially twofold covalently bonded chalcogenide atom can turn into an anion possessing a single covalent bond and an excess electron,



While there have been significant refinements to the photodoping process to optimize it for use in current technology applications, several questions regarding the physics of photodoping remain unsolved. For example, the precise role anions play in the photo-induced diffusion of metal into ChG films is not well understood. Modeling chemical reactions with carrier statistics enables standard semiconductor Poisson solvers to be used in the analysis of photodoping as well as ion transport and RedOx processes. In order to investigate the relationship between anion formation/ dissolution and well known principles of device physics, we have developed for this effort an equivalence mapping between the chemical reaction presented in Eq. 38 and conventional semiconductor device theory equations, by treating the chalcogenide atom as an acceptor-like trap. The physical model, which utilizes Shockley-Read statistics [17] is shown to be equivalent to anion formation and dissolution reaction models in both equilibrium and non-equilibrium steady state conditions (i.e., constant photogeneration). This model can be generalized to all chemical reactions in which there is an electron and/or hole reaction with immobile neutral and/or charged species. The model is verified by 2D Technology Computer-Aided-Design (TCAD) simulations.

5.2.4.2 Mathematical model

TCAD simulations are performed with Silvaco's ATLAS device simulator. Unlike, most device simulation tools, ATLAS is capable of simulating the transport of and chemical reactions between a limited number of atomic species. Transport properties for each species are primarily controlled by the diffusion coefficient (D) which is defined in Eq. 22. Because we are equating trapping statistics to chemical reactions and that traps generally do not move in a material, we assume that the chalcogenide atoms (both neutral and charged) are immobile. Thus the diffusion coefficient for each species (C_2^0 , and C_1^-) should be very small ($D \ll 10^{-10} \text{ cm}^2/\text{s}$). In equilibrium, the forward reaction rate is equal to the reverse reaction rate in each chemical reaction as follows:

$$fN_{C_2^0} n \exp\left(\frac{-E_{af}}{kT}\right) = rN_{C_1^-} \exp\left(\frac{-E_{ar}}{kT}\right). \quad (39)$$

In Eq. 39, the left side of the equation is the forward reaction, where f is the forward reaction rate, E_{af} is the forward activation energy, $N_{C_2^0}$ and n are C_2^0 and electron concentrations, respectively. The right side of Eq. 39 is the reverse reaction, where r is the reverse reaction rate, E_{ar} is the activation energy and $N_{C_1^-}$ is the concentration of C_1^- in Eq. 38. Using standard carrier statistics equations, the ratio of concentration C_1^- to the total concentration of $C_1^- + C_2^0$ is calculated as

$$\frac{N_{C_1^-}}{N_{C_2^0} + N_{C_1^-}} = \frac{f}{r} n_i \exp\left(\frac{E_{Fn} - E_i}{kT}\right) \exp\left(\frac{E_{ar} - E_{af}}{kT}\right), \quad (40)$$

where E_{Fn} is the quasi Fermi energy level for electrons and n_i is the intrinsic carrier concentration in the material. An acceptor-like trap is neutral when empty and negatively charged when filled with an electron. Based on this definition, we may define the species C_2^0 in Eq. 38 as an acceptor-like trap. Donor-like traps can be used for the complementary equation of Eq. 38 ($C_2^0 \rightarrow C_1^+ + e^-$). The probability of ionization of acceptor-like traps assumes that the capture cross sections are constant for all energies and the ionization probability is calculated as

$$F_{tA} = \frac{\nu_n SIGNn + e_{pA}}{\nu_n SIGNn + \nu_p SIGPp + e_{nA} + e_{pA}}, \quad (41)$$

where $SIGN$ and $SIGP$ are the carrier capture cross sections for electrons and holes respectively, and ν_n and ν_p are the thermal velocities for electrons and holes. For acceptor-like traps, the electron and hole emission rates, e_{nA} and e_{pA} , are defined as

$$e_{nA} = DEGEN \nu_n SIGN n_i \exp\left(\frac{E_t - E_i}{kT}\right), \quad (42)$$

and

$$e_{pA} = \frac{1}{DEGEN} \nu_p SIGP n_i \exp\left(\frac{E_i - E_t}{kT}\right), \quad (43)$$

where E_i is the intrinsic Fermi level, E_t is the trap energy level, and $DEGEN$ is the degeneracy factor of the trap center. $DEGEN$ takes into account that spin degeneracy exists and that empty and filled traps have different spin and orbital degeneracy. To simplify equations, we set $DEGEN$ equal to 1. Since holes play no role in the reaction described in Eq. 38, we assume $SIGP \ll$

SIGN to eliminate hole reactions from the statistical calculation. Without holes, the ionization probability of acceptor-like traps is reduced to Eq. 44, the standard Fermi-Dirac statistical form,

$$F_{tA} = \frac{1}{1 + \exp(\frac{E_t - E_{Fn}}{kT})}. \quad (44)$$

Using the above equations, it is possible to define an acceptor-like trap that produces an effect equivalent to the reaction presented in Eq. 38. By setting Eqs. 41 and 44 equal, the equivalent acceptor-like trap energy is found to be a function of the forward and reverse reaction rates and activation energies of the chemical reaction, i.e.,

$$E_t = kT \ln(\frac{r}{fn_i}) + E_{af} - E_{ar}. \quad (45)$$

It should be noted that in Eq. 45 E_{Fn} is assumed without loss of generality to be pinned to zero energy when no bias voltage is applied. The significant advantage of Eq. 45 is that it is applicable to both equilibrium and steady-state conditions. To verify, we use the numerical device simulator ATLAS to calculate equilibrium and steady-state (non-equilibrium) solutions on a ChG material often used in cation-based memristors. Figure 60 shows the 2D structure used for the simulations while there is not any bias applied to the device. The bulk material is a pure chalcogenide glass ($\text{Ge}_{30}\text{Se}_{70}$) without any metallic dopants and the device anode and cathode terminals are defined for simplicity as neutral contacts. The parameters of the $\text{Ge}_{30}\text{Se}_{70}$ material and parameters for the chemical reaction of Eq. 38 are listed in Table 8 and Table 9, respectively. The length of the device, which corresponds to the distance between two contacts, is 10 μm and its height/thickness is also 60 nm.

By substitution of parameters from Table 9 in Eq. 45, the trap energy is found to be 0.65 eV above E_{Fn} . As previously mentioned, the ATLAS code can solve not only standard carrier statistics for solid state material, but chemical reactions similar to those shown in Eq. 38 between a limited number of species. This allows us to use ATLAS to compare both methods and thereby validate the equivalence function, Eq. 45. We model the chemical reaction in one simulation with the initial C_2^0 concentration of 10^{20} cm^{-3} and a second simulation uses acceptor-like traps of equal concentration with trap energies set by Eq. 45 (specifically 0.65 eV above E_{Fn}). Simulations are performed under equilibrium and non-equilibrium steady-state conditions. For the non-equilibrium case, carrier generation is modeled with a virtual light source. As mentioned above, exposure to light, specifically UV, is a common post-processing manufacturing technique, used for some variants of ChG-based non-volatile memory. For the steady state light exposure condition, a fixed generation rate (G) is set to $2.72 \times 10^{21} / \text{cm}^3 \text{ s}$ which is consistent with what might be expected during exposure to UV light at the power density of 10 mW/cm^2 .

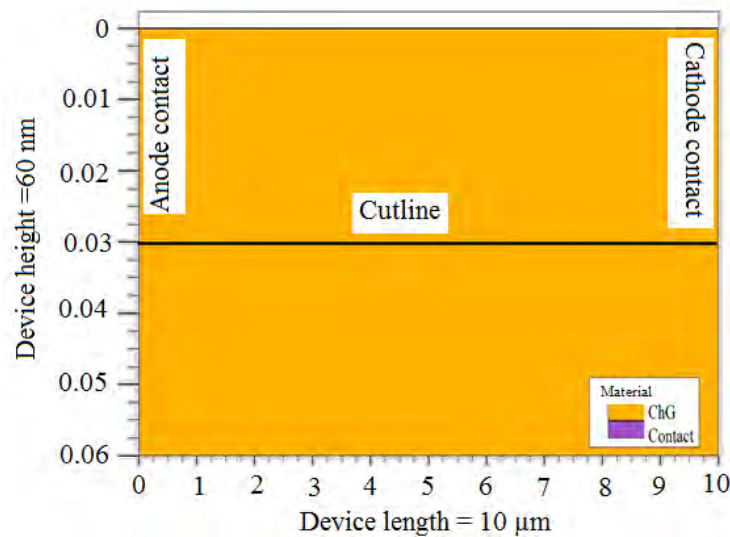
Table 8. Parameters of Ge₃₀Se₇₀ material

Material Parameter for Ge ₃₀ Se ₇₀	Value
Bandgap (eV)	1.86
Affinity (eV)	3.05
Density of States in Conduction Band (per cc)	1×10^{19}
Density of States in Valence Band (per cc)	1×10^{20}
Electron Mobility (cm ² /Vs)	10^{-5}
Hole Mobility (cm ² /Vs)	10
Dielectric Constant	40.9

Table 9. Parameters of chemical reaction based on Eq. 38

Parameter	Value
f	1
r	8×10^{19}
E_{af}	0.7 eV
E_{ar}	1 eV

Figure 61 plots C_1^- , from the chemical reaction solver method and compares the results to the concentration of filled acceptor-like traps calculated from carrier-trap statistics for both equilibrium and non-equilibrium steady-state (photogeneration). As seen in Figure 61, there is an excellent agreement between chemical reaction results and those of model with traps. The sensitivity of the filled trap concentration to trap energy is shown in Figure 62. As shown in this figure, the concentration in the log scale is linearly dependent to the trap energy with constant slope of $1/[\log(e)kT]$, which can be derived from Eq. 44.

**Figure 60. Cross-section of the ChG simulation structure**

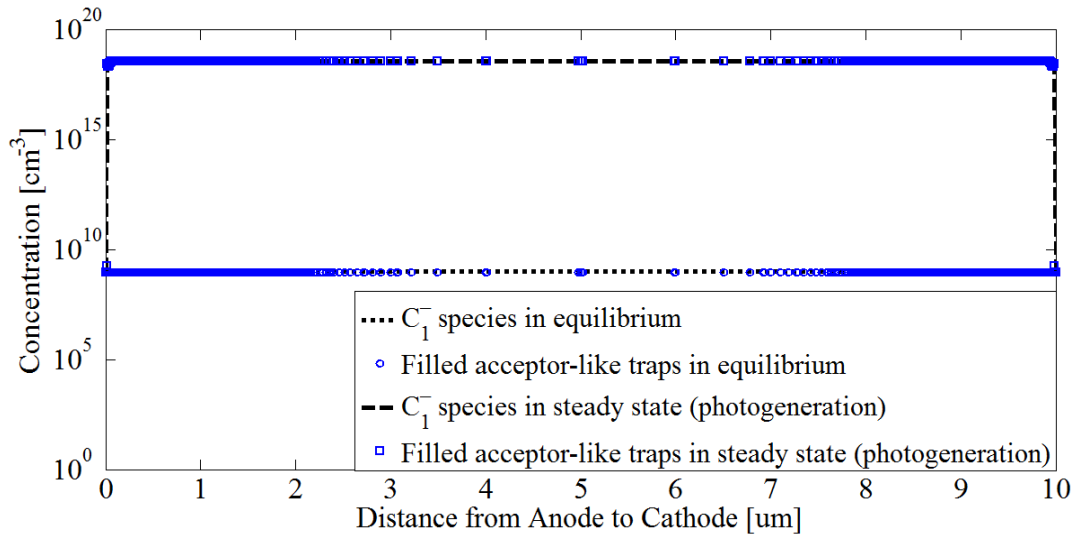


Figure 61. The C_1^- concentration vs filled trap concentration in the equilibrium and steady-state (photogeneration)

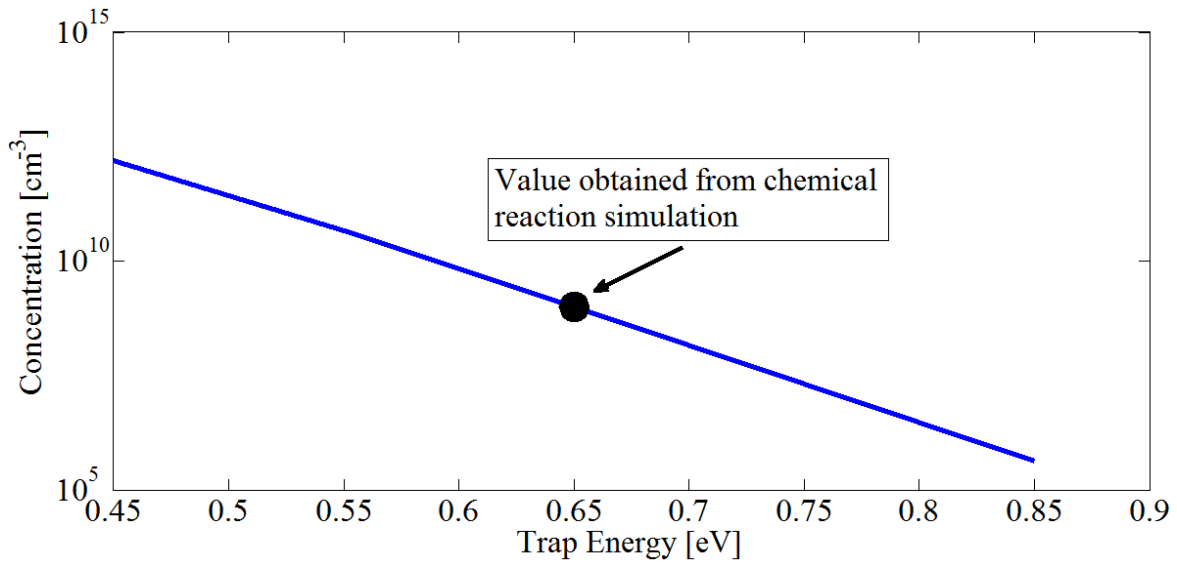


Figure 62. Filled trap concentration vs trap energy

5.2.5 TCAD Photodoping Modeling

To model the photodoping process, the Ag layer that connects to the chalcogenide films is illuminated by UV light. For the UV exposure condition, the power density (P) of the light with wavelength (λ) of 324 nm is 10 mW/cm². Eqs. 46 and 47 show the calculated photon flux (ϕ_p : the number of created photons per area per second) and generation rate (G : the number of

generated electron/hole pairs per volume per second) respectively, if each photon creates one electron/hole pair,

$$\phi_p = \frac{p\lambda}{hc} \quad (46)$$

and

$$G = \frac{\phi_p}{\text{Device Height}} \quad (47)$$

To present the simulation results, we create a cutline in the middle of the device from anode to cathode as shown in Figure 60. Figure 63 shows the neutral Ag concentration across the cutline for the equilibrium (undoped) and steady state (photodoped) cases. For the undoped simulation, Ag atoms are oxidized at the anode contact and transport, primarily via drift processes, through the glass as cations. The incorporation of Ag⁺ into the film leads to a reduction in the field at the interface, ultimately suppressing the drift and establishing an equilibrium condition. Exposures to UV light creates electron/ hole pairs that increase the field in the film attracting more Ag ions into the ChG layer. Therefore, Ag concentration in the film increases upon photo exposure. This behavior is in the agreement of experimental data presented in Figure 19.

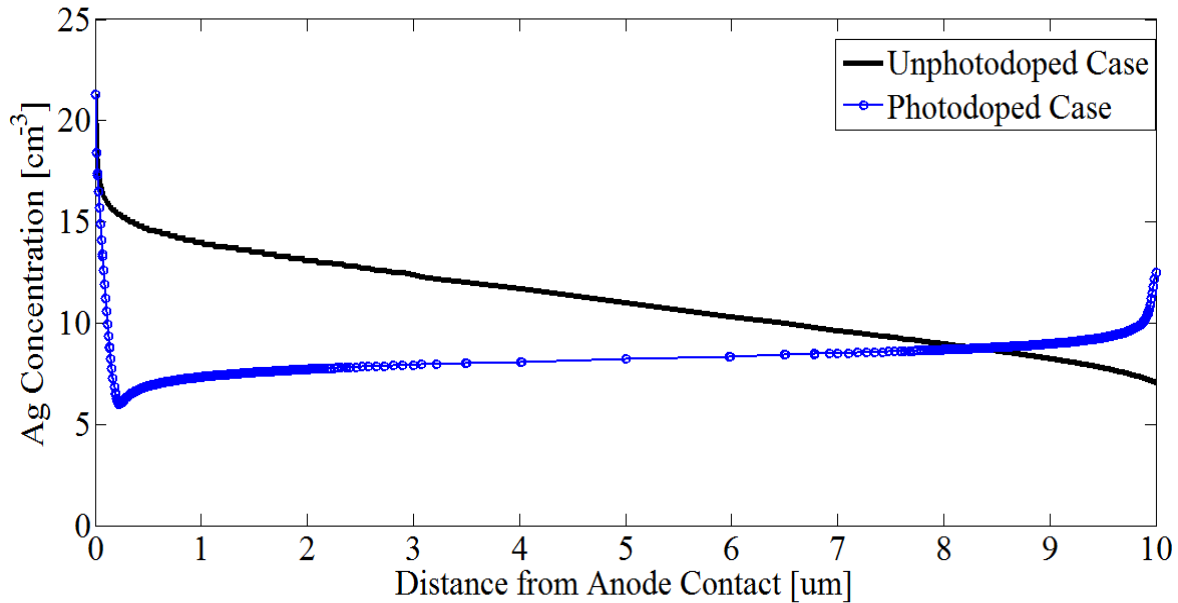


Figure 63. Neutral Ag profile across the device from anode contact to anode one for both unphotodoped and photodoped cases

The electric field and potential profiles are shown in Figure 64 and 65, respectively. Photodoping makes the high electric field regions near to the interface with Ag and Ni contacts wider. This happens near to Ag contact because more cations have a chance to diffuse more in the ChG material while high electric field near to Ni contact is because of the accumulation of Ag atoms near to Ni contact. This behavior is so called double-layer capacitance. According to Figure. 65, photodoping decreases the potential in the bulk region of ChG and the potential barrier against ion hopping reduces as well that confirms previous explanation.

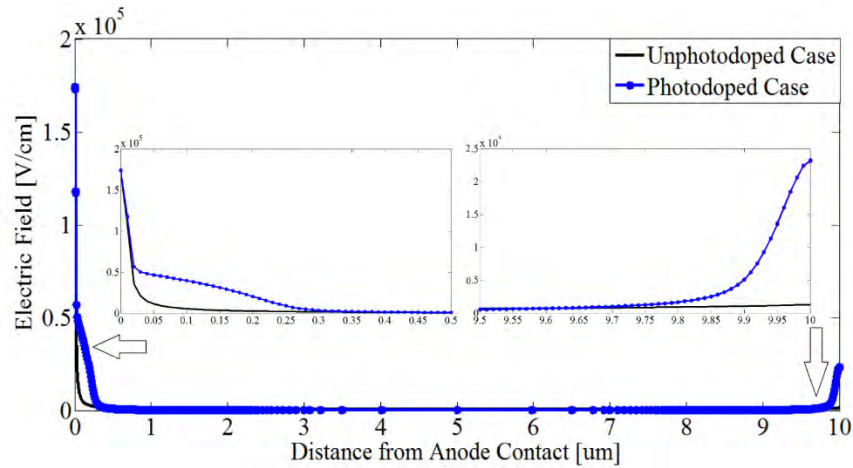


Figure 64. Electric field profile across device from anode to cathode contact for both unphotodoped and photodoped cases

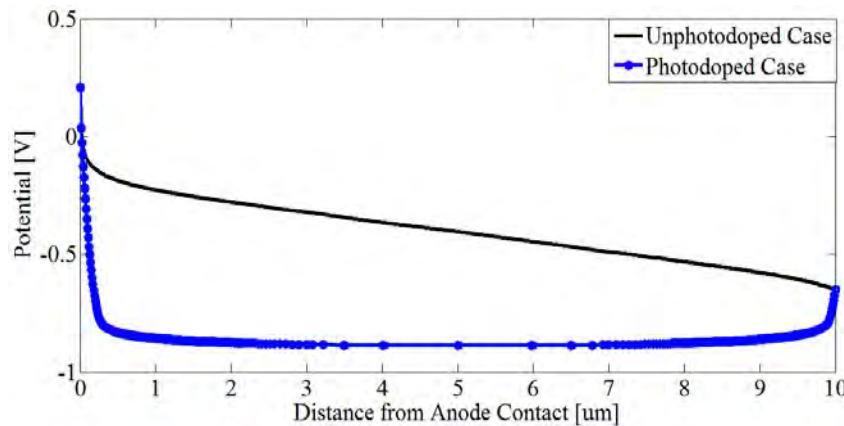


Figure 65. The potential profile across device from anode to cathode for both unphotodoped and photodoped cases

The electron and hole concentrations for both equilibrium and steady state cases are presented in Figure 66. By electron/ hole pair generation in the photodoping process, the shortage of electrons is compensated, and the concentrations of electrons and holes are almost the same. Figure 67 plots the band diagram of the structure before and after photodoping process. As represented in Figure. 67(a), the electron quasi-Fermi level (QFL) is far below the conduction band while the

hole QFL is near to the valence band. Therefore, the electron concentration is much lower than the hole concentration that confirms Figure 66. On the other hand, Figure 67(b) clarifies that the hole QFL is pinned at the fixed level even in the photodoped case and the valence band approaches to the hole QFL while the electron QFL approaches to the conduction band. Consequently, both of the electron and hole concentrations increase.

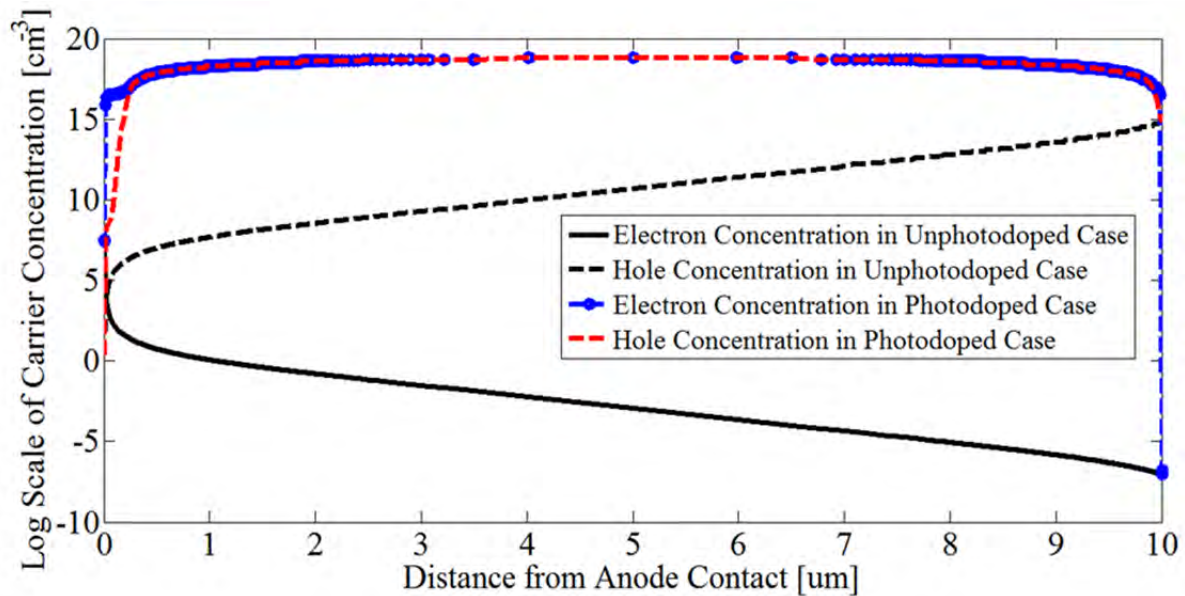


Figure 66. Carrier concentrations across device from anode to cathode contact for both unphotodoped and photodoped cases

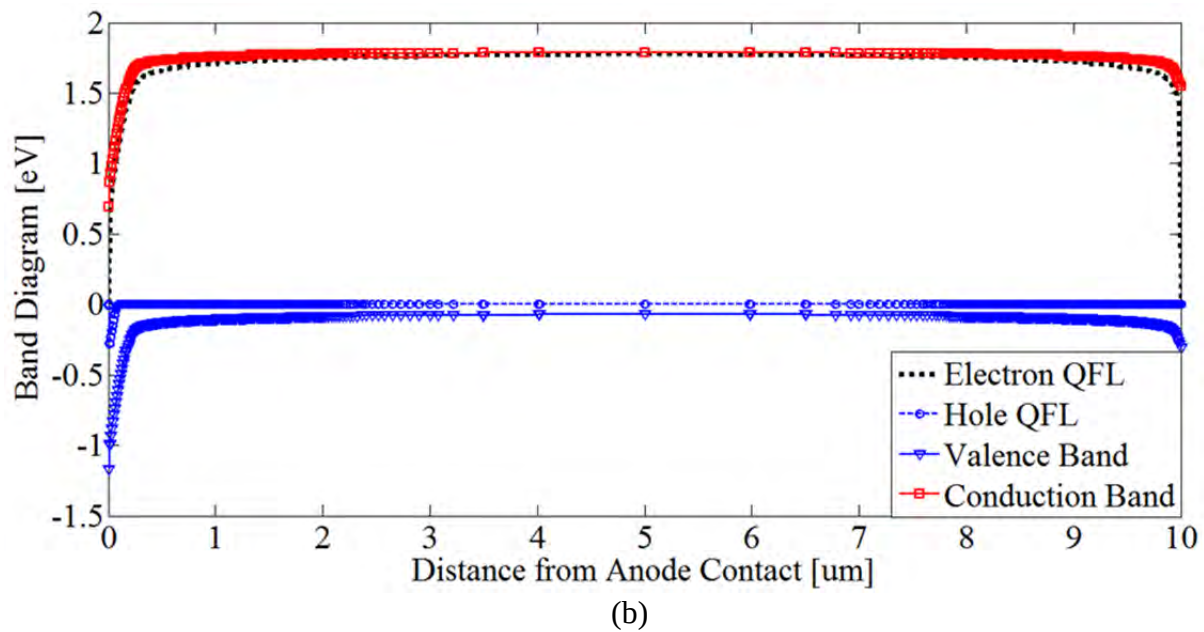
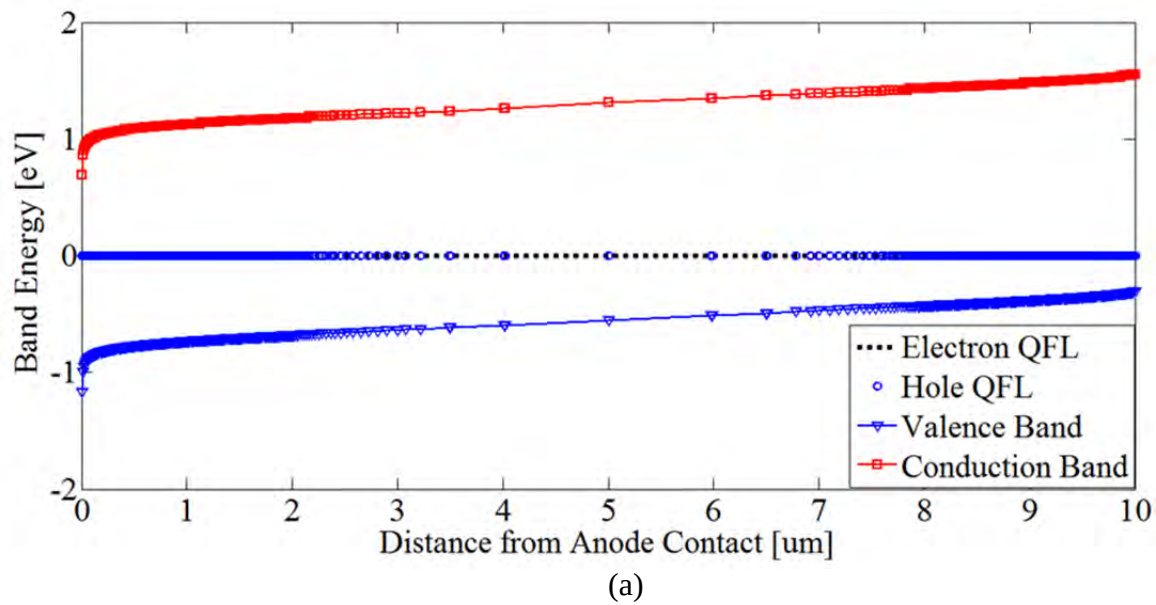


Figure 67. The band diagram of device across the device for (a) unphotodoped case and (b) photodoped case

5.3 Conclusions

The simulation results of the physics-based numerical model are shown to effectively model the ASU PMC. The numerical TCAD model has enabled us to accurately describe the physical

mechanisms underlying the operation and performance of PMC devices, both in static and dynamic conditions. With respect to static performance, we have developed and verified a precise physical model that captures the electrical behavior of programmable metallization cell devices in both their low resistance on-state and high resistance off-state. Parameter extraction has been performed by adjusting material parameters used for numerical device simulations to calibrate the model to the results of electrical measurements on actual PMC devices with different via areas. This has enabled for the first time quantitative measurements of material bandgaps, workfunctions, density of states, carrier mobilities, dielectric constants, and affinities for these systems. Obtaining an accurate set of material parameters for both Ag-rich and Ag-poor ChG systems enables greater fidelity in PMC device simulation, which significantly enhances our ability to understand the underlying physics of ChG-based resistive switching memory.

The results of dynamic finite element (FE) simulations that incorporate the processes of particle movement and reactions in conjunction with standard carrier statistics and transport equations have shown to effectively model the resistive switching behavior of ChG-based resistive memory. The simulations are performed on virtual two-dimensional structures representative of the existing CBRAM technology based on ASU's ChG PMC platform. Key parameters for the system of equations solved by the Silvaco's device simulator ATLAS are obtained from first principles DFT calculations or, where possible, extracted from experimental data. The FE simulation models the growth of neutral Ag within the ChG film under applied bias. The simulations also reveal that the neutral Ag density is left unchanged once the bias is removed. These dynamic modeling approaches have been successfully adapted for modeling the key process of photodoping in these materials, which is key to the understanding of radiation effects (task 5).

The following list represents publications and conference presentations that were the outcome of work in this task:

1. S. Rajabi, M Saremi, H.J. Barnaby, A Edwards, MN Kozicki, M Mitkova, D Mahalanabis, Y Gonzalez-Velo, A Mahmud, "Static impedance behavior of programmable metallization cells," *Solid-State Electronics*, vol. 106, pp. 27-33, 2015.
2. M. Saremi, S. Rajabi, H. J. Barnaby, and M. N. Kozicki, "The effects of process variation on the parametric model of the static impedance behavior of programmable metallization cell (PMC)," presented at the Proc. 2014 MRS Spring Meeting, San Francisco, CA, 2014.
3. M. Saremi, H. J. Barnaby, A. Edwards, and M. N. Kozicki, "Analytical Relationship Between Anion Formation and Carrier-Trap Statistics in Chalcogenide Glass Films," *ECS Electrochemical Letters*, vol. 4, no. 7, pp. H29-H31, 2015.

6 TASK 4 –DEVELOPMENT OF AN ANALYTICAL (COMPACT) MODELING FRAMEWORK

6.1 Methods, Assumptions, and Procedures

Closed form analytical models are derived from the physics-based model (see Task 3). Analytical equations are converted into compact models for use in small scale memory and digital circuit simulations. Compact models are realized as equivalent sub-circuits and/or Verilog functions and calibrated from results obtained of numerical TCAD simulations and experimental data. Analytical model development utilizes Silvaco's SmartSPICE circuit simulation tool available at ASU.

6.2 Results and Discussion

In this section, we present the following:

1. A description and validation through comparisons to experimental data, a Verilog-A compact model of the ChG PMC.
2. A circuit-level demonstration of the compact model for use in simulating digital and neuromorphic circuits

6.2.1 PMC Compact Model

6.2.1.1 Programming Dynamics

The programming operation of PMCs (and other metallic ion transport based resistive memory devices) consists of a series of electrochemical oxidation/reduction reactions and subsequent ion migrations occurring under external electrical bias. The oxidation and reduction of Silver (Ag) takes place mainly at the anode side and allows for Ag ions to be created for CF, while reduction of these same Ag ions occurs both at the cathode side and in the electrolyte (Chalcogenide) layer. Thus an electrochemically active metal is required for the anode. The oxidation and reduction reactions are given, again, below, respectively-



In order to overcome the electrochemical energy barrier, an external voltage bias needs to be applied across the device electrodes. A condition where the anode is sufficiently positively biased with respect to the cathode initiates the write process; oxidation of Ag at the anode and its subsequent migration towards cathode followed by reduction to grow the conducting filament (CF). Conversely, a sufficiently negatively biased anode with respect to the cathode starts the erase process; oxidation of Ag in the formed CF and its migration towards the anode where it undergoes reduction to form metallic Ag again. The silver ions react with the electrolyte to form conductive phases which then combine together to form the conductive filament. Each set of

oxidation and reduction reactions at the two electrodes cause a charge transfer and generate an electrode current which has been modeled by the Butler-Volmer equation as,

$$I = I_o \left[e^{\frac{\alpha\eta}{kT/q}} - e^{-\frac{(1-\alpha)\eta}{kT/q}} \right] . \quad (50)$$

Where, I_o is the equilibrium current which refers to the current when the rate of reaction at anode is equal to the rate of reaction at the cathode. The first exponential term refers to cathode current and the second term refers to anode current, while α is the transfer co-efficient, η is the current-over potential and kT/q is the thermal voltage. However, of relatively more importance from device modeling perspective is the current flow associated with the Ag^+ ion transport inside the electrolyte ultimately leading to formation/growth/dissolution of the conductive filament and thereby determining the change in PMC resistance. This current flow is associated with electrical field influenced “hopping” of ions between adjacent sites in the solid electrolyte layer in the device under external bias, and can be modeled by a drift current density following the Mott-Gurney ionic transport model as,

$$J_h = 2ZqN_iav_o e^{(-E_a/kT)} \sinh\left(q\alpha E/2kT\right), \quad (51)$$

where Zq is the total charge of the ions, N_i is the density of ions in the electrolyte; v_o is the vibration frequency of the ions, α is the ion hopping distance and E is the net electric field at the tip of the growing filament given by,

$$E = V/(L + h \cdot (\rho_f/\rho_e - 1)) , \quad (52)$$

where V is the potential difference between anode and cathode, ρ_f and ρ_e are the resistivity of the filament and the bulk electrolyte respectively, while L is the electrolyte layer thickness. As $\rho_f \ll \rho_e$ (refer to table 4.1), the denominator of (2.5) can be simplified to $(L-h)$.

Regarding the modeling of the temporal evolution of the conductive filament inside the electrolyte in PMC, the filament is modeled two dimensionally with variable vertical height $h(t)$ and lateral radius $r(t)$. The vertical growth rates of the filament can then be modeled as,

$$\frac{dh}{dt} = \frac{J_h}{ZqN_m} , \quad (53)$$

where N_m is the density of electrodeposited metal (cm^{-3}) in the electrolyte. By combining (2.4) and (2.6), the following expression can be used to model the vertical filament growth rate as,

$$\frac{dh}{dt} = v_h e^{(-E_a/kT)} \sinh\left(q\alpha E/2kT\right), \quad (54)$$

where v_h is a fitting parameter. Once the filament is formed, the LRS current density can be modeled as J_r , given by

$$J_r = v_r' e^{(-E_a/kT)} \sinh\left(q\beta V/kT\right), \quad (55)$$

where v_r' is fitting parameter and the term βV is a substitute for the vertical electric field E representing the lateral electric field, β being the lateral electric field fitting parameter.

The filament itself can be modeled either as conical or cylindrical. Microscopic images suggest a conical shape, being wider near the cathode and narrower near the anode. The volume (Vol) of the filament in LRS condition can be expressed in terms of the variable top radius r and the bottom radius R as,

$$Vol = \frac{\pi L}{3} (R^2 + Rr + r^2), \quad (56)$$

The incremental change in the filament volume ($dVol$) given by,

$$dVol = \frac{J_r \cdot dt \cdot \pi r(t)^2}{ZqN_m}. \quad (57)$$

Using the above equations, the lateral filament radius growth rate can be derived as,

$$\frac{dr}{dt} = \frac{r \cdot v_r}{LqN_m} e^{(-E_a/kT)} \sinh\left(q\beta V/kT\right), \quad (58)$$

where v_r is a fitting parameter (proportional to v_r') and r is the current filament top radius. The above analytical equations will be used to estimate the variable PMC resistance and develop a compact model for circuit simulations.

6.2.1.2 Estimation of the variable PMC Resistance

Based on the derivation of the conductive filament growth rates above, a time dependent expression for the change in resistance of a PMC device under electrical bias can be derived. For the conical filament assumed previously, the variable filament resistance $R_f(t)$ can be derived as

$$R_f = \frac{\rho_f h}{\pi r R}, \quad (59)$$

where ρ_f is the filament resistivity, R is the bottom surface radius of the filament and h and r are the variable height and top radius, calculated using (54) and (58) respectively. The resistance of the filament in the initial state (in the HRS) can be expressed as,

$$R_{f,i} = \frac{\rho_f h_0}{\pi r_0 R}, \quad (60)$$

where h_0 and r_0 are the initial height and radius respectively of the filament ($h_0 < L$). These initial conditions in the 'Off' state may vary from device to device based on several factors, e.g.

the filament height h_0 depend on the amount of photodoping performed during fabrication or the magnitude and duration of the erase pulse. For the purpose of modeling, the following values were assumed - $h_0 = 15$ nm and $r_0 = 0.1$ nm. The resistance of the bulk portion of the electrolyte (excluding the filament) can be expressed as,

$$R_e = \frac{\rho_e \cdot L}{\pi \cdot (r_c^2 - R_{CF, bottom}^2)} , \quad (61)$$

where ρ_e is the bulk electrolyte resistivity. The overall resistance of the device can be expressed then as a parallel combination of the filament resistance and bulk resistance as,

$$R_{PMC} = \frac{1}{\frac{1}{R_e} + \frac{1}{R_f}} . \quad (62)$$

Hence the overall PMC resistance is dependent on the applied voltage across the device (V) and the current flowing through the PMC can be expressed as,

$$I_{PMC} = V / R_{PMC} . \quad (63)$$

In order to enforce the compliance current functionality implemented by the 4156 PA during I-V characterization using by the quasi-static voltage sweep, the current computed using (63) is compared with a compliance current parameter (I_{comp}) during each simulation step and when $I_{PMC} \geq I_{comp}$, the voltage across the device becomes different from the applied voltage (V) and is given by

$$V_{comp} = I_{comp} \cdot R_{PMC} \cdot \text{sgn}(V) , \quad (64)$$

where, $\text{sgn}(V)$ represents the signum function to assign the appropriate sign to V_{comp} based on the polarity of the applied voltage V. Figure 68 shows simulation results for a voltage sweep induced write-erase operation and the corresponding change in the simulated filament height and radius.

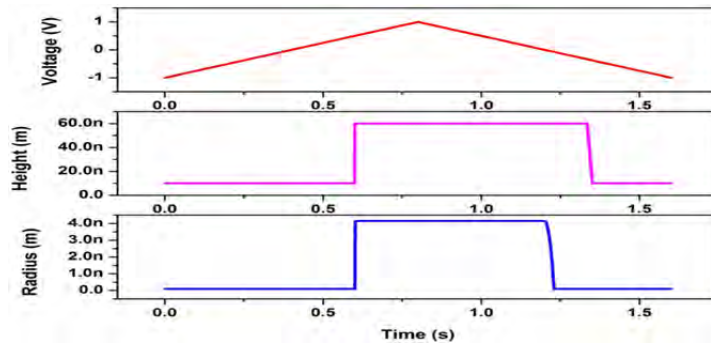


Figure 68. Simulated voltage double sweep (from -1 V to +1V and back to -1V) to generate I-V characteristics

6.2.1.3 Model Simulation Results

Simulation results using this model were fitted to experimental device characteristics. The experimental data was collected for Ag-Ge_{0.3}Se_{0.7} based two-terminal PMC devices and also for Ag-GeS₂ based 1T-1R PMC memory elements. Figure 69 (a) demonstrates an example fit for experimental I-V characteristics for a two-terminal PMC. Figures 69(b) and 69(c) compare experimental and simulated PMC LRS and peak reset current values respectively for different compliance currents. Finally, Figure 69(d) compares the experimental and simulated LRS values vs. applied voltage pulse magnitude.

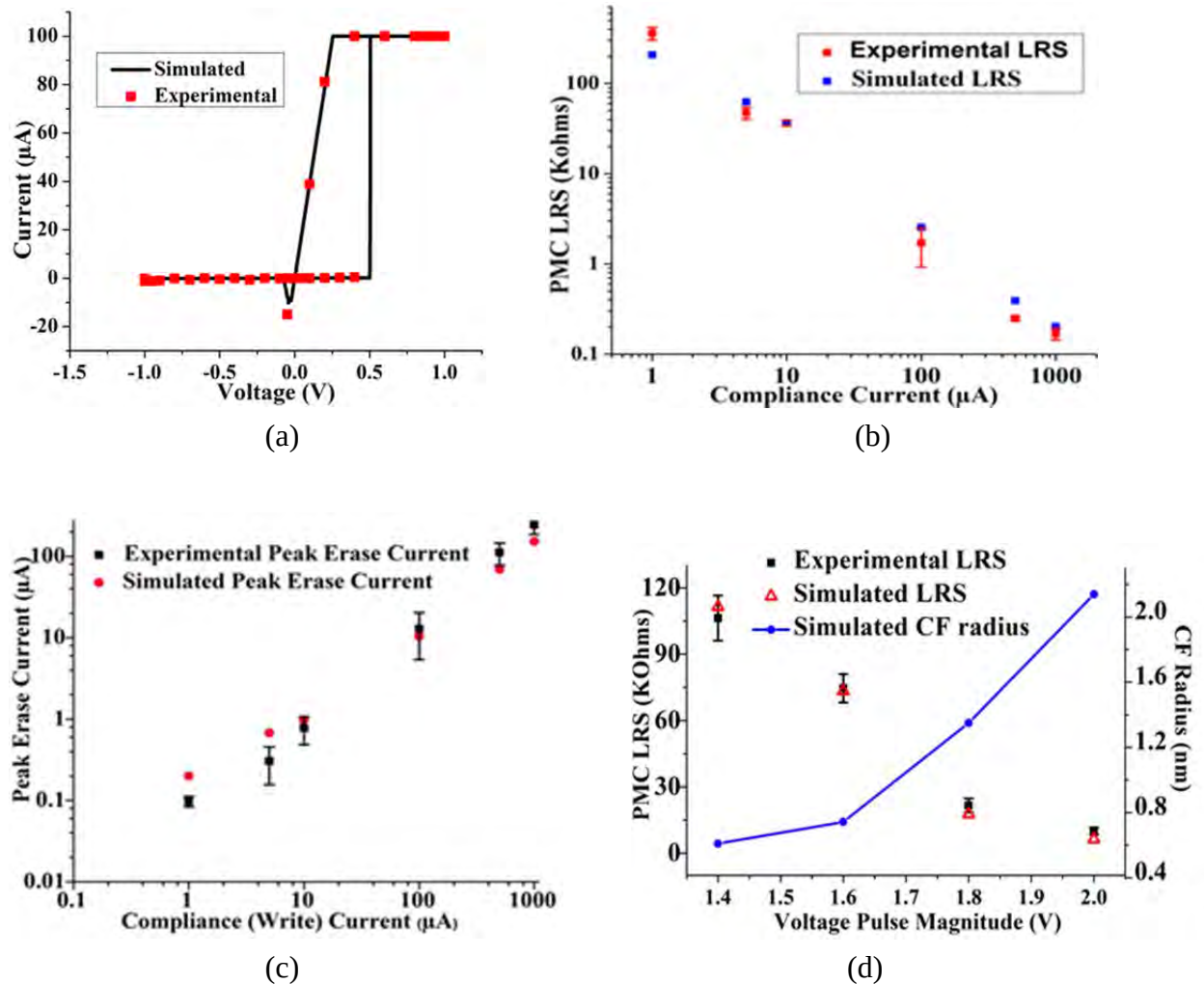


Figure 69. (a) I-V characteristics, (b) LRS dependence on compliance current, (c) Peak reset current and (d) LRS dependence on applied voltage pulse

Commercially manufactured PMC memory arrays usually consist of 1T-1R elements, i.e., a PMC device in series with a NMOS selector switch. The Ag-GeS₂ based PMC devices used for characterization in this work were fabricated in back end of line (BEOL) in a 130 nm standard

CMOS process. Figure 70(a) shows a cross-section of a 1T-1R element. Figure 70(b) shows simulated I-V characteristics of a 1T-1R PMC (during a single sided anode voltage sweep) for different applied gate voltages. In the case of 1T-1R element, the applied gate voltage magnitude determines the maximum programming current through the NMOS and consequently the LRS level during a write operation. The source is grounded during these operations.

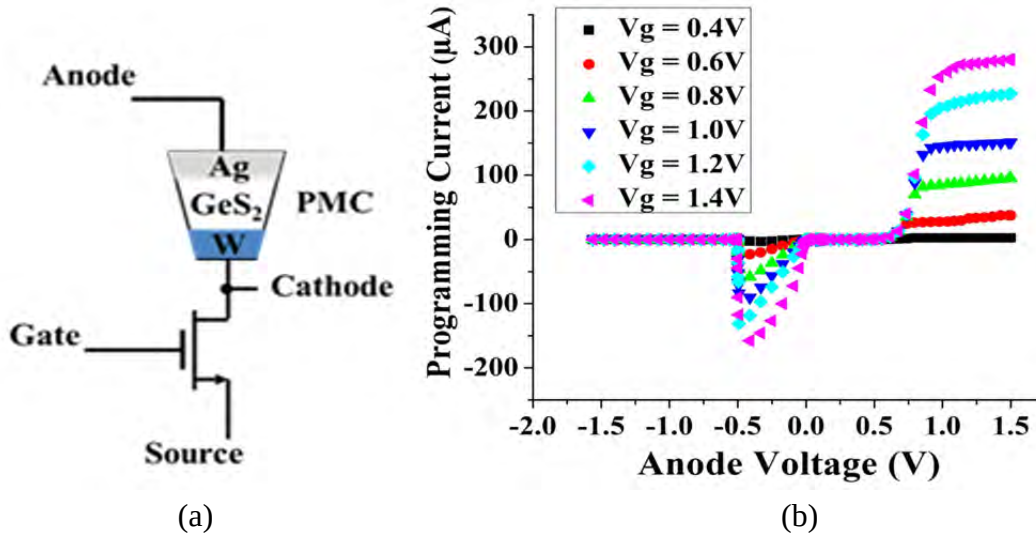


Figure 70. (a) A 1T-1R PMC and (b) simulated I-V characteristics

Figure 71 shows experimentally obtained HRS and LRS levels during 100 write-erase operations performed by sweeping the anode voltage. Stable HRS (LRS) conditions were obtained by sweeping the PMC anode from 0 to +2V (-2V), while applying NMOS gate bias of 0.7V and keeping NMOS source at 0V. HRS is approximately 5MΩ and LRS is approximately 10KΩ.

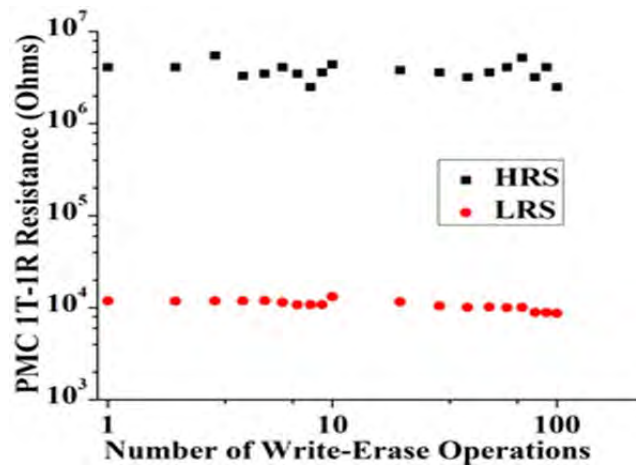


Figure 71. Experimental resistance cycling of 1T-1R element during 100 write-erase operations performed by sweeping the anode voltage

The on switching threshold voltage (during HRS to LRS transition) of PMC devices exhibits a dependence on the applied voltage ramp rate, i.e., greater the rate of voltage rise the greater the switching voltage threshold. This behavior is demonstrated in Figure 72(a) and the model was fitted to experimental data to estimate the value for α . The parameter β for the write operation can be extracted by fitting the model simulation results to the multiple LRS levels, as shown in Figure 72(b). Figure 72(c) shows programming current (NMOS selector saturation current) vs. gate voltage data for a 1T-1R memory cell (corresponding to the different LRS levels) and the corresponding fit obtained from simulation. Lastly, Figure 72(d) shows comparison between simulation and experimental data for peak currents during erase for anode voltage sweep at different gate voltages, which enables extraction of the value of β during erase operation.

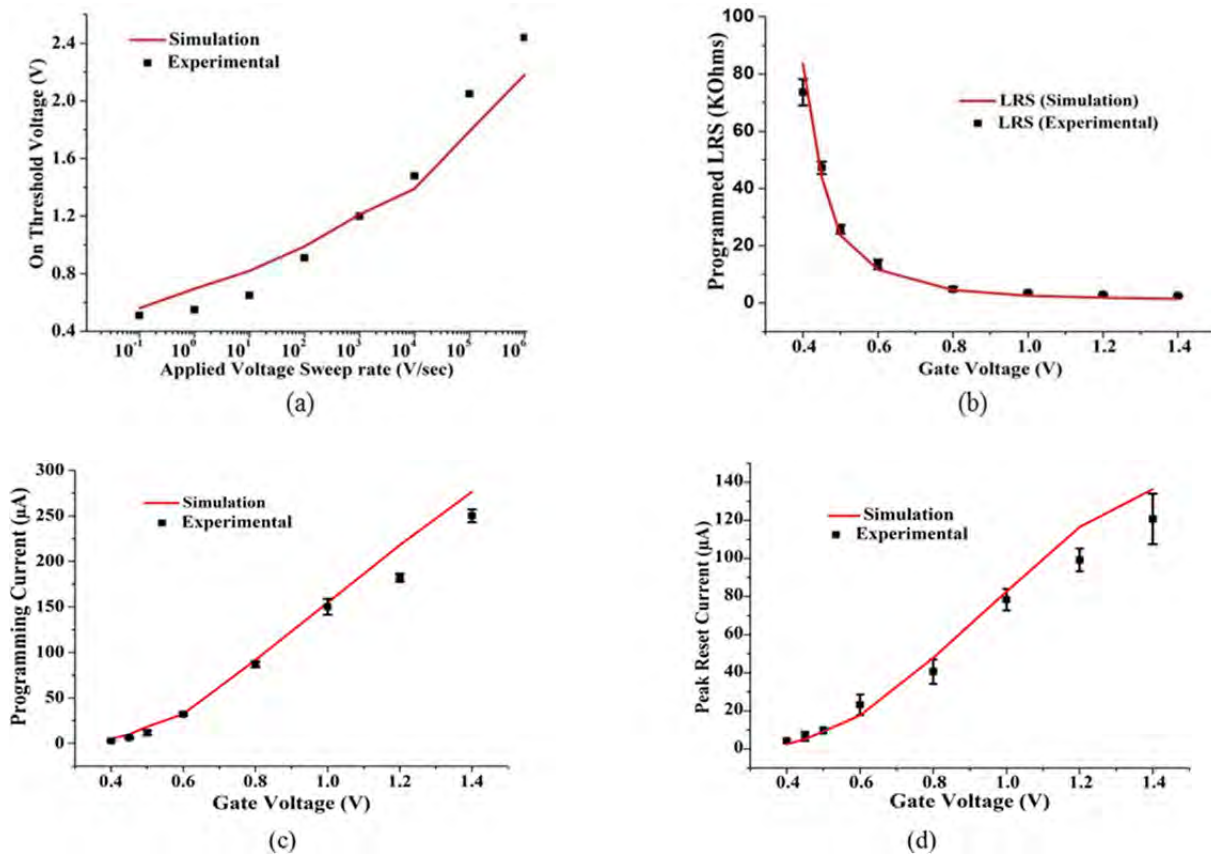


Figure 72. (a) Dependence of on voltage, (b) multilevel LRS, (c) programming currents and (d) peak erase currents

In addition to DC response characteristics, the model was also verified for transient pulsed voltage inputs, as it is useful in circuit simulations. A comparison between a typical transient pulsed write-erase operation performed experimentally and via simulation is shown in Figure 73 with the associated voltage and current transients. No current limiting resistor was used for this operation and it can be seen that write-erase times of the order of 100 ns can be achieved with such devices.

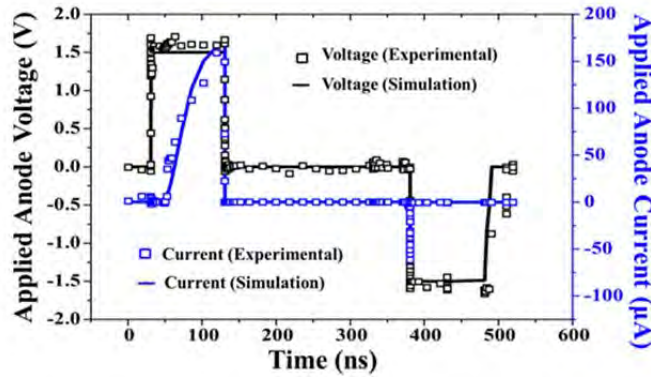


Figure 73. Simulated and experimentally obtained anode voltage and current transients

Table 10 defines and lists the values for all the relevant optimized simulation parameters for both Ge_{0.3}Se_{0.7} based and GeS₂ based PMC devices based on the fitting of the simulation results to experimental data. Appendix A contains the complete Verilog-a code for the compact model.

Table 10. PMC Compact Model Parameters

Symbol	Quantity	Fitted Values	
		2 terminal PMC (Ag-Ge _{0.3} Se _{0.7})	1T-1R (Ag- GeS ₂)
vh	Vertical growth fitting parameter	0.1 m/s	0.5 m/s
vr	Lateral growth fitting parameter	0.1 m/s	0.1 m/s
Ea	Activation Energy	0.4 eV	0.46 eV
L	PMC via thickness	60 nm	60 nm
α	Ion hopping distance	3 nm	15nm
β	Electric field parameter	0.26, $V > 0$, 0.5, $V < 0$	0.52, $V > 0$, 1.4, $V < 0$
pe	bulk electrolyte resistivity	8000 Ω .m	8000 Ω .m
pf	filament (CF) resistivity	2.3x10 ⁻⁶ Ω .m	5.3x10 ⁻⁴ Ω .m
rc	PMC cell via radius	2.5 μ m	500nm
T	Cell Temperature	300 K	300K

6.2.2 Circuit Level Demonstrations

6.2.2.1 Digital Circuits- Nonvolatile FlipFlop

With the scaling down of CMOS technology, leakage power consumption during idle/inactive periods tend to dominate over active power consumption in traditional CMOS based sequential

logic elements such as flip-flops, especially for low power applications such as wireless sensor networks and biomedical applications. In order to reduce leakage power consumption, power gating techniques using high-threshold transistor based latches has been proposed to reduce sub threshold leakage. However, high-threshold transistors can only reduce sub threshold leakage current but does not reduce other forms of leakage (such as gate tunneling leakage current) which increases with scaling of CMOS technology. To completely eliminated leakage power consumption during inactive periods, the flip-flop should be completely disconnected from power supply (Vdd), which results in loss of data in pure CMOS circuits.

Previously proposed non-volatile flip flops were based on the standard tri-state inverter based master-slave flip flop topology, utilizing different memory devices such as magnetic tunnel junction (MTJ) devices, memristors and oxide based RRAMs. In this task, a non-volatile flip flop circuit is proposed based on the existing sense amplifier flip flop architecture that can take advantage of the prolonged state retention capability and very high HRS to LRS ratio of PMC devices to operate at sub-threshold voltage levels reliably. The sense amplifier based architecture enables a compact flip flop design which has demonstrated high performance at sub threshold voltage levels and demonstrates near-zero setup time, true single phase clocking and also reduced clock load in comparison to master slave flip flops. An additional advantage of the sense Amplifier architecture is its inherent symmetry in comparison to the master slave latch based flip flop which requires additional transistors to eliminate any asymmetry and ensure reliable low voltage supply operation.

As shown in Figure 74, the sense amplifier flip-flop generally consists of two stages- a clock and data signal driven pulse generating stage followed by a slave latch for storing the acquired data. The conventional sense amplifier flip flop combines a clocked sense amplifier first stage with a NAND-based slave S-R latch as shown.

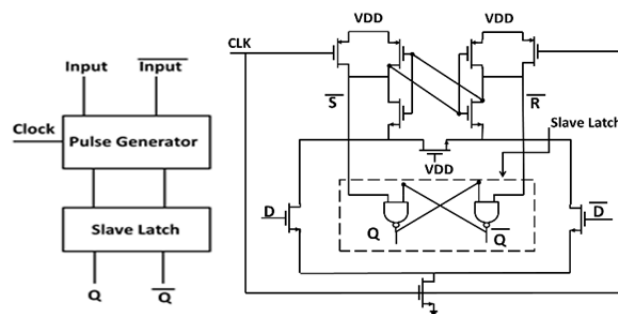


Figure 74. Flip flop topology with pulse generator followed by slave latch with conventional sense amplifier flip flop.

The flip-flop operation is as follows: sense amplifier outputs $\overline{S}$ and $\overline{R}$ are precharged to power supply (VDD) when clock signal (CLK) is low. As the clock signal goes high, depending on the input data and its complement (D and $\overline{D}$), only one of $\overline{S}$ and $\overline{R}$ discharges to ground, while preventing the other signal from discharging. This transition in turn triggers the slave latch and the resulting outputs (Q and $\overline{Q}$) are stored till CLK remains high. An additional NMOS with

VDD as input was incorporated to provide a discharge path to ground during the scenario when input data changes after the CLK rising edge, thereby potentially changing the flip-flop state. Although variations of this basic sense amplifier flip-flop exist, in this work the circuit of Figure 74 is modified to incorporate non-volatile data storage and restore functionality. By storing the latched flip flop data in non-volatile PMC devices, the flip flop can be entirely disconnected from power supply during idle state and leakage power loss can be completely avoided. Two potential non-volatile flip-flop topologies are shown in Figure 75(a) and 75(b). Both utilize complementary resistance programming of two PMC devices to store the data during inactive period and then restore the saved data to the outputs by performing a PMC read operation upon wake-up.

The only difference between the two topologies is in the read circuit implementation. The mode of operation for both the flip flops are the same and can be described as follows. The flip flop enters normal mode of operation as the clock (CLK) goes from low to high, and acts like the conventional sense amplifier flip flop. The Evaluate signal is set to Vdd during normal operation for reasons explained earlier in relation to sense amplifier flip-flop operation. Instead of the clock (CLK) signal, a separate signal (Precharge) is used to precharge the nodes $\overline{S}$ and $\overline{R}$ goes to Vdd at the rising edge of clock. In preparation for storing the latch outputs (Q and $\overline{Q}$) in the PMC devices, the circuit enters write mode of operation (Write = Vdd, Precharge = Vdd, Evaluate = Vdd). During this phase, the outputs Q and $\overline{Q}$ are used to program the two PMCs in a complimentary manner (one to HRS, other to LRS) such that the correct latch outputs are restored eventually. At the end of the sleep period, the flip flop goes through two phases in order to restore the stored data – Precharge phase followed by Read/Restore phase. During Precharge phase (Write = 0, Precharge = 0, Evaluate = Vdd), both the nodes $\overline{S}$ and $\overline{R}$ are charged to Vdd via PMOS transistors P_1 and P_2 which are now on. This is followed by the Read phase (Write = 0, Precharge = Vdd, Evaluate = 0, Read = 1), during which as Precharge is high, nodes $\overline{S}$ and $\overline{R}$ are free to discharge to ground, and only one of the two signals discharges depending on the programmed PMC resistance levels, while also preventing the other node from discharging due to the cross-coupled inverter latch action. It may be noted here that the CLK signal goes high only during normal operation and stays low otherwise, thus allowing the main pull down network (PDN) involving transistors activated by the complimentary data inputs to operate separately from the PDN involving PMC read/write circuitry. The control signals Precharge, Evaluate, Write and Read can be globally generated for all the non-volatile flip flops in the entire system. Figure 76 shows the control logic and sequence of the different control signals in the design.

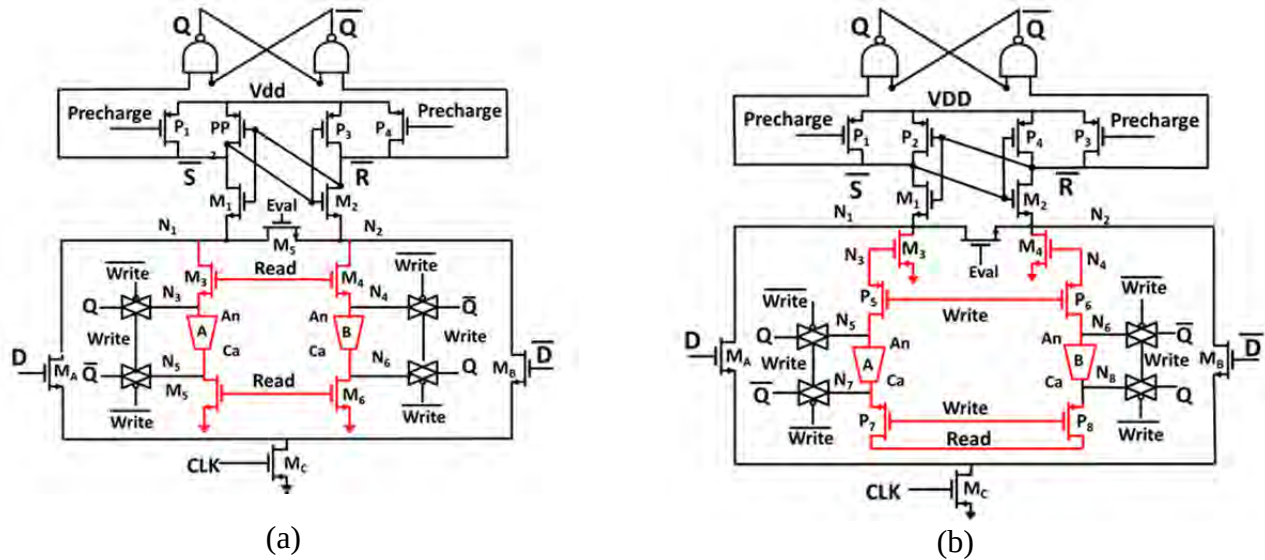


Figure 75. (a) Non-volatile flip flop architecture using PMC and (b) architecture using PMC with different read circuit

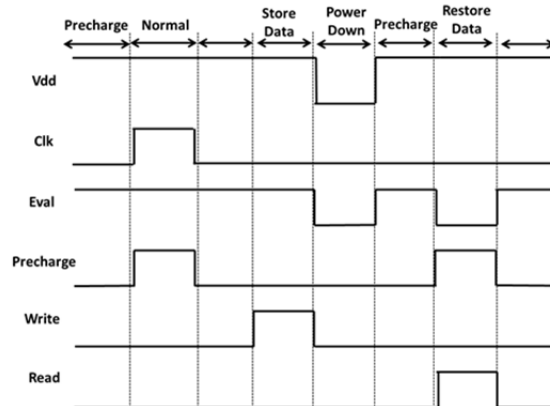


Figure 76. Timing sequence

Read Circuit Implementation: While differential sense amplifier based designs offer high speed and low power consumption, its operation may suffer from errors due to device mismatch and noise which impact the design symmetry. Hence design of the circuit for reading and restoring the data to the flip flop outputs is crucial to ensure reliable read operation even at ultra-low voltage supply levels. CMOS Sense amplifier based flip-flops have already demonstrated reliable operation at sub-threshold voltage supply levels of 200 mV. Hence in this work the read circuit design for successful operation at sub-threshold voltage levels will be the main focus. The read circuit (highlighted) shown in the design of Figure 75(a) (FF I) is based on previously proposed non-volatile flip flops, where both the nodes $\overline{S}$ and $\overline{R}$ start discharging simultaneously but at different rates determined by the difference in impedance of the discharge paths through

the complementarily programmed PMC devices A and B respectively. This simultaneous initiation of the discharge/read process is in contrast to the proposed modified read circuit of FF II in Figure 75(b) where the Read signal is used to trigger the two sides of the differential sense amplifier separately through the complementarily programmed PMC devices. This ensures that one of the two nodes (S and R) actually begin discharging before the other and also slow down the initial discharge rate of the other node via feedback action of the cross-coupled inverters respectively. This modification can improve the robustness of the non-volatile flip-flop especially for sub-threshold operation in comparison to the read circuit of FF I in which the rates of discharge are dependent not only on the difference in programmed PMCs but also on all the transistors in the discharge paths. Typical transient simulation plots using the PMC compact model described earlier demonstrating all the different phases of operation are shown in Figures 77(a) and (b) for storing and restoring data for D= '0' and D= '1' respectively.

Write Circuit: A nominal voltage supply (Vdd) level of 1.5 V for 130 nm CMOS process is used for the entire non-volatile flip-flop circuit (FF II). It is possible to operate this flip-flop at power supply voltages much lower than 1.5 V at sub-threshold levels for low power applications; however the write circuit needs to be modified in that case. This is because the switching threshold voltage of PMC devices is much higher for the pulsed programming voltages commonly used in circuit applications compared to quasi-static DC signals. Programming voltage pulse amplitude higher than 1.2 V was estimated to be the minimum voltage required to program the devices considered in this work. Hence for operating Vdd lower than 1.5V, level shifters can be added to the existing write circuit to ensure the write voltage level remains at 1.5 V. Another possible solution is to use dynamic supply voltage scaling techniques to raise the Vdd of the non-volatile flip flops during write operation, which would not require additional level shifter circuitry.

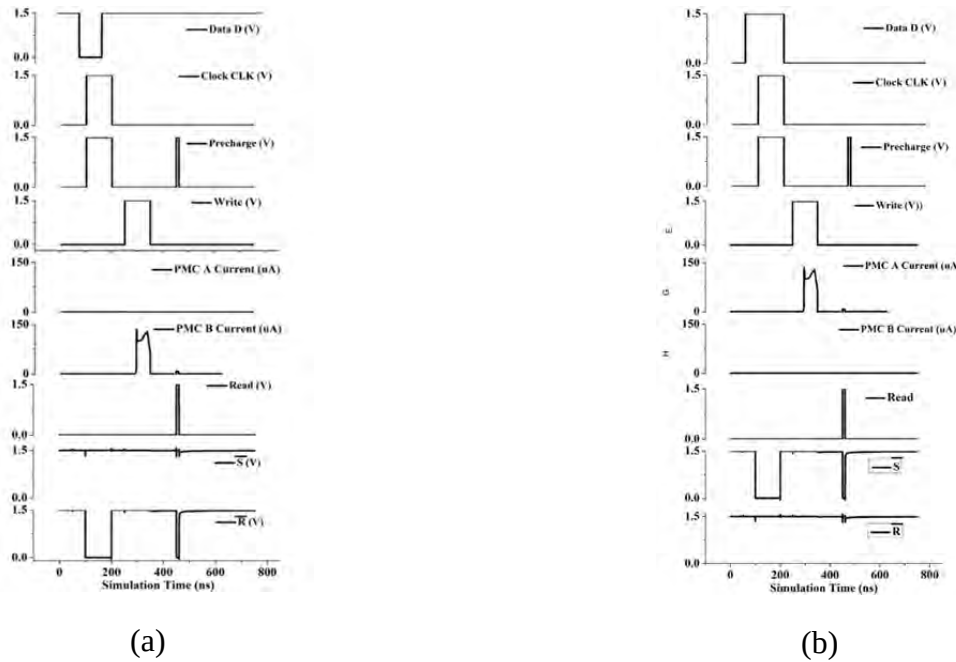


Figure 77. Transient simulation results

Static noise margin of a differential sense amplifier can be defined as the maximum DC voltage offset that can be applied to one side before the amplifier senses incorrectly. The static noise margins of the proposed modified read circuit of FF II is compared with that of FF I in Figure 78 for two different HRS/LRS ratios of 5 and 150 across a range of voltage supply (V_{dd}) levels. It can be seen that FF II demonstrates much higher sense margin than FF I in all cases.

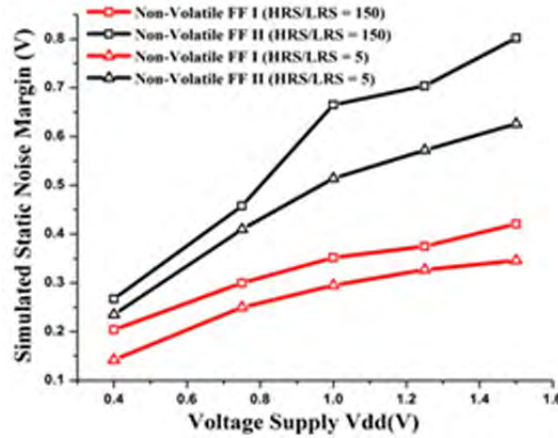


Figure 78. Comparison of static noise margins during read operation vs. supply voltage

6.2.2.2 Neuromorphic Circuits

Spike timing dependent plasticity (STDP) is an important biological learning mechanism in which the change in strength of a synapse connecting two neurons (called pre and post synaptic neurons) depends on the temporal correlation of the neuronal spiking behaviors. Traditional CMOS based STDP implementations have not achieved the dense connectivity and efficiency of their biological counterparts due to large area and power consumption. Low-power nanoscale non-volatile resistive memory (ReRAM) devices can be potentially used as electronic synapses along with CMOS neurons to drastically improve neuromorphic hardware performance. However, previous work in this regard has mainly been limited to STDP modeling and simulation or to experimental data from standalone ReRAM devices for simplified STDP rules. This work uses anionic ReRAM technology called Conductive Bridge Random Access Memory (CBRAM) as electronic synapse along with CMOS spiking neurons. Biologically accurate STDP based learning functionality in an integrated CMOS-CBRAM chip is experimentally demonstrated in post-silicon for the first time to the best of our knowledge, showing promise for more complex neuromorphic hardware design.

6.2.2.2.1 Spike Timing Dependent Plasticity

Figure 79(a) shows an overview of a hybrid CMOS-CBRAM neuromorphic architecture. If a parameter ΔT is defined as the relative timing delay in arrival of the post synaptic spike with respect to the pre synaptic spike, then as shown in Figure 79(b), for an electronic synapse (e.g., CBRAM) to adapt according to STDP rule, its strength (i.e. conductance) should increase if presynaptic spike arrives before postsynaptic spike ($\Delta T > 0$) and should decrease for the reverse case ($\Delta T < 0$).

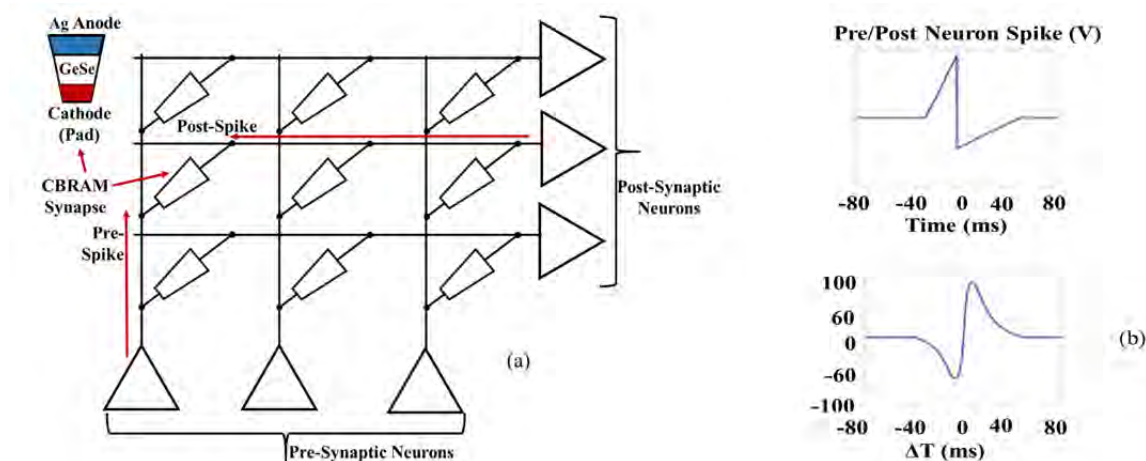


Figure 79. (a) Spiking neural array architecture and (b) neuron spike shape used in this work

6.2.2.2.2 Hardware Implementation

Pre-programmed low resistance state (LRS) of CBRAM is modulated as a synaptic weight to demonstrate STDP. The analog CMOS spiking neuron circuit used here (Figure 80) is based on biologically accurate circuits.

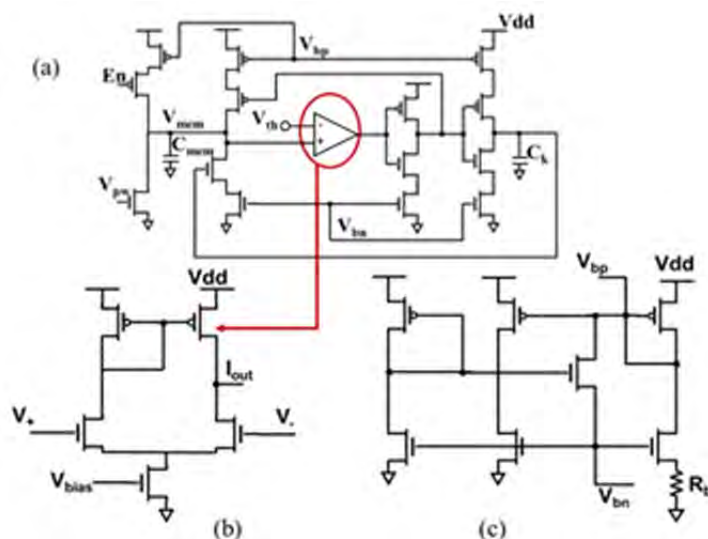


Figure 80. (a) Spiking neuron circuit design and (b) operational transconductance amplifier

An Enable (En) signal was added to externally synchronize the arrival of pre and post neuron spikes and control value of ΔT . All CMOS circuits were fabricated in a $0.6\mu\text{m}$ AMI process (Figure 81(a)).

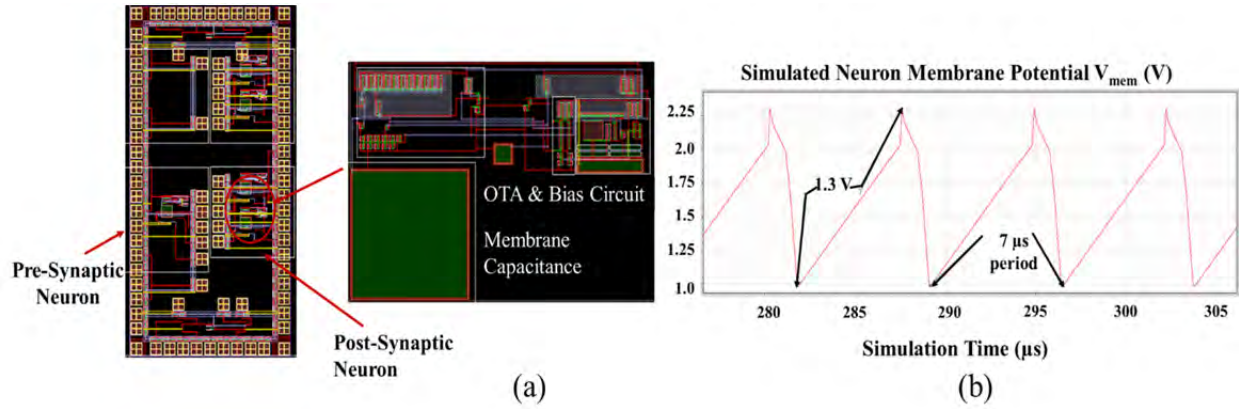


Figure 81. (a) Test chip layout and (b) simulated transient spiking output waveform

$\text{Ag}/\text{Ge}_{0.3}\text{Se}_{0.7}$ based CBRAM device layers were then deposited via post-processing on top of the contact pads. Figure 82 shows the schematic overview of the STDP measurement circuit, a sample on-chip CBRAM I-V characteristics and experimentally generated pre and post neuron spike traces. Figure 83(a) shows the hybrid chip after post processing which produces neuron spike outputs (Figure 83(b)) that match well with simulated results (Figure 81(b)). Finally, Figure 84 shows experimental evidence of CBRAM conductance change (% of initial value) vs. spike timing difference (ΔT) according to biologically realistic STDP behavior for two different spike durations of $7\mu\text{s}$ (Figure 84(a)) and $15\mu\text{s}$ (Figure 84(b)). A change in conductance between 20-40 % for three different initial LRS values (1 $\text{k}\Omega$, 5 $\text{k}\Omega$ and 10 $\text{k}\Omega$) is observed.

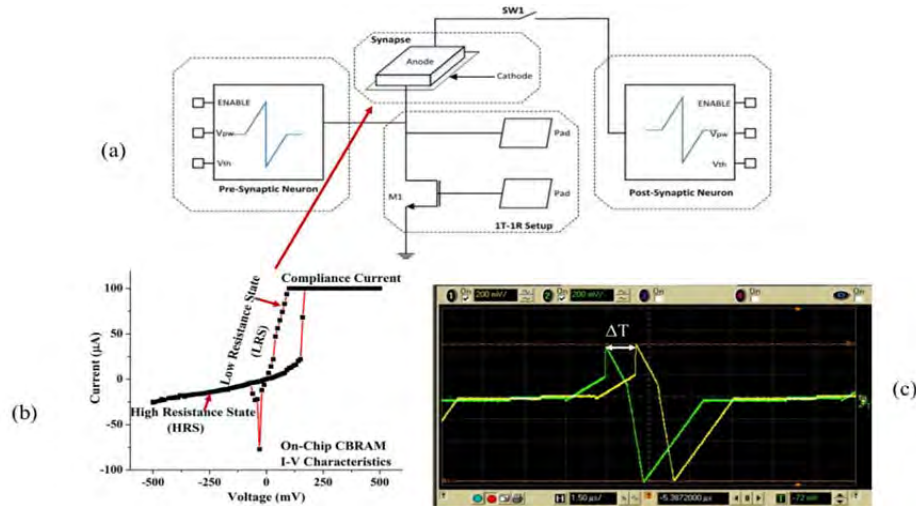


Figure 82. (a) Circuit used to demonstrate CBRAM STDP learning, (b) CBRAM I-V characteristics and (c) oscilloscope traces

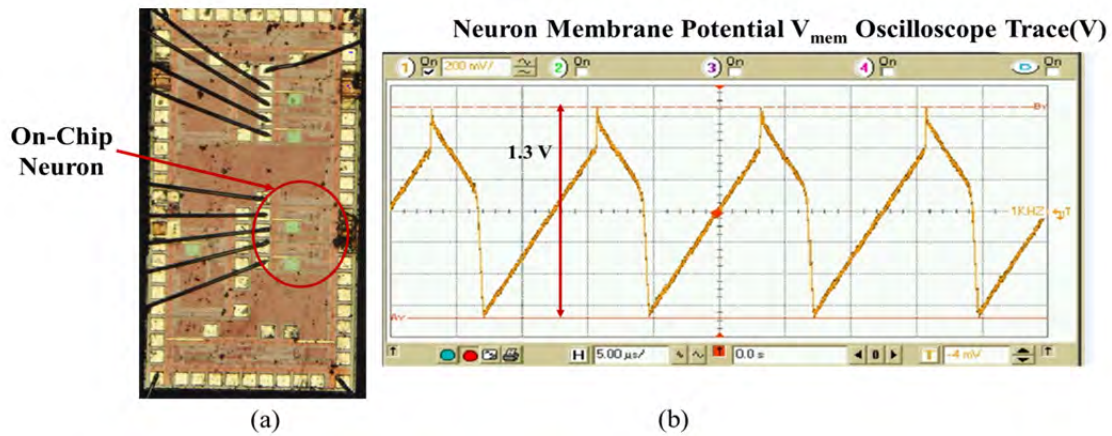


Figure 83. (a) Wire-bonded test chip and (b) generated spike output

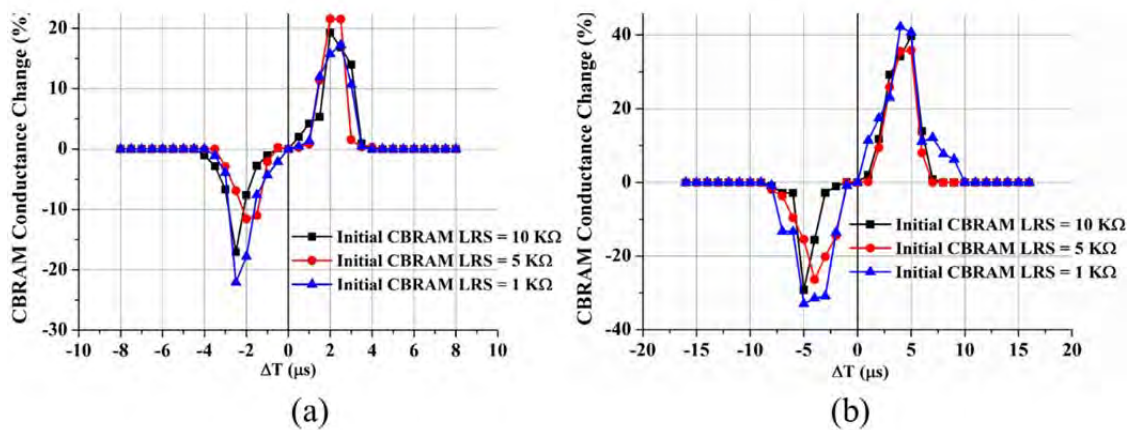


Figure 84. On-chip CBRAM conductance modulation (%) with spike timing difference (ΔT) for a pre/post neuron spike

6.3 Conclusions

A verilogA model for a Programmable Metallization Cells (PMC) has been developed in this task based on the results of experiments and data obtained in tasks 2 and 3.. The working of the PMC has been modelled by replicating the formation and dissolution of the conducting bridge. The DC characteristics of the PMC was simulated using the verilogA model. The simulation results were verified against experimental data for a wide range of compliance currents. The transient response of the PMC was simulated using the verilogA model. This was done using the write-read-erase-read pulse sequence. The ability of PMC to switch from HRS to LRS upon the application of a write pulse and remain in LRS until an erase pulse is applied has been

demonstrated. Multi-programming of the PMC has been shown by applying write pulses of different magnitudes.

In this task, a non-volatile sense amplifier flip-flop design was presented for ultra-low power applications that utilizes PMCs to store data during inactive period in absence of power supply, and then restore the data to the flip flop outputs when system resumes operation. Two flip-flop topologies with different data restore (read) circuits were presented and compared for robustness in noise margin. The Verilog-A compact model that fits experimental PMC switching behavior was used to perform simulations for functionality, energy and reliability analysis of the proposed design. The proposed flip-flop was shown to be sufficiently reliable even while operating at sub-threshold voltage supply levels. Since PMCs offer multi-level low resistance state (LRS) programmability, the effect of the choice of the LRS on the energy consumption and reliability of operation was investigated. It was concluded that even a sub-nominal HRS to LRS ratio of 10 can be sufficient to ensure reliable ultra-low voltage read operation at 250 mV power supply which is lower than previously reported non-volatile designs employing resistive memory devices.

We have also demonstrated the possibility of the PMC being used to replicate a synapse in neuromorphic circuits. Biologically realistic spike timing dependent plasticity (STDP) learning in an integrated CMOS-CBRAM resistive memory chip has been experimentally demonstrated for the first time, which can lead to large scale neuromorphic hardware realization using such devices..

The other major application area for the PMC model discussed is in large scale memories. A 1T-1R memory cell which can act as the building blocks for large scale memories has been simulated using the verilogA model. The I-V characteristics of the 1T-1R has been matched with experimental data. Multi-programming property of 1T-1R cell which can be used to create high density memory has also been demonstrated through the work in this task

The following list represents publications and conference presentations that were the outcome on work in this task:

1. D. Mahalanabis, V. Bharadwaj, H. J. Barnaby, S. Vrudhula, and M. N. Kozicki, "A Non-volatile Sense Amplifier Flip-flop Using Programmable Metallization Cells," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* (accepted April 2015).
2. D. Mahalanabis, M. Sivaraj, W. Chen, S. Shah, H.J. Barnaby, M.N. Kozicki, J. Blain Christen and S. Vrudhula, "Post-Silicon Demonstration of Spike Time Dependent Learning in CBRAM based Electronic Synapse," *submitted to the International Electron Devices Meeting (IEDM)*.

7 TASK 5 – RADIATION AND TEMPERATURE EFFECT TESTING AND MODELING

7.1 Methods, Assumptions, and Procedures

Co⁶⁰ gamma irradiation tests performed on ChG lateral test structures and ChG and SiO₂ PMCs with the GammaCell 220 source in the Radiation Effects Laboratory at ASU. Memory devices were also characterized for SEU response to heavy ions at the Lawrence Berkeley National Laboratory. Numerical device (TCAD) and circuit simulations, based on the physics-based models developed in Tasks 3 and 4, are used to model radiation effects. Models were validated, and refined based on comparisons to experimental data.

7.2 Results and Discussion

7.2.1 TID Effects in Lateral PMC Structures

7.2.1.1 Test description and Optical Results

The lateral devices were manufactured with three different sets of shadow masks. The first mask was designed to make an array of 2 mm diameter electrodes with variable spacing (2 mm, 4 mm, 6 mm, 8 mm and 10 mm) between nearest electrodes (Figure 85(a)). In mask two, the spacing was kept constant (2 mm) with arrays of two different electrode sizes: 2 mm and 8 mm diameter (Figure 85(b)). Finally, in the third mask, spacing was also kept constant (3 mm) and an array of two different electrode sizes, 4 mm and 6 mm diameter, was designed (Figure 85(c)). After fabrication, samples were placed into a Gammacell 220 for ⁶⁰Co gamma-ray exposure at a dose rate 477.5 rad(Ge₂₀Se₈₀)/min. They were periodically unloaded from the Gammacell chamber for a short amount of time to measure the electrical resistance between nearest electrodes using a semiconductor PA. The same measurements were performed on unexposed control samples. To avoid redox reaction at the electrodes, a very small bias voltage (10 mV) has been used to sample the resistance level. Optical images were taken after each measurement step to visually monitor the transport of Ag from the surface electrodes into Ge₂₀Se₈₀ film at increasing dose levels (Figure 86).

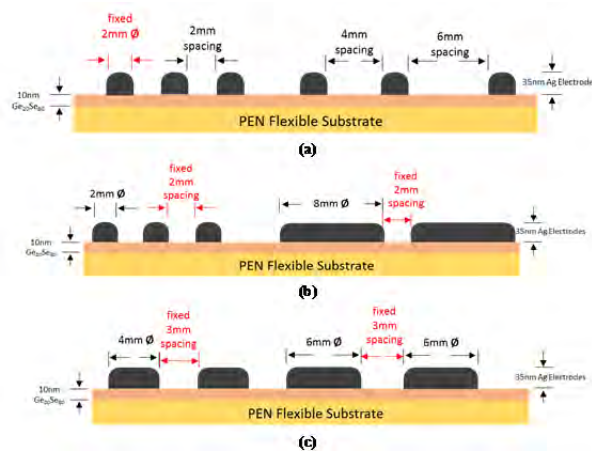


Figure 85. Cross-section view of the manufactured samples

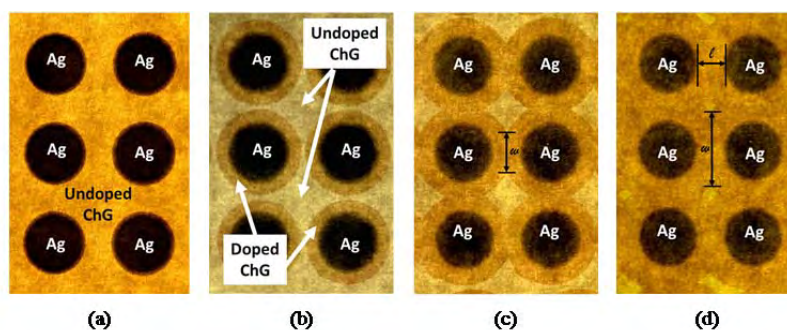


Figure 86. (a) pre-exposure state of the samples and (b) after 1.31 Mrad($\text{Ge}_{20}\text{Se}_{80}$), (c) after 2.55 Mrad($\text{Ge}_{20}\text{Se}_{80}$) and (d) after 4.56 Mrad($\text{Ge}_{20}\text{Se}_{80}$)

The ^{60}Co gamma ray exposure continued up to a maximum dose level of 4.5 Mrad($\text{Ge}_{20}\text{Se}_{80}$). During exposure, all the test samples were left floating by keeping the electrodes unconnected. Figure 87 shows optical images of the control and test samples (fixed electrode diameter, variable spacing) after 4.5 Mrad($\text{Ge}_{20}\text{Se}_{80}$).

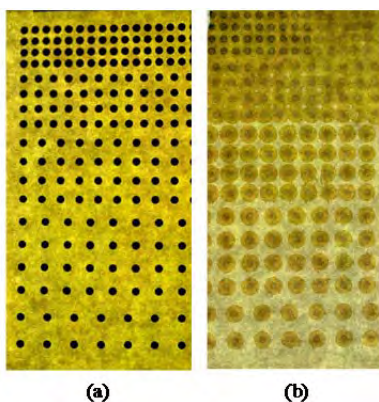


Figure 87. Images of (a) control and (b) test samples after 4.56 Mrad($\text{Ge}_{20}\text{Se}_{80}$) dose level

7.2.1.2 TID Results

Figure 88 shows the evolution of resistance with increasing dose level when the electrode area is fixed and the spacing between adjacent electrodes is varied. After the maximum dose level of 4.5 Mrad($\text{Ge}_{20}\text{Se}_{80}$), out of five arrays of electrodes with different spacing, the intermediate ChG region of only two arrays with minimum spacing (2 mm and 4 mm) were completely doped by Ag from surface electrodes (see Figure 88(b)). From Figure 88, we can see that the Limit of Detection (LOD) for a 2 mm spaced array is much lower compared to the array with 4 mm spacing. Both Figures 87(b) and 88 shown that even after the maximum dose level of 4.5 Mrad($\text{Ge}_{20}\text{Se}_{80}$), arrays with higher spacing (6 mm, 8 mm and 10 mm), did not reach full doping saturation. This indicates that the LOD of this Ag-ChG lateral sensing devices can be optimized by adjusting the spacing between nearest electrodes.

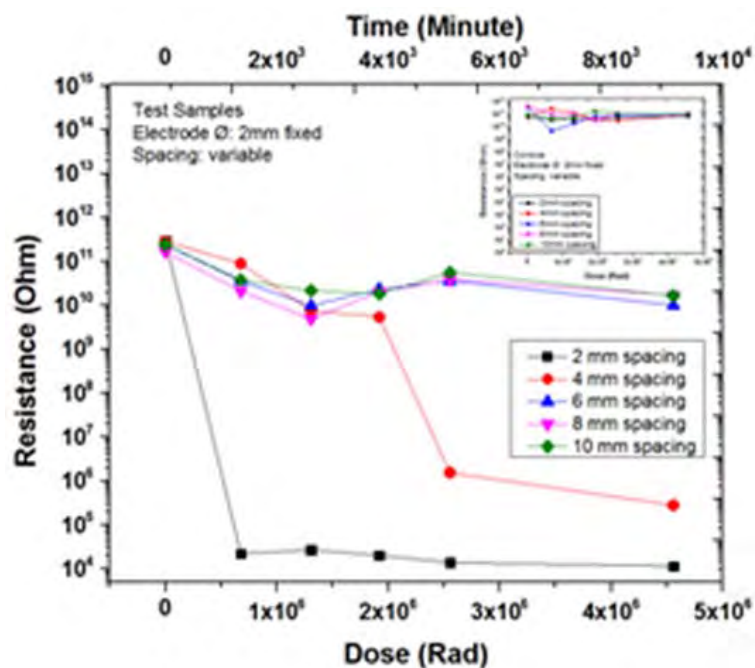


Figure 88. Evolution of resistance of the test and control samples (inset).

Apart from that, Dynamic Range (DR) can also be controlled by changing the spacing. The doped resistance/LRS between two nearest electrodes can be computed as $R = \rho l / (wt)$ where ρ is the resistivity of the Ag-Ge-Se ternary, which depends on the atomic fraction (x) of Ag present in $\text{Ag}_x\text{Ge}_y\text{Se}_z$, l is the spacing between two electrodes, w is the width/spread of the doped region (Figure 86c, 86d) and t is the thickness of ChG film. Figure 89 shows that by reducing spacing (l) between the nearest electrodes, DR can be increased (as LRS reduces when l decreases). This same control capability can also be attained with a different approach. By increasing the electrode area while keeping the intermediate spacing between the electrodes fixed, the DR can be increased as well. An electrode with bigger surface area can supply greater amount of Ag^+ ions when exposed to ionizing radiation. Thus, when the spacing remains fixed, larger electrodes will create wider doped region ($\sim$ bigger w) (Figure 86d). This larger w value results in a smaller doped resistance/LRS that increases the Dynamic Range. This phenomenon was observed with samples that had fixed spacing of 2 mm and 3 mm respectively while electrode diameter was varied from 2 mm to 8 mm (Figure 89a) and 4 mm to 6 mm (Figure 89b). However, we have not observed any role of electrode area on controlling the Limit of Detection (LOD) of these sensors. Table 11 shows the performance characteristics obtained from this experiment.

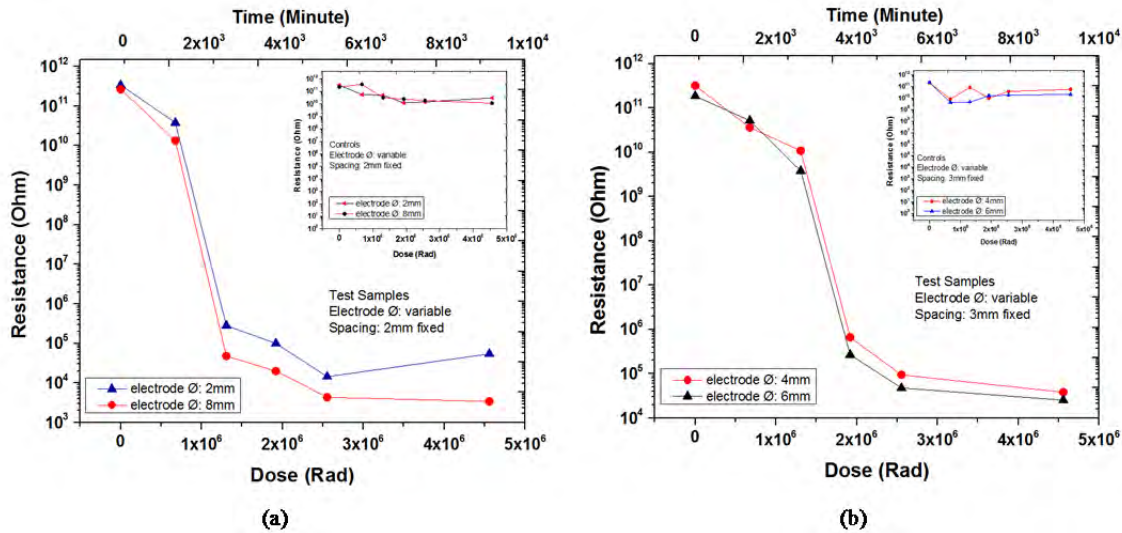


Figure 89. (a) Evolution of samples with fixed 2 mm spacing and (b) evolution with fixed 3 mm spacing

Table 11. Lateral Structure TID Results

	Fixed 2 mm electrode $\varnothing$ variable spacing (mm)					Fixed 2 mm spacing, variable electrode $\varnothing$ (mm)		Fixed 3 mm spacing, variable electrode $\varnothing$ (mm)	
	2	4	6	8	10	2	8	4	6
<i>DR (Ohm)</i>	3.0×10^{11}	5.4×10^{09}	NA	NA	NA	3.8×10^{10}	1.4×10^{10}	1.1×10^{10}	3.8×10^{09}
<i>Sensitivity</i>	-4.4×10^{05}	-8.6×10^{03}	NA	NA	NA	-6.0×10^{04}	-2.1×10^{04}	-1.8×10^{04}	-2.7×10^{04}
<i>LOD (Dose)</i>	0.0×10^{00}	1.9×10^{06}	NA	NA	NA	6.8×10^{05}	6.8×10^{05}	1.3×10^{06}	1.3×10^{06}

7.2.2 TID Effects in ChG PMCs

This subtask explores the response of ChG PMCs to a total ionizing dose γ -ray irradiation environment. Specifically, this chapter will cover the ability of PMC devices to retain their programmed HRS or LRS state while being subjected to ionizing ^{60}Co irradiation. Two different scenarios are explored. In the first scenario, studied devices were exposed up to 3.1 Mrad(Si) while device pins were left floating. Table 12 summarizes the dose steps for this scenario. In the second scenario devices were exposed, in one dose steps, to 15.1 Mrad(Si) with a constant 50 mV bias applied to the anode while the cathode pins were grounded. This second scenario was performed with *in situ* measurement, allowing any changes in resistance state to be observed real time.

7.2.2.1 Test Setup

All devices tested were fabricated using the method detailed in Task 1. Several device tiles were packaged into 28-pin ceramic dual in-line packages (CDIP), as shown in Figure 90. Before exposure to radiation, each package of devices was placed into an Agilent 16442B test fixture, as

shown in Figure 91, to conduct electrical characterization. During measurements, the lid of the test fixture remained closed to ensure that light did not affect the measured current-voltage (I-V) characteristics. The inputs of the test fixture were connected via low noise triaxial cables to the source monitor unit (SMU) outputs of an Agilent 4156C parameter analyzer. To perform an I-V measurement, the SMU connected to the cathode of a PMC device was set to constant common ground output while the SMU connected to the anode was staircase swept from 0 V to 0.5 V then back to 0 V in steps of 10 mV. The positive voltage sweep results in the I-V characteristic for programming the PMC device to a LRS. The LRS can be controlled by defining a compliance current on the parameter analyzer. The greater the compliance current value, the lower the LRS will be. To obtain the I-V characteristics for dissolving or *erasing* the filament, the anode is instead swept between 0 V and -0.5 V. Each device considered for testing was swept approximately thirty times to verify its functionality and obtain statistics concerning the LRS and HRS states. This measurement process was automated using LabView to control the parameter analyzer and collect data.

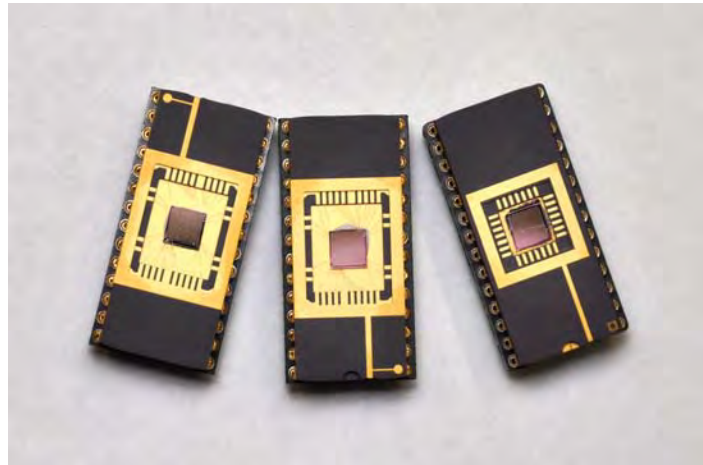


Figure 90. Crossbar device tile wire bonded into a 28-pin CDIP



Figure 91. Test fixture used for performing automated electrical measurements

Table 12. Radiation dose steps

Step Time (min)	Dose Step (rad(Si))	TID (rad(Si))
1523	8.075×10^5	8.075×10^5
1500	7.949×10^5	1.602×10^6
2934	1.555×10^6	3.158×10^6

Before exposing the devices to radiation, five devices were erased into their HRS and five others were programmed with an I-V sweep at a current compliance level of $1 \mu\text{A}$. The $1 \mu\text{A}$ programming compliance resulted in a LRS of approximately $100 \text{ k}\Omega$. After the devices were programmed, they were placed into a light tight box and walked to the irradiation facility. The devices were exposed to ^{60}Co γ -ray irradiation in a Gammacell 220. The Gammacell used is shown in Figure 92. The inner chamber of the Gammacell contains a ring of forty eight 21.11 cm tall *pencils*, each of which contains seven ^{60}Co slugs. Figure 93 shows the source cage contained inside the Gammacell 220. Devices to be irradiated were loaded into a sample chamber at the bottom of the shielding plug. When the plug is lowered into the chamber, the sample chamber is positioned at the center of the source ring.



Figure 92. The Gammacell 220 used for γ -ray exposure

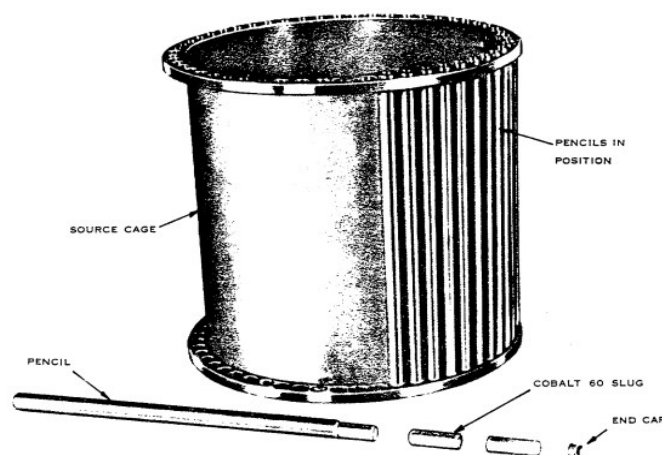


Figure 93. The source ring inside the central chamber of the Gammacell 220

Figure 94 shows a prototyping board with drawn on dose contour. The packaged devices were placed in the sockets along the center most contour to maintain equivalent exposure. The board was placed onto a wooden stand to hold the board during irradiation. The sample chamber was lowered into the Gammacell and left for exposure for the time steps listed in Table 12. The device pins were left floating during irradiation. At the end of each dose, the packages were removed from the chamber, placed inside a light tight box, and transferred to the lab to sample the resistance state of each device. The resistance state was sampled by applying a 10 mV signal to the anode. The samples remained outside of the irradiation chamber for less than two hours. The control devices (not irradiated) were tested in a similar fashion to the devices irradiated. Due to a limitation of available parts, only four control devices were used. Two of the devices were erased into the HRS and two were programmed using a DC sweep with a compliance current of $1 \mu\text{A}$. Measurements were performed in the test fixture used for the irradiated parts. Every 24 hours, the resistance state of the control devices were sampled. Once the measurements were completed, the device package was removed from the test fixture and placed in the same light tight box used to house the irradiated parts during transfer between labs. The purpose of removing the control device from the test fixture was to mimic the treatment of the irradiated packages.

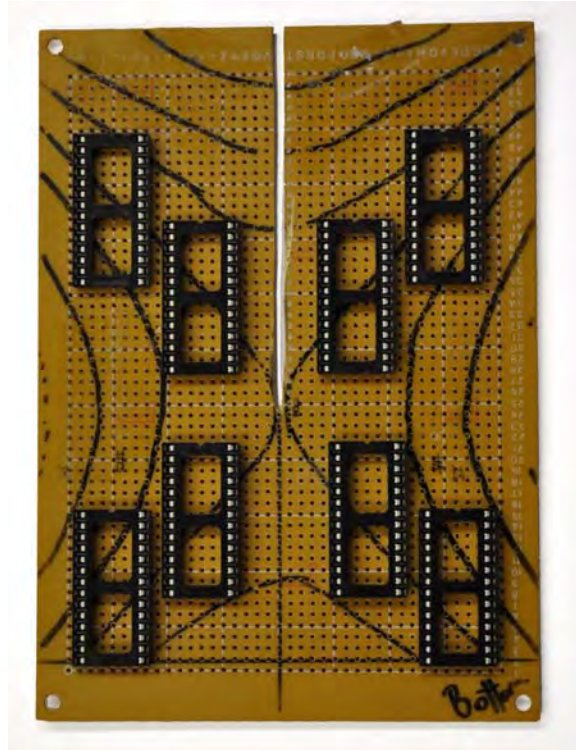


Figure 94. Prototyping board with marked dose contours of the Gammacell 220 chamber

7.2.2.2 Results and Discussion

The results in Figure 95 show that the irradiated PMC devices maintain their programmed state for the 3.1 Mrad(Si) TID. The gray cross hatched area defines the HRS region while the white region below is the LRS. The boundary between HRS and LRS was determined by calculating the median HRS value of the irradiated and control devices prior to irradiation. The irradiated devices (red line with open circle symbols) programmed to a HRS are shown to be fairly stable with dose. The plot shows the average HRS control device (pink dashed line) drifted to a higher resistance over time. Both the irradiated (blue line with open triangle) and control (green dashed line) devices in the LRS are shown to drift to a higher resistance within the first 24 hours of being programmed. After this initial drift, the irradiated devices remain approximately constant for the remainder of the test, while the control parts show a slight reduction. During the four day duration of the test, the irradiated devices maintained a window between HRS and LRS of two orders of magnitude.

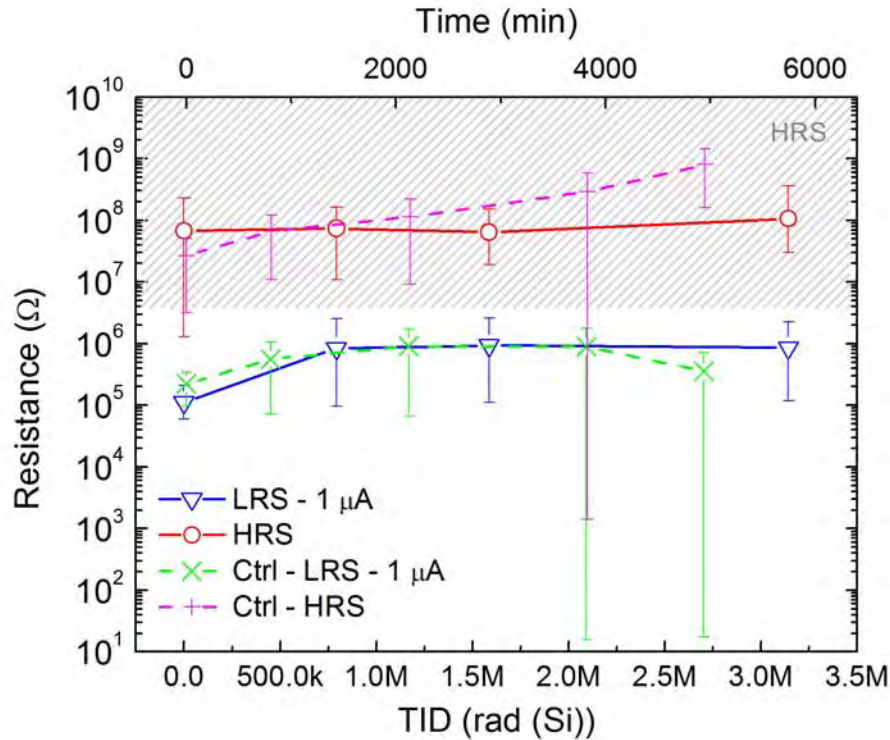


Figure 95. Retention of PMC devices during ionizing γ -ray irradiation to a TID of 3.1 Mrad(Si)

Due to the limited number of devices tested, the error bars represent the spread of resistance values measured at each dose step instead of standard error. The control devices are shown to have a larger variance than the irradiated devices. The drastic changes to a lower resistance by the control devices may be due to the way in which the devices were tested. For each measurement step, the packaged device was placed into the test structure for the measurement and removed afterward. The action of taking the package in and out of the socket may have induced static discharge which caused some devices to program to a lower resistance.

Previous studies [18, 19] on the effects of ionizing irradiation have shown that irradiation promotes the diffusion of Ag into the ChG layer. As part of the photodoping process, UV light exposure generates electron-hole pairs (ehp) in the Ag layer and encourages diffusion as well as chemical interaction with Se. If the γ -rays penetrate the metal contacts to interact with the filament itself, the Ag in the filament should become ionized and begin to diffuse into the surrounding ChG. The results presented in Figure 95 show that for the LRS, when the CF is formed, the state follows the behavior of the control devices, suggesting that the Ag in the CF is not dissolving due to irradiation. The stability of the CF is likely due to the presence of Ag in the ChG introduced by photo-doping. The background Ag concentration reduces diffusion forces on the filament which could cause it to dissolve.

During the fabrication of the devices, the ChG layer is photo-doped with approximately a 33 at.% concentration of Ag. The 33 at.% concentration has been shown to be the saturation point

for Ag diffusion into a Se based ChG. When Ag diffuses into $\text{Ge}_{30}\text{Se}_{70}$, the material becomes denser as the Ag fills pores that exist throughout the layer, preventing further diffusion of Ag. Simulated models have also investigated the roll the Ag doping profile has on the retention and switching capability of the devices. During irradiation, for non-biased (floating) devices, ehp production may not instigate significant photo-diffusion, as Ag^+ ion diffusion would be restricted by the saturation of Ag throughout the ChG.

In the work presented in section 4.2 the ChG layer is shown to have two regions (Figure 23), a Ag rich section and a Ag poor region [20]. Impedance spectroscopy also shows evidence of the two concentration regions. The Ag rich region is the volume at Ag saturation. The Ag poor region exists near the cathode contact and contains less than 10 at.% of Ag. The Ag poor region would be the region most likely to be effected by photo-diffusion instigated by ionization. If the Ag in the CF becomes ionized and begins to diffuse through the Ag poor region, the CF would begin to thin causing an increase in the resistance state. The HRS would also be observed to decrease slightly in resistance as the Ag poor region becomes further doped. Previous TID tests have shown that there is no noticeable shift in either the average LRS or HRS after exposure up to 10 Mrad [19, 21].

The TID retention tests presented in this section were performed on devices with contacts left floating during exposure. During normal operation of a memory array, depending on the architecture, device contacts would most likely be either biased or grounded. To appropriately observe the retention behavior, the PMCs need to be biased and exposed to a larger TID; as no significant effects were seen at a 3.1 Mrad(Si) exposure. The tests presented in the next chapter will explore the retention behavior of biased devices.

7.2.2.3 State Retention for TID up to 15 Mrad

The following experiments were performed at Sandia National Laboratories at the Gamma Irradiation Facility (GIF). The GIF features several dry-cell concrete rooms each with a unique ^{60}Co source to offer a wide variety of dose rates. The cells themselves are several square meters, allowing for the radiation exposure rate to be controlled by varying the distance from the source. While not in use, the ^{60}Co source is lowered into a water pool, making it safe for humans to enter the irradiation cell. Figure 97 shows the source ring raised out of its pool. The cell chosen for use in the following irradiation experiment contained a source with dose rates appropriate for MIL-STD883 method 1019.9 TID testing.

7.2.2.3.1 Test setup

The devices used for irradiation at the GIF were the cross bar structures described in task 2. Two chips were packaged into 40 pin CDIP packages to allow for access of more devices than the 28 pin CDIP. Each chip contains 32 devices with 20 devices accessible. The devices were voltage swept between -0.5 V and 0.5 V approximately 30 times using an Agilent 4155B PA controlled by LabView to verify device functionality. The device package to be irradiated was placed onto a test board that allowed each pin to be accessed with a ribbon cable connection. Four thermoluminescent dosimeters (CaF_2 TLD) were placed at the top of the test board and another four at the bottom of the board, just below the package socket. The test board was placed inside a

Pb/Al enclosure to shield the devices from low energy scattered radiation. The enclosure was suspended between two stands, like the ones shown in Figure 96, and oriented such that the package-side of the board faced the source ring. The stands were placed on the lip of the pool to achieve a high dose rate. The dose rate inside the enclosure was measured at 210 rad(Si)/s. Prior to radiation exposure, five devices were erased into a HRS and four were programmed to a LRS with a 100 μ A compliance current using a Keithley 2450 source monitor unit (SMU).

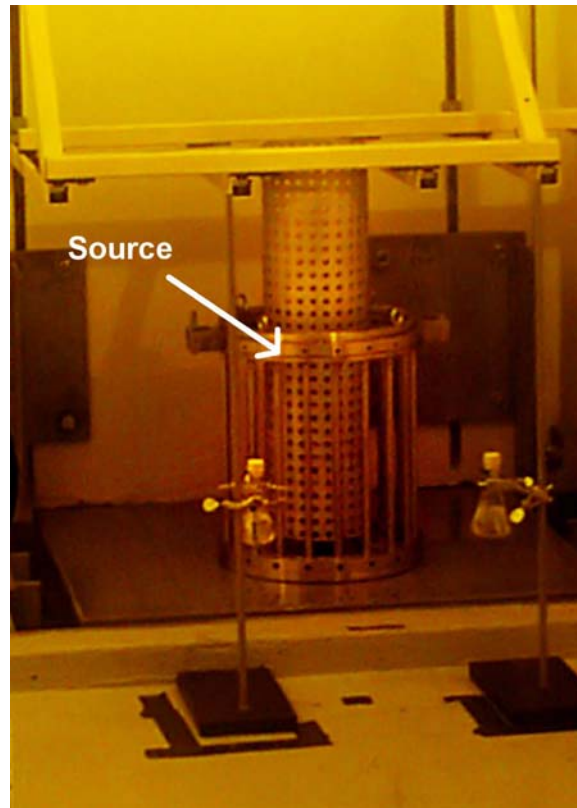


Figure 96. Dry-cell at GIF with raised ⁶⁰Co source ring

A packaged tile of control devices was kept outside of the radiation cell. The configuration used to monitor both the irradiated devices and control devices is shown in Figure 97. The devices inside the irradiation cell were individually accessed using two 60 ft ribbon cables connected to a printed circuit board (PCB) that converted the ribbon cable connections to BNC coaxial connections. Coaxial cables were connected from the PCB to individual inputs of a Yokogawa DL750 oscilloscope. The PCB used for accessing the control devices featured individual BNC connections for each pin of the device. The four control devices were also connected to the inputs of the oscilloscope. The remaining input was used to monitor the bias voltage applied to both the control and irradiated devices. During testing, a 50 mV read bias was applied to the circuit in Figure 97.

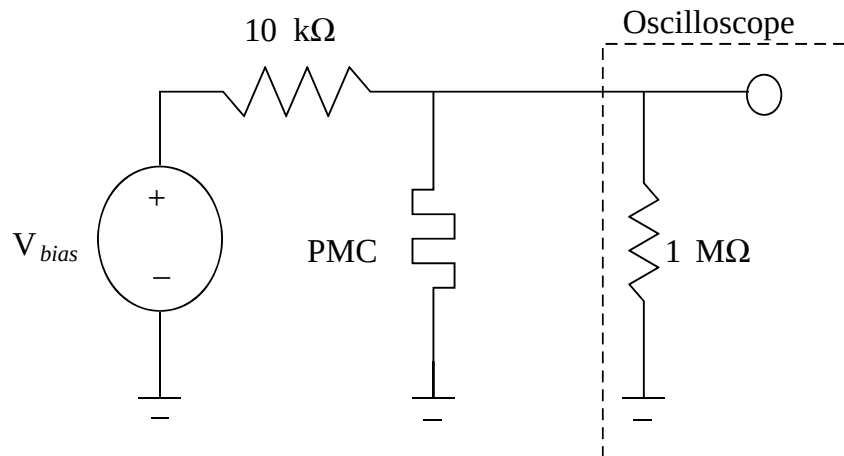


Figure 97. Circuit configuration used to actively monitor PMC devices

The PMC devices were irradiated at 210 rad(Si)/s for 20 hours to a TID of 15.1 Mrad(Si). During irradiation, the resistance state of the devices were sampled at a rate of 50 samples/s. Control devices were programmed to a LRS with a 100 μ A compliance current while two other devices were erased to a HRS.

7.2.2.3.2 Test Results

Using the configuration in Figure 97, the voltage vs. time signal measured on the oscilloscope was converted to the resistance values shown in Figure 98. The HRS is marked on the plot with a gray hashed area. The minimum HRS boundary is defined as the minimum observed value of the HRS while cycling the devices prior to irradiation (50 k Ω). The HRS state is shown to be very stable for the entire exposure. The largest variation in the HRS was 92.9 k Ω from the initial resistance. The plot in Figure 99 highlights the HRS with the mean of the two HRS control devices marked with a dashed magenta line. The HRS of the exposed devices did not vary significantly during the exposure, though small fluctuations are observed to occur after a dose of 300 krad(Si).

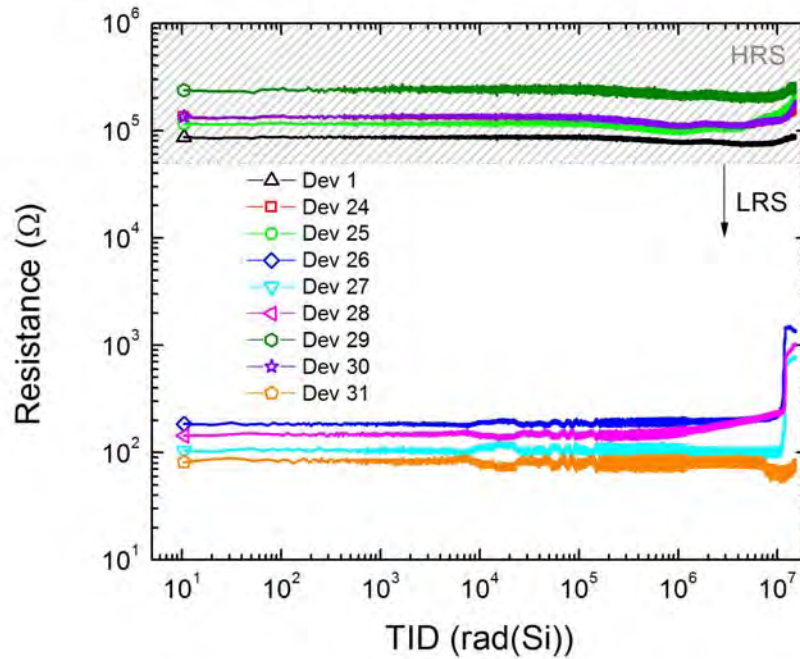


Figure 98. Retention of programmed resistances up to a TID of 15.1 Mrad(Si)

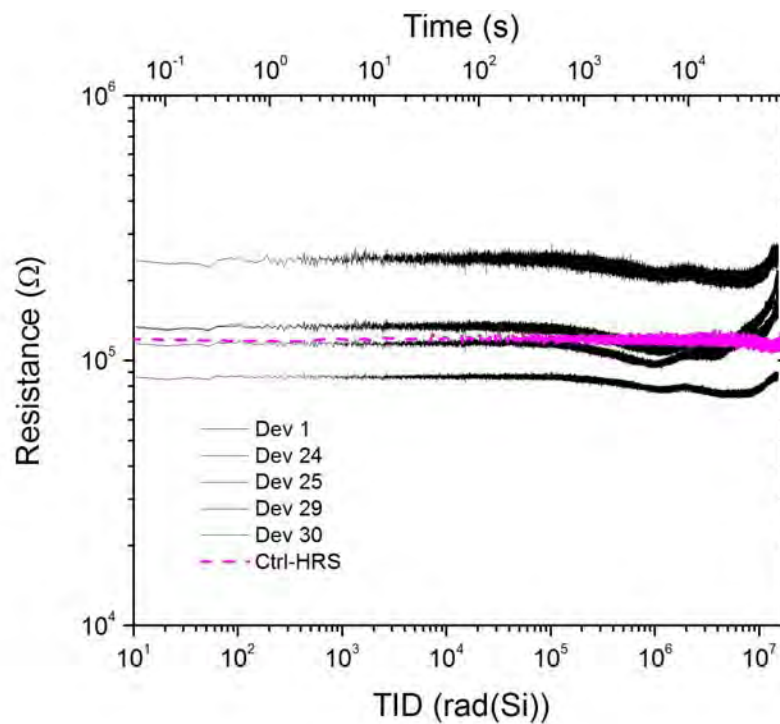


Figure 99. Retention of the HRS

The LRS is observed to be stable until a TID of 10 Mrad(Si), when three of the four devices rapidly decay to 1 k Ω . The fourth device slightly decreases in resistance before returning to its original state at a TID of 15 Mrad(Si). Though the devices shift a full magnitude in resistance, the final state is still within the defined LRS and it is beyond two orders of magnitude from the HRS. For a simple 1-bit logic scenario, no change in state is observed to occur. Looking at the control device behavior in Figure 100, the control devices are also observed to decay toward 1 k Ω shortly after the irradiated devices drifted in state. This decay may therefore not be related to radiation exposure, but to time. The time of the drift occurred at approximately 7 a.m., the beginning of the workday. It is possible that movement of people and equipment outside of the radiation cell electrically disturbed the circuit in some way. Changes in the noise observed in the LRS traces also suggest that something external may have affected the circuit.

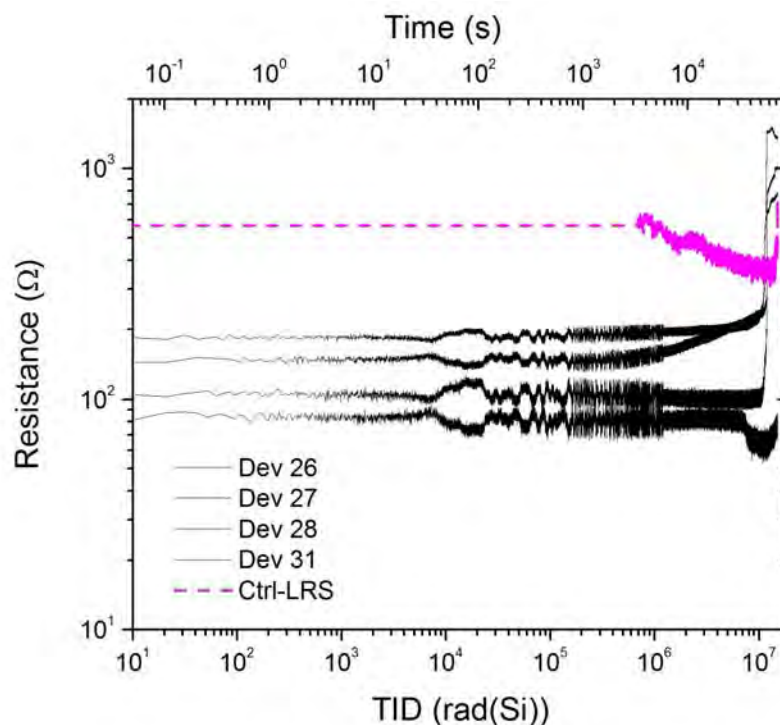


Figure 100. Retention of the LRS

One of the benefits of the PMC technology is the ability to reliably program a cell to multiple state levels [22]. For this application to function correctly in a radiation environment, it will need to retain its state and not transition to a different logic defined resistance level. For the presented case of a 100 Ω resistance level, the PMC devices are shown to remain at their programmed level until a TID of 10 Mrad(Si). Other LRSs will need to be observed to verify that multilevel program retention is possible in a radiation environment. The capability of the a high LRS state retaining its programming suggests that LRS retention between 100 k Ω and 100 Ω is likely.

Figure 101 shows that the PMCs tested in this thesis exhibit a TID tolerance, several orders of magnitude higher than commercial NAND flash devices [21]. The retention data presented in Figure 101 features the percent of errors observed per chip for NAND flash 8 Gb single-level

cell (SLC) and multi-level cell (MLC), 32 Gb SLC, and a 64 Gb MLC. The 8 Gb memory was fabricated at the 51 nm node and the 32 Gb and 64 Gb memory was fabricated at the 25 nm node. Each curve represents the average number of errors for three separate memory chips. The flash chips were operated in No Refresh Mode, meaning that at the end of each dose step, the programmed state was read to determine the retention of the initial programmed state.

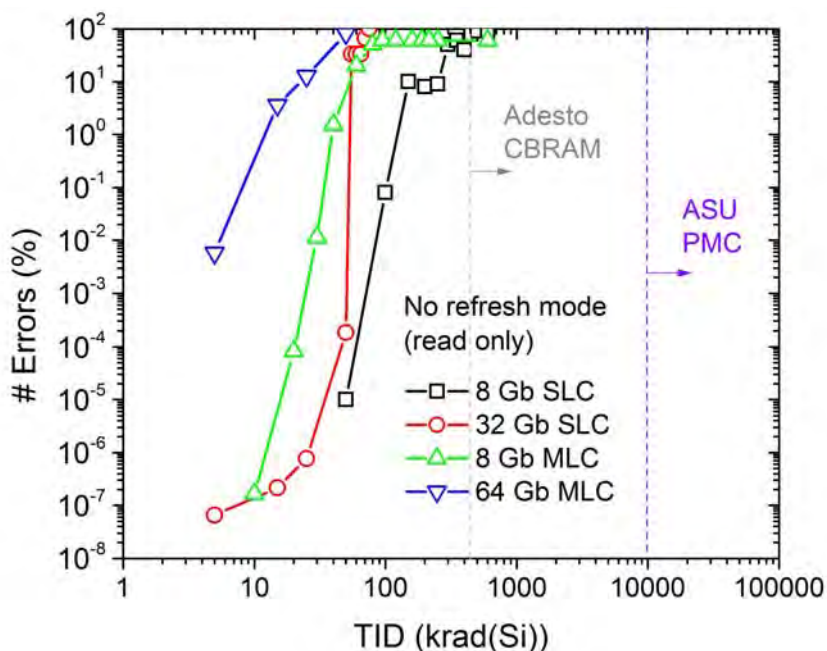


Figure 101. Percent errors as a function of TID in NAND flash no refresh mode retention

Preliminarily PMC devices are observed to have a greater tolerance to ^{60}Co γ -ray irradiation than NAND flash devices, but the tens of devices tested in this thesis do not compare to the billions of memory cells tested on the flash chips. To provide a better understanding of how ChG based PMC devices compare in performance to NAND flash, results for a GeS_2 based 128 kb CBRAM chip from Adesto Technologies Corporation is marked as a gray dotted line. The Adesto CBRAM devices function with the same mechanisms as the PMC devices presented. No errors were found up to the maximum tested TID of 447 krad (GeS_2).

7.2.3 TID Effects in SiO_2 PMCs

7.2.3.1 TID Effects on Virgin-state Resistance

Virgin-state resistance is defined as the resistance of an un-electroformed SiO_2 PMC. Figure 102 shows the I-V curves of virgin $\text{Cu/SiO}_2/\text{W}$ PMCs before and after different levels of ionizing dose. Devices with 10 μm and 100 μm size are investigated to find if area impacts the radiation response, which it does not. For each size, three devices were DC swept before and after each dose step. The voltage sweep stops at 100 mV to avoid electroforming and unintentional incorporation of Cu ions. The data indicate that there are no significant shifts in virgin resistance caused by TID exposure. This result differs from what has been reported on Ag-ChG radiation

sensors where the virgin-state resistance decreases with increasing TID [23]. The reduction of this virgin resistance in Ag-ChG is thought to be caused by radiation-induced doping of Ag into chalcogenide glasses. The absence of virgin-state resistance reduction of Cu-SiO₂ PMCs indicates that Cu is *not* incorporated into the un-electroformed SiO₂ layer after exposure. This is a major difference in the two technologies.

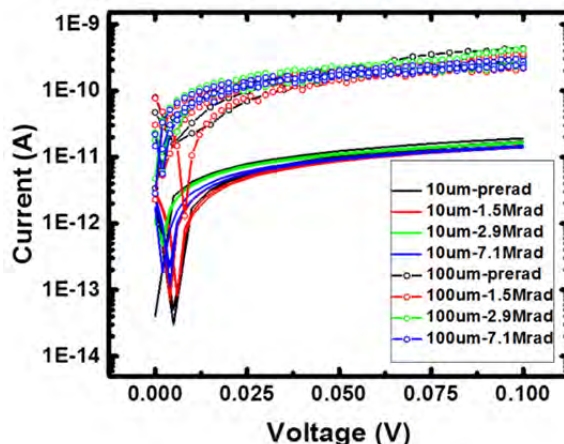


Figure 102. I-V characteristics of pristine devices with a size of 10um and 100um at different TID level

7.2.3.2 TID Effects on ON- and OFF-state Resistance

Ionizing radiation effects on the ON- and OFF-states are investigated in this sub-section. A set of 10 devices (5 for on-state and 5 for off-state) with 10 μm size were tested at different dose levels. Each device was DC swept for 10 cycles with a compliance current of 5 μA . Devices were step stressed up to 7.1 Mrad(SiO₂). Dose levels are differentiated by colors as shown in Figure 104. To minimize the inherent ‘noise’ introduced by voltage cycling and environmental variation, another set of control samples, labeled as ‘non-irrad’, was measured at the same test frequency as the irradiated samples.

Figure 103(a) plots the cumulative probability distribution of resistance for ON-state (electroformed) PMCs prior to and after ⁶⁰Co irradiations up to 7.1 Mrad(SiO₂). While the distribution in OFF-state resistance is considerably broader than the ON-state, it can be observed in Figure 103(b), that exposure to gamma rays, even at high levels of TID, does not change the distribution in any significant way. A potential explanation for the higher skew in the OFF-state distribution even prior to exposure may be due to some devices not being fully reset, which is somewhat common in resistive switching memory. For irradiated samples, the average ON-state resistance for different dose level ranges from 27.3k Ω to 35.3k Ω , while the average OFF-state resistance is between 1.41G Ω to 2.47G Ω , which is significantly higher than the reported M Ω -range OFF-state resistance in Ag-ChG PMCs. The ON-state resistances of these two technologies are comparable. Note that the G Ω -range OFF-state resistance is particularly suitable for PMC crossbar arrays and switches in FPGA circuits, as this will reduce current leakage and standby power. In addition, the large difference between ON- and OFF-state resistances in

Cu/SiO₂/W PMCs not only facilitates data sensing, it also supports more multilevel ON-states for compact data storage.

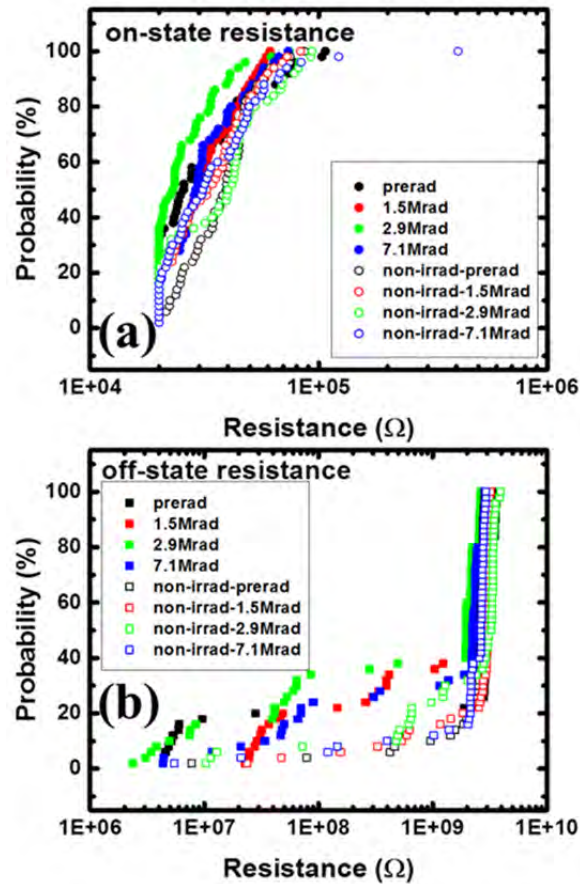


Figure 103. (a) Cumulative probability of ON-state resistance and (b) probability of OFF-state resistance at different TID

Since cumulative distribution reflects only general trends, it is possible that subtle changes are not observable in the plots. Thus, it is necessary to investigate how each individual device responds to TID. Figures 104(a) and 104(b) show the device-to-device comparison results. In each figure, irradiated samples and control samples are plotted in the left and right half windows, respectively. Figure 104(a) compares ON-state resistance value after different TIDs from device to device. Again, the same as the cumulative plots have shown, for both irradiated and non-irradiated samples we find that data overlap randomly at different dose levels, which means the irradiation has no significant influence on ON-state resistance. The situation for OFF-state resistance is slightly different. Here, we focus only on OFF-state resistances in GΩ-range (complete reset). It can be seen in the left-half of Figure 104(b) that the overall average OFF-state resistance decreases slightly after the 1.5 Mrad exposure but this reduction saturates if the devices are exposed to higher TID levels. This is not the case for the control samples, where no discernable change is observed at any dose.

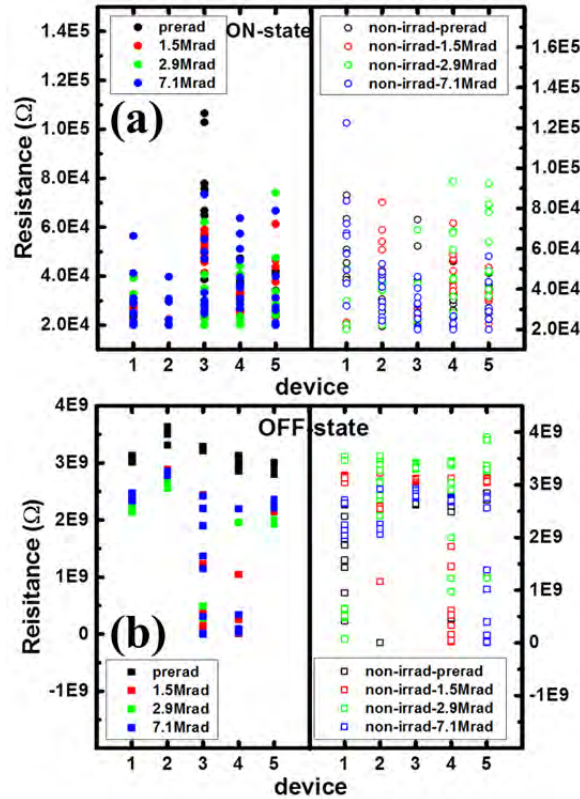


Figure 104. (a) device-to-device comparison of TID effects on ON-state resistance and (b) OFF-state resistance

7.2.3.3 TID Effects Set(Threshold) Voltage

Unlike chalcogenide glass in which the metal ion moves fast, ions move much more slowly in oxides. The result is that the ions in oxide tend to be reduced by electrons before reaching inert cathode. The source of electrons can be tunneling electrons and/or trapped electrons in the film. Filaments grow faster in oxides with higher leakage current. Since ionizing radiation is capable of inducing leakage current, it is interesting to investigate the influence of ionizing radiation on the growth speed of the filament. This speed can be qualitatively related to the set voltage (V_{set}) if a fixed voltage-sweep rate is applied. The faster a filament grows, the smaller the V_{set} . Figure 105 plots the cumulative distribution of V_{set} at different radiation dose levels. As shown in the figure, the V_{set} of irradiated and control samples randomly overlap each other, suggesting that gamma-ray irradiation has a negligible impact on the speed of filament growth. This may be due to the fact that in evaporated SiO_2 there is typically a very high density of pre-existing defects. The leakage current induced by those pre-existing defects overwhelms any potential effect from leakage current enhanced by irradiation. Another reason could be due to the relatively long voltage stress in DC sweeps. Such subtle changes in growth speed is likely to be covered up in the long DC stress. For example, either the device is set at the beginning or the end of a 0.4V voltage step, the DC curve can only reflect that the device is turned on at 0.4V. Thus, the conclusion that ionizing radiation does not affect filament growth speed is at present only valid for a quasi-DC condition. It needs to be further investigated for transient pulse measurements.

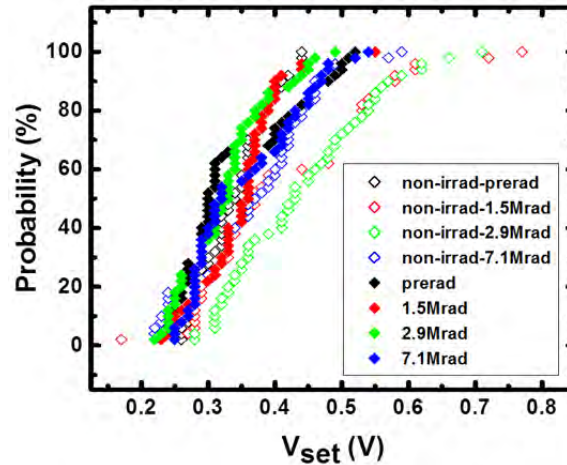


Figure 105. Cumulative probability of Vset at different TID

7.2.3.4 TID Effects on Multilevel Switching

Multilevel switching ability is a key property of PMCs that supports their use in Multi-level Cell (MLC) memory as well as neuromorphic computation. Assessing the reproducibility of multilevel switching after ionizing radiation exposure is therefore of interest. Figure 106 plots the ON-state resistance vs. programming current in a log-log scale for unexposed PMCs and PMCs that were irradiated for 7.1 Mrad(SiO_2). Both pre- and post-rad responses follow similar power law trends to those observed in ChG PMCs. The extracted A and n for irradiated samples are 3.9 and 0.8, respectively, which is essentially the same as the values extracted for non-irradiated control samples. Thus, the data shows that ionizing radiation has a negligible impact on multilevel switching.

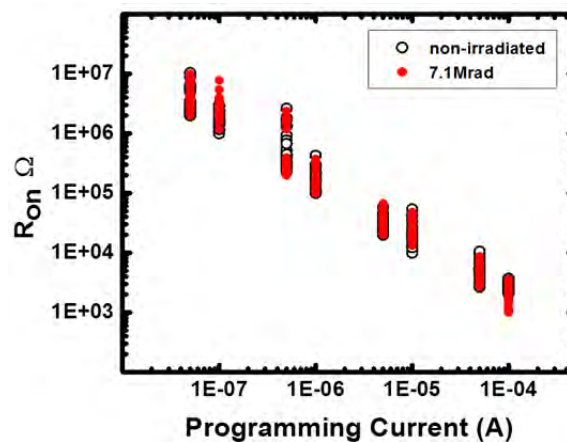


Figure 106. Comparison of Ron vs. Iprog before and after 7.1Mrad TID

7.2.3.5 TID Effects on Endurance

Data presented in the previous sections shows only minor changes in the characteristics of Cu-SiO₂ PMCs caused by TID. This could be because the effects are too subtle to be observed. Endurance tests were performed on two sets of five devices to potentially amplify these small changes. One set was irradiated up to 7.1 Mrad (SiO₂) and the other was an un-exposed control sample set. In order to minimize the effect of long term annealing of radiation-induced-traps all devices were cycled until failure or manually stopped at a maximum of 500 cycles to shorten the test duration. Figure 107(a) shows a typical endurance result for an irradiated device and a non-irradiated device. Both of them show the same failure mechanism: resistive switching gets stuck in the ON-state. It is likely caused by the introduction of excess Cu ions into oxide during cycling. Figure 107(b) summarizes the results from this experiment. The x-axis is the number of cycles that can be attained by DC sweeps and the y-axis represents the cumulative probability. For the control sample, two out of five devices can be cycled at least 500 times, the other three fail before 500 cycles. For the irradiated samples, one device can be cycled for 500 times. Even though some differences in endurance between irradiated and un-irradiated devices are observed, this is most likely caused by process variations, not radiation damage. It should be noted that the PMCs tested in this work are simple two terminal structures over-stressed by the DC characterization technique. Endurance can be improved by using 1T1R structures and/or applying electrical pulses.

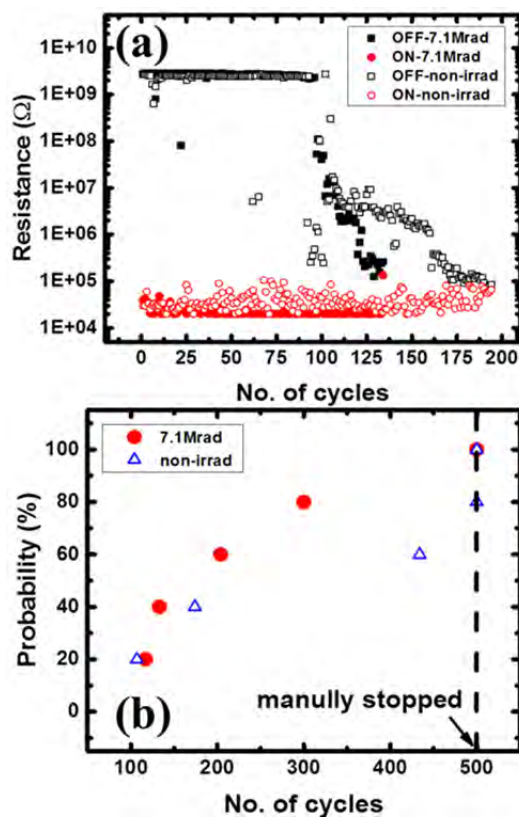


Figure 107. (a) Cycling of irradiated and control devices and (b) cumulative plot

7.2.3.6 Discussion

Several interpretations can be made of the results presented above. First, we observe that the virgin-state Cu-SiO₂ PMC does not seem to be affected by ionizing radiation up to 7.1Mrad. This is not the case for PMCs fabricated with active Ag on ChG, specifically Ge_xSe_{1-x}, films, which normally exhibit radiation-induced photo-doping. Photo-doping in the Ag-ChG PMC is triggered by the interaction between Ag and electron-hole pairs (ehps) generated in the electrolyte. Density functional theory (DFT) calculations show that Ag atoms will auto-ionize on entering the interstitial sites of Ge₂Se₃ [24], because the singly occupied atomic Ag 5s-state is above the conduction band edge, and there are essentially no Ag levels in the bandgap. The calculations predict that Ag loses its 5s electron to the Ge₂Se₃ conduction band edge (CBE). Subsequently, the electron self-traps on one of the many Ge-Ge dimers. The projected density of states (PDOS) for the Ag- Ge₂Se₃ system near the band gap is shown in Figure 108. The bulk Se (black line) delineates the valence and conduction band-edges. The Ag states (in green) are either buried in the valence band, or above the CBE. The Fermi level is at the conduction band-edge, just above the localized self-trapping state. Note this state has very little Ag character, and is comprised of nearly equal Ge and Se contributions. In Figure 109, we show the PDOS for interstitial Cu in SiO₂. Here the band edges are delineated by the Silicon (red) density, with the CBE at -2.0 eV, confirmed in separate, bulk SiO₂ calculations. The Cu density is in green. Here Cu has a continuum and two apparent discrete states in the band gap. The continuum is predominantly Cu 3d. Thus, the calculations predict that Cu²⁺ is not stable, i.e., it will readily trap electrons and neutralize, suppressing ion transport, particularly in its virgin state.

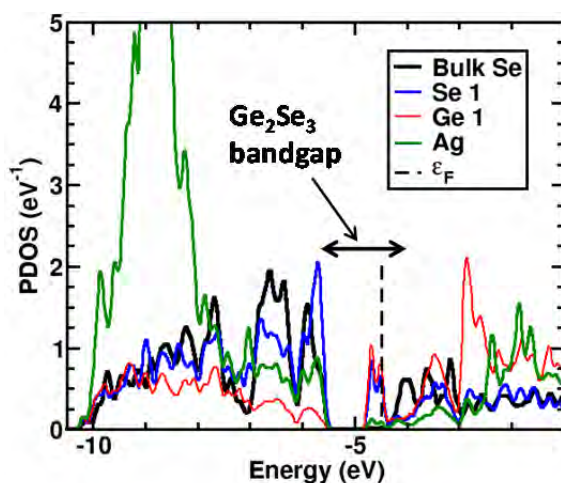


Figure 108. DFT calculations showing projected density of states for Ag- Ge₂Se₃ system

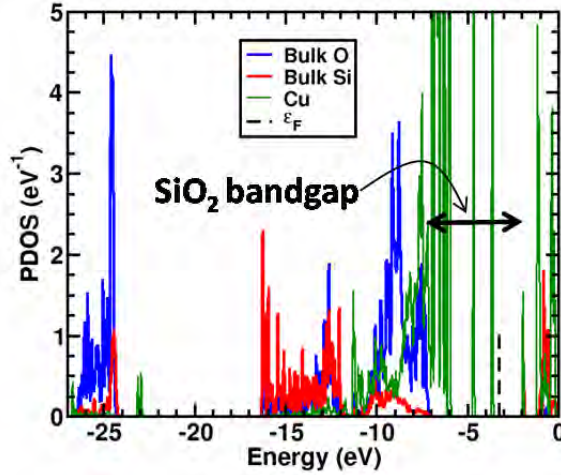


Figure 109. DFT calculations showing projected density of states for Cu-SiO₂ system

In addition to differences in the charge state of Cu in SiO₂ vs. Ag in Ge_xSe_{1-x}, another potential explanation for the suppression of photo-doping in the virgin-state Cu-oxide PMC is the much larger bandgap of SiO₂ (> 8 eV) relative to GeSe (< 2 eV). The number of generated ehps per rad is determined by the bandgap of the target material according to

$$\frac{\#ehp}{cm^3 rad} = 100 \cdot \frac{1}{1.6 \times 10^{-12}} \cdot \frac{1}{E_p} \cdot \rho, \quad (65)$$

where ρ is the material density and E_p is the mean energy needed to ionize a material. E_p is proportional to the bandgap (approximately 2X to 3 X). Many ehps are generated in ChG by gamma-rays because of its relatively small bandgap. However, this is not the case in Cu-SiO₂ films. The amount of electron-hole pairs generated in SiO₂ is considerably lower than the Ge₂Se₃ since SiO₂ has a larger bandgap. In addition to the impact of the material's metallic states and bandgaps, an added distinction between the ChG and oxide systems is the nature of carrier traps. Although it is well known that ehps generated in dielectrics can be trapped in defect precursor sites the prevalent type of trap is different from one material to another. Electron-traps play a major role in chalcogenide glasses, such as Ge₂Se₃. DFT calculations predict that electrons tend to be self-trapped in pairs because of Ge-Ge dimers [24]. The electron-traps may play an important role in photo-doping of Ag in the Ge₂Se₃ layer, either by breaking Ge-Ge and Ge-Se bonds that act as sites for Ag incorporation or by attracting positive ions into the ChG film through drift mechanisms. This causes the resistance of virgin Ge₂Se₃ films to drop, due to the incorporation of Ag ions, by orders of magnitude after gamma-ray irradiation [18]. However, the trapped charge in SiO₂ is net positive due to the capture of holes in neutral oxygen vacancies [25]. Thus, the positively charged hole would repel rather than attract Cu since the trapped hole has the same charge polarity as any residual Cu ions. Radiation induced hole-traps in SiO₂ is thus another potential explanation for why the virgin state resistance is barely impacted by ionizing radiation. Indeed, all three of these mechanisms (neutral Cu in SiO₂, low ehp generation rates, and hole trapping) are reasonable explanations for the suppression of the photo-doping process and reduced resistance in CuSiO₂ virgin state PMCs.

Our results show that in the OFF-state, there is an initial drop but saturation in the resistance change after 1.5 Mrad. While this response needs further investigation, one explanation for this, particularly after considering the virgin state response, may be the presence of either transient or permanent electron traps generated during irradiation. These might include positively charged E' centers and transient self-trapped holes. Both of these examples have o/+ defect levels in the lower half of the band gap. These defects could serve as sinks for electrons from neutral copper atoms, setting up an electrostatic potential leading to greater mobility. Saturation could arise because irradiation does not lead to more Cu atoms being liberated from the top electrode, so that only those already in the oxide would be available for radiation-induced ionization and transport.

7.2.4 Single Event Effects in PMC-Based Memory

7.2.4.1 Single Event Effect Simulation

The MOSFET drain to body junction is a particularly sensitive strike location in bulk CMOS technologies. Drain strikes can cause forward biasing of drain-substrate junction, leading to generation of drain voltage transients which can even go negative. Therefore, in this subtask only ion strikes at the drain are considered. Two possible types of upset are considered- a HRS 1T-1R element changing to a LRS, and a previously LRS cell changing to a HRS.

The linear energy transfer (LET) of the charged particles striking the CMOS layer of 1T-1R memory can be expressed in terms of the total energy lost per unit path length traversed by the particle (E) as $E = LET \cdot \rho$, where ρ is density of the irradiated material. This in turn can be used to calculate specific ionization (SI) i.e. number of ion pairs formed per unit volume traversed by the charged particle as $SI = E / (w \cdot \pi \cdot r^2)$, r being the path track radius and w being a material property that indicates the energy required to generate a single ion pair. The ion pair generation rate (G) can hence be calculated as $G = SI / \tau$ (in ions/cm³.s), τ being the ion transit time. In this way the ion pair generation rate (G) can be estimated for a given incident ion LET.

Magnitude and duration of current and voltage transients generated due to heavy ion strike existing bias conditions in a MOSFET depend heavily on the existing bias conditions at the time of ion strike. The most likely bias condition for a SEU in a 1T-1R memory array is depicted in Figure 110(a), i.e., when a write operation is being performed on a 1T-1R cell in a row. During this operation, all cells in the same row receive a voltage VDD (nominally 1V - 2V) on the bit line and 0 V on the select line. If a cell in this row is not being written (word line is at 0 V), but its access NMOS drain is struck by an ion during this time, the resulting current transient can cause the voltage at the NMOS drain (PMC cathode) to drop below the initial condition (VDD) and can even go negative. Hence a net transient positive voltage difference develops across the PMC and makes it susceptible to a SEU. If this cell is in HRS and undergoes transition to a resistance comparable to the LRS, then data stored in the cell switches to a '1' from a '0'. Under this operating condition, an ion strike-induced transient voltage pulse generated at the drain (also the PMC cathode) can be modeled by the equivalent circuit shown in Figure 110(b) consisting of the PMC in series with the parasitic drain-bulk junction diode and an ion-induced current (modeled by an ideal current source). This current (I_{ph}) resulting from electron hole pair generation can be defined as [26].

$$I_{ph} = qAG(x_j + L_e) , \quad (66)$$

where A is the drain area (in cm^2), x_j is junction depth of the drain (in cm), L_e is electron diffusion length (in cm) and G is the carrier generation rate (in $\text{ions}/\text{cm}^3.\text{s}$) which can be estimated from the incident ion LET as described earlier. For a given LET, the generation rate is obtained by assuming an ion strike profile diameter of 200 nm and 5 ps duration [27]. The ion strike generated current is then estimated using (6). The circuit simulation is performed using the PMC model discussed previously (variable resistance RCF) in parallel with an intrinsic PMC capacitance (C_P) whose value is estimated by extrapolating experimentally measured device capacitance. The diode is modeled as the drain-body junction in a 130 nm CMOS process. For a sufficiently high photocurrent, the drain (PMC cathode) voltage, which is initially at V_{DD} , drops to a negative value. This generates a corresponding net positive voltage transient across the PMC. Figure 111(a) shows a voltage transient waveform generated during simulation and corresponding transition of HRS 1T-1R element to a LRS for an LET of $8\text{MeV}.\text{cm}^2/\text{mg}$. Figure 111(b) shows the simulated PMC resistance after transient generation in the circuit of Figure 110(b) for different ion LET values. A threshold LET can be estimated beyond which PMC resistance becomes comparable to the designated LRS for the binary memory array (taken to be $\sim 10\text{ K}\Omega$) Finally, it may be noted here that an increase in strike profile diameter will reduce generation rate (G), which in turn will reduce the photocurrent generated. As an example, for the simulation shown in Figure 111(a), the corresponding photocurrent magnitude is $\approx 540\text{ }\mu\text{A}$. A 10% increase (decrease) in the nominal profile diameter can cause this photocurrent magnitude to decrease (increase) to approximately $440\text{ }\mu\text{A}$ ($656\text{ }\mu\text{A}$). On the other hand, an increase (decrease) in ion strike duration can increase (decrease) the duration of the transient voltage pulse generated across the PMC, which in turn can increase (decrease) the total change in PMC resistance.

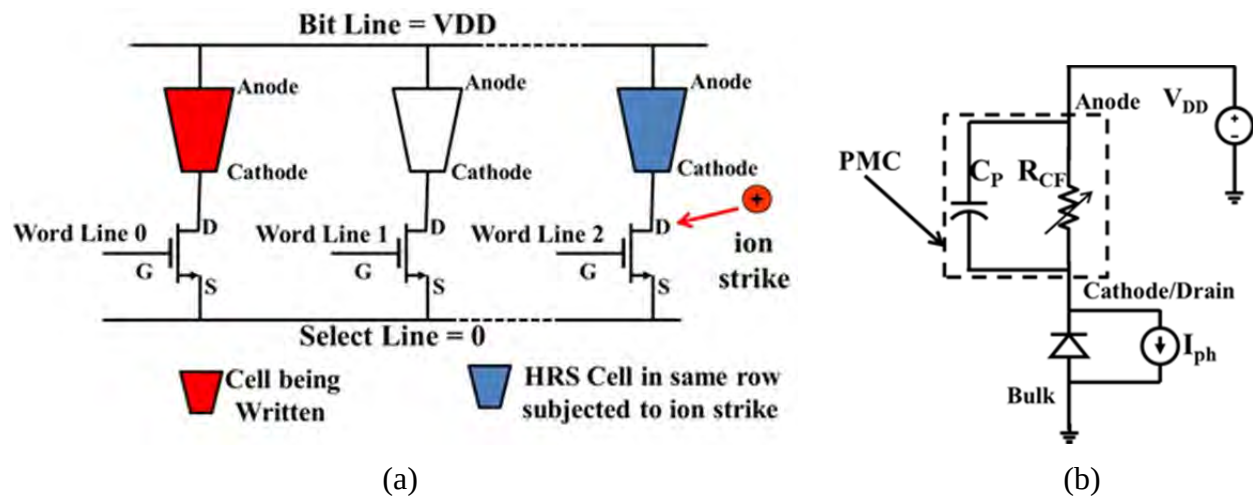


Figure 110. (a) Ion strike induced single event on a HRS element and (b) equivalent circuit for the HRS cell

The simulation results thus show that spurious HRS to LRS transitions may occur in 1T-1R PMCs during write operation on another element in the same row leading to errors in stored data. It is also worth noting that the likelihood of an upset increases substantially in presence of higher positive bias (V_{DD}) on the bit line during the ion strike, as this increases the voltage transient

magnitude across the PMC, which in turn increases change in PMC resistance. For the case when there is lower bias being applied on the bit line, such as the read operation (≈ 200 mV), the threshold LET for upset is expected to be much larger due to lower magnitude of the voltage transient generated. Thus, during erase or storage mode, when the bias on bit line is 0 V, the possibility of an upset would be highly unlikely for the same reason.

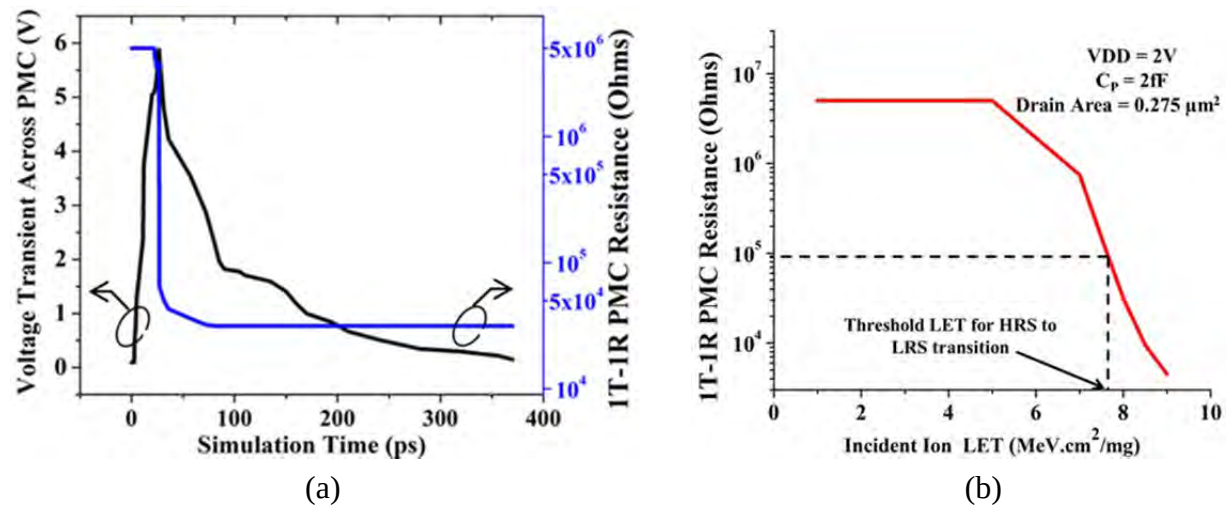


Figure 111. (a) Voltage transient generated across 1T-1R PMC and (b) results showing 1T-1R PMC resistance after ion strike

There is also the possibility of a SEU characterized by the transition of an LRS 1T-1R cell to HRS. In this case, the SEU-induced transient voltage generated at the cathode will need to be more positive than the anode voltage, thus creating a net negative voltage drop across the PMC. Figure 112(a) shows the condition where an ion strike occurs on the drain of a LRS cell, while another cell in the same row is being erased. The bit line (anode) in this case is grounded, while the select line is at V_{DD} (2V). From the equivalent circuit of the cell under consideration shown in Figure 112(b), it can be seen that only a negative voltage can be generated at the drain due to forward biasing of the drain-body junction, while the source-body junction remains reverse biased. Hence LRS to HRS transition is unlikely for such a single event.

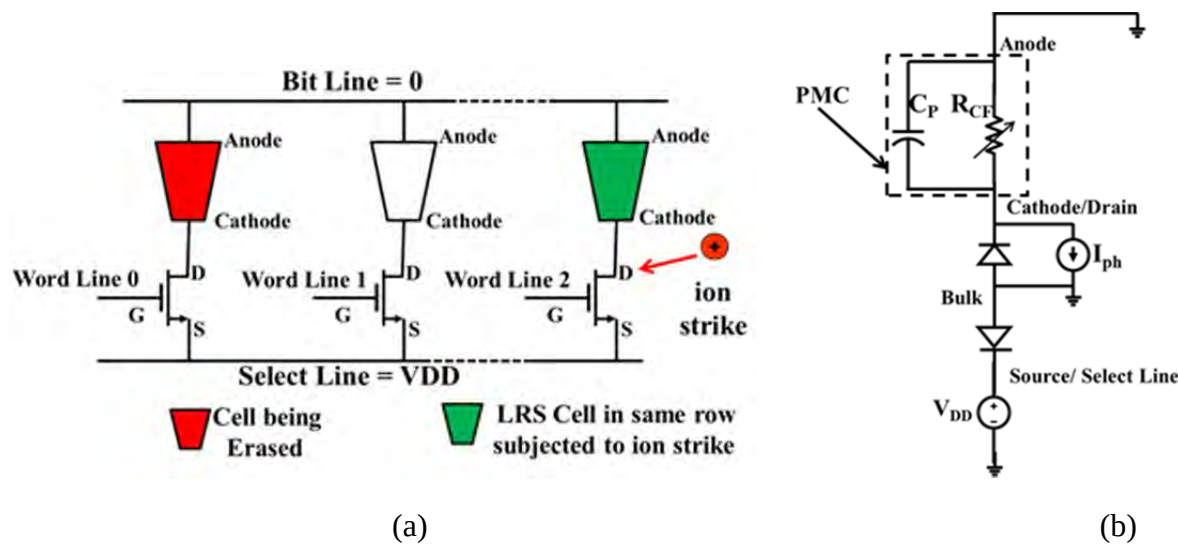


Figure 112. (a) Ion strike induced single event on a LRS element and (b) equivalent circuit for the encircled LRS cell

7.2.4.2 Experimental Results

Previously, experimental data on radiation effects on PMC devices have focused on cumulative total ionizing radiation effects. PMC memory devices have already demonstrated resistance switching endurance with adequate sense margin (ratio of HRS to LRS) for up to 105 write-erase cycles ($\approx 1.2V$ voltage pulse magnitude) over a wide range of temperatures ($0^{\circ}C$ - $100^{\circ}C$) without exposure to ionizing radiation. Results of endurance testing on irradiated devices have been reported for upto a total ionizing dose (TID) as high as 10 Mrad, while data retention without errors have been reported for PMC memory arrays for up to 447 krad which is superior to existing flash based technologies. Hence, the experimental results presented in this section solely focus on transient radiation effects on PMC devices.

Heavy ion strike experiments on 1T-1R test chip were performed at the Ion Beam Analysis of Materials (IBeAM) laboratory in the LeRoy Eyring Center for Solid State Science at Arizona State University, using a Cockroft-Walton gas-insulated high frequency 1.7 MeV tandem accelerator with a beam line and analysis chamber at room temperature ($27^{\circ}C$). The test chip consisted of a 1T-1R array of 11 1T-1R elements fabricated using methods described in Section II. After being programmed to HRS or LRS the array was subjected to a beam of a specific type of ions (H, He or O) in the accelerator. Appropriate voltage bias (discussed in more detail in section V) was applied to the array during ion beam exposure so as to investigate both HRS to LRS and LRS to HRS transitions. For this purpose a constant bias voltage of 2V was used for anode/select line. Four separate tests were performed for 1.5 MeV Hydrogen, 2 MeV Helium and Oxygen ions (2 MeV and 4 MeV) at a fluence of approximately 10^{15} ions/cm². After each test, resistances of the array elements were measured by applying a dc voltage sweep from 0 V to 25mV at the anode, a constant 1.2V at the gate and 0V at the source.

Figure 113 shows the measured mean resistance of all the pre-programmed HRS and LRS elements vs. incident ion LET measured after each exposure. It can be observed that when pre-programmed to HRS ($\approx 5 \text{ M}\Omega$), the mean resistance level of the cells decreased with increasing LET. After exposure to the highest measured LET (4 MeV Oxygen ions), one HRS programmed device resistance decreased to $59 \text{ K}\Omega$. This significant change in HRS reduces the ratio of HRS to LRS to below a factor of 10 and can hence be interpreted as an upset, as the sense amplifier may not distinguish between the two states for such a low sense margin. Another HRS programmed device resistance was observed to be $\approx 161 \text{ K}\Omega$ post exposure. While the HRS to LRS ratio for this device was still > 10 , such a change can leave it vulnerable to multiple event upsets (MEUs). The abrupt lowering of HRS of these devices at the highest LET causes the standard deviation from the mean HRS to increase drastically as can be seen in Figure 113. Based on these results, a SEU error cross section was also plotted. Similar effect has been observed in other resistive memory technologies [28]. When programmed into LRS state ($10 \text{ K}\Omega$), none of devices showed any significant deviation from pre-programmed values. Hence based on the experimental results, a threshold LET for an upset (HRS to LRS transition) can be predicted to be $\approx 8 \text{ MeV.cm}^2/\text{mg}$.

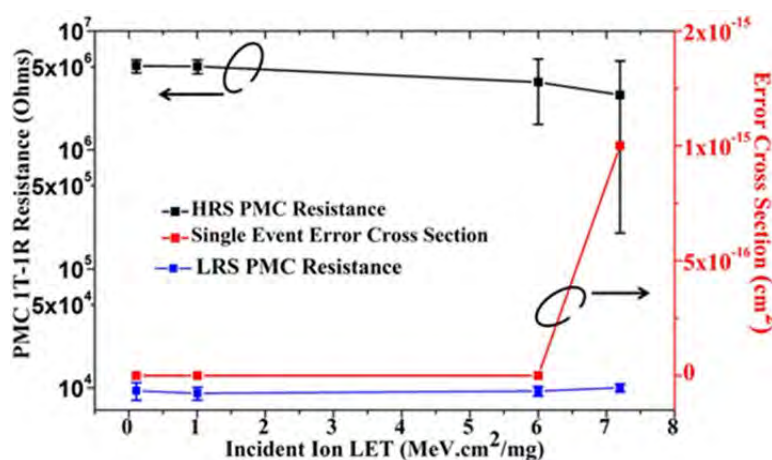
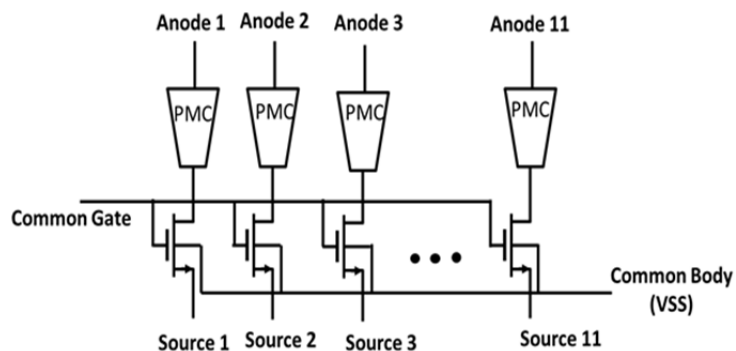
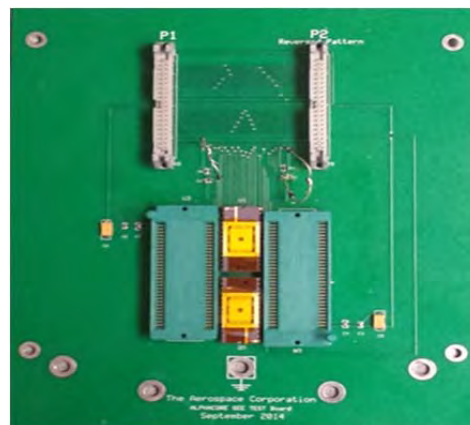


Figure 113. Experimental results showing mean resistance of 1T-1R test array elements after ion strike vs. incident ion LET

Further testing was performed at a much higher LET at the 88 inch cyclotron facility in Lawrence Berkeley National laboratories. A significantly higher incident ion LET of $58.78 \text{ MeV}/(\text{mg}/\text{cm}^2)$ (Xe ions) were used at a fluence of $109 \text{ particles}/\text{cm}^2$ ($106 \text{ particles}/\text{cm}^2/\text{s}$ flux for 1000 seconds). Of the two arrays, one array was pre-programmed to have devices in HRS and in the other array all devices were pre-programmed to be in LRS. Two sets of control devices (devices not exposed to heavy ion testing) were also programmed separately before the experiment to HRS and LRS and then measured after the test duration to verify data retention capability. Figure 114(a) shows a schematic of the 1T-1R array used for collecting data, while Figure 114(b) shows the printed circuit board that was designed to hold the packaged parts in order to apply bias during programming and also during exposure.



(a)



(b)

Figure 114. (a) 1T-1R array and (b) board designed for heavy ion testing

After exposure, all devices were measured with a DC voltage sweep upto 50 mV at the anode, with gate biased at 1.4V, to measure any change in pre-radiation resistive states of each 1T-1R PMC. Based on previous analysis, it was concluded that presence of electrical bias (similar to during write/erase operation) increases the likelihood of an upset. Hence, a bias of 2V was applied to all anodes of the HRS array during ion exposure, while all sources, gate and body were grounded. For the LRS array, all the source terminals were biased at 2V and the anodes, gate and body were grounded. These constitute the most likely respective worst case bias scenarios depending on programmed state that can lead to an upset in the stored data.

Figure 115(a) shows pre-radiation and post-radiation measurements on HRS programmed devices exposed to heavy ion testing, while Figure 115(b) shows the HRS programmed control devices. Also, LRS here is defined to be values $< 105 \Omega$. It can be seen that 4 devices pre-programmed to HRS underwent significant decrease in resistance (decrease in the range of an order of magnitude from an initial resistance of 100 K Ω or more) post-radiation (indicated by red arrows). There was no significant change in pre-programmed control array resistance levels during the same time period as can be seen from Figure 115(b).

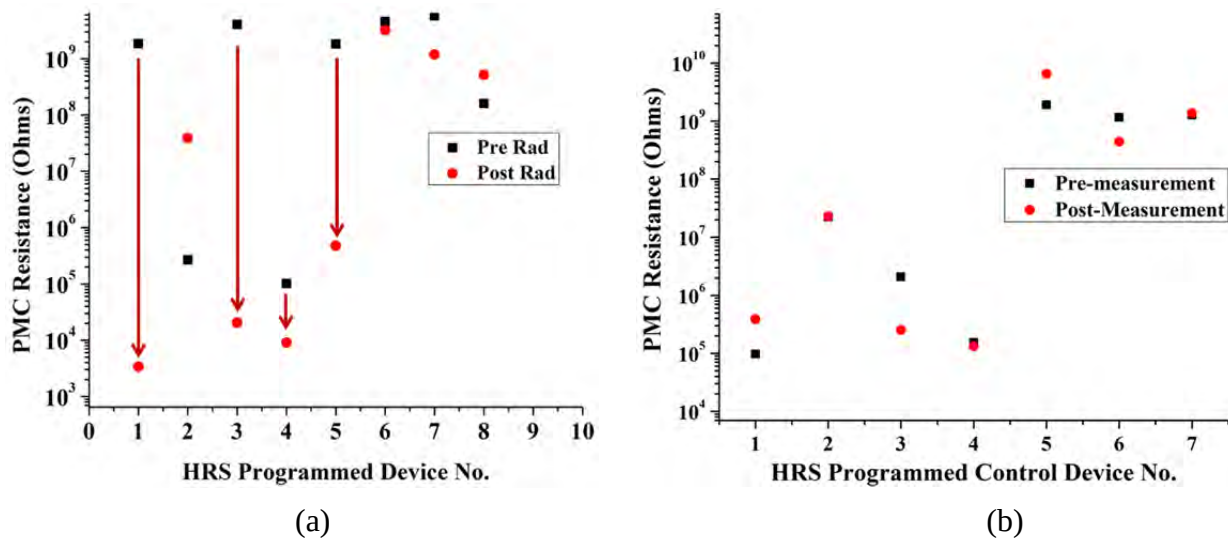


Figure 115. LBNL heavy ion test results for HRS

Figure 116 (a) shows the resistance values of the devices pre-programmed to LRS before and after ion beam exposure, while Figure 116 (b) shows the resistance values of the LRS programmed control devices measured along with the exposed devices. Contrary to what the electrical analysis and simulations predicted earlier, 2 out of the 8 LRS devices underwent an increase in resistance, thus reverting to HRS. One likely cause for this can be retention failure unrelated to ion beam exposure, although the control devices successfully retained their programmed LRS levels. Hence, further testing at different ion LETs and on a larger set of devices may be necessary for a more complete analysis.

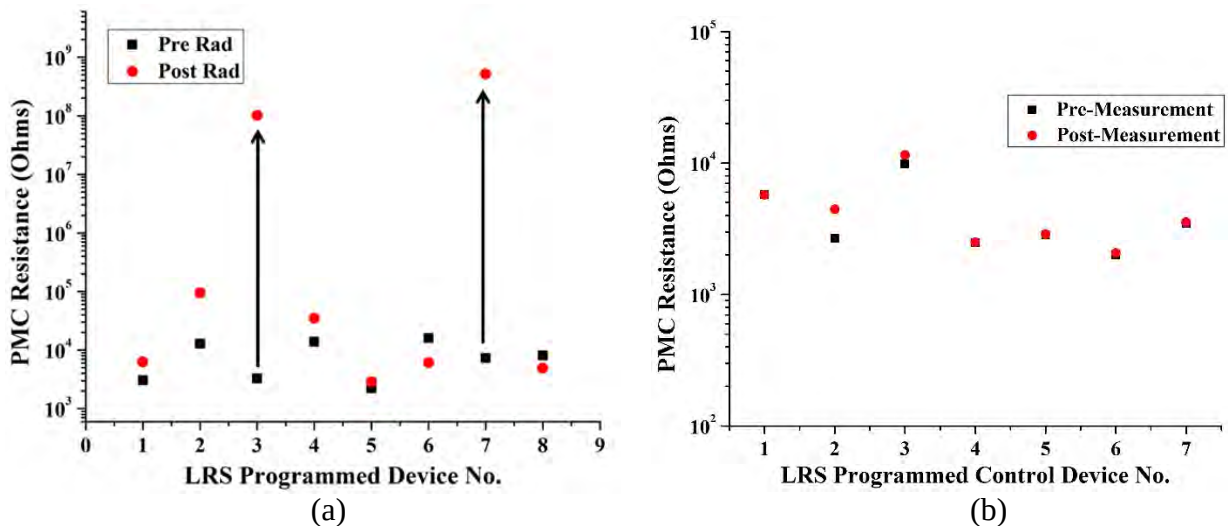


Figure 116. LBNL heavy ion test results for LRS

7.3 Conclusions

In this task, we have reported test results on Ag-ChG lateral structures with different electrode design parameters. The results show that by changing the spacing between Ag electrodes, or by modifying the total area of the Ag electrodes, it is possible to change the dynamic range of obtained resistance then to tune the detection range. In addition, the Limit of Detection can also be changed to a desired dose level by changing the spacing between nearest electrodes. This easily implemented design enable radiation sensor designers to optimize sensors for intended applications.

In addition, the effects of total dose ionizing radiation on ChG PMC devices was examined. Two different test setups were performed. In the first test setup, the devices were exposed to ^{60}Co γ -rays while the device contacts were left floating. The devices were exposed up to 3.1 Mrad(Si). In the second scenario, the devices were biased at the anode with a 50 mV read current during irradiation. The TID for the *in situ* test was 15.1 Mrad(Si). The devices used for each test were both of the same structure but from two separate fabrication batches. In both tests, the data retention was seen to be excellent with very little observed effect due to irradiation. For the 3.1 Mrad(Si) exposure, the devices left in a HRS were shown to remain in the HRS with very little deviation in resistance over time. The devices in the LRS were programmed with a 1 μA current. Both the irradiated and control devices in the LRS were shown to drift to a higher resistance within the first 24 hours of being programmed. After the increase in resistance, the devices remained at that secondary value for the duration of the exposure. During the TID exposure to 15.1 Mrad(Si), the devices were monitored in real time. The trace data presented in Chapter 4 shows that the retention state of all exposed devices remained constant until 10 Mrad(Si), when several of devices in the LRS increased from 100 Ω to 1 k Ω . The control devices were also observed to make this transition, suggesting that the change in resistance was not due to radiation. The devices in the HRS did not change state for the duration of the 15.1 Mrad(Si) exposure.

The Cu-SiO₂ PMC technology was also shown to perform favorably when exposed to high doses of radiation. This work shows that this expectation is not unreasonable as virgin, ON- and OFF-states do not show any obvious changes after Co-60 gamma-ray irradiation up to 7.1 Mrad(SiO₂). Moreover, set voltage (V_{set}) is similarly stable and programmable resistance (multilevel) switching capability and endurance are maintained after exposure.

Lastly, experimental results from biased 1T-1R heavy ion testing were presented and simulations combining both 3-D TCAD and Spectre circuit modeling were performed to analyze single event transients generated in 1T-1R CBRAM resistive memory elements under write, read and erase bias conditions. It was found that the angle of incidence can be important in determining whether such transients can cause a LRS to HRS upset during erase bias conditions. Upsets under write bias conditions was found to be much more likely than under read bias conditions. The ion LET dependence of CBRAM resistance change was simulated for different conditions. The simulations were shown to correlate well to the experimental results demonstrating the accuracy of the PMC compact model.

All radiation results reveal that in general the PMC technologies investigated during this program are highly resistant to the effects of cumulative ionizing damage and single event effects

The following list represents publications and conference presentations that were the outcome of work in this task

1. J. L. Taggart, Y. Gonzalez-Velo, D. Mahalanabis, A. Mahmud, H. J. Barnaby, M. N. Kozicki, K. E. Holbert, M. Mitkova, K. Wolf, E. Deionno, A. L. White, "Ionizing Radiation Effects on Nonvolatile Memory Properties of Programmable Metallization Cells," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 2985–2990, 2014
2. D. Mahalanabis, H. J. Barnaby, M. N. Kozicki, V. Bharadwaj, and S. Rajabi, "Investigation of Single Event Induced Soft Errors in Programmable Metallization Cell Memory," *IEEE Trans. Nucl. Sci.*, vol. 61, pp. 3557-3563, 2014.
3. J. L. Taggart, Y. Gonzalez-Velo, D. Mahalanabis, A. Mahmud, H. J. Barnaby, M. N. Kozicki, K. Holbert, M. Mitkova, K. Wolf, E. DeIonno, and I. A. L. White, "Ionizing radiation effects on non-volatile memory properties of programmable metallization cells," IEEE Nuclear and Space Radiation Effects Conf., Paris, FR., July 2014.
4. D. Mahalanabis, H. J. Barnaby, M. N. Kozicki, and S. Rajabi, "Investigation of Single Event Induced Soft Errors in 1T1R PMC Memory," IEEE Nuclear and Space Radiation Effects Conf., Paris, FR., July 2014
5. D. Mahalanabis, H. J. Barnaby, M. N. Kozicki, E. Deionno, A. Mahmud, M. Kay, "Analysis of Single Event Upset Susceptibility in CBRAM 1T-1R Memory," IEEE Nuclear and Space Radiation Effects Conf., Boston, MA., July 2015.
6. A. Mahmud, Y. Gonzalez-Velo, H. J. Barnaby, M. N. Kozicki, K. E. Holbert, M. Mitkova, T. L. Alford, M. Goryll, M. Saremi, W. Yu, D. Mahalanabis, W. Chen and J. Taggart, "Optimization of Flexible Ag-Chalcogenide Glass Sensors for Radiation Detection," accepted for the Radiation and Its Effects on Components and Systems (RADECS) Conf., Moscow, RU., September 2015.
7. J. L. Taggart, M. L. McLain, H. J. Barnaby, M. N. Kozicki, "Combined Neutron/Gamma-Ray Effects in Ag-Ge₃₀Se₇₀ Based Programmable Metallization Cells," presented at the 2014 HEART conference, 2014.

8 RECOMMENDATIONS

We recommend several actions that would improved the modeling of the technology. For the muerical simulations, a more complete model would include the ability to convert reduced species into either dopant or conduting layers. This would improve upon the existing model by supporting better simulations of filament foramation and desolution. This would also better facilates the use of TCAD models in mixed mode simulations of circuit and system applications. This added effort will require closer coordiantation will simulation tool providers like Silvaco International. Imporvemnts to the compact model would include modifications such as the addition of the Butler-Voltage charge transfer equation. Further testing and refinemnts to the foundry ready Cu_SiO2 PMC is also recommended.

Going forward, we also recommend using the model to explore more sophisticated circuit design applications in memory as well as computation. In memory, more extensive experimental data on single event effects on PMC memory arrays and estimation of soft error rate is the next step. Another interesting application is design of non-volatile low power digital applications using PMCs to store data in absence of power supply. The other potential application of these devices is in computation. Both Boolean and non-Boolean (neuromorphic) computation are research areas of interest. Boolean computation will involve threshold logic functions which form a subset of Boolean functions such as AND, OR etc. Such functions can be implemented in reconfigurable threshold logic gate design where the PMCs can act as programmable weights. This is possible due to the ability to accurately control the PMC resistance depending on the electrical bias e.g. the current allowed to flow through the device. Non-Boolean computation in the domain of neuromorphic circuits is possible, as has been shown here, due to the gradual resistance change behavior demonstrated experimentally in this work. Such a property can be useful to demonstrate important neural learning rules. An extensive neural network array comprising of CMOS neuron and PMC synapses can be designed to perform complex learning tasks e.g., image processing and pattern recognition. Lastly, we recommmned continued research to determine and demonstrate the viability of electrochemical resistive RAM (RRAM) as a viable non-volatile-memory (NVM) technology for space electronics and to optimize RRAM array architectures and peripheral circuitry for space applications. RRAM is regarded as one of the most promising candidates for non-volatile memory (NVM) applications beyond the scaling limit of FLASH. This research will support the development and transition of innovative high-payoff space technologies supporting the warfighter. The effort will also leverage commercial, civil, and other space capabilities to ensure USA's advantage. As this effort has shown, when compared to the mainstream FLASH technology, the RRAM PMC technology has much better total ionizing dose (TID) tolerance, better programming cycle endurance, faster programming speed, lower programming voltage requirements, and better scalability to sub 10 nm feature sizes, making RRAM a strong candidates for supplanting FLASH as the most widely used NVM technology. Given these advantages, the RRAM technology shows improved performance and radiation hardness as compared to FLASH technology, bringing significant benefits to the next generation of DoD space systems and industries developing robust non-volatile memory for space flight. We recommend an extensive effort whereby high density arrays of PMCs are fabricated and characterized in response to stress, radiation exposure. Such a program would

further develop and validate models, examine RRAM architectures to assess suitability for space, and design architectures using layout and radiation-hardening-by-design methodologies.

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APPENDIX: VERILOG-A CODE FOR PMC COMPACT MODEL

```
// VerilogA for trial, PMC, veriloga

`include "constants.vams"

`include "disciplines.vams"

module PMC(an,ca);

  inout an,ca;

  electrical an, ca;

  //structure parameters

  parameter real rho_f = 5.3e-4;//2.3e-6

  parameter real rho_e = 8e2;

  parameter real rcell = 1e-6;// adesto

  parameter real Rcf_bottom = 5e-9;

  parameter real Kb = 1.38e-23;

  parameter real Kb1 = 8.617e-5;

  parameter real T0 = 300;

  parameter real Isf = 1.8e-6; //filament diode rev sat current

  parameter real Ise = 1.4e-9; //electrolyte diode rev sat current

  parameter real nf = 1; //filament diode quality factor;

  parameter real ne = 2; //electrolyte diode quality factor

  //filament growth parameters

  parameter real q = 1.602e-19;

  parameter real h0 = 15e-9;

  parameter real rmin = 0.1e-9;

  parameter real vh = 0.5;

  parameter real vr = 0.1;
```

```

parameter real alpha = 15e-9;

parameter real beta = 0.52;

parameter real beta1 = 1.4;

parameter real Ea = 0.46;

parameter real L = 60e-9;

//parameter real Icomp = 500e-6;

parameter real Vwrite = 0.05;

parameter real Verase = -0.05;

parameter real zecaf = 18.826e3;

parameter real mAg2Se = 294.7;

parameter real Na = 6.022e23;

parameter real rho_Ag2Se = 8.216;

parameter real a = 240e-10;

parameter real alpha1 = 15n;

real
h,Vol,r,store,r_limit,Wa,Jhop,Jhop_on,E,dhdt,drdt,Rsf,Rse,Re,Rf,R,m,n,sgn,state,dh,th,dr,r_dummy,I_dummy,Rd,T;

analog begin@(initial_step)

begin

Vol = 0;

m = h0;

I_dummy = 0;

n = rmin;

r = rmin;

h= h0;

store =0;

r_limit =0;

```

```

dhdt = 0;

drdt=0;

state = 0;

T = T0;

end

if (V(an,ca) > Vwrite) begin

    dhdt = vh*exp(-Ea/(Kb1*T))*sinh((alpha*q*(V(an,ca)))/((L-h)*(Kb*T)));

    if (h == L) begin

        // drdt = vr*exp(-Ea/(Kb1*T))*sinh((beta*q*(V(an,ca)-delta))/(Kb*T));

        drdt = 0.5e9*r*(vr*exp(-
Ea/(Kb1*T))*sinh((beta*q*(V(an,ca)))/(Kb*T)))/(L*q*((2e6*Na*rho_Ag2Se)/(mAg2Se)));

        dr = drdt;

        store = 1;

    end

else begin

    store = 0;

    dh = dhdt;

end

end

else if (V(an,ca) < 0) begin

    // drdt = vr*exp(-Ea/(Kb1*T))*sinh((beta1*q*(V(an,ca)))/(Kb*T));

    drdt = 0.5e9*r*(vr*exp(-
Ea/(Kb1*T))*sinh((beta1*q*(V(an,ca)))/(Kb*T)))/(L*q*((2e6*Na*rho_Ag2Se)/(mAg2Se)));

    if (r > rmin) begin

        dr = drdt;

    end

end

```

```

else begin

    dr = 0;

    dhdt = vh*exp(-Ea/(Kb1*T))*sinh((alpha1*q*(V(an,ca)))/((L-h)*(Kb*T)));

    dh = dhdt;

    if (h>h0) begin

        dh = dhdt;

    end

    else begin

        store = 0;

    end

    end

    end

else

    begin

        dh = 0;

        dr = 0;

    end

    n = idt(dr,rmin);

    m = idt(dh,h0);

    Rse = ((rho_e*L)/(3.14*((rcell*rcell)- (Rcf_bottom*Rcf_bottom))));

    Rsf = rho_f*h/(3.14*r*Rcf_bottom);

    Rd = 1/((1/Rsf)+(1/Rse));

    if (store == 1) begin

        R = Rd;

    end

end

```

```

else begin

R = (rho_f*h0)/(3.14*rmin*Rcf_bottom); // off state resistance

end

if (V(an,ca) >= 0) begin

sgn = 1;

end

else begin

sgn = -1;

end

if (m >= L) begin

h=L;

end

if (L > m > h0) begin

h=m;

end

if (m <= h0)begin

h = h0;

end

//if (n >= rcell) begin

//r = rcell;

//end

if (rmin < n) begin

r = n;

end

if (n < rmin)begin

```

```

r = rmin;

n= rmin;

end

//compliance current check

//if (V(an,ca)/R >= Icomp)

//Vol = Icomp*R*sgn;

//end

//else begin

//Vol = V(an,ca);

//end

//I(an,ca) <+ Vol/R;

I(an,ca) <+ V(an,ca)/R;

end

endmodule

```

LIST OF ACRONYMS, ABBREVIATIONS, AND SYMBOLS

Acronym/ Abbreviation	Description
AFRL	Air Force Research Laboratory
BEOL	Back-End-Of-Line
BOE	Buffered Oxide Etch
CANi	Center for Applied Nanoionics
CBE	Conduction Band Edge
CBRAM	Conductive Bridge Random Access Memory
CF	Conductive Filament
CHG	Chalcogenide Glass
CMOS	Complementary Metal-Oxide-Semiconductor
CSSER	Center for Solid State Electronics Research
DFT	Density Functional Theory
DR	Dynamic Range
EDS	Energy Dispersive X-ray Scattering
GIF	Gamma Irradiation Facility
HRS	High Resistance State
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
LE-CSSS	LeRoy Eyring Center of Solid State Science
LOD	Limit of Detection
LRS	Low Resistance State
MD	Molecular Dynamics
MEM	Metal–Electrolyte–Metal
PA	Parameter Analyzer
PDOS	Projected Density of States
PMC	Programmable Metallization Cell
QFL	Quasi-Fermi Level
REDOX	Reduction/Oxidation
RRAM	Resistive Random Access Memory
SEU	Single Event Upset
SMU	Source Monitor Unit
STDP	Spike Timing Dependent Plasticity
TCAD	Technology Computer Aided Design
TID	Total Ionizing Dose
UV	Ultra-Violet
WCCML	Wireless Communication Circuits Measurement Laboratory

Symbol	Description
E_g	Bandgap (eV)
χ	Affinity (eV)
N_C	Density of States in Conduction Band (per cc)
N_V	Density of States in Valence Band (per cc)
n_i	Intrinsic Carrier Concentration (per cc)
μ_n	Electron Mobility (cm^2/Vs) ^c
μ_p	Hole Mobility (cm^2/Vs)
ϵ	Dielectric Constant
σ	Conductivity ($\Omega^{-1} \cdot \text{cm}^{-1}$)

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