DEVICE OPTIMIZATION AND PERFORMANCE OF 3.5 CM^2 SILICON SGTO FOR ARMY APPLICATIONS

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Abstract

The U.S. Army Research Laboratory (ARL) has been investigating silicon super gate turn-off thyristors (SGTOs) for high action pulse switching necessary for Army survivability and lethality applications. The silicon SGTO designed by Silicon Power Corporation (SPCO) was evaluated to determine its repeatable pulse current capability at a 1 ms pulse width. The initial SGTO design was a 3.5 cm^2 chip rated for 4 kV forward blocking and 10 kA peak current at 10 µs pulse width or 100 A continuous. The previous work by ARL on these switches reported repetitive peak current of 5 kA with a charge voltage of 4 kV. Additionally, the switches failed short at peak currents of 6 kA, with calculated action of 1.3 x 10^4 A^2 s at 5 kA. This work highlights the device optimization that SPCO has since made on the Si SGTO to improve the device pulsing performance. The latest Si SGTO evaluated maintains the same chip area and active area as the previous devices. Modification to the mask layout and the enhancement of the emitter design enables the latest Si SGTO to exhibit repeatable peak current of 5.5 kA (a 10% increase compared to the previous batch). The calculated action for the latest switches was 1.6 x 10^4 A^{2}s at 5.5 kA.

I. INTRODUCTION

Future Army pulsed power applications will require improved device technologies that can provide higher power density, better efficiency, and increased reliability.

The objective of this work is to evaluate Si SGTOs for these high action applications.

When High pot tested, most of the Si SGTOs exhibited hold off voltage beyond 4 kV. The majority of the Si SGTOs blocked 7 kV while displaying a leakage current of 100 µA. The active (cathode mesa) area of the device was 2.0 cm^2. The minimum recommended gate pulse required to turn on the device ranges from .5 A to 1 A. Rapid turn-on and even current distribution across the device area was achieved because of the cell based emitter design and the integrated gate and cathode fingers [1-2]. The entire Si SGTO die used in this work was packaged by SPCO. SPCO used a ThinPak^{TM} lid and high voltage potting compound to package the SGTOs. The ThinPak^{TM} lid eliminates wire bonds and reduces parasitics such as stray inductance and bond resistance. ThinPak lidded devices can increase device reliability and performance by reducing mechanical and electrical stresses in the die. A ThinPak package as illustrated in Fig. 1 is a solder assembly of semiconductor power devices (in this particular case Si SGTOs) that consists of metalized lids on both the bottom and top side that mates to the semiconductor power device electrode through metalized vias. Fig. 2 displays a picture of the 3.5 cm^2 Si SGTO chip. More information on ThinPak packages may be found in the following reference [3]. The 3.5 cm^2 Si SGTOs are intended to be combined in modules for higher current switching and SPCO plans on fabricating larger Si SGTO chips in the near future.

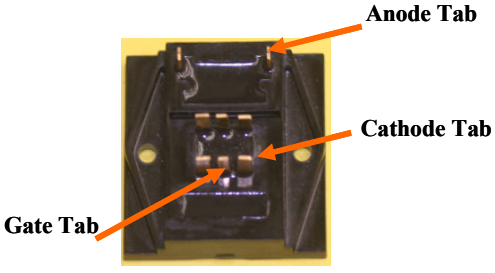

Figure 1. ThinPak package of Si SGTO

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14. ABSTRACT
The U.S. Army Research Laboratory (ARL) has been investigating silicon super gate turn-off thyristors (SGTOs) for high action pulse switching necessary for Army survivability and lethality applications. The silicon SGTO designed by Silicon Power Corporation (SPCO) was evaluated to determine its repeatable pulse current capability at a 1 ms pulse width. The initial SGTO design was a 3.5 cm2 chip rated for 4 kV forward blocking and 10 kA peak current at 10 ìs pulse width or 100 A continuous. The previous work by ARL on these switches reported repetitive peak current of 5 kA with a charge voltage of 4 kV. Additionally, the switches failed short at peak currents of 6 kA, with calculated action of 1.3 x 104 A2 s at 5 kA. This work highlights the device optimization that SPCO has since made on the Si SGTO to improve the device pulsing performance. The latest Si SGTO evaluated maintains the same chip area and active area as the previous devices. Modification to the mask layout and the enhancement of the emitter design enables the latest Si SGTO to exhibit repeatable peak current of 5.5 kA (a 10% increase compared to the previous batch). The calculated action for the latest switches was 1.6 x 104 A2s at 5.5 kA.

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Figure 2. Photo of 3.5 cm^2 Si SGTOs. The anode contact is on the bottom side, and the gate and cathode contacts is on the top side.

II. EMITTER STRUCTURE AND PROCESS

The original SGTO cell structure consisted of long narrow emitters and gates that encompassed the entire device active area. The early design as illustrated in Fig. 3 displayed undesirable turn-off performance.

It was believed that certain sections of the emitter were turning off at an unequal rate. Furthermore, it was hypothesized that the emitter sections with delayed turn-off carried current to other active portions of the emitter. This particular phenomenon led to the creation of current filamentation which resulted into the thermal failure of the Si SGTOs [4].

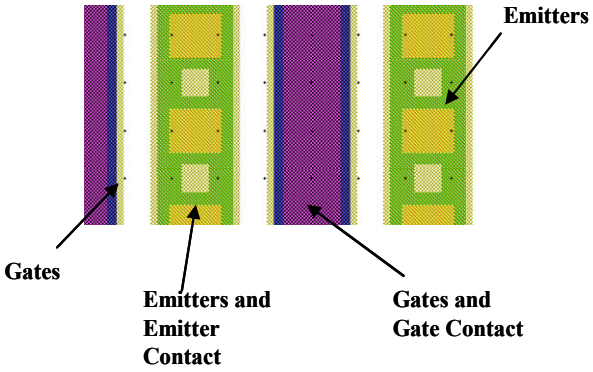

Figure 3. Si SGTO original cell structure. Purple: gates and gate contact; blue: gate; yellow: emitters and emitter contact; green: emitters; [4]

To further prevent current filamentation, a new Si SGTO cell design approach was developed. The SGTO emitter design was divided into many large disconnected squares as illustrated in Fig. 4. The intent was changed enabling the device active area to be divided into many large rectangles making it difficult for current crowding to occur in the active area.

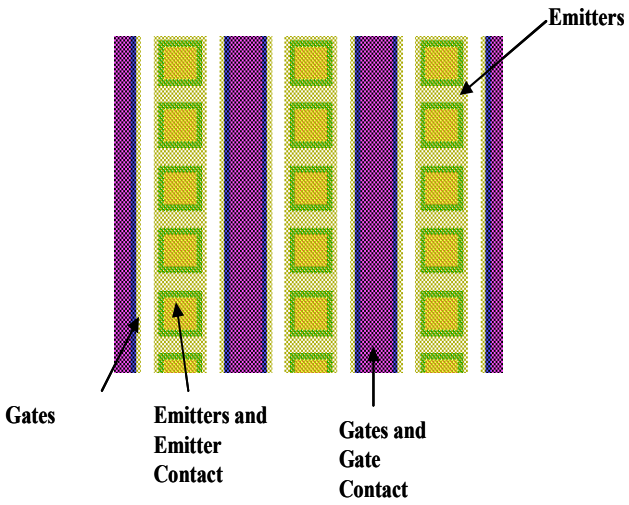

Figure 4. Si SGTO emitter square design [4]

Current crowding in the emitter generates higher on-resistance, which leads to higher forward voltage drop when the SGTO is in the on-state. Furthermore, current crowding also leads to anisotropic heat generation.

The anisotropic heat generated could impact the silicon and the contacts if it is not distributed evenly across the active area or removed through an external heat sink. Devices tend to experience thermal failure due to anisotropic heat. It is known that anisotropic steady state current distributions reduce the turn-off capability of the device due to the long removal of excess charge which leads to high current density regions in the active area of the device [4]. The division of emitter cells into rectangular groups was intended to reduce current filamentation during turn-off; however, there are some drawbacks using the topology. It has been noted from SPCO studies that dividing emitters into rectangular groups promotes anisotropic current distribution, leading to an increase in the forward voltage drop of the SGTO in the on-state. Furthermore, the heat generated from the anisotropic current distribution leads to difficulty in the turn-off capability of the SGTO [4].

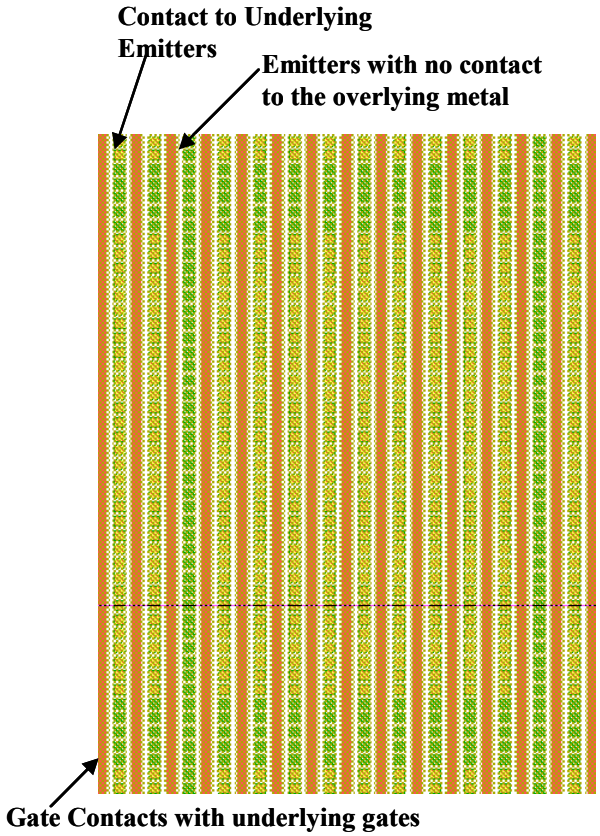

Figure 5. Si SGTO modified emitter cell design [4]

To further minimize the current filamentation, another modification was made to the SGTO emitter cell as displayed in Fig. 5. The emitter area was divided into numerous rectangles with the intent of preventing current from jumping between the emitter squares. Despite the intricate change made to the emitter cell structure, there was no real significant change in the turn-off performance of the SGTOs. It was decided to revert back to the emitter cell design displayed in Fig. 2 due to the inadequate change in the turn-off performance. After further investigation, it was realized that the actual depth and charge of the emitter plays a vital role in decreasing the forward voltage of the SGTO in the on-state. The study done at SPCO concluded that the enhanced emitter processing is quite essential in optimizing the forward voltage drop as opposed to the emitter mask design that increases the emitter area [4].

III. DEVICE EVALUATION

In order to evaluate the wide-pulsed performance of Si SGTOs, a capacitor discharge circuit was used. A PSPICE simulation was used to determine the appropriate values of the passive components required to design the test circuit to produce a half-sine current waveform that was 1 ms across the base and peaked within 4 to 6 kA at charging voltages ranging from 4 to 5 kV. The charging voltage of the wide pulsed circuit was determined by the low-end voltage hold-off potential of the SGTO. The diagram of the test circuit is displayed in Fig. 6. A picture of the wide test bed used to evaluate the Si SGTO can be seen in Fig. 7.

The circuit inductance was approximately 180 µH. A charging resistor of 4.7 kΩ was used to charge up a 525 µF capacitor bank to the desired voltage. The Si SGTO was utilized as a closing switch to discharge the capacitor into a resistive load. A total load resistance of 0.2Ω was used to conduct the experiment. In the high energy test beds, a power diode is connected in anti-parallel with the circuit inductor in order to clamp negative current that would cause the switch to fail short. The series diode acts as a safety mechanism to the voltage source in case the evaluation switch fails. Moreover, the series diode blocks any reverse voltage generated from the inductor that the SGTO cannot hold off. Without these diodes, the switch would arbitrarily turn-on several times. This particular characteristic is truly undesirable in any pulse power system.

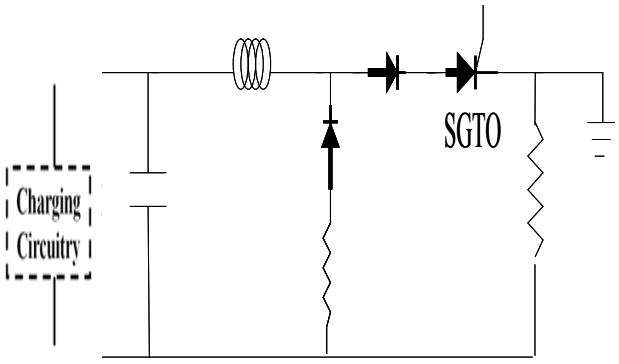

Figure 6. Wide-pulse circuit topology

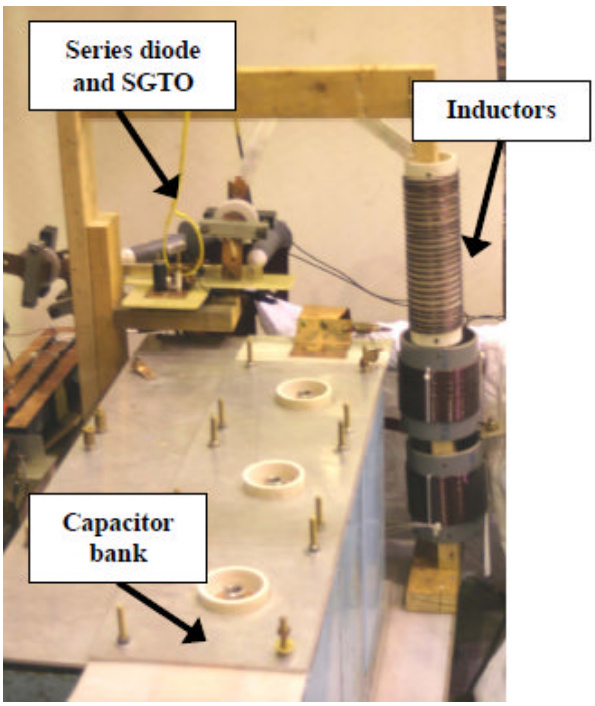

Figure 7. Photo of Wide Pulsed Test Bed

IV. RESULTS AND DISCUSSION

The previous lots of SGTOs had standard (shallow) emitters and displayed an unusual increase in forward voltage drop at certain peak currents levels. The standard emitter SGTOs were pulsed at incremental charge voltages to asses the reproducible peak current suitable for switching the device at a pulse width of 1 ms. ARL reported that the reliable repeatable peak current of operation for the standard emitter SGTO was 5 kA with a pulse width of 1 ms [5]. It can also be noted that the peak current failure for these devices was over 6 kA.

With the previous lots of SGTOs, once 5 kA was exceeded, a slight increase in the forward voltage drop would appear well over halfway through the current pulse. If the device was repeatedly pulsed at peak current levels above 5 kA, it would fail short across the anode-to-cathode after a several shots. It is believed that the forward voltage increase at the higher current levels is attributed to localized heating around the active area of the devices due to non-uniformity of the current distribution.

Furthermore, the point at which the voltage drop increases suggests that it maybe due to current crowding, which leads to the build-up of heat over the course of the 1 ms current pulse. As stated earlier, current crowding in the emitter generates higher on-resistance which leads to higher forward voltage drops. It may also be noted that the heating may have affected the resistance of the solder joints within the package and it could have also impacted certain segments of the silicon, possibly affecting the voltage drop [4]. A repeatable 5 kA current pulse of the previous SGTO tested is shown in Fig 8, followed by a single shot with a peak current of 5.8 kA in Fig. 9. Note that there is a slight increase in the forward voltage drop near the point when the switch is starting to turn-off.

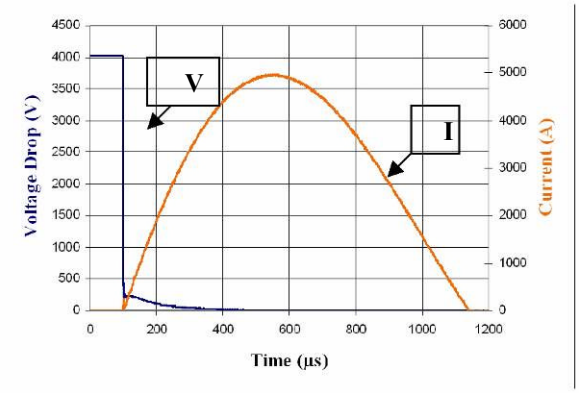

Figure 8. Voltage and current waveforms of previous SGTO evaluated at 1 ms pulse width with a peak current of 5 kA [5].

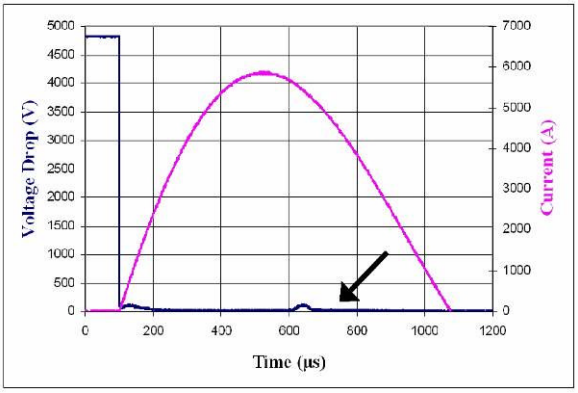

Figure 9. Voltage and current waveforms of previous SGTO evaluated at 1 ms pulse width. Note slight increase in forward voltage drop at a peak current of 5.8 kA [5].

The optimized Si SGTO evaluated maintains the same chip area and active area as the previous devices. Modification to the mask design and processing changes which permitted the emitter to be deeper, heavily doped, and contain more charge enables the latest Si SGTO to exhibit repeatable peak current of 5.5 kA (a 10% increase compared to the previous batch) when pulsed several times as displayed in Fig. 10. The initial voltage drop of the switch was 12 V at 5.5 kA. After 1000 shots, the voltage drop of the switch increased to 13 V. The repetition rate for switching the Si SGTO was one shot every 15 seconds. Furthermore, these devices can handle single-shot currents up to 5.8 kA without failure as shown in Fig. 11. The calculated action for the latest switches was 1.6 x 10^4 A^2s at 5.5 kA.

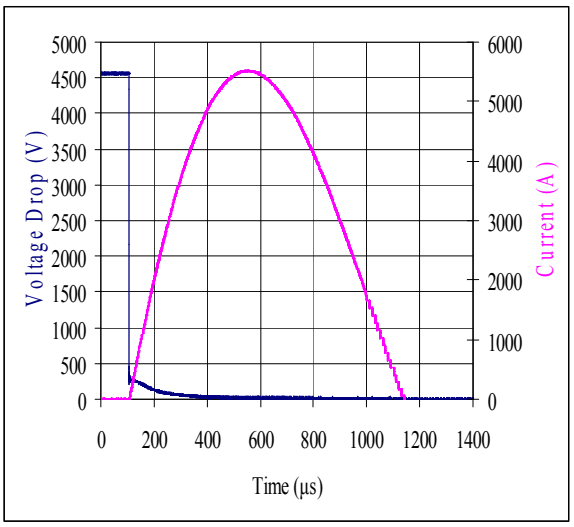

Figure 10. Voltage and current waveforms of enhanced emitter SGTO evaluated at 1 ms pulse width with a peak current of 5.5 kA .

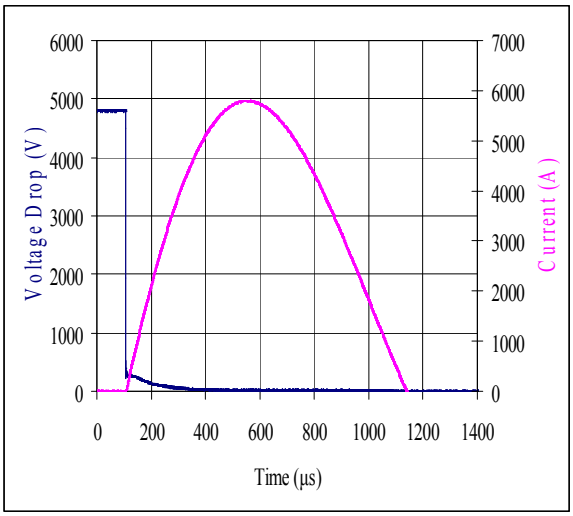

Figure 11. Voltage and current waveforms of enhanced emitter SGTO evaluated at 1 ms pulse width. Note there is no slight increase in forward voltage drop at a peak current of 5.8 kA.

Additionally, a study was conducted on the effects of varying gate current on the device forward voltage drop at 1 ms. It can be noted that the gate amplitude and width did not affect the Si SGTO voltage forward drop at 1 ms pulse width. For a 5.5 kA pulse, gate current amplitude was varied from 5 A to 17 A and gate pulse widths that varied 200 µs to 900 µs. Very little change was seen in forward voltage drop for the various gate currents pulses amplitudes and widths applied as shown in Fig. 12. Also, at a higher pulse current of 5.8 kA there was a notable bump (> 16 V) in the anode voltage waveform after several shots as shown in Fig. 13.

It was decided to reduce the peak current level in concern that the device maybe on the verge of thermal runaway. Therefore, it was concluded that the safe, repeatable peak current operation for the enhanced emitter SGTO device was 5.5 kA at 1 ms. The gate current pulse was varied once more to 20 A with a pulse width 900 µs, however, the gate pulse amplitude and width did not improve the conductivity of the device when operating at the wider pulses.

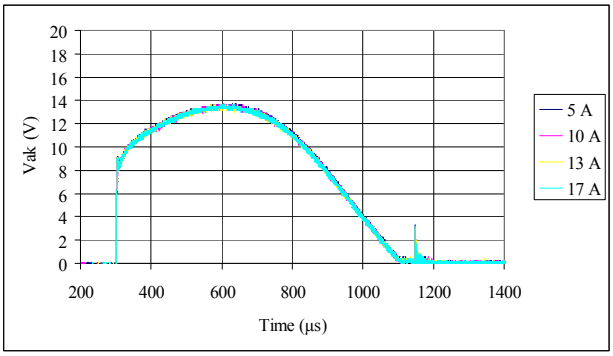

Figure 12. Varying gate current vs. Forward voltage drop @ 1 ms current pulse width.

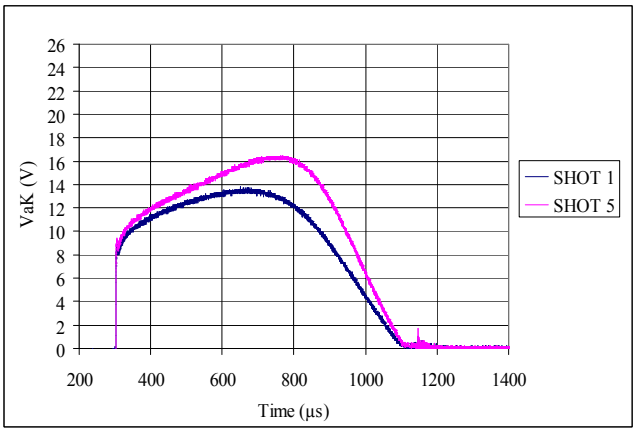

Figure 13. Voltage drop @ 5.8 kA after several shots. Note that the voltage increased from 14 V to greater than 16 V after the fifth shot.

V. SUMMARY

A description of the various SGTO emitter cell design development by SPCO was presented. Silicon Super - GTOs were switched at wide currents pulses suitable for high action applications for the army. It was realized by the studies done by SPCO that an enhance emitter and modified processing procedure would solve the forward voltage drop that occurred in the previous lot of SGTO devices. The latest Si SGTO exhibited repeatable peak current of 5.5 kA (a 10% increase compared to the previous batch). The calculated action for the latest switches was 1.6 x 10^4 A^2s at 5.5 kA with a current density of 2.8 kA/cm^2. Furthermore, it was discovered at the wider pulses that gate current magnitude and pulse width does not improve the conductivity of the device.

VI. REFERENCES

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