A 10-MHz HIGH-VOLTAGE MODULATOR WITH PULSE-WIDTH AND REPETITION-RATE AGILITY

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Requirements for control and rapid switching of the proton beam at the Los Alamos Meson Physics Facility (LAMPF) are continually revised to support accelerator upgrades and modifications. A recent upgrade required the development of a 10-MHz high-voltage modulator for an electrostatic kicker with real-time control of pulse width and repetition rate over a range of four decades. The modulator must be capable of producing a voltage pulse across a capacitive load with a rise time of $\lesssim$20 ns (10%-90%). In addition the falling edge undershoot must be controlled to less than one part in 10^3. The following paper describes in detail the circuit design philosophy, layout, and critical areas in system design.

INTRODUCTION

The ion source for the 800-MeV proton beam at LAMPF is subject to a turn-on overshoot as shown in Fig. 1b. If this portion of the beam is removed with a deflector it must be done quickly to minimize beam contact time with system components not capable of dissipating high power in a vacuum. However, this action produces an abrupt step in beam current to the rf cavities of the linear accelerator. To eliminate these problems and provide a fast-protect function (the process of truncating beam current to prevent damage to accelerator components), the deflector/modulator was developed. Referring to Fig. 1c, at t_0 the deflector is pulsed high. This puts the beam into a beam stop for the period t_0 to t_2 while the ion source current stabilizes. During the period t_2 to t_3 the beam is allowed into the linear accelerator in small pulses of increasing duration, see Fig. 1c. This produces the average beam current as shown in Fig. 1d thus providing stable operation and minimizing power surges in the rf cavities.

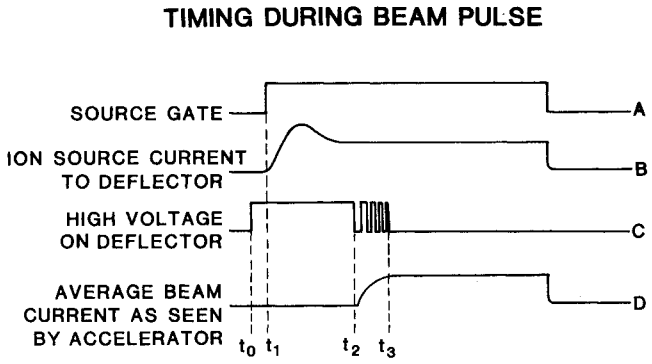

Fig. 1a-d

Timing During Beam Pulse

CIRCUIT DESIGN PHILOSOPHY AND OPERATION

The original design criteria for the high-voltage modulator are shown in Table 1. Given these criteria the circuit of Fig. 2 was selected as the most viable approach. This circuit allows all parameters in the design criteria to be met and minimizes power consumption by limiting the maximum power to the interval of rise and fall times. Therefore the average output-power is

$$W_{ave} = CV\left(\frac{N}{S}\right) \qquad (1)$$

where $\frac{N}{S} = \frac{\text{number of cycles}}{\text{second}}$ and

C and V are fixed system parameters. Therefore N/S must be constrained to the safe operating limits of the switch tube. As previously stated the beam switching must be done quickly, requiring a system slew rate for the rise and fall time of approximately 300v/ns. This high dV/dt precludes the use of active feedback to stabilize the system parameters during beam time.

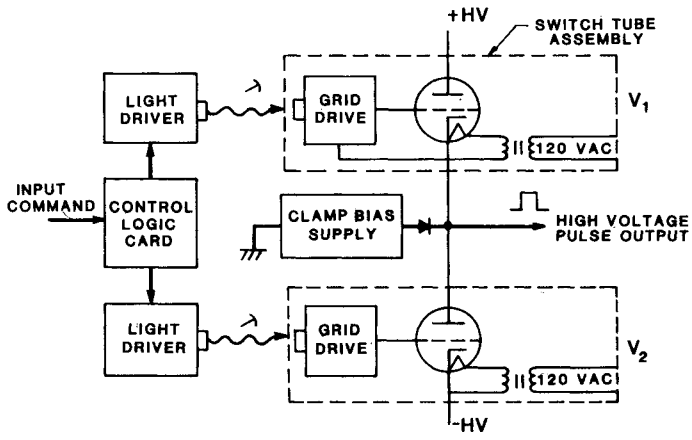

Fig. 2

Modulator Block Diagram

Therefore the system relies on a fixed load and circuit stability to reach its performance goals.

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Once the beam has been switched into the beam stop its exact position is unimportant. This results in the relaxed overshoot and droop specifications as shown in Table 1. The settling time, however, is quite different. Figure 1c and 1d show that the beam is switched into the accelerator when the voltage on the deflector is at ground. Any change from a near-ground potential will cause unwanted beam steering. Therefore the high-voltage off or ground state and the settling time are critical specifications. To meet these criteria, system geometry was optimized for minimum loop inductance; the system damping was increased until constrained by rise- and fall-time limits; and the high-voltage-power diode for the clamp circuit was selected on the basis of very high speed. This last item is a continuing problem area. To date there are no very high-speed (< 5 ns) high-voltage power diodes available with recovery times < 100 ns. This results in a settling time of 0.1% in 150 ns instead of a preferred settling time of 0.1% in < 50 ns.

In the simplest scenario circuit operation is as follows. An input command is applied to the input port of the control logic card (see Fig. 2) and this causes the grids of the two switch tubes to be driven as shown in Fig. 3. At t_0 the grid of V_1 is driven from near cutoff into a heavily conducting state for the period t_0 to t_1. The width of this pulse is set by the circuitry at ground level. Furthermore, pulse width must be set consistent with the preceding constraints on power disipation. The switch response is to produce a large current pulse with an approximate magnitude given by

$$I_{pk} = (C_L + C_S) \frac{dv}{dt} \qquad (2)$$

where $C_L = C_{Load}$ and $C_S = C_{Stray}$

For this system configuration and layout the peak current is approximately 100 A. In the interval t_1 to t_2 the grid drive of V_1 is reduced such that the anode current is in equilibrium with system losses. At t_2, V_1 switches back to a state near cutoff. V_2 operates inversely to V_1. At t_0, V_2 switches from a conducting state designed to hold the output near ground into a state near cutoff. At t_2, V_2 switches into a heavily conducting state for the period t_2 to t_3. At t_3, V_2 grid drive is reduced such that the anode current is in the original conducting state in order to hold the output near ground. The output waveform of the modulator is an exact copy of the input command with respect to pulse width and repetition rate. However, the output is displaced in time by system propagation delay. This delay is approximately 150 ns.

CRITICAL AREAS IN SYSTEM DESIGN

In order to understand some of the more critical points in system design it is necessary to look at switch tube limitations, the grid input of a planar triode as a load, and the circuit layout.

The Eimac (YU114) switch tube was selected as the closest match to system requirements and device capabilities. Table 2 shows some of the maximum ratings of the device. Note that instantaneous peak grid-cathode voltage and pulse cathode current parameters may be exceeded if the duration is short. For example for current pulses of 50 ns or less testing has shown that peak currents in excess of 35 A are consistent with acceptable tube life. Figure 4 shows the dynamic impedance of the grid for the YU114 switch tube for positive grid drive through the anode voltage range of 5 kV to 15 kV. It is apparent that for the portion of the grid drive that is above 0 V the source impedance of the grid driver must be $\leq$ 20Ω; however, for the condition when the grid drive is $\leq$ 0 V the driver need only drive the grid-to-cathode capacitance of the switch tube and the stray capacitances of the grid driver. In addition to driver impedance the maximum output voltage swing of the grid driver is a

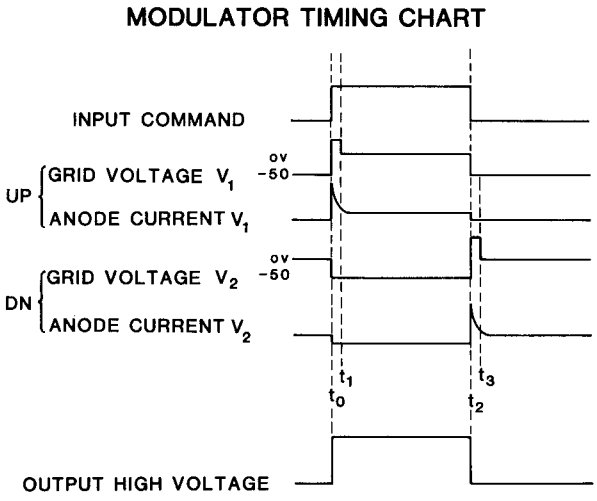

Fig. 3

Modulator Timing Chart

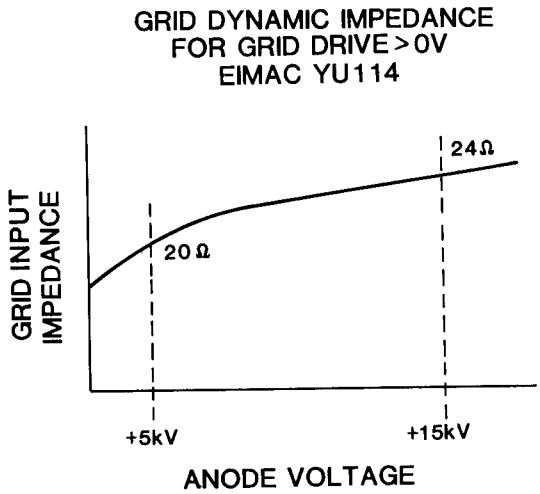

Fig. 4

Grid Dynamic Impedance

key element in grid-driver circuit design. Recalling that the peak output current of the modulator is ≈100 A, as given by Eq. (1), and assuming four YU114's in parallel this implies I_{peak}/tube ≅25 A. From Fig. 5 and the required grid drive wave forms shown in Fig. 3, we see that the grid driver must be capable of a grid voltage-swing of at least +175 V to -50 V.

With +175 V on the grid and about 8 A of grid current the peak power to the grid is 1400 W. Folding in the net duty cycle from Table 1, the average dissipation of the grid is about 0.7 W, well below the 2 W design maximum of the YU114. The circuit shown in Figs. 6 and 7 was designed based on the preceding discussion and the required system performance. Figures 6 and 7 show the schematic diagram of the grid driver, which is divided into two separate pulse generators, the positive grid drive and the control bias drive. Both positive grid drive and the control bias driver float (or are hot decked) with respect to each other and they track the cathode of the switch tube they drive. Their respective outputs are superimposed on the grid of the switch tube, in time such that the resultants are the wave forms in Fig. 3. Both pulse generators and their associated circuitry take their primary power from the filament supplies, see Figure 2. Figure 8 shows the power supply arrangement for these two cards. By using this approach only two simple isolation transformers are required to support the two switch-tube assemblies as shown in Fig. 1. With the exception of two sets of two jumpers on the control-bias driver the two assemblies are identical.

As shown in Figs. 6 and 7 the switch-tube assemblies are controlled by fiber-optic links. The timing and light driver levels must be set with care so that the timing and wave forms of Fig. 3 are preserved. This allows the output high-voltage pulse width and repetition rates to be varied through the full design range of the modulator while maintaining high-voltage isolation between the switch-tube assemblies and the ground-level control system.

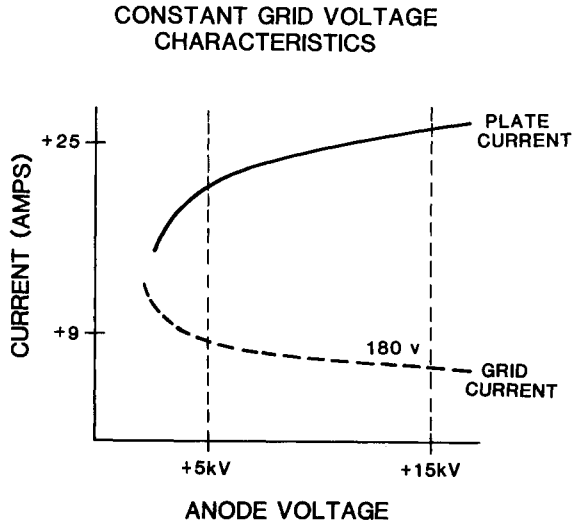

Fig. 5

Constant Grid Voltage Characteristics

The overall system layout is shown in Fig. 9. Because the load is in essence a capacitor the layout was optimized for minimum stray capacitance. The result of this approach is a system stray capacitance of about 125 pF for the modulator.

The switch-tube assemblies are clearly visible in Fig. 9, just off center. They are approximately 15 cm by 70 cm. Table 3 shows their input power requirements and their switching capability. Because of the wide range of operation, these switch-tube assemblies have proven to be easily adaptable to a variety of applications.

CONCLUSION

Since the completion of the design and testing phase of the switch-tube assemblies for the deflector modulator these assemblies and the system design philosophy outlined in the preceding article have become central elements in several systems at LAMPF. They have proven themselves to be both versatile and reliable. Furthermore, the maximum voltage range of these assemblies could be expanded from the present limit near 25kV to more than 100kV, thus extending their range of application greatly.

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TABLE I

DEFLECTOR/MODULATOR SPECIFICATIONS

Deflector (Load)

$C_{Load} \simeq 80$ pF

$R_{Load} \simeq 1$ MΩ

H.V. Modulator Output

Pulse Height $\geq$ 10kV

Pulse Width 80 ns to > 8 ms

Rise and Fall time ≃ 20 ns

Pulse Recurrence Time 100 ns to > 8 ms

H.V. Overshoot and Droop < 20%

H.V. Off, Ground ±10 V

Settling Time 0.1% in 150 ns

Grid Current Duty Cycle 0.0025

TABLE II

ABSOLUTE MAXIMUM RATINGS FOR THE YU114

DC Plate Voltage	25 kV
Peak Plate Voltage	30 kV
DC Grid Voltage	-150 V
Grid negative to cathode	-500 V
Grid positive to cathode*	100 V
Pulse Cathode Current**	12 A
DC Plate Current	150 MA
DC Grid Current	45 MA
Average Plate Dissipation	400 W
Grid Dissipation	2 W
Pulse Duration	6.0 μs
Cut-off mu	400
Duty	0.0033

*>35 A for pulse width ≤50 ns

**>500 V for pulse width ≤50 ns

TABLE III

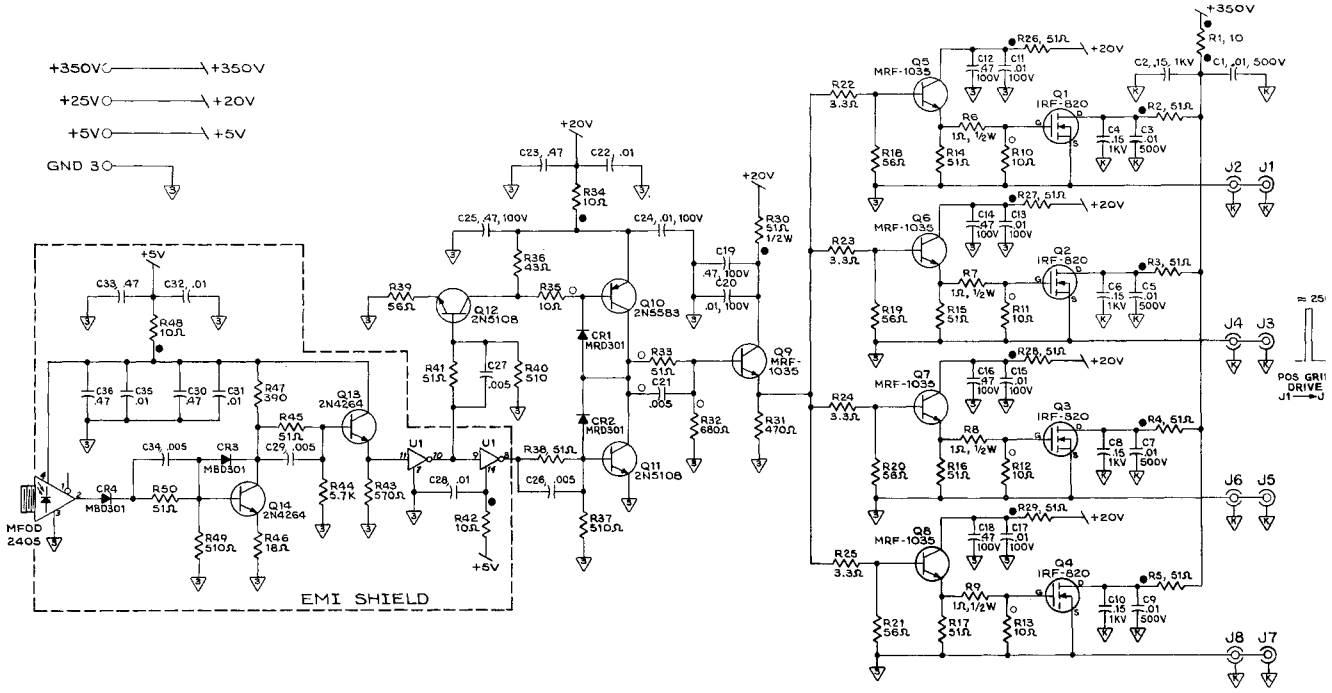
SWITCH-TUBE ASSEMBLY SPECIFICATIONS

Primary Power

6.0 VAC @ 5.7A = 34.2 W

Switching Specifications

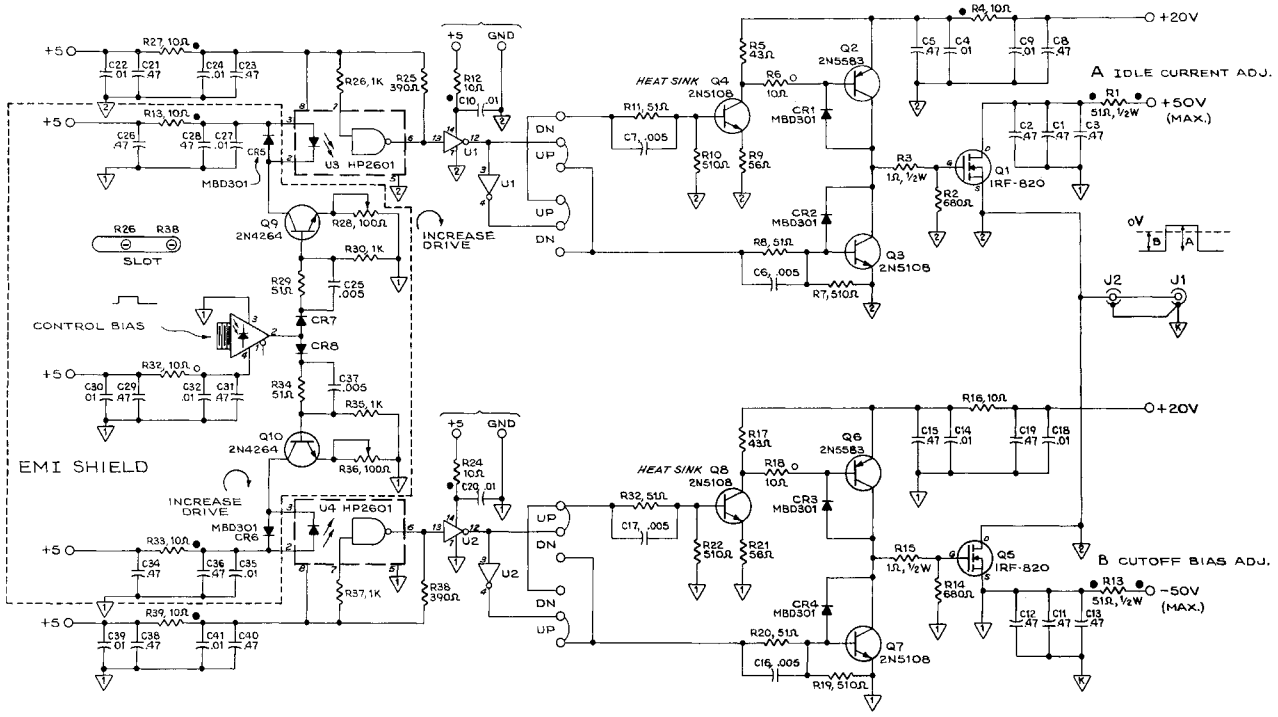
Pulse Height 25 kV max
Pulse Current 70 A max
Rise Time ≤ 20 ns
Pulse Width 80 ns to > 8 ms
Pulse Recurrence Time 100 ns to > 8 ms
Pea k Output Power > 800 kW
Average Output Power ≅ 1 kW



NOTES:

1. ALL RESISTORS ARE 1/4W UNLESS NOTED OTHERWISE.
2. ○ = FERRITE BEAD N=250
   ● = FERRITE BEAD N=900
3. U1 = FAIRCHILD 74F04PC

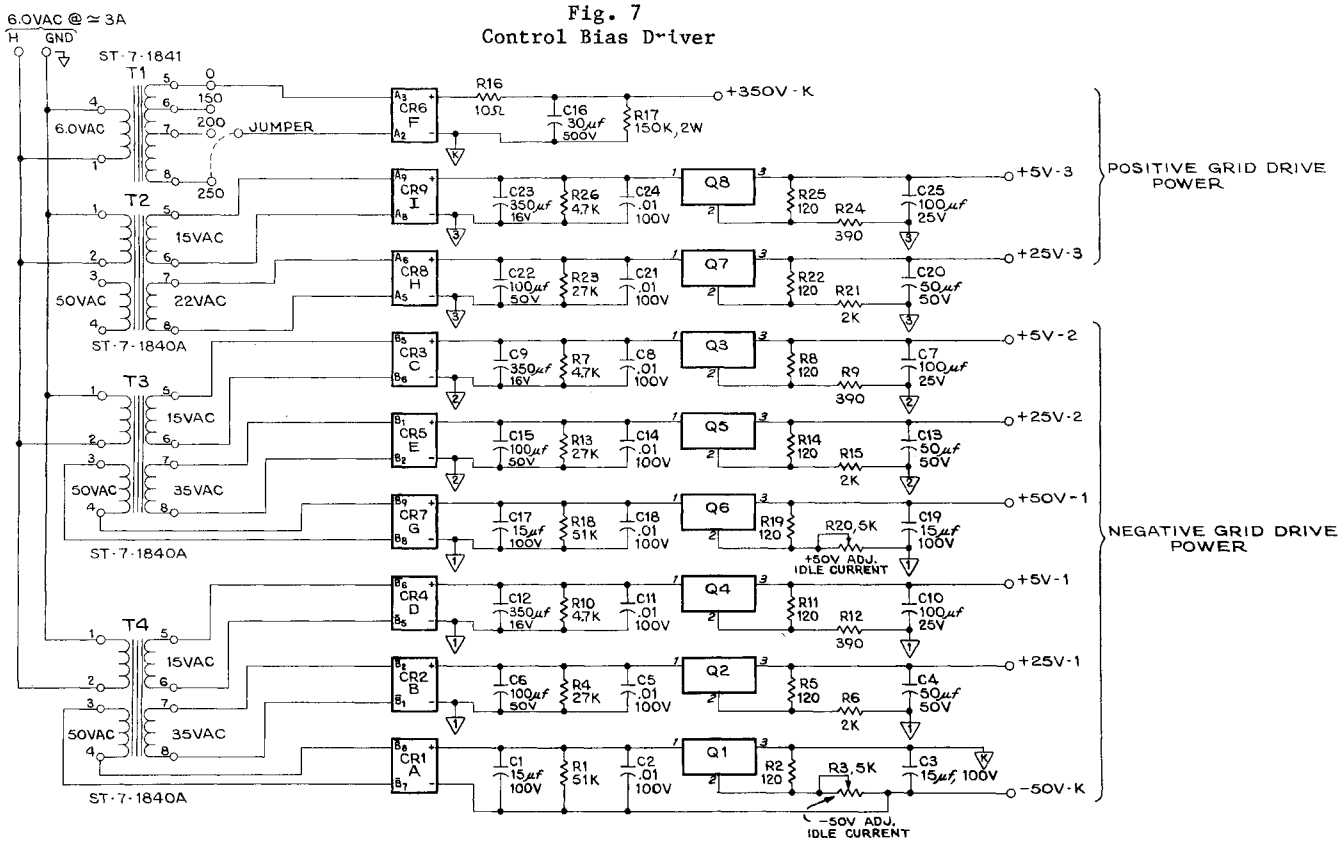
Fig. 6
Positive Grid Driver



NOTES:

1. FERRITE BEAD ● = μ = 900, ○ = μ = 250
2. Q1 & Q5 USE AAVID ENG. INC. #5772B SINK.
   Q4 & Q8 USE THERMALLOY #2209-4A SINK. *(AND KAPTON WASHER)*

Fig. 7
Control Bias Driver



NOTES:

1. CR1 THRU CR8 ARE MDA 920A6, CR9 IS 920A7.
2. Q1 THRU Q8 ARE LM317 HVH.
3. T1 THRU T4 ARE SPLIT/TRAN. TYPE MANF. BY SIGNAL TRANSFORMER.

Fig. 8
Grid Drive Power Supply

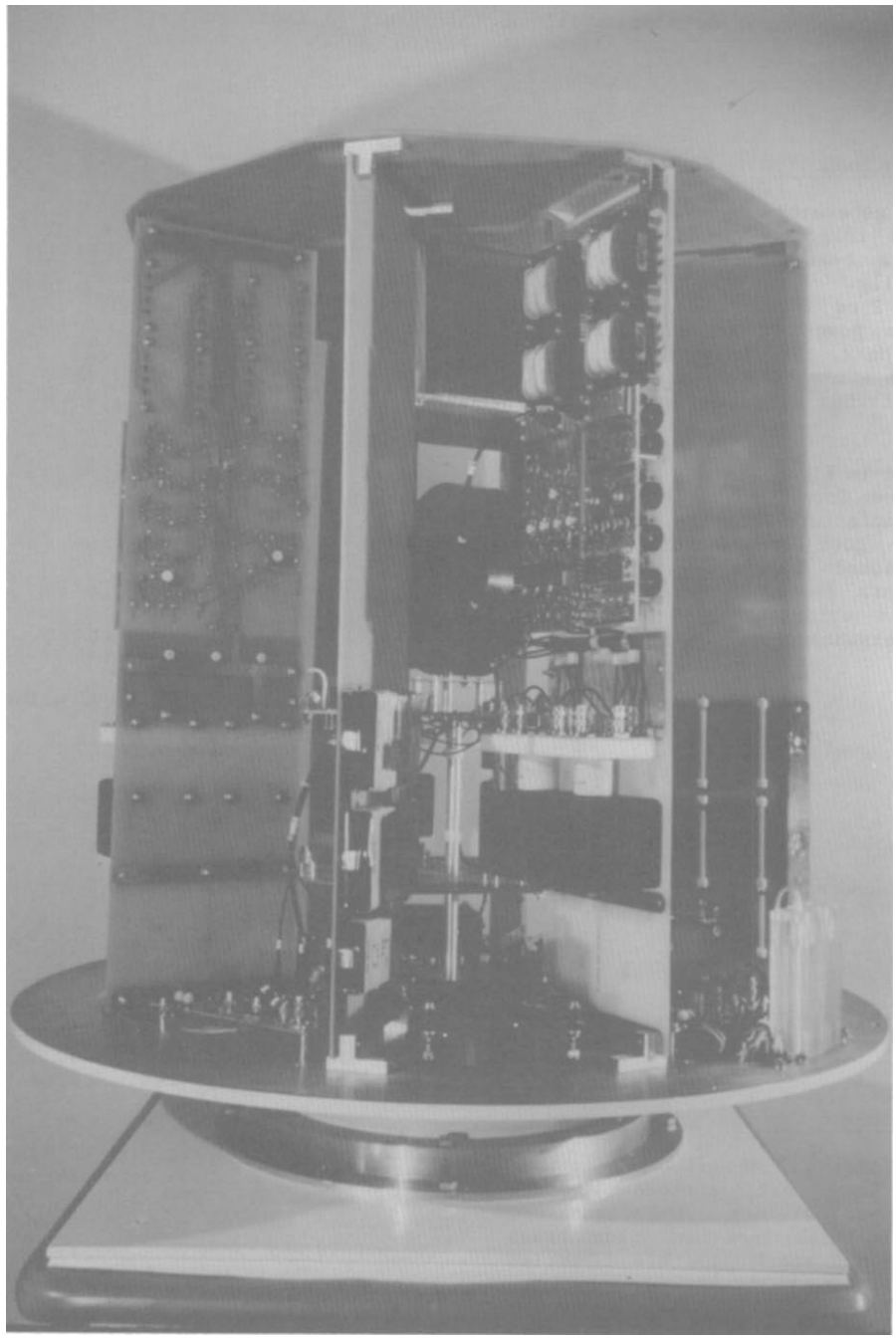


Fig. 9

In the above photo of the modulator the switch-tube assemblies are clearly visible just off center.