A Programmable Controller With Overcurrent Latch for Constant Primary Peak Current in Capacitor Charging FET Switcher for Nova*

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Summary

New switching power supplies were designed for the 10 mm laser amplifiers in the Nova Master Oscillator Room. The flashlamp supply must be repratable. Therefore, we designed a constant current, linearly charging power supply. Refer to a related paper, "An FET Full Bridge Switcher for Inductorless Capacitor Charging for Nova," for specifications and details on the power circuit.

Since it is a capacitor, the load varies throughout the charge cycle. At first the load is great, and di/dt of load current is at a maximum. As the capacitor charges the initial conditions for each cycle change, the power supply in effect sees a smaller capacitance, and di/dt decreases. We need a way of gradually increasing the on-time of the current pulses so that the transistors in the power bridge are turned off when they reach their maximum peak current. The normal current sense response of the control chip is not fast enough to be useful for our application. The deadtime, or the time that all the bridge transistors are turned off, is fixed so that as the pulse width varies so does the period. We end up with a constant peak current, switching power supply whose frequency varies from 50 khz to 20 khz. Finally, an overcurrent latch protects the transistors from bridge or transformer faults. The circuit is described and results are shown.

Circuit Description

The power supply is designed around the Silicon General 3526 Regulating Pulse Width Modulator. We use function blocks on the chip for purposes other than their original intent. Pins 6 and 7 are normally used for pulse-by-pulse current limiting; we use this inverting comparator to determine the pulse width. The positive input is tied to a Zener reference and the negative input CS- is the timing capacitor voltage of our soft start board. Since a single comparator, reference and control voltage are used, the width of positive and negative pulses will be the same. The function of our soft start board must not be confused with that of the normal control chip soft start by which we gradually increase the pulse width over a period of 1.5 milliseconds during voltage regulation. Rather, the soft start referred to here involves controlling the pulse width of a large number (about 33k) of pulses.

Figure 1 is a block diagram of our soft start circuit. The output CS- is input to the control chip comparator and varies the pulse width by its rate of discharge. The input $\overline{\text{DRIVE}}$ when low indicates that a pulse is occurring. When RESET goes from high to low all the counters will start from zero. The outputs of the ripple counters must be jumpered so that the user has freedom to select his maximum count.

$\overline{\text{DRIVE}}$ is connected to the clock of the first ripple counter, a 14 stage counter which successively divides the input down by two. A second 12 stage counter is available in case more pulses are needed between stages. Also, a triple input AND gate is provided to chose a count between 2^n and 2^{n+1}, where n is an integer.

The AND gate is connected to the clock of the binary up-counter. When the maximum number of pulses is reached for each step the up-counter is clocked and increases its binary output by one. The output is connected to the decoder, which in turn selects one of eight different PNP transistors. When turned on, the transistor discharges the timing capacitor through the resistor connected between the capacitor and its emitter. By programming R1 through R8 we vary the capacitor voltage decay time and hence the pulse width. When $\overline{\text{DRIVE}}$ goes low after each pulse Q9 turns off, and the timing capacitor is recharged through R9 and R11.

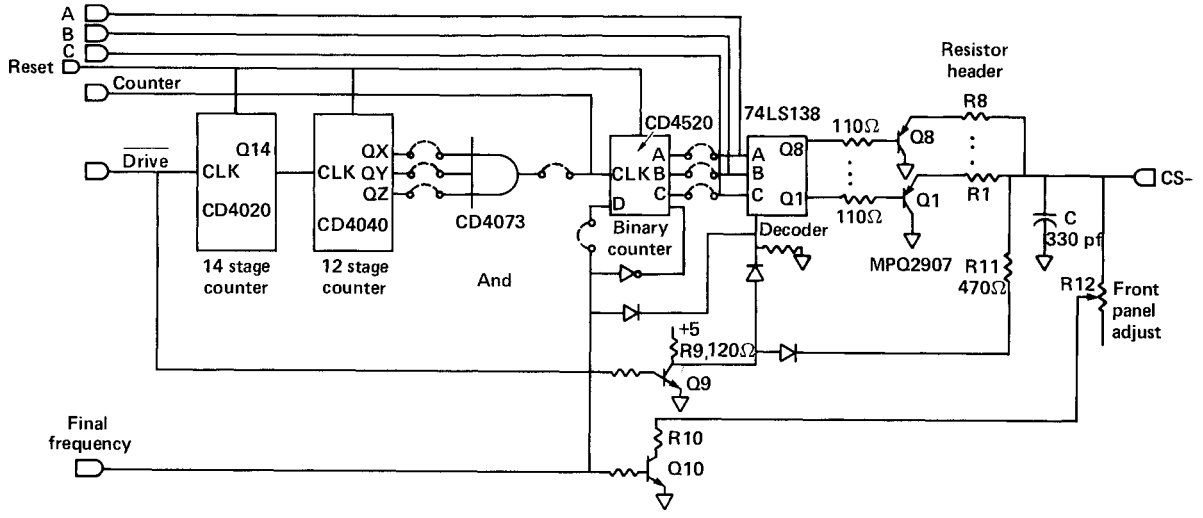

FIGURE 1

SOFT START BLOCK DIAGRAM

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After the eighth step, the next pulse leaves the binary counter with an output of 1000 which looks like the first step to the decoder. When output D goes high it disables the decoder and also the up-counter itself through an inverter and stays high until RESET is cycled by a new charge command. Output D also turns on Q10 which discharges the timing capacitor through R10, a user-selectable value, and R12 the front panel pot. Since R10 and R12 are very much greater than R9 and R11, the capacitor can recharge to virtually 5 volts even though Q10 is permanently on after the eight step.

The signals determining the pulse width are brought out to the edge connector for external control by a microprocessor or a computer. In this way special load requirements can be met, and the steps may occur in any order. All that is required is the removal of the appropriate jumper wires.

Current Waveforms

Figure 2 shows from top to bottom the drive voltage, transformer primary current, leg current of both diagonal pairs (refer to related paper) and load current at 10 microseconds/div. all at some point during the charge. Figure 3 shows these same signals at 0.5 seconds/div. The first step is half the length of the second step, since the up-counter is clocked on the rising edge. Each step thereafter has the same number of pulses, but since the pulse width increases each successive step takes more time. Steps seven and eight were programmed with the same value resistor, which does not have to be the case, but shows the limitations of using a single pulse width. The envelope of each step is an exponential, which is to be expected for capacitor charging. Finally, step nine is the final, constant pulse width and the current peaks are constant. By varying pulse width we have increased the average power output of the supply.

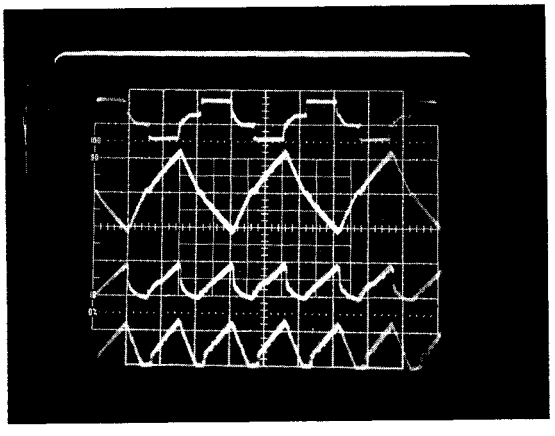

FIGURE 2

1. Drive Voltage 20V/div
2. I_{pri} 5A/div
3. I_{legs} 5A/div
4. I_{load} 200ma/div

10 μs/div

In Figure 3 the voltage was set high enough that regulation did not occur and the supply is still charging in step 9. We use the ninth step to get our final simmer current. The simmer power supply is set to the desired high voltage for breaking down the lamp. It reaches that voltage and regulates, and the ninth step is reached. This pulse width is narrow, but is able to maintain output voltage since there is only the capacitor load. The trigger signal is given, the lamp breaks down and the supply keeps the lamp turned on by providing current. However, since the pulse width is narrow, the rms current is limited. In this way we use the front panel potentiometer to control pulse width and simmer current. Of course, the output voltage never reaches the set voltage and the power supply runs continuously, but this method of operation is smoother and quieter than that of controlling current through voltage regulation.

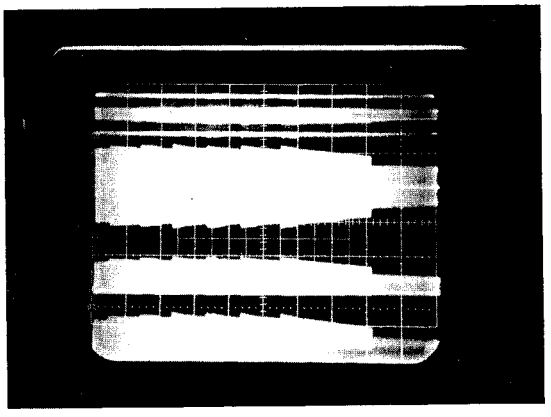

FIGURE 3

1. Drive Voltage 20V/div
2. I_{pri} 5A/div
3. I_{legs} 5A/div
4. I_{load} 200 ma/div

0.5 sec/div

Overcurrent Latch

A considerable amount of time and expense was spent replacing failed transistors during the power supply development stage. Every type of control, transistor and transformer fault was well represented in our search for the optimum control and bridge configuration. Finally, we developed the overcurrent latch circuit shown in Figure 4. A differential amplifier eliminates noise from our current transformer and feeds a set of LM306 high speed comparators. Not shown here are two more sets of parallel comparators for other current control functions. The comparators feed a simple NAND latch whose output disables the control chip by holding $\overline{\text{SHUTDOWN}}$ low. A one shot inhibits charging at power-up and resets the latch when $\overline{\text{CHARGE}}$ goes low.

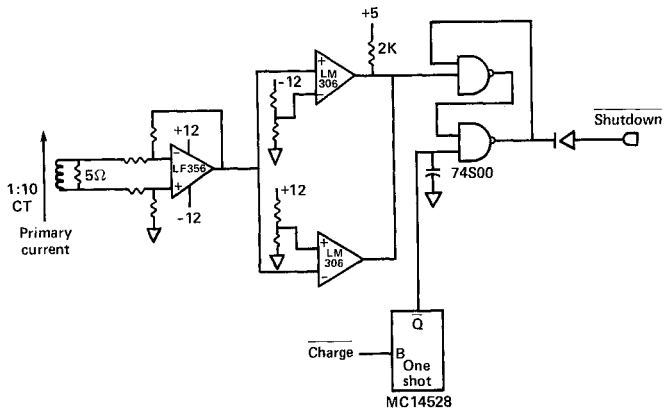

FIGURE 4

OVERCURRENT LATCH CIRCUIT

Normally the transistors failed due to excessive current vaporizing the internal leads. The power supply continued to run under a fault condition and overheated them. By limiting overcurrent to one time, we are able to continually reissue the charge command when there is a fault condition and the transistors will not fail. Figure 5 shows leg current when one transistor in the bridge is shorted while the supply is charging. A peak current of 47 amperes is the largest we were able to get. Most current peaks were between 15 and 25 amperes. This circuit has served us well since it was installed. We continue to have a number of faults, but have not had a single transistor failure in nine months.

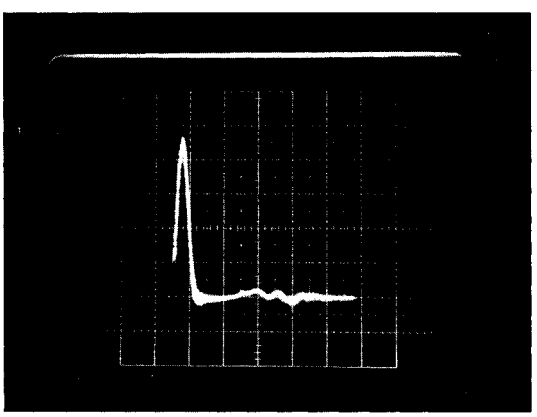

FIGURE 5

I_{leg} 10A/div

1 μs/div

Conclusion

A control system for a repratable capacitor charging switching power supply has been developed and has proved to be reliable. Output current can be dynamically controlled by adjusting the pulse width. A reliable overcurrent latch was installed for power supply development.

References

1. Silicon General Linear Integrated Circuits, Product Catalog.