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SPUTTERING TECHNOLOGY FOR IMPROVED ELECTRON DEVICES

D.H. GRANTHAM
J.L. SWINDAL

REPORT NO. N921820-4
FINAL REPORT

PERIOD COVERED: 1 JAN. 1974 TO 31 DEC 1974

NAVAL AIR SYSTEMS COMMAND
CONTRACT NO. N00019-74-C-0256

United Aircraft
Research Laboratories

UNITED AIRCRAFT CORPORATION

EAST HARTFORD, CONNECTICUT 06108

RESEARCH LABORATORIES
UNITED AIRCRAFT CORPORATION
EAST HARTFORD, CONNECTICUT

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FOREWORD

This report describes work performed from 1 January 1974 through 31 December 1974 under Contract N00019-74-C-0256 for the Naval Air Systems Command. NAVAIR program managers for this work were Messrs. C. D. Caposell, A. S. Glista, and S. M. Linder of code: AIR-52022. This report was prepared by the United Aircraft Research Laboratories, East Hartford, Connecticut and describes work performed in the Electromagnetics Laboratory headed by Dr. A. J. DeMaria. Dr. D. H. Grantham, Chief, Microelectronics Technology was the principal investigator and technical assistance was provided by Mr. J. L. Swindal.

Publication of this report does not constitute approval by the Naval Air Systems Command of the findings or conclusions contained herein. It is published for the exchange and stimulation of ideas.

Report N921820-4

Final Technical Report Under Contract N00019-74-C-0256
for the Period 1 January 1974 to 31 December 1974

Sputtering Technology For Improved Electron Devices

TABLE OF CONTENTS

TABLE OF CONTENTS
(Continued)

LIST OF ILLUSTRATIONS AND TABLES

3.0 INTRODUCTION

Phase I of this program was undertaken to demonstrate the feasibility of a reliable silicon dioxide-aluminum based multilevel interconnection technology for integrated circuits. The need for such a technology is based on the ever-increasing demands of increased speed, reduced size and low cost-of-ownership being placed on integrated electronics data processing equipment. Much higher device density can be realized in such components by the use of multilayer thin film metal interconnects stacked one layer above the other and separated by appropriate thicknesses of electrically insulating thin films. Thus, an interconnection between two devices may pass directly over another device, permitting the utilization of all of the semiconductor "real-estate" for devices and sacrificing none of the silicon area to the interconnections.

Phase II of this program was directed toward a technology for depositing layers of amorphous or small-grained polycrystalline beryllium oxide onto silicon and silicon dioxide-covered silicon substrates. The need for this technology stems from the lifetime and reliability problems introduced by the use of smaller and smaller devices closer together and operating at higher power levels and at associated higher temperatures. Thin film beryllium oxide offers the possibility of greatly improved thermal resistance in device packaging and, therefore, improved performance, reliability, and life.

4.0 EXPERIMENTAL APPROACH

4.1 Phase I

Statement of the Problem and Discussion of Multilevel Interconnect Problem

A multilevel interconnection technology for silicon integrated circuits must meet the following requirements. An ohmic metal contact to silicon must be made. It is preferable that the interconnect metal be suitable for this purpose also. The interconnect metal must be adherent to silicon dioxide or other insulator used without excess chemical reaction with the oxide. Selective etching of the metal to define the interconnections must be possible without significant attack on the silicon dioxide or other insulator. By the same token, the metal must be reasonably resistant to the insulator etch. The metal itself must exhibit reasonable stability toward the usual atmospheric ambient experienced in electronics device processing. That is to say the metal properties should not seriously limit device performance.

Insulator-interconnect compatibility has already been discussed briefly. In addition, the insulator must be amenable to reasonable etch procedures in reasonable times. The dielectric breakdown strength must be high enough to permit use of layers only a few micrometers thick. Dielectric constants of candidate insulators should be low to avoid line-to-line capacitive coupling. The deposition techniques for the insulator must be compatible with the semiconductor or other devices involved in the structure. Temperature during deposition must not, for example, alter diffusion profiles or melt metal contacts already on the devices. Insulator films must possess an extremely high integrity -- pin holes would produce layer-to-layer short circuits and useless devices.

During the course of making integrated circuits with a multilayered interconnect system, an insulator layer covering a given layer of interconnecting metal must be penetrated at selected points so that electrical connection to the next layer of metal interconnect can be made. Chemical etching is, of course, the preferred technique for removing the insulator at these feedthrough points. The etch used must not attack the underlying metal, yet it must completely remove the oxide to permit a very low resistance metal-metal contact to be made.

When thin film depositions are made by thermal evaporation in vacuum or by sputtering at ambient pressures below 100 millitorr, line of sight paths are generally very nearly followed by the material being deposited. This behavior is due to the absence of enough gas molecules in the path to cause appreciable scattering. For substrates with non-planar surfaces parallel to the source plane, an edge inclined at 45° to the plane will receive a flux of deposite reduced by the value of $\cos 45^\circ$ or only 70% as great as that received on the parallel plane surface. The greater the angle of inclination, the thinner will be the deposit on the incline. Metal etch techniques must not produce sharply inclined edges along interconnecting strips lest the edge coverage be inadequate.

At higher power levels, current densities in metal interconnects may rise to values in excess of 10^6 amps/cm^2. At this level, electromigration sets in to varying degrees with different metals and becomes more serious at elevated temperatures and higher current densities. This migration of metal and thinning of conducting stripes leads to catastrophic open circuit failures of conducting thin film interconnects either directly by the electromigration process or by fusing of the thinned metal section due to excessive local heating.

It has been asserted that the metal grain size is important in the electromigration process. Very large grains and single crystals are less susceptible to failure by this mechanism. It has also been suggested that very fine-grained or amorphous films should also exhibit a reduced electromigration failure rate. The grain size of metal films can be controlled by controlling deposition parameters -- particularly temperature of the substrate -- and can also be controlled by heat treating of films after deposition. Chip processing immediately after metal depositions should also be conducted at as low temperatures as possible consistent with requirements of the process. This adherence to low temperature processing will retard grain growth and formation of highly irregular topography which can lead to locally high current density and to poor coverage by the oxide.

Temperature control of the substrates at as low temperatures as possible was, therefore, made a part of both the metals and the silicon dioxide deposition processes. Since silicon dioxide etch rate is a function of substrate temperature during deposition, an optimization was necessary. Because the silicon dioxide etch also attacks aluminum to some extent, it became necessary to control both thickness and uniformity of the oxide in order to completely remove the oxide from a feedthrough without overexposing the metal to the oxide etch. Thickness and etch rate must be accurately known so that immersion of a slice in the oxide etch for appropriate lengths of time could be relied upon to produce a complete feedthrough.

The program activity for Phase I involved a number of distinct tasks which can be enumerated. They were: (1) mask making. Masks were designed for evaluating electromigration stability of the metals, for evaluating oxide integrity (i.e., pinholes), for evaluating feedthrough resistance, and for evaluation of the metal definition (etching) process; (2) silicon dioxide sputtering parameters optimization; (3) metal sputtering parameter optimization; (4) evaluation of metal for electromigration stability; (5) evaluation of multilevel test cells; and (6) evaluation of feedthrough (or via) resistances. The details of the experiments and the results are presented in this order.

4.1.1 Maskmaking

Masks were made by conventional procedures in this program. Rubylith was cut on a manually controlled cutting table at 200 x size. Photoreduction was by means of a David-Mann first reduction camera and step-and-repeat machine.

Figures 1(a), (b), (c), (d) and (e) are the five masks of a test pattern set designed and fabricated for (1) evaluation of the sputtered silicon dioxide for pinholes; (2) evaluation of the metallization for continuity; (3) evaluation of the feedthrough etch procedures by measuring contact resistance of a series connected assemblage of feedthroughs; and (4) incidence of unopened feedthrough holes in the cell.

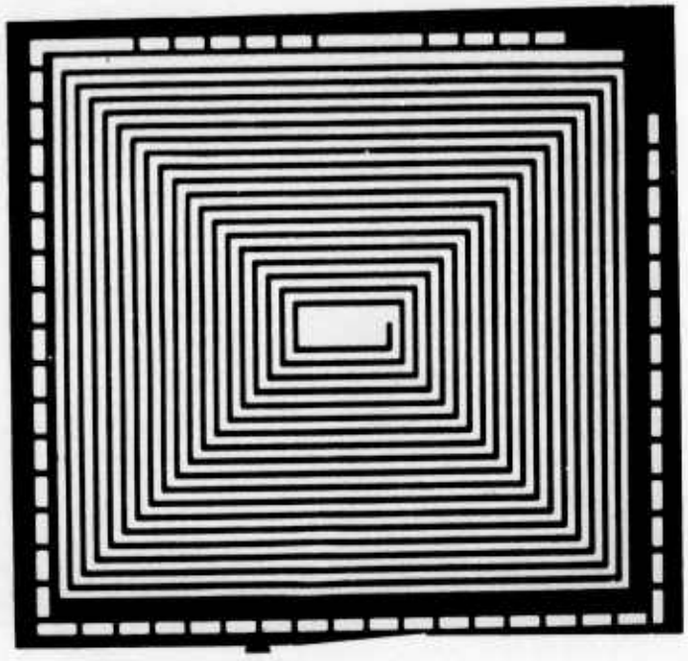
Figure 1(a) shows the first or lower level metal pattern, a rectangular spiral continuous from the center to the outer edge. A series of short metal bars surround the pattern. After deposition of the first insulating layer of oxide, feedthrough holes are etched aboveeach end of each bar and above the large pad in the center of the first level metal pattern using the mask of 1(b). After this oxide deposition and etch step, a second level of metallization is deposited and patterned using the mask depicted in Figure 1(c). Note that the first level is now contacted by a single metal bar leading from the center to outside edge of the pattern and terminating in a probe pad. This pattern introduces second layer metal lines largely running in the y-direction with each end terminated in a probe pad. The first metal layer contacted in the center as just mentioned can have a potential applied with respect to either end of this second metal layer as a check for oxide integrity. Continuity between these probe points implies pinholing. Two sets of short metal bars are introduced in this level -- one to provide the continuity check for the feedthroughs already etched with the mask of Figure 1(b) and the other to provide the lower of a second set of bars for feedthrough checks between second and third level metal.

After deposition of the second insulating layer, the upper vias or feedthroughs are etched in the oxide using the mask shown in Figure 1(d). The metal deposition followed by pattern definition using Figure 1(e) completes the test cell for a quite complete characterization of the integrity and usefulness of the metal insulator system. Thus, some 1700 1 mil x 1 mil crossover points are tested for pinholes between first and second level metal in each cell, approximately 1550 crossovers are tested for pinholes between second and third level metal, 114 first to second level feedthroughs are tested, and 101 second to third level feedthroughs checked.

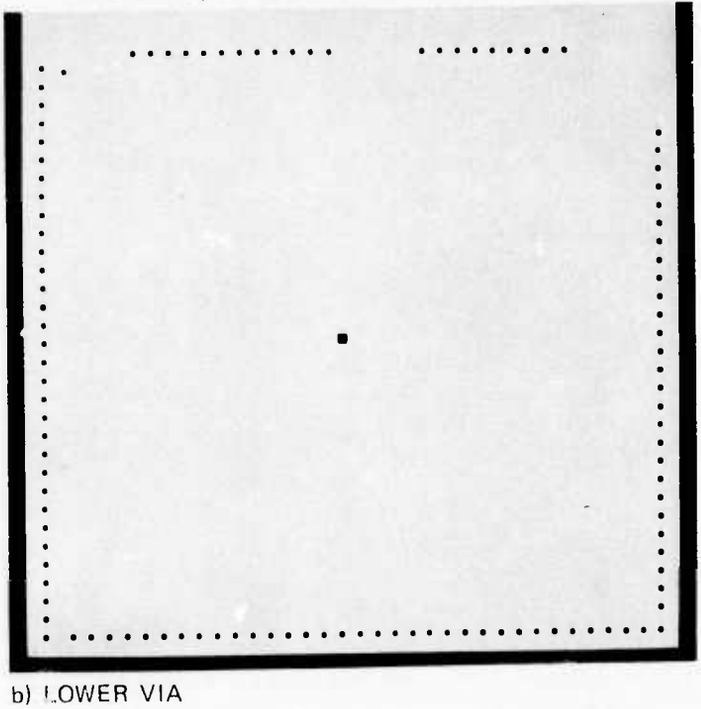
The test cell is, thus, a five layer sandwich structure with three metal layers alternating with two dielectric layers. Each metal layer is a one mil wide line that has been folded to pass back and forth over as much of the cell area as possible, each segment being one-half mil from its neighbors. On the upper layer the segments run parallel to the line of bonding pads at the edge of the cell while the segments of the middle metal level are perpendicular to this line. The

FIG. 1

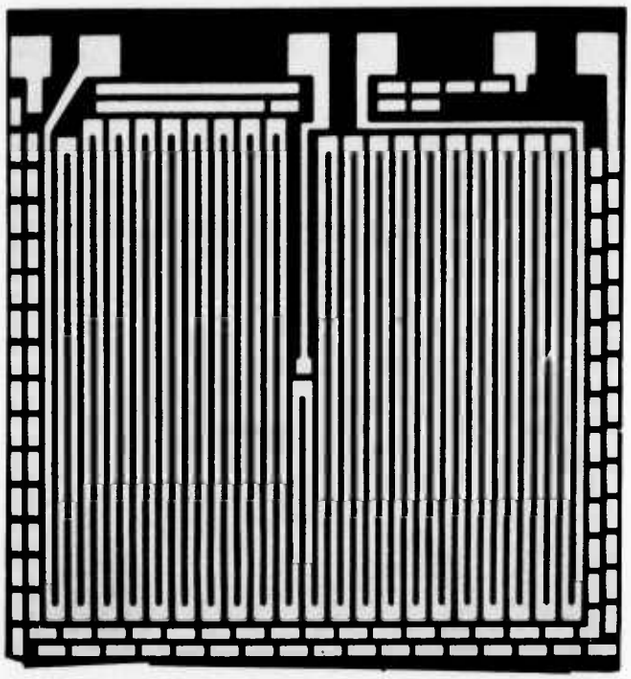
THREE LEVEL METALLIZATION TEST PATTERN



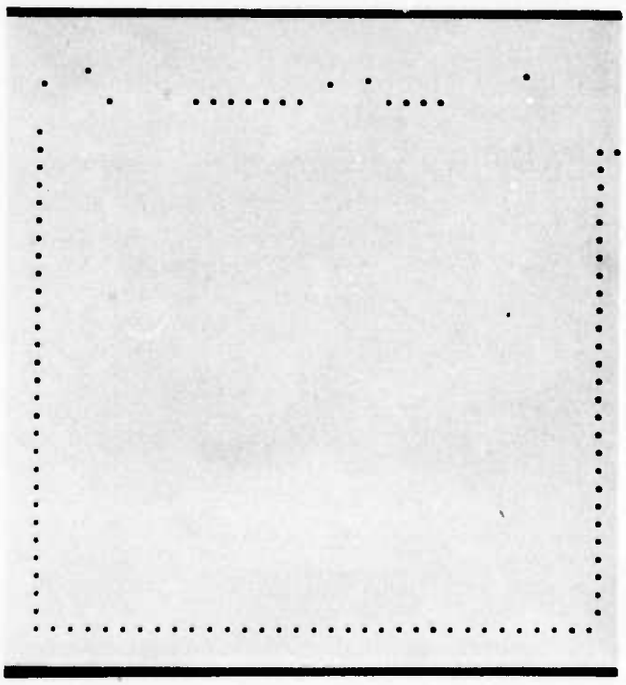
a) LOWER LEVEL METAL
1 MIL LINES, 0.5 MIL SPACES



b) LOWER VIA

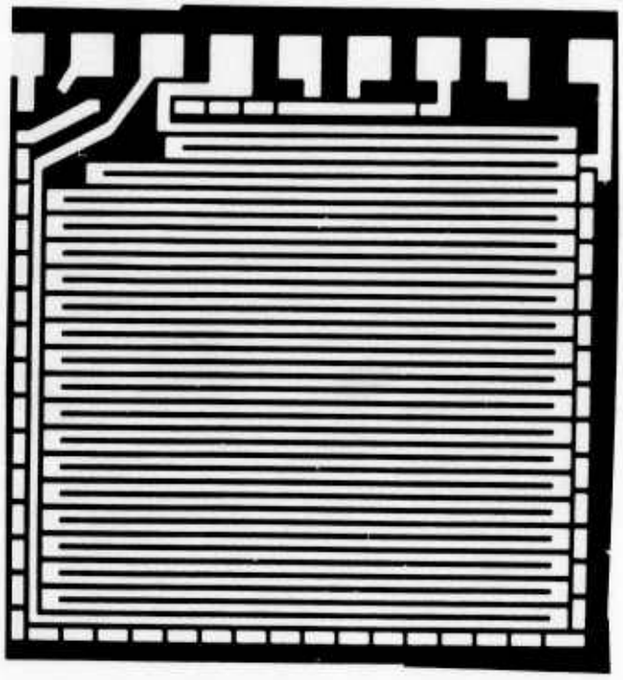


c) MIDDLE LAYER METAL
1 MIL LINES, 0.5 MIL SPACES



d) UPPER VIA

FIG. 1 CON'T



e) UPPER METAL

lower level is a rectangular spiral terminating at the center of the cell. Around the edge of the cell are two metal lines that pass back and forth through the dielectric layers by way of etched vias one line through the upper, the other through the lower dielectric. One end of each line is connected together and is in Fig. 2 labeled vias (common). The test pads along the edge of the cell provide access to each end of the three folded metal layers as well as the free end of each via line and vias (common) for a total of nine contacts. Note that along one side of the cell (Fig. 3) the upper vias fall directly over an edge of the lower metal, providing a very severe test of both the sputtering process and the photolithographic via opening process. Figures 4 and 5 illustrate other such difficult-to-define vias.

The lower and middle metal layers have been arranged to provide information on a number of different situations that could occur in a multi-level integrated circuit. For example, Fig. 6 shows the metal lines on the two levels parallel with almost coincident edges forming a step of double height to be covered with dielectric and upper metal. Figure 2 is an overall view of the test cell with the four quadrants labeled. Bonding pads along the cell edge are labelled to identify segments of the test pattern and are also keyed to the test set-up shown later. Figure 6 through February 11 are SEM micrographs of representative areas in these quadrants. Note the complexity of the patterns, one level of metal overlapping another in particularly tortuous topographical convolutions. Figures 7, 10, and 11 show areas with severe photoresist and etching constraints. The middle and upper layers are lines at right angles to one another where a crossover is simply a one square mil intersection area. In the case of the intersection of the lower metal with the other two layers only about half of the common area consists of one mil square crossover points while the remainder consists of partial superpositions of parallel strips. It may be, then, that it is more realistic to consider crossover area rather than number of one square mil areas. The approximate crossover areas for the pairs of layers are then given for each cell:

(a) Lower and Middle - 1730 $mils^2$ 30% area

(b) Middle and Upper - 1600 $mils^2$ 29%

(c) Upper and Lower - 1670 $mils^2$ 29%

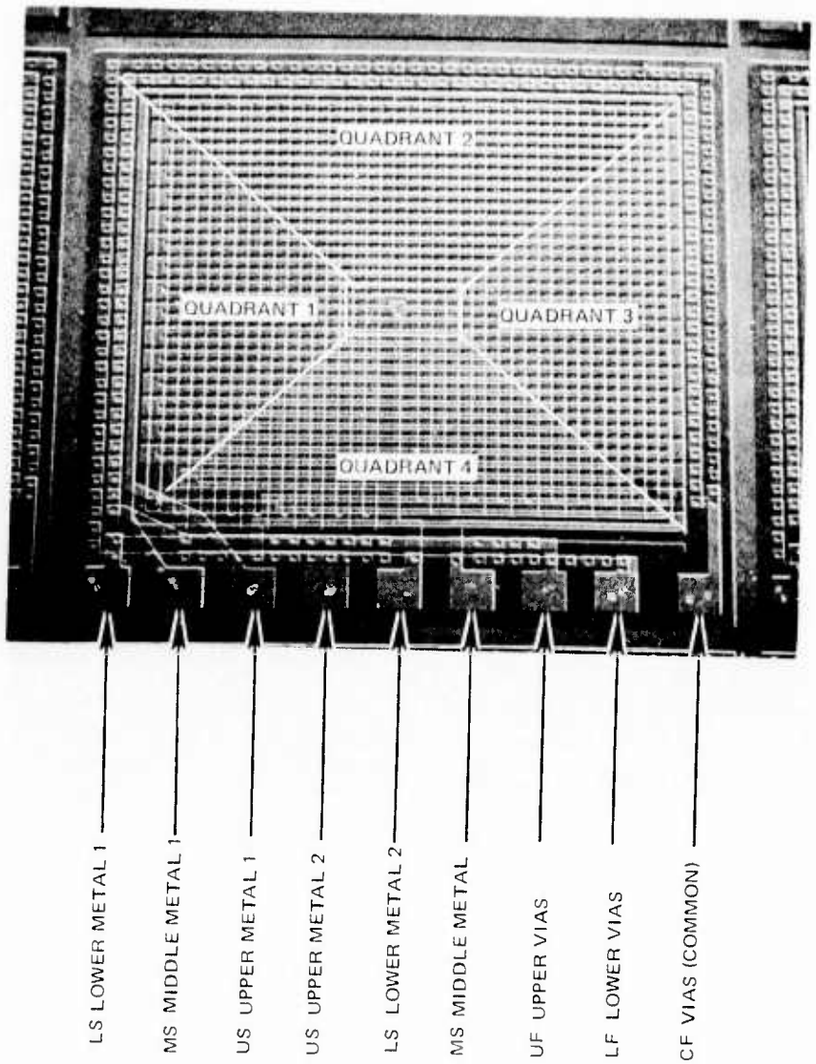
Each cell is 76 mils x 76 mils -- 5776 $mils.^2$

In Figs. 12 through 15 are shown the set of masks for generating links for evaluation of electromigration of aluminum and aluminum-4% copper. Note that ten links per cell are included (Fig. 12).

Metal links protected by sputtered silicon oxide can be contacted at the appropriate pads by opening contacts with the mask shown in Fig. 13 and using the mask shown in Fig. 14 to define upper level contacts in a second layer of sputtered aluminum. Figure 15 shows a mask used to produce metal or oxide steps or oxide-over-

FIG. 2

CROSS-OVER TEST PATTERN
SEM 50X



N11-204-5

FIG. 3

CROSS-OVER TEST PATTERN

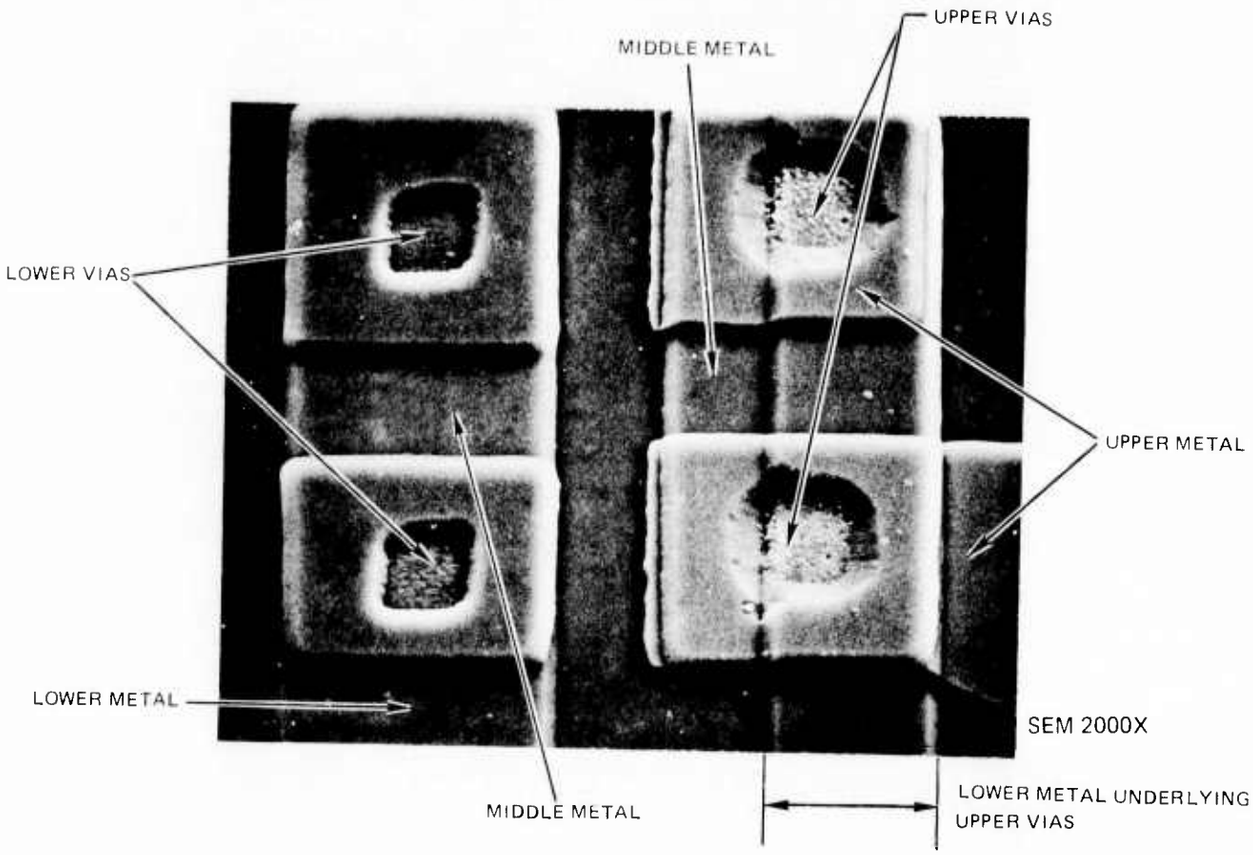


FIG. 4

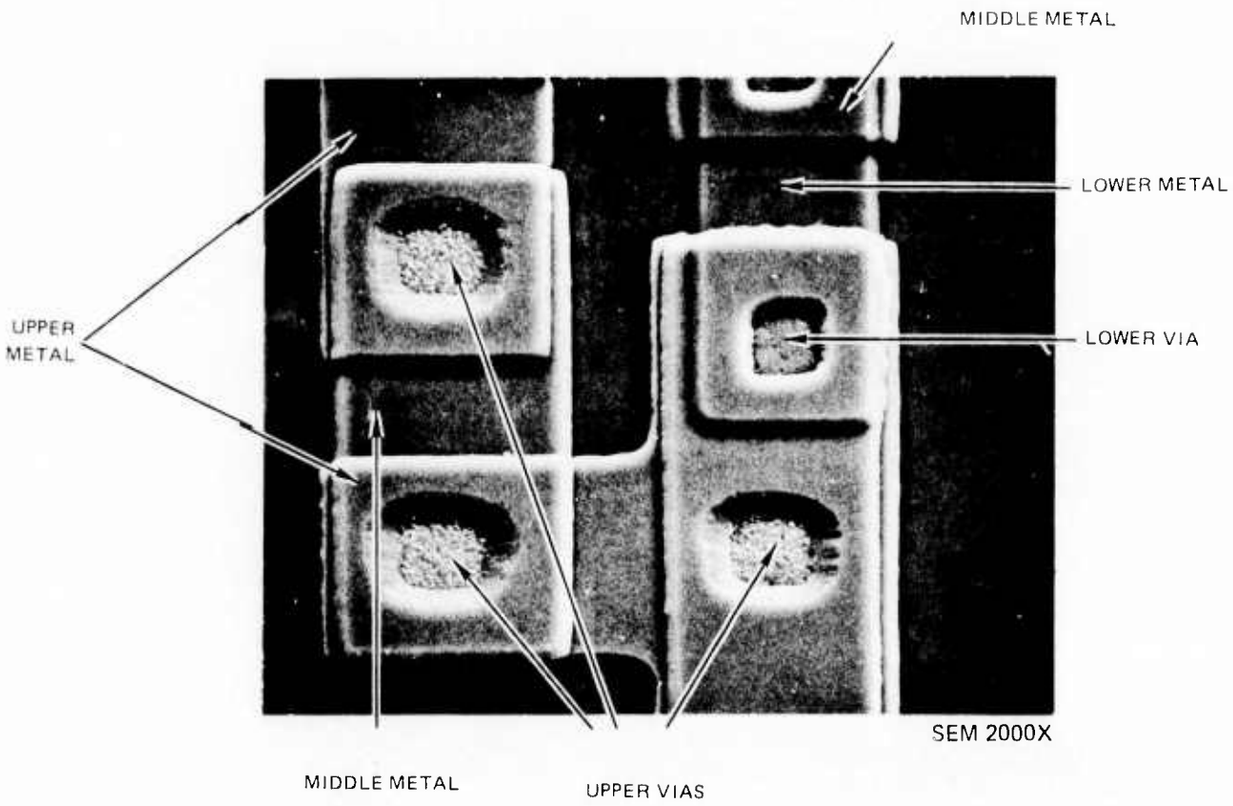
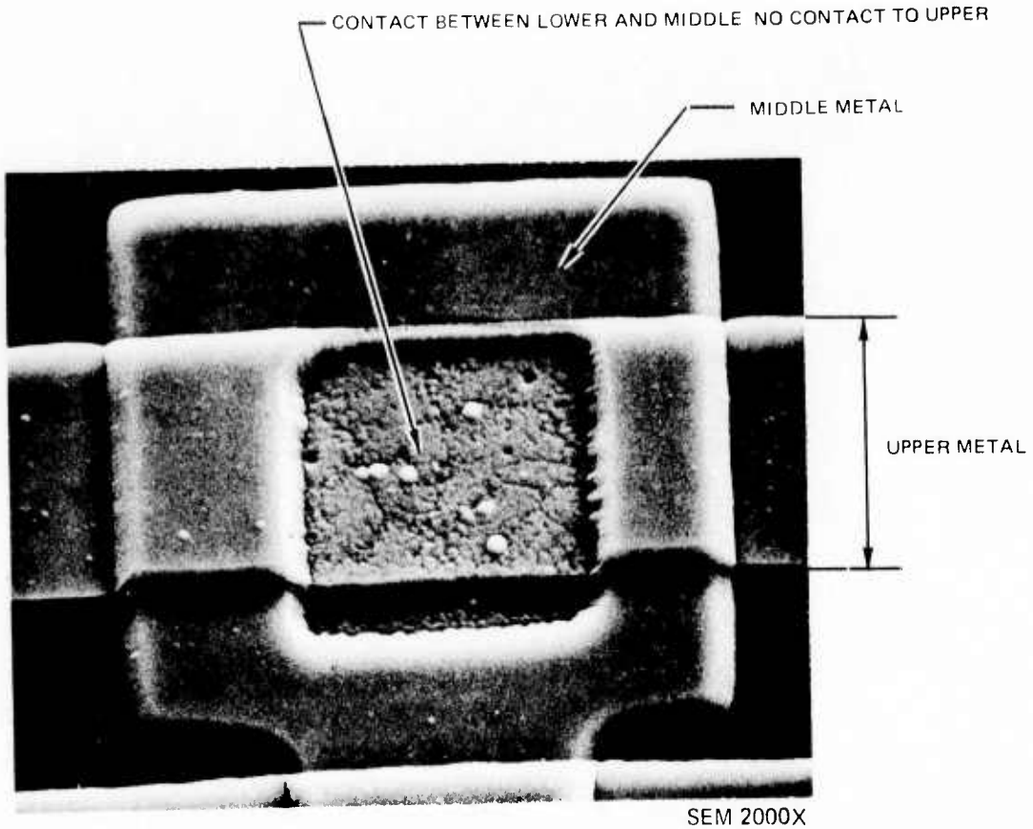

MIDDLE METAL
LOWER METAL
LOWER VIA
UPPER METAL
SEM 2000X
MIDDLE METAL
UPPER VIAS

FIG. 5

CROSS–OVER TEST PATTERN CENTRAL VIA

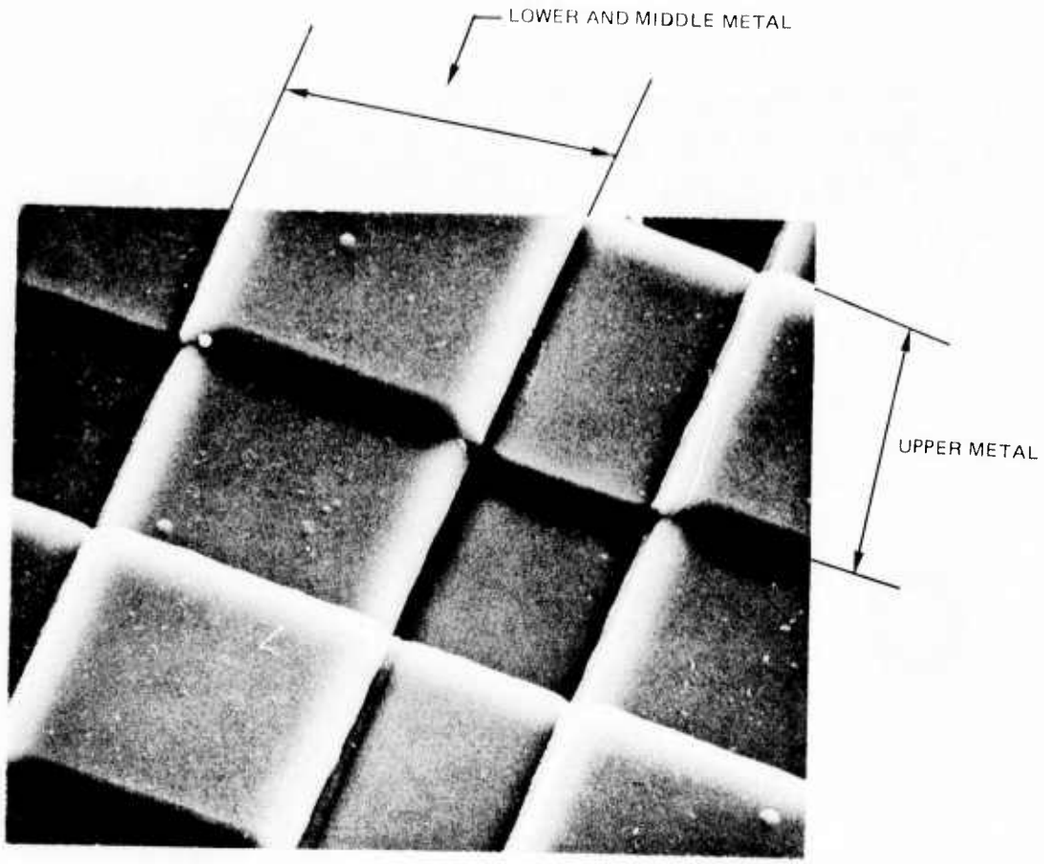


SEM 2000X

LOWER METAL UNDERLIES ENTIRE AREA

FIG. 6

CROSS-OVER TEST PATTERN QUADRANT 1



SEM 2000X

FIG. 7

CROSS-OVER TEST PATTERN QUADRANT 2

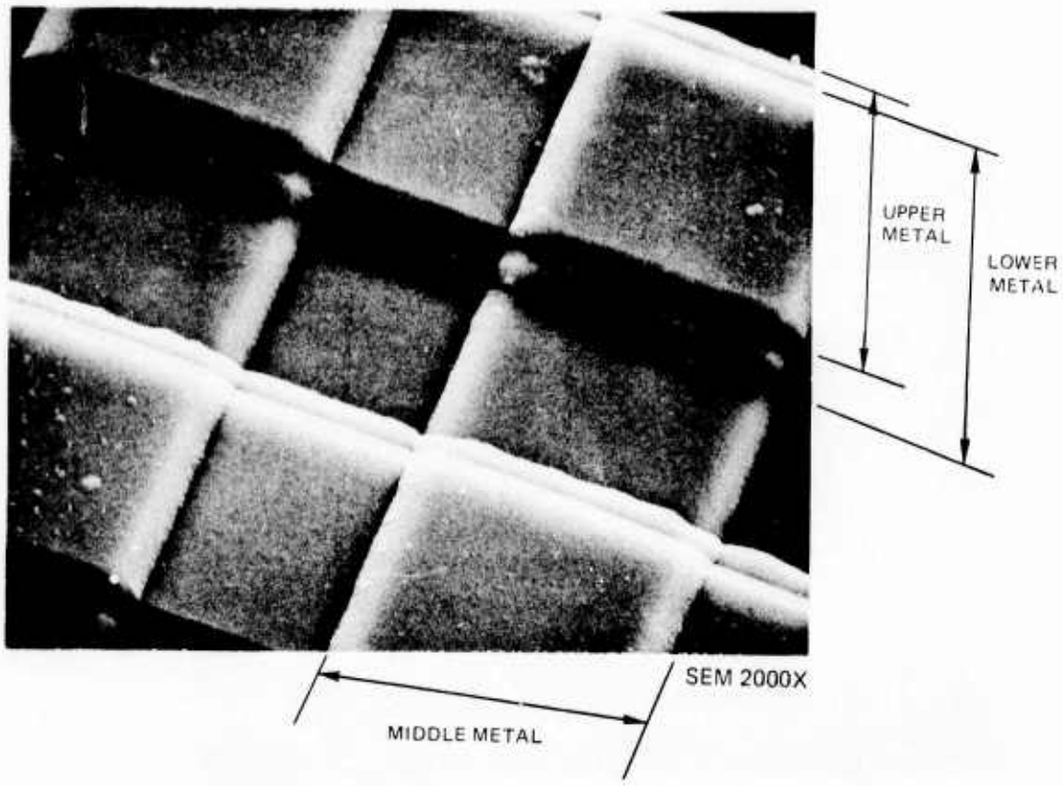


FIG. 8

CROSS-OVER TEST PATTERN QUADRANT 3

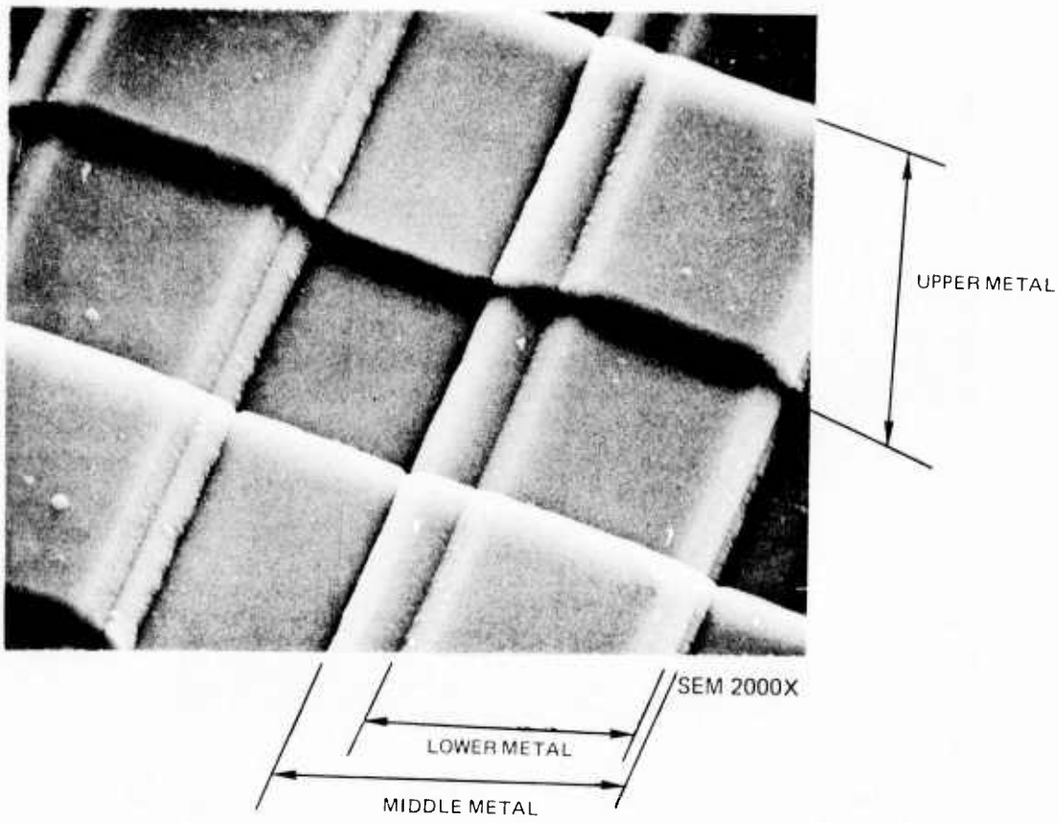
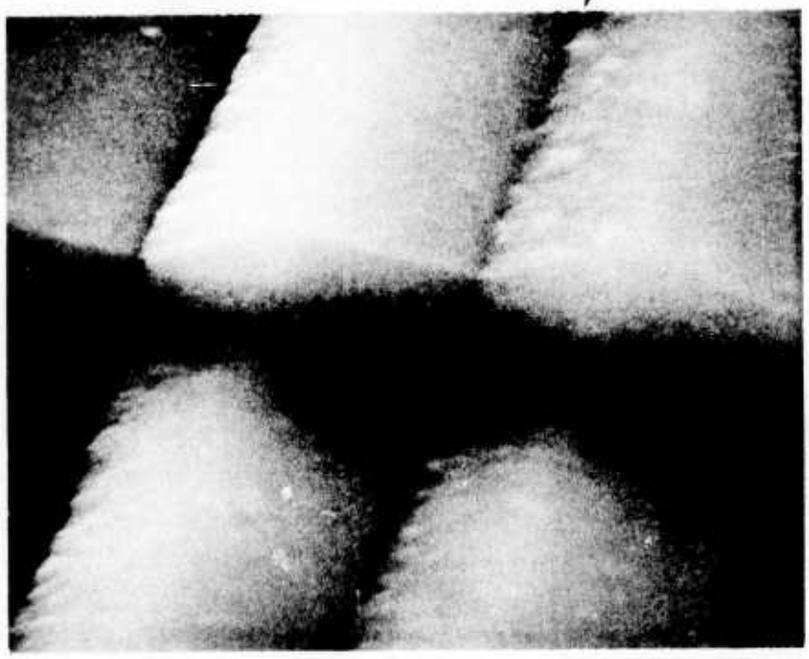


FIG. 9

CROSS-OVER TEST PATTERN QUADRANT 3



SEM 10,000X

FIG. 10

CROSS-OVER TEST PATTERN QUADRANT 4

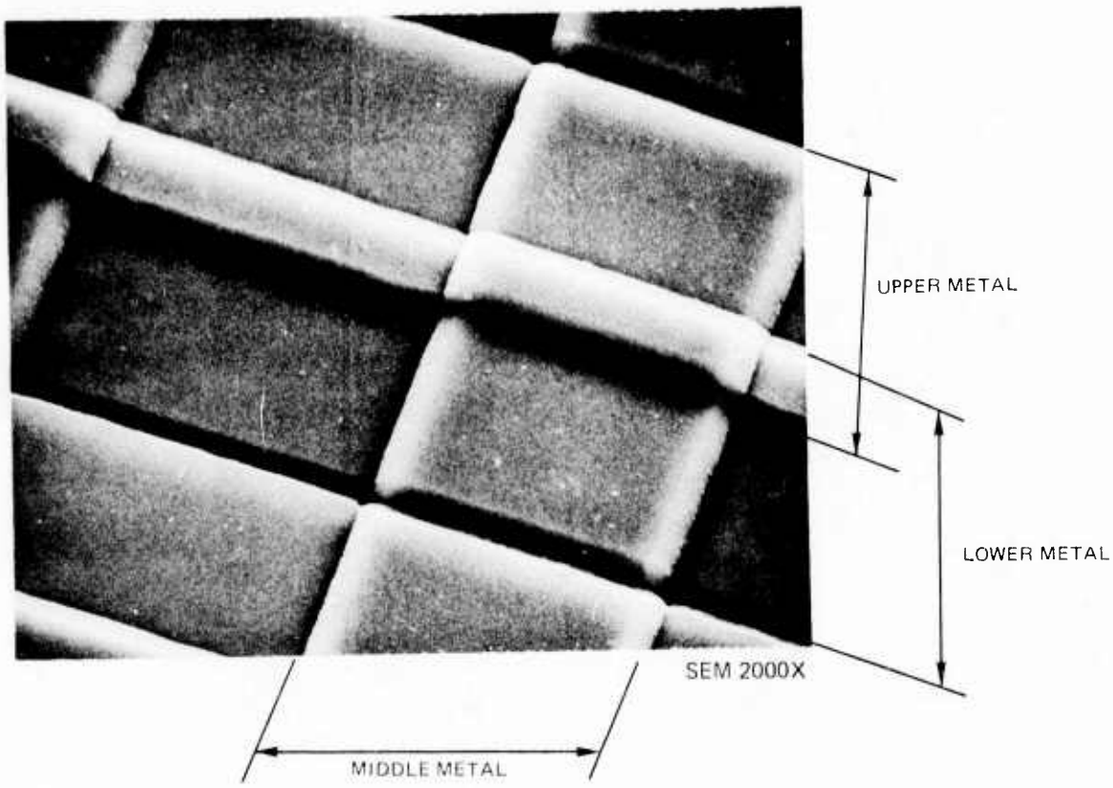


FIG. 11

CROSS–OVER TEST PATTERN

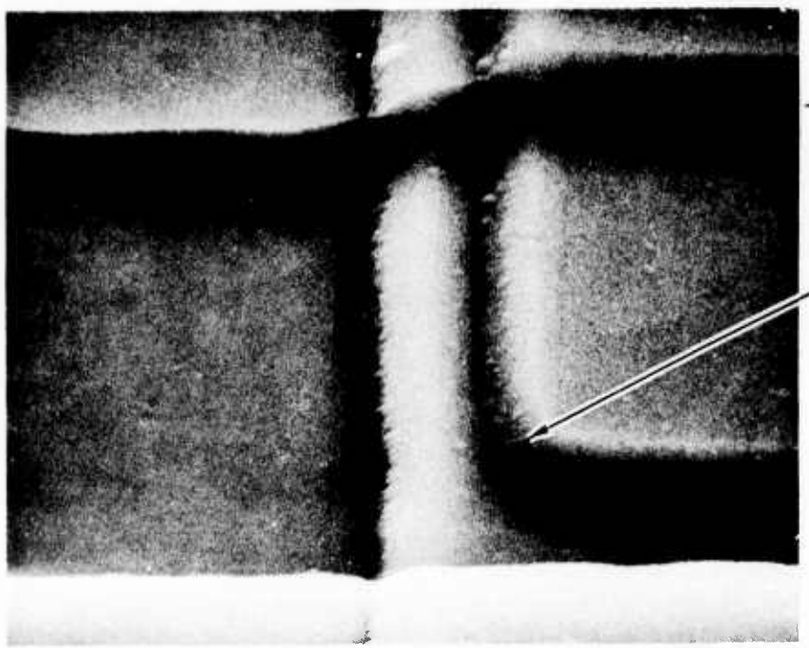
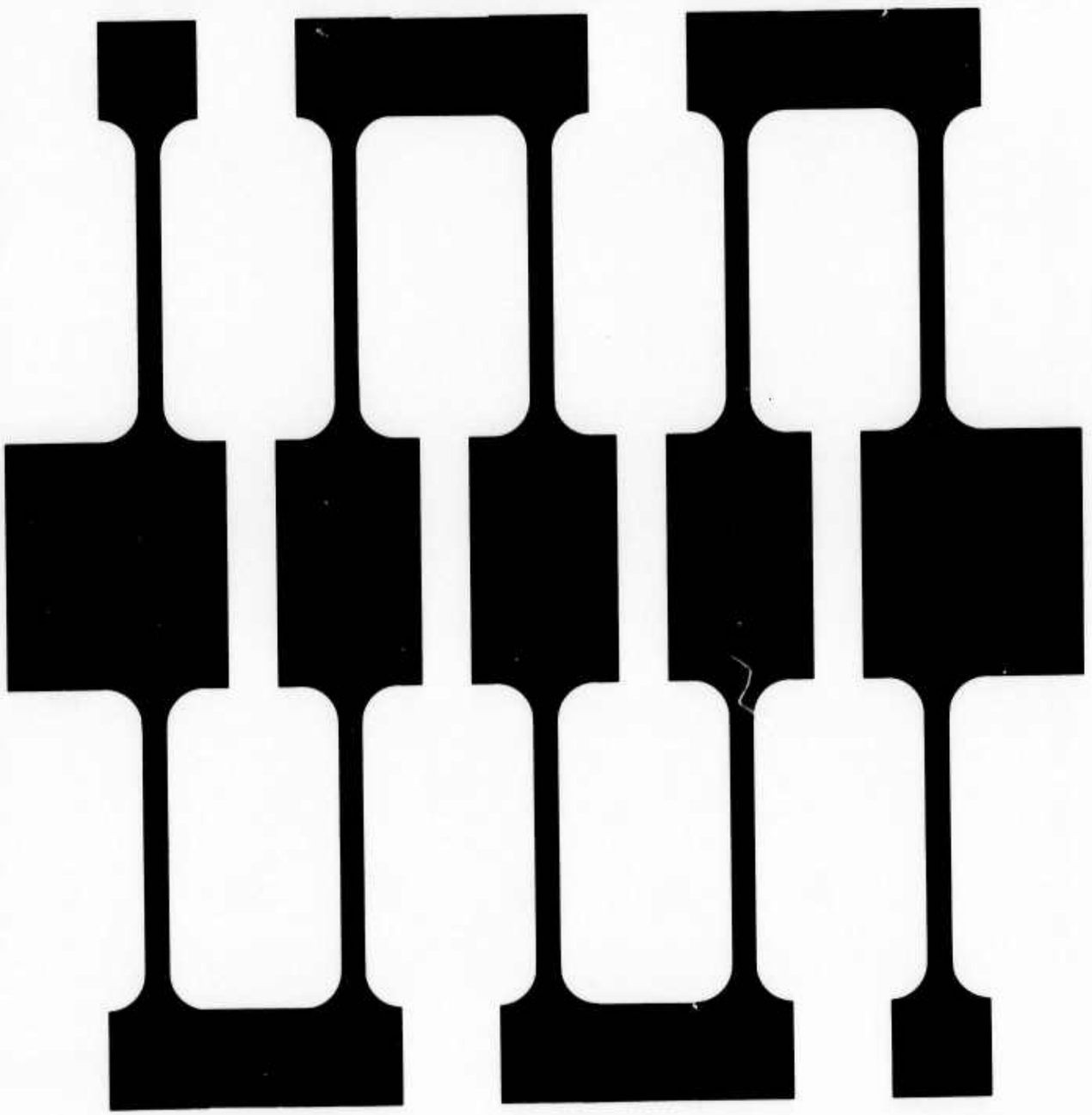


FIG. 12

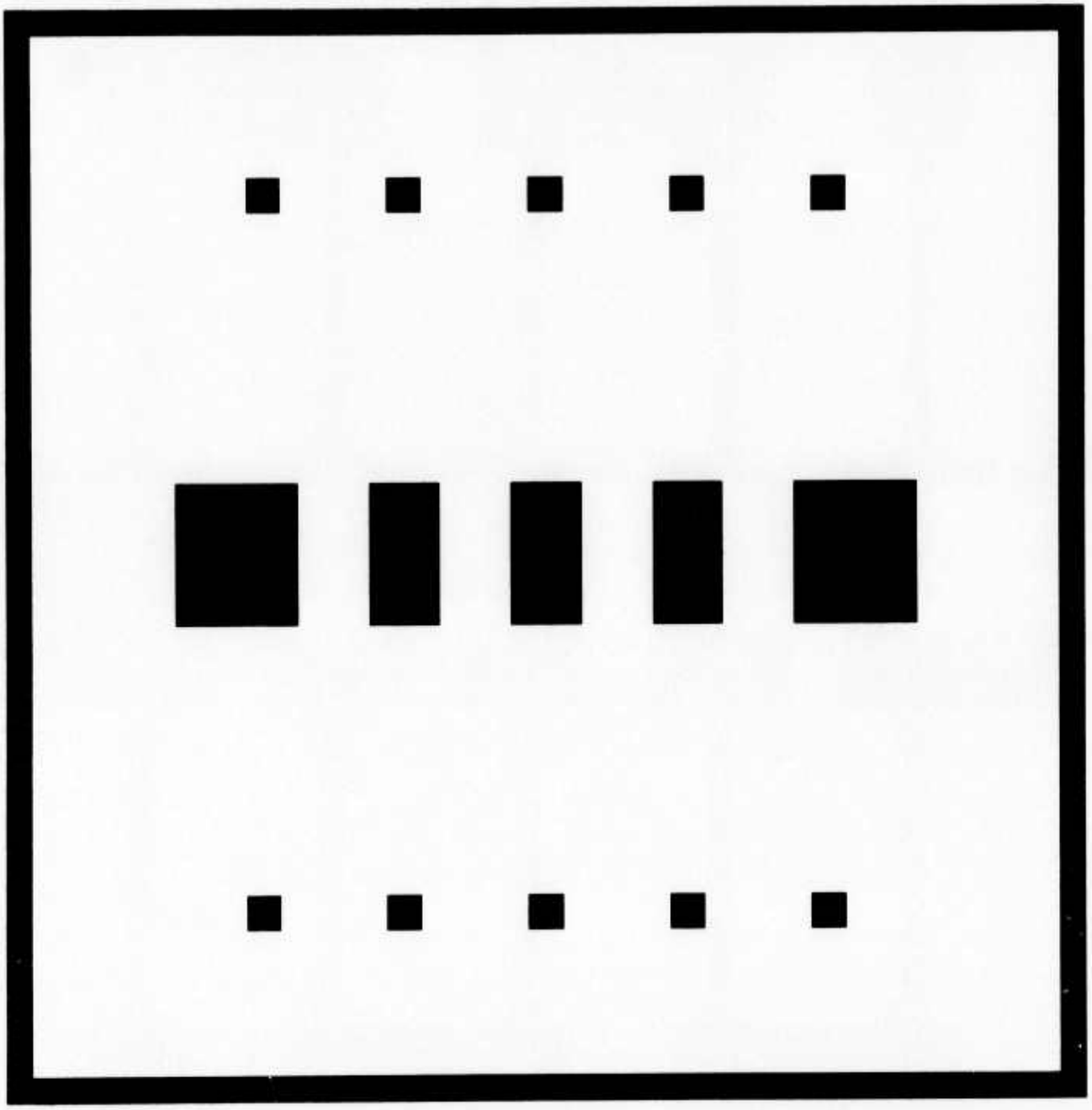
METAL LINK ELECTROMIGRATION TEST PATTERN



N07-34-6

FIG. 13

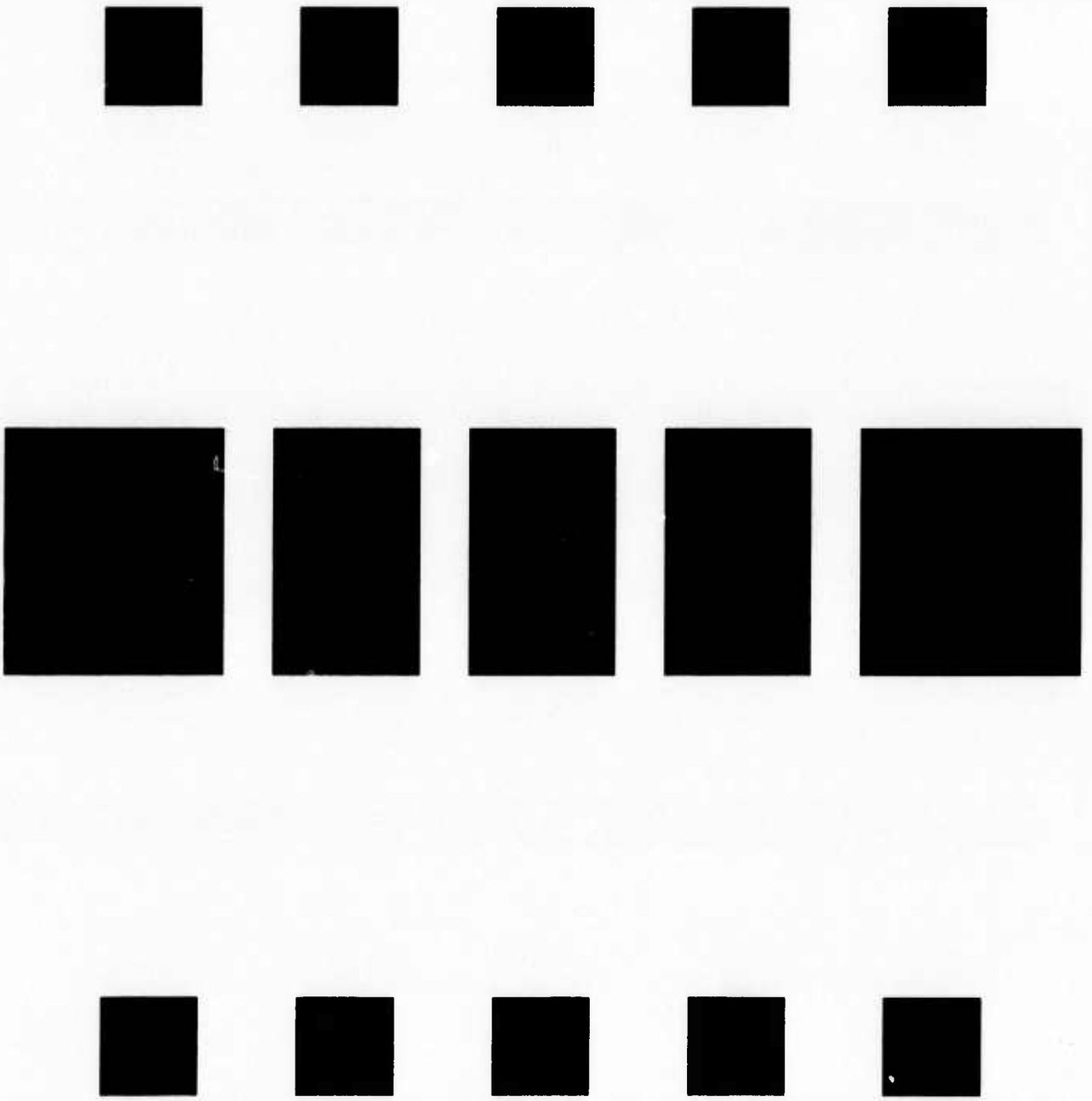
CONTACT HOLE MASK FOR PROTECTED METAL LINKS



N07-34-7

FIG. 14

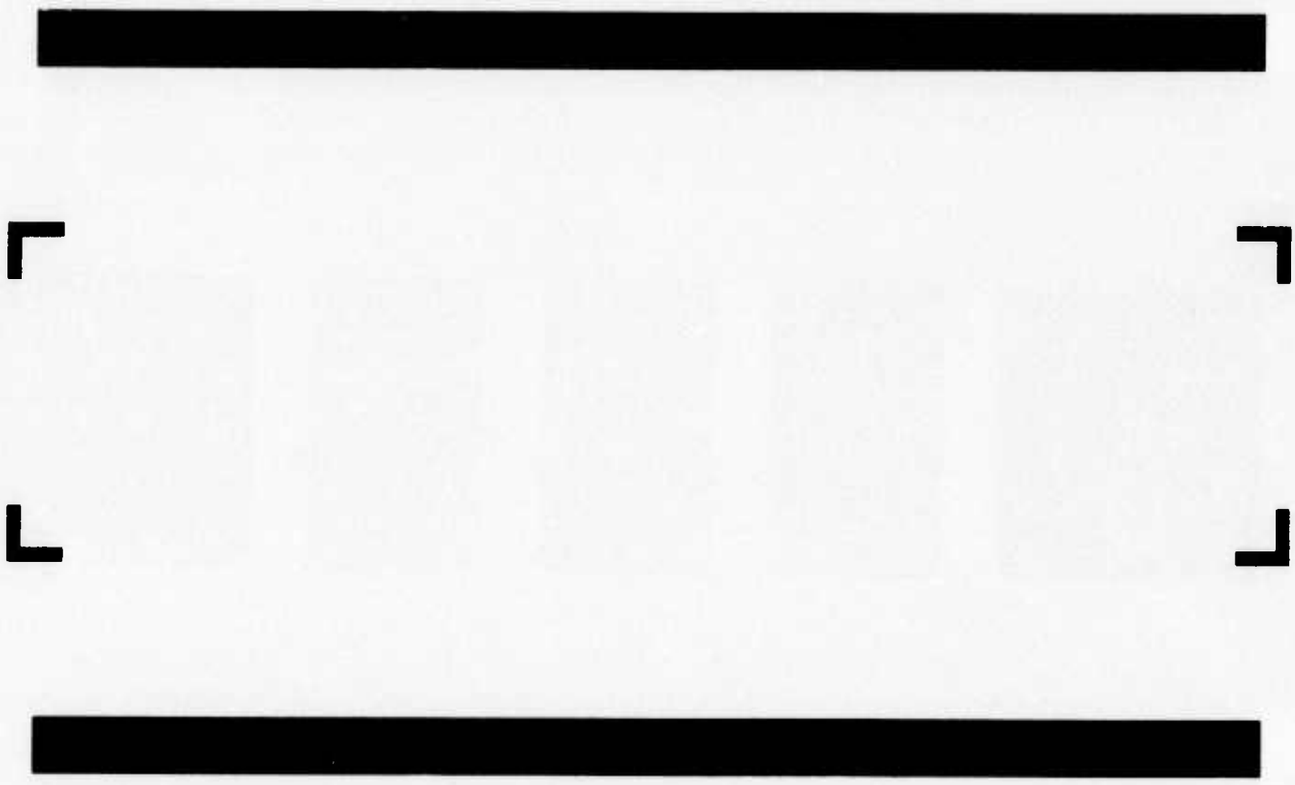
TOP LEVEL METAL BONDING PAD



N07-34-8

FIG. 15

OPTIONAL ETCH MASK FOR TOPOGRAPHIC EFFECTS STUDIES

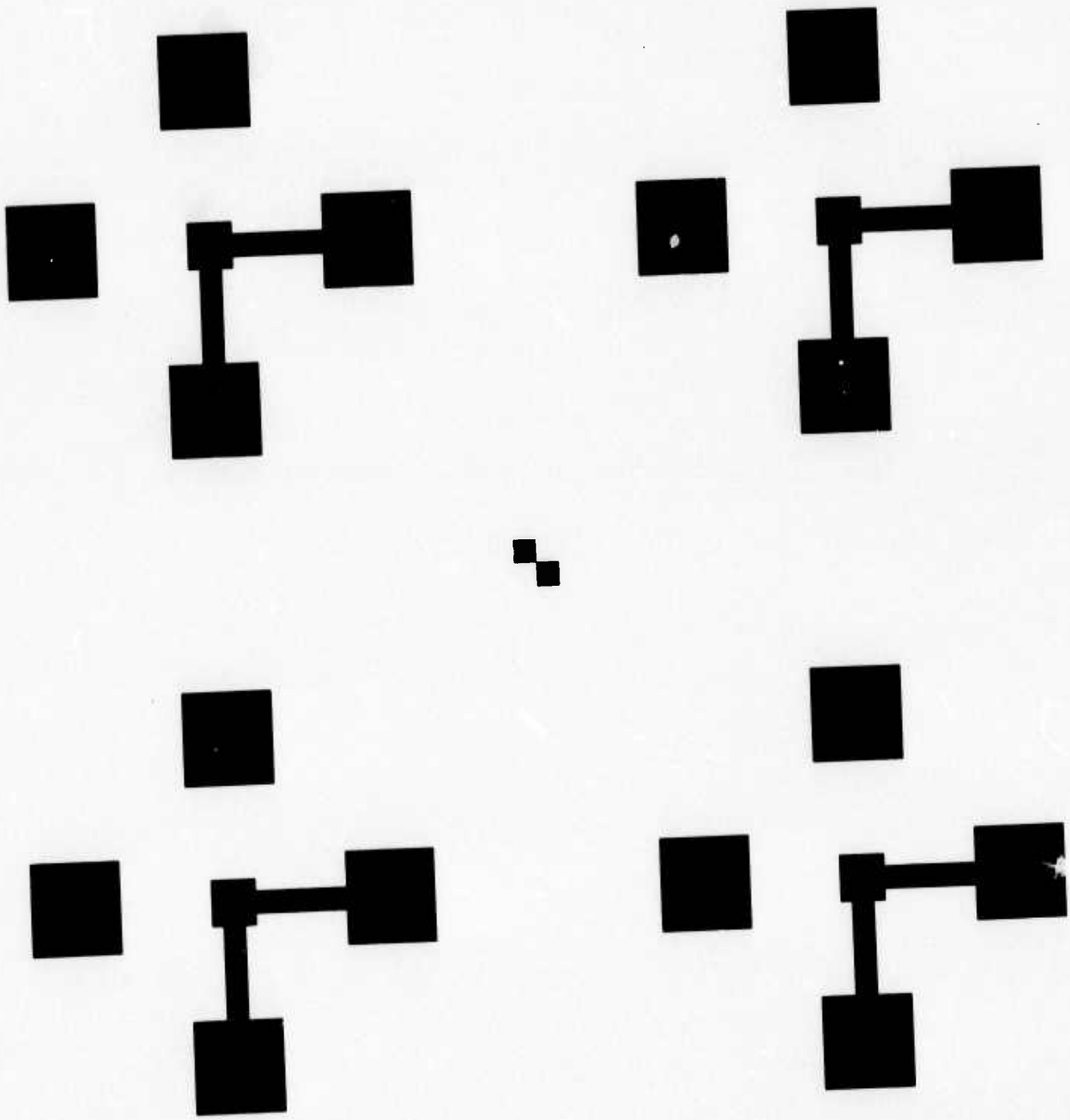


N07–34–9

metal steps over which the electromigration links can be deposited. Figure 16 shows the metal pattern used to measure metal-to-metal contact resistance at oxide feed-through holes. The metal pattern produced on the first metal level is covered by sputtered silicon dioxide and the same pattern rotated by 180° is produced in a second upper level of metal so that a four point measurement can be made.

FIG. 16

METAL PATTERN FOR CONTACT RESISTANCE MEASUREMENTS OF OXIDE FEEDTHROUGH POINTS



N07-34-10

4.1.2 Silicon Dioxide Deposition

The silicon dioxide deposition process required optimization with respect to several parameters. Magnetic field, argon pressure, rf power to the cathode or target, and substrate temperature were the obvious parameters. The magnetic field served to confine the discharge during sputtering, thus increasing the deposition rate and offering a means of improving uniformity.

Optimization of the magnetic field profile for thickness uniformity was accomplished by varying the distance from the face of the cylindrical permanent magnets with respect to the six inch dia. silica target was chosen which gave best uniformity of deposition across the substrates. The radial and axial components of the magnetic field were measured as a function of distance from the axis of the magnet in several planes above the face of the magnet. The SiO_2 thickness profile for a target to substrate distance of 2.5 cm and a target to magnet face distance of 9.9cm is shown in Fig. 17. SiO_2 thickness was determined by etching diametral sections in the SiO_2 layer and measuring SiO_2 step height with a Taylor-Hobson Taly Surf. 4. The accuracy-repeatability limitations of this instrument are approximately the same as the deviations from the average thicknesses indicated in Fig. 17. Magnetic field profiles are shown in Figs. 18 and 19.

With the optimized magnetic field profile with respect to the target and best placement of the substrate holder for uniform thickness across several substrates, a parametric study was conducted to find the effects of power, argon pressure and substrate temperature on the deposition rate. These effects are shown in Figs. 20, 21 and 22. Temperature of the substrates was maintained by coating the obverse surface of the substrates with gallium and placing them in contact with a temperature-controlled copper block. The block temperature was maintained by using gaseous nitrogen cooling through channels in the block and electrical resistance heaters driven by a Wheelco controller. Some details of the construction of the heater block, substrate holder with the configuration of the pedestals, as well as the sputtering cathode are shown in Appendix A along with a complete description of the procedure used in applying the gallium and that used for "taping" to remove strongly adherent particulates from the substrate.

It is to be noted that argon pressure and rf power to the cathode have the greater effects on deposition rate. Significant variations in deposition rate with temperature are seen only above 200°C (Figure 22). The peaking seen in the pressure versus deposition rate plot in Fig. 21 points up a problem and presents a solution as well.

At lower argon pressures, one can see pressure control to be very critical in accurately fixing deposition rate. Near 10μ of argon pressure, however, the change in deposition rate with pressure is small and an operating point for best control is thus suggested to lie in this neighborhood.

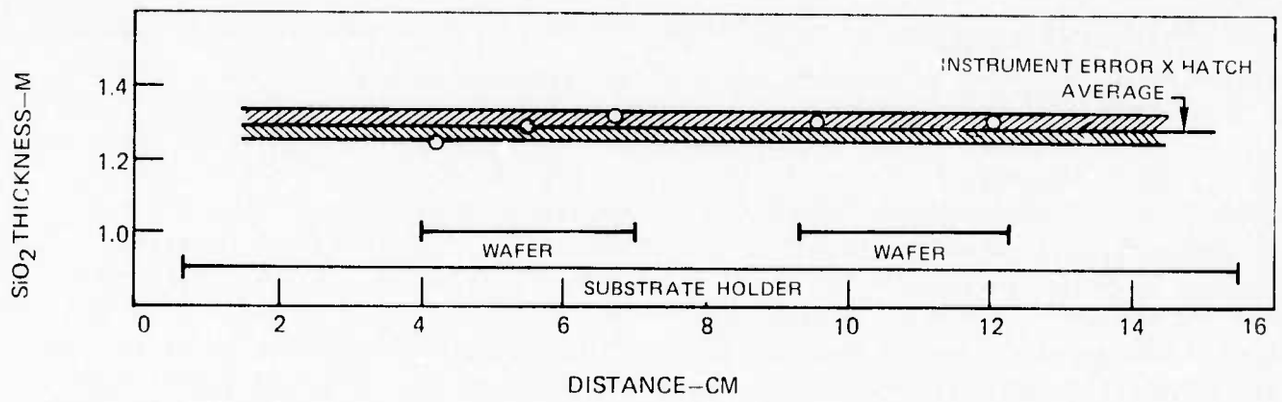
FIG. 17

THICKNESS DISTRIBUTION ACROSS SUBSTRATE HOLDER

POWER 600W

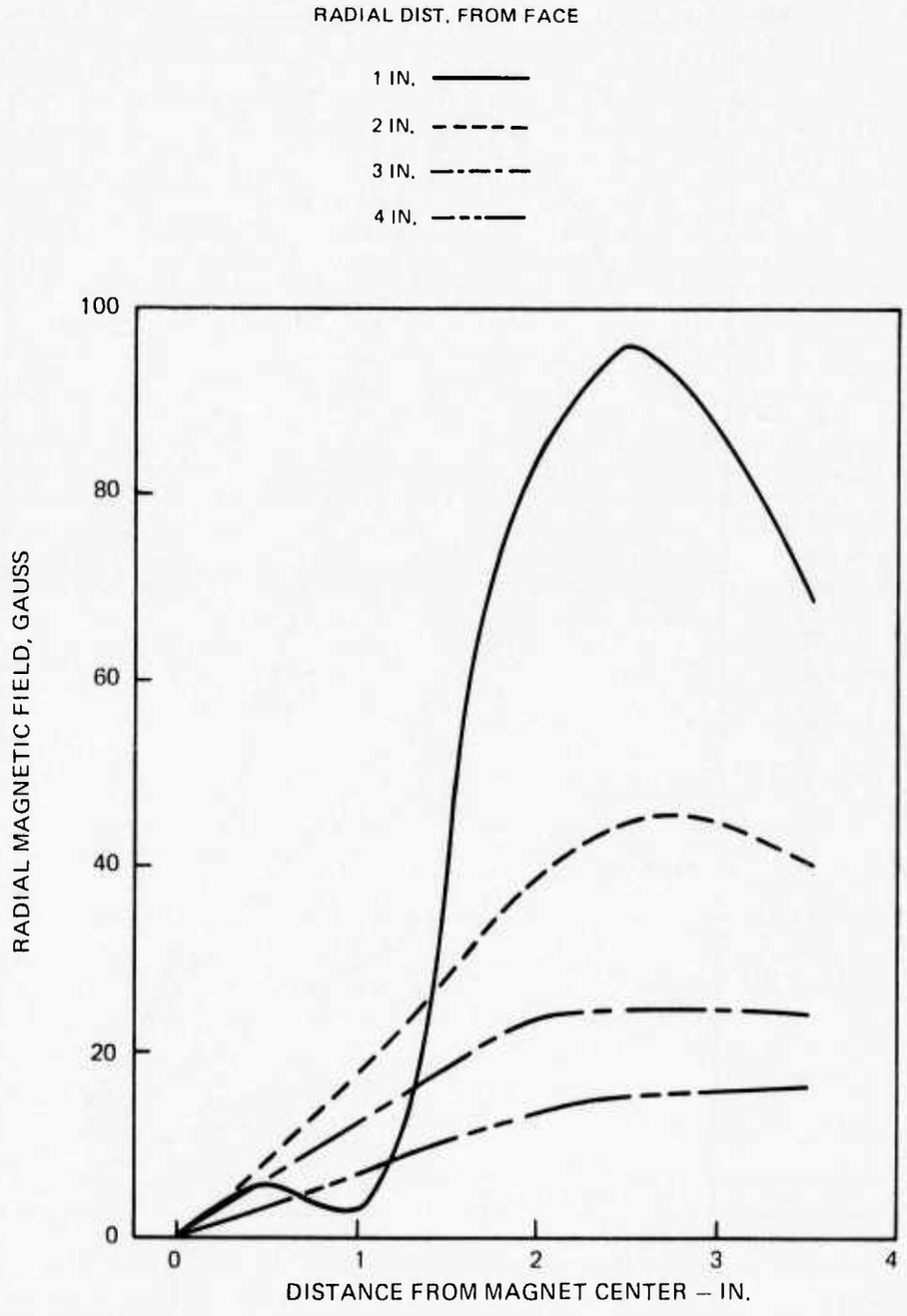
PRESSURE 6μ

TEMPERATURE 200°C



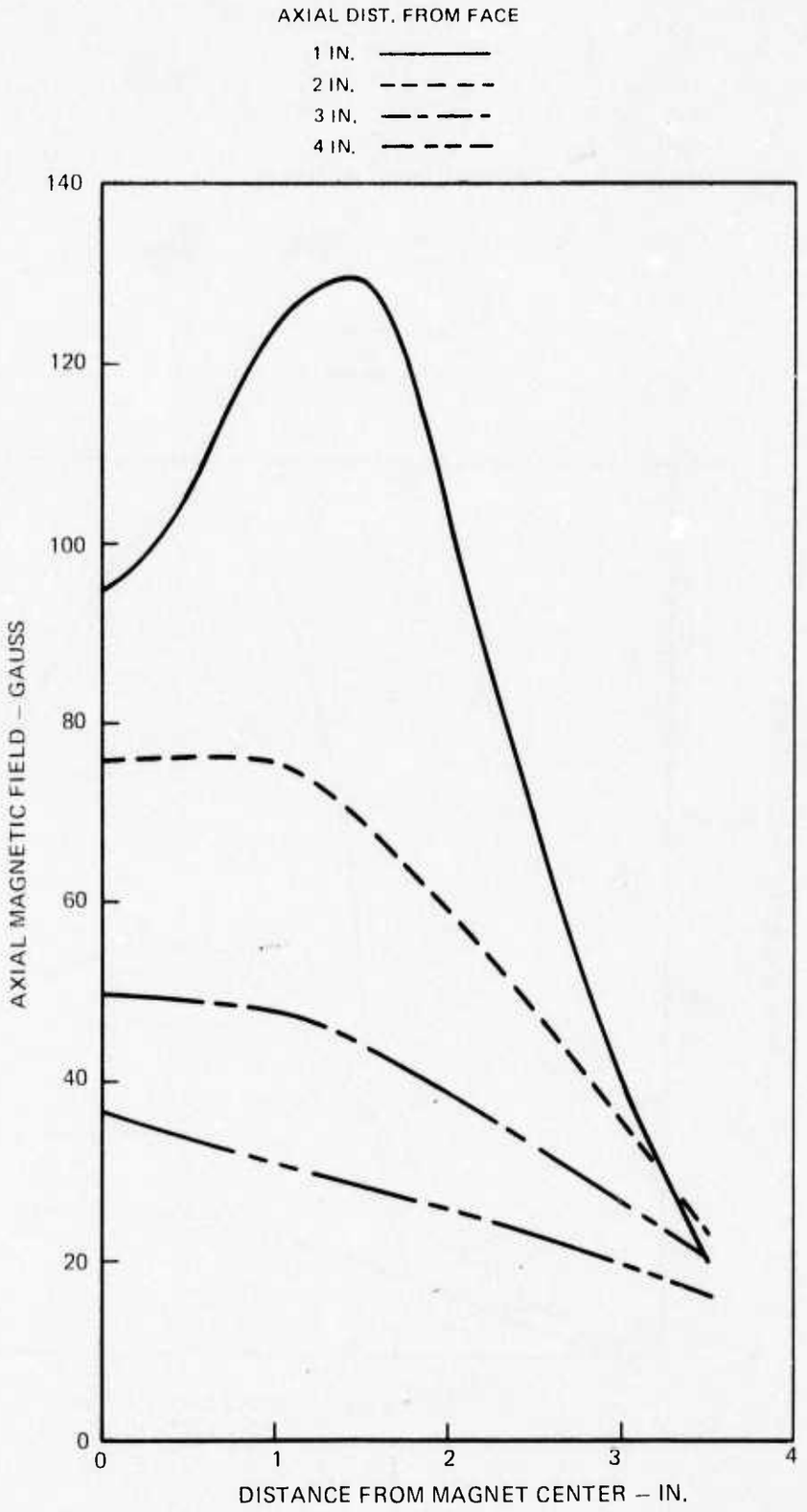
N03-287-1

FIG. 18



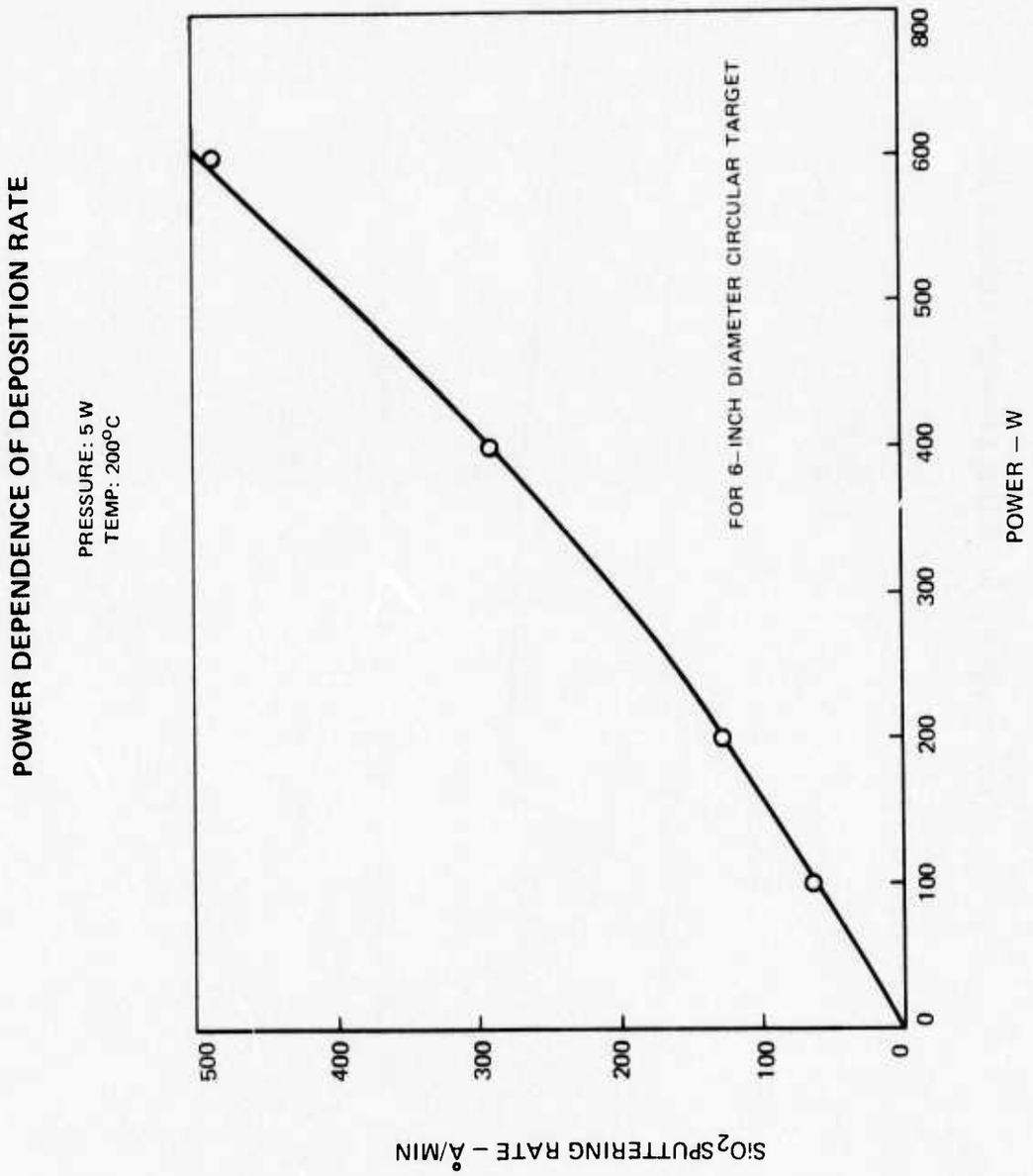
N03–227–1

FIG. 19



N03–227–2

FIG. 20

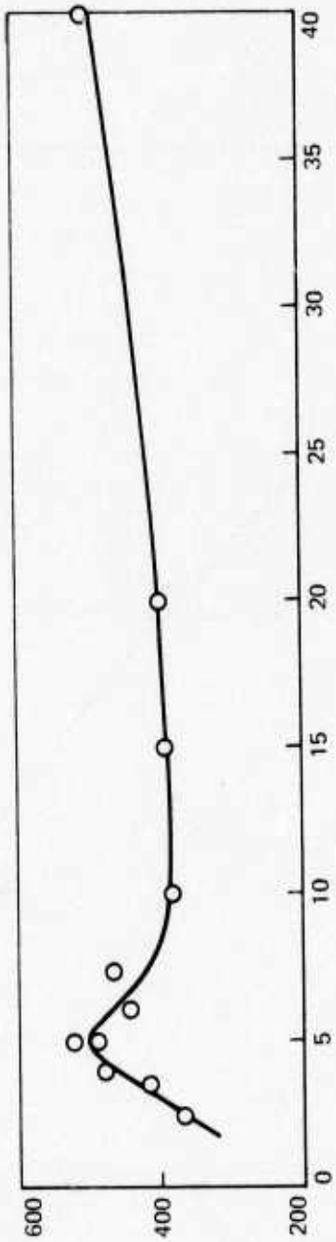


N03-227-6

FIG. 21

PRESSURE DEPENDENCE OF SPUTTERING RATE

P = 600 W
T = 200°C



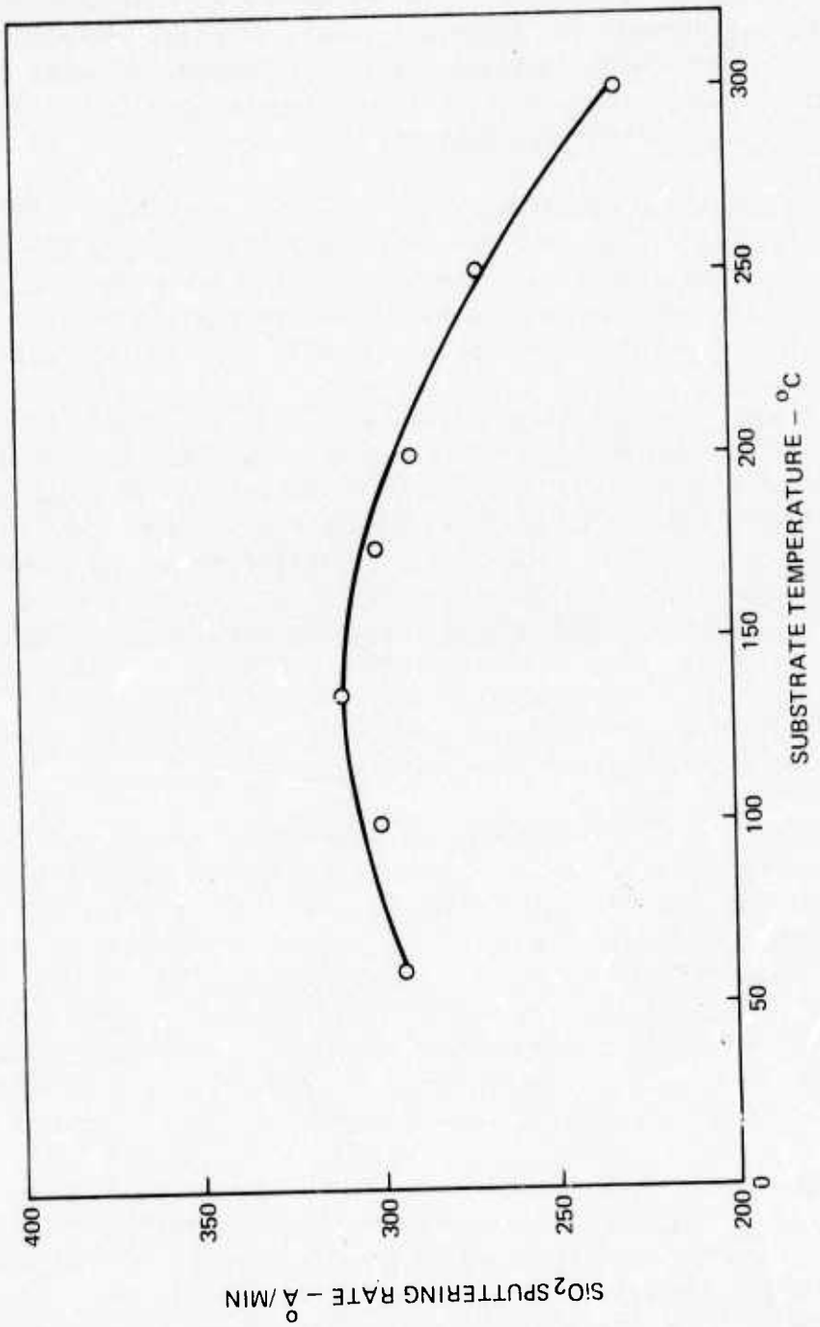
SiO_2 SPUTTERING RATE – Å/MIN

BJ PRESSURE, μ

N03-227-5

FIG. 22

TEMPERATURE DEPENDENCE OF DEPOSITION RATE



N03–250–2

The films deposited in the parametric study were evaluated for etch rate, perhaps the most important single property of the insulator film in a multilevel interconnect technology. The basis for this statement is in the data presented here and the further observation that both aluminum and aluminum oxide may be attacked by the buffered hydrofluoric acid solutions used in etching feedthrough holes in the silicon dioxide. Feedthrough holes are needed so that continuity can be established where required between two different levels of metal interconnect. A precisely controlled uniform SiO_2 etch rate is thus necessary to avoid the danger of destroying the aluminum pad at the bottom of a feedthrough hole or of introducing a reliability problem or a high resistance contact.

Below 10μ argon pressure, Figs. 23 and 24 show only slight dependence of etch rate on pressure for two etches--one, the 7.5:1 buffered hydrofluoric acid solution normally used for feedthrough etching and, the other, p-etch used for diagnostics etching. Note that the two figures appear nearly identical except for a scale change. (See Appendix B for silicon dioxide etch procedure.)

In Figs. 25 and 26 is presented etch rate as a function of power for a fixed pressure of the sputtering gas. A dramatic increase in etch rate is seen for films deposited at a power input of less than 200 watts. This may perhaps be better described as a deposition rate dependence since lower power input results in a slower deposition rate. This very sharp increase may be related to the trapping of the sputtering gas in the deposited film. As the ratio of rate of arrival of sputtered species to gas pressure (or argon arrival rate) increases, the trapped gas content of the film should decrease, producing a denser, slower etching structure. This can be qualitatively compared to Fig. 24 for the etch rate dependence on argon pressure at fixed power. This suggests an optimum power input of ≈ 400-600 watts for useful films with well-controlled etch rates.

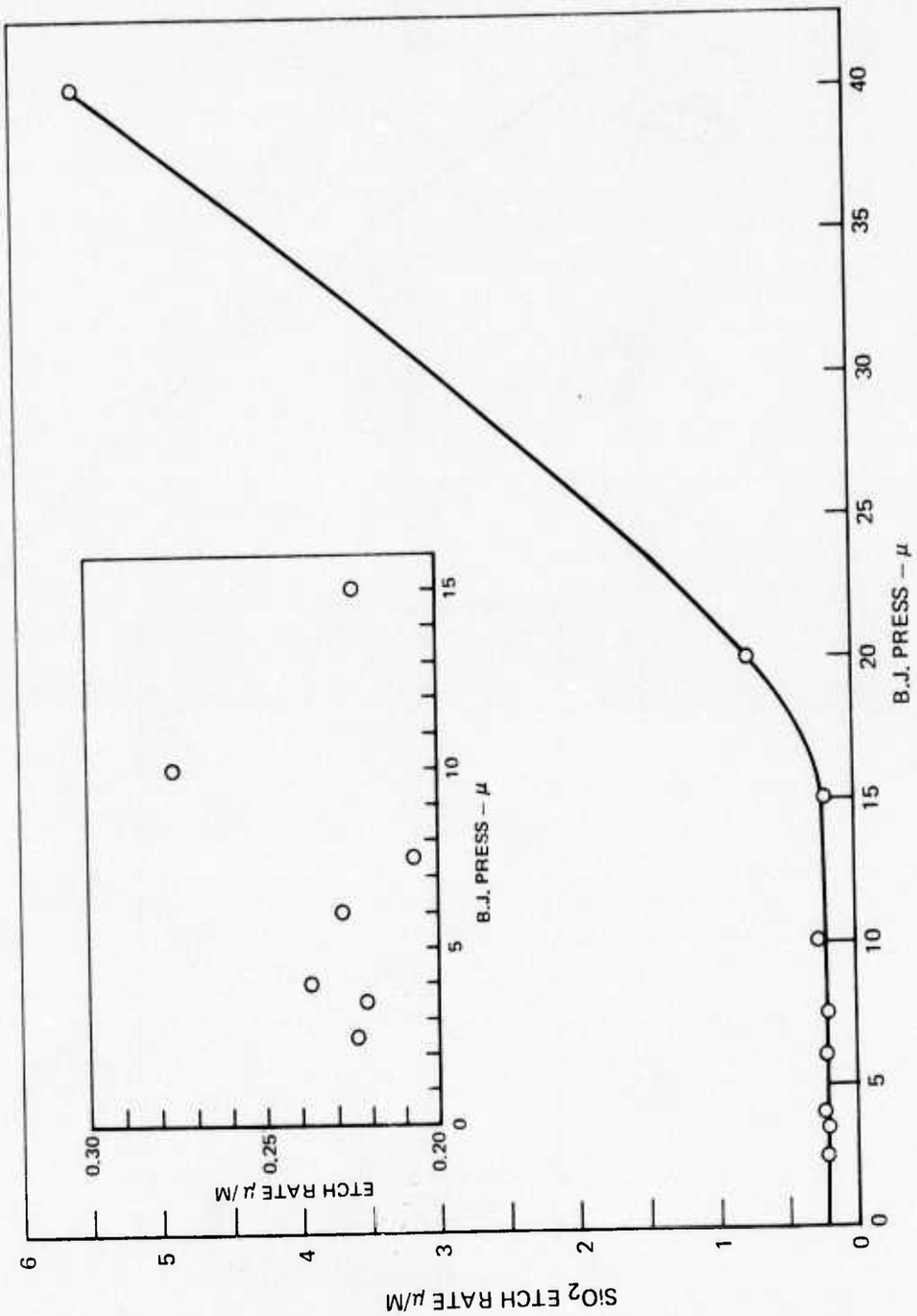
Figure 27 shows optical photomicrographs of etched surfaces of silicon dioxide characteristic of films deposited at high pressure (15μ or greater) compared to films from lower pressure depositions. Note the severe pitting of the etched surfaces for the high pressure films. These photos support the idea of local gas trapping under high pressure conditions and point up the need for controlling this parameter to the appropriate range. The nonplanar nature of an etch front progressing through the films would lead to excessively prolonged etchant attack on portions of an aluminum contact at the bottom of a feedthrough hole while other portions were cleared of slower etching silicon dioxide.

It can be seen that the best conditions for silicon dioxide deposition which can be used in the range of parameters reported here are 200°C substrate temperature, 5 to 10 millitorr argon pressure, a power to the rf cathode greater than 200 watts (a power density greater than 6.5 or 7.0 watts/in^2), and a source-to-substrate separation of 2.5cm (this separation is, of course, somewhat dependent on the magnetic field profile and is somewhat unique to the field shown mapped earlier in this report).

FIG. 23

PRESSURE DEPENDENCE OF SiO_2 ETCH RATE

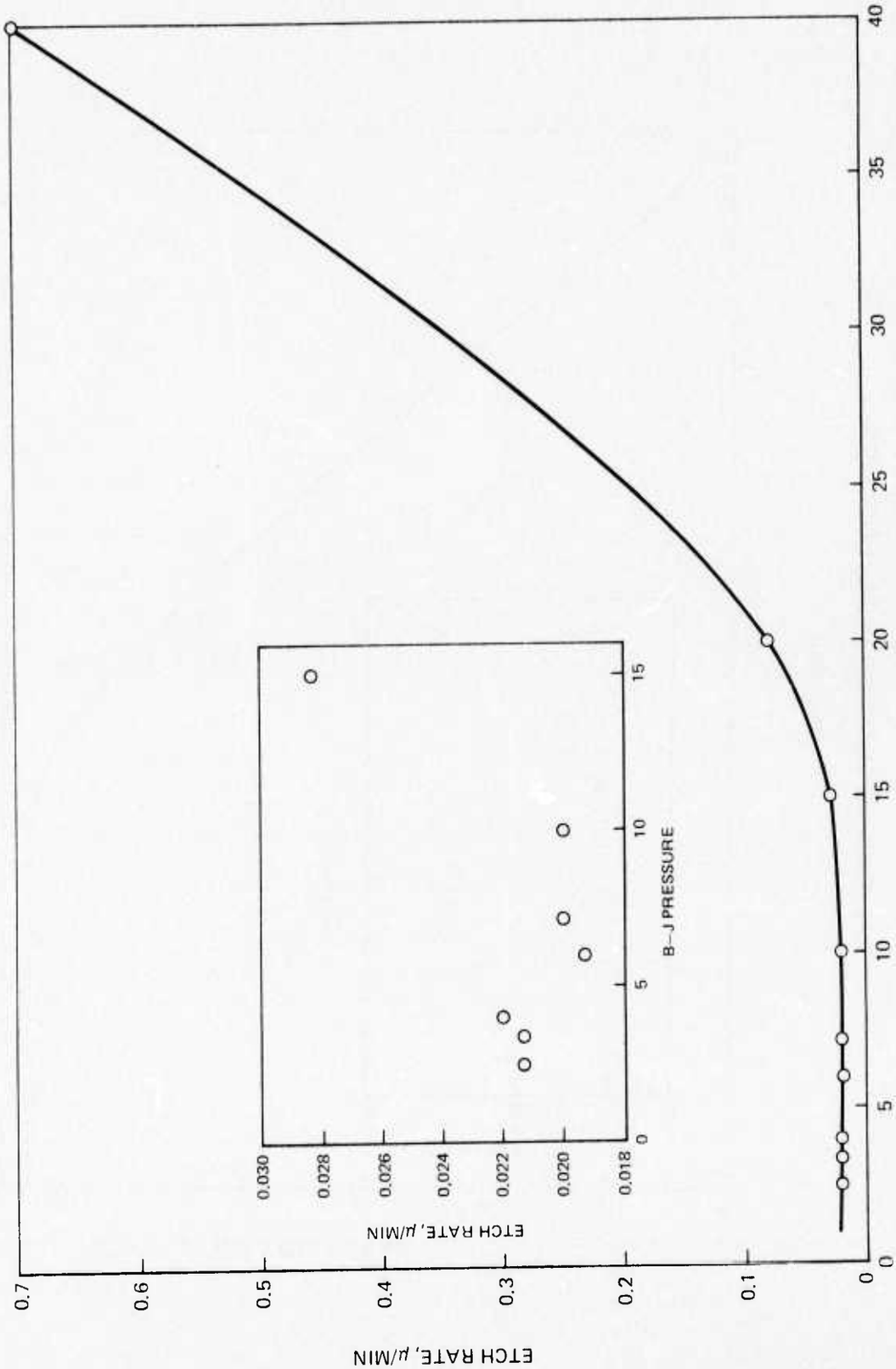
POWER 600 W



N03–227–3

FIG. 24

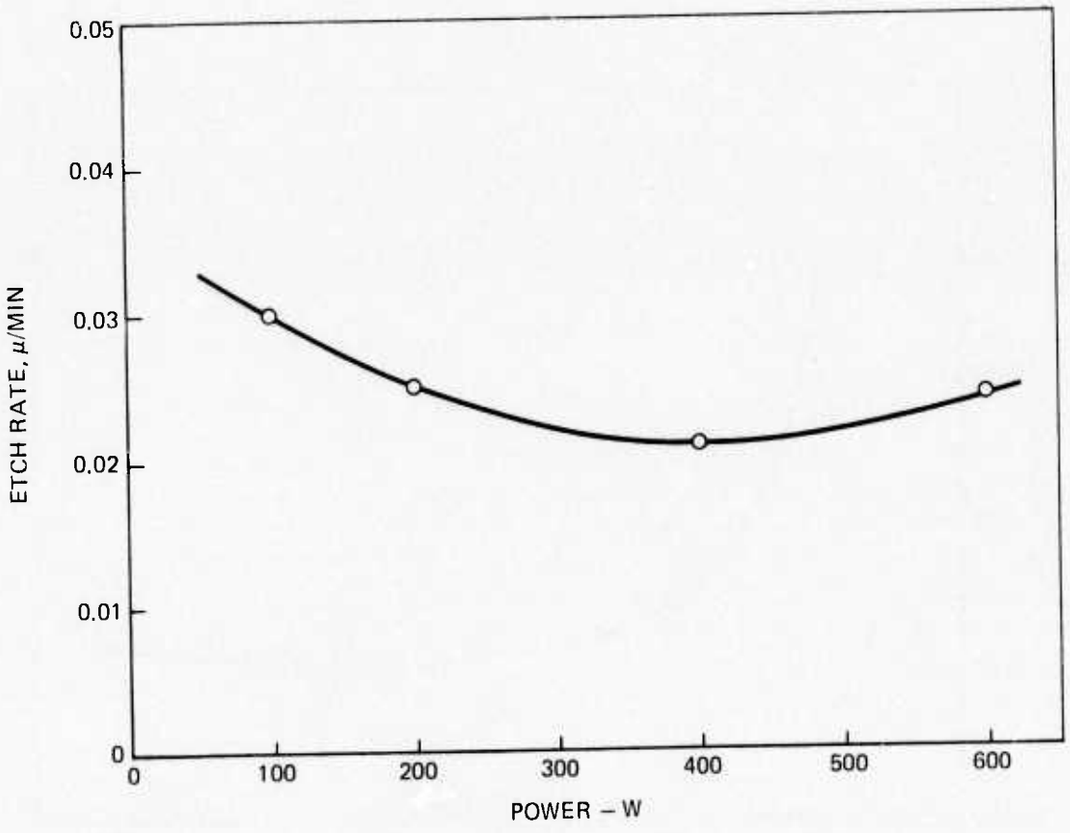
PRESSURE DEPENDENCE OF SiO_2 ETCH RATE IN P–ETCH



N03–250–4

FIG. 25

POWER DEPENDENCE SiO_2 ETCH RATE IN P-ETCH

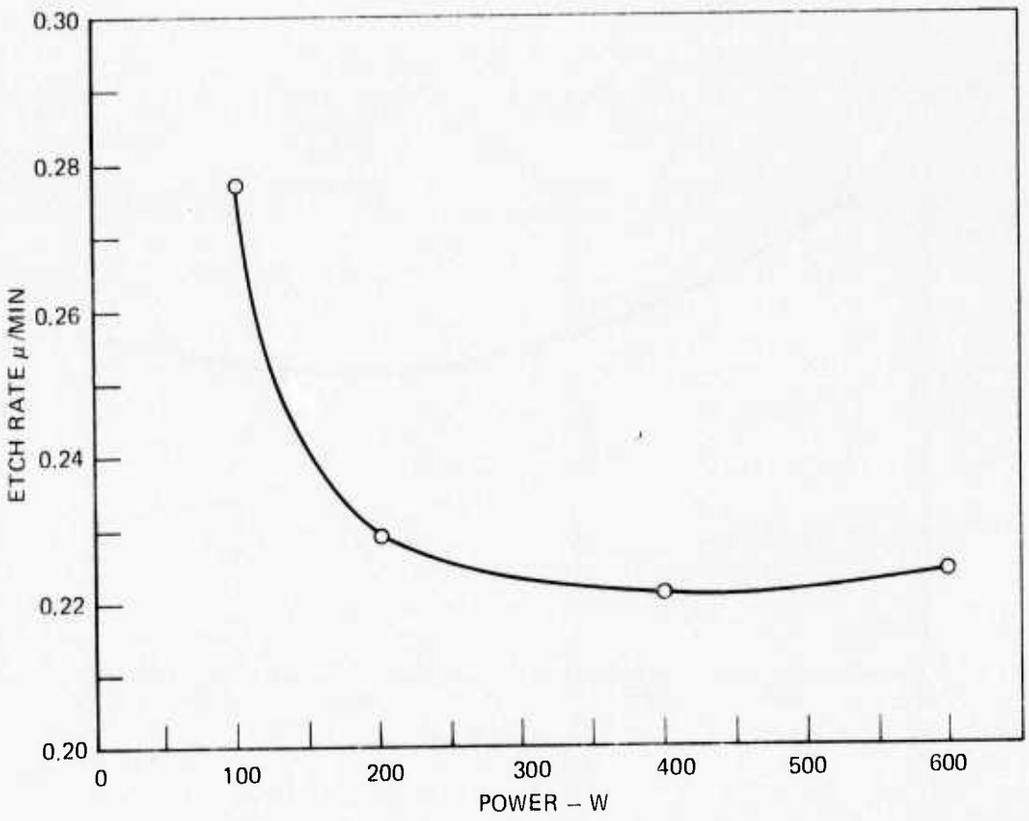


N03-250-3

FIG. 26

POWER DEPENDENCE S_iO_2 ETCH RATE

PRESSURE 5 μ



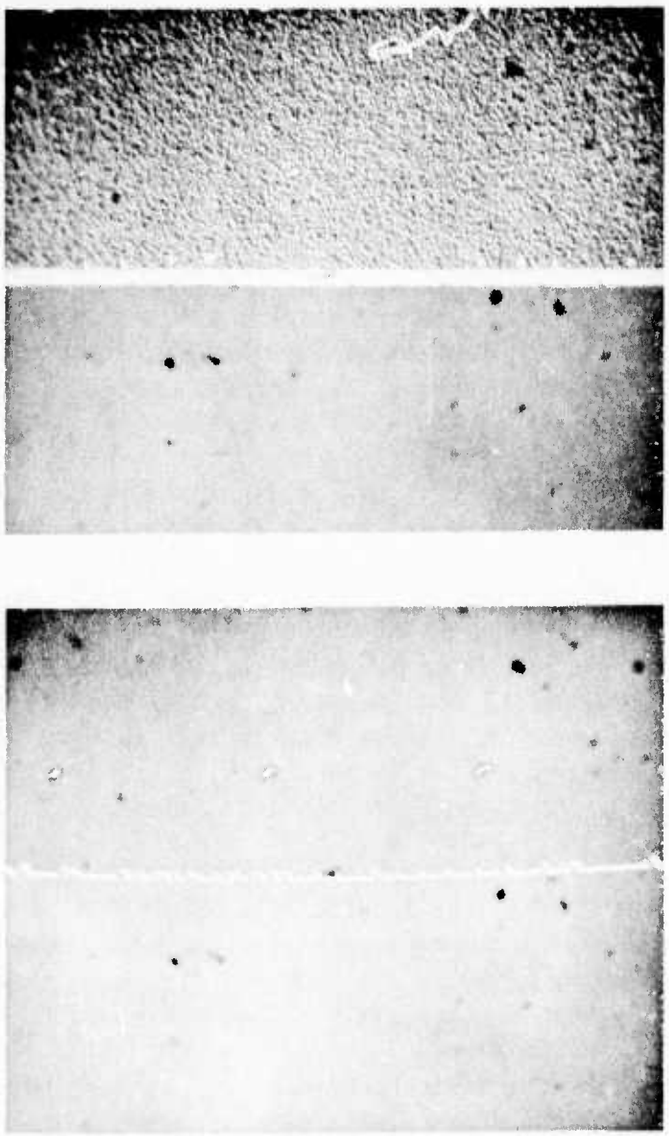
N03-227-4

TYPICAL APPEARANCE OF SPUTTERED SiO_2 AFTER PARTIAL ETCHING IN BUFFERED HF

a) OXIDE DEPOSITED AT ARGON PRESSURE 15 MICRONS AND HIGHER

c) OXIDE DEPOSITED AT ARGON PRESSURE 10 MICRONS AND LOWER

b) & d) UNETCHED SURFACES



a)

b)

c)

d)

4.1.3 Metal Deposition

Turning now to the metal deposition, the same sputtering parameters need attention as for sputtering silicon diozide. Sputtering was chosen because of the recognized need for a low temperature metal film deposition process which could give good adhesion on substrates which would not later be subjected to a high temperature alloying or sintering operation. Thermally evaporated films deposited in vacuo in general do not adhere well to substrates which are not glow discharge cleaned or held at some elevated temperature (~300°C) for some time. Either of these techniques is difficult to implement while maintaining film thickness uniformity during evaporation. The higher deposition temperature has the added disadvantage of leading to rough granular surfaces.

In Figs. 28(a) - 28(g) are shown aluminum deposition uniformity curves for several pressures at source-to-substrate separations ranging from $1\frac{1}{8}$" to $1\frac{5}{8}$". Figure 29 shows deposition rate as a function of pressure at $1\frac{3}{8}$" source-to-substrate separation. The range of pressure above 5 microns has least effect on the deposition rate and suggests an operating pressure which does not impose excessive requirements on the controlling gear required for maintaining fixed pressure. Using known rate data and time of deposition reasonably accurate reproducible film thickness may be achieved without the need for complex film thickness monitors operating in the glow discharge.

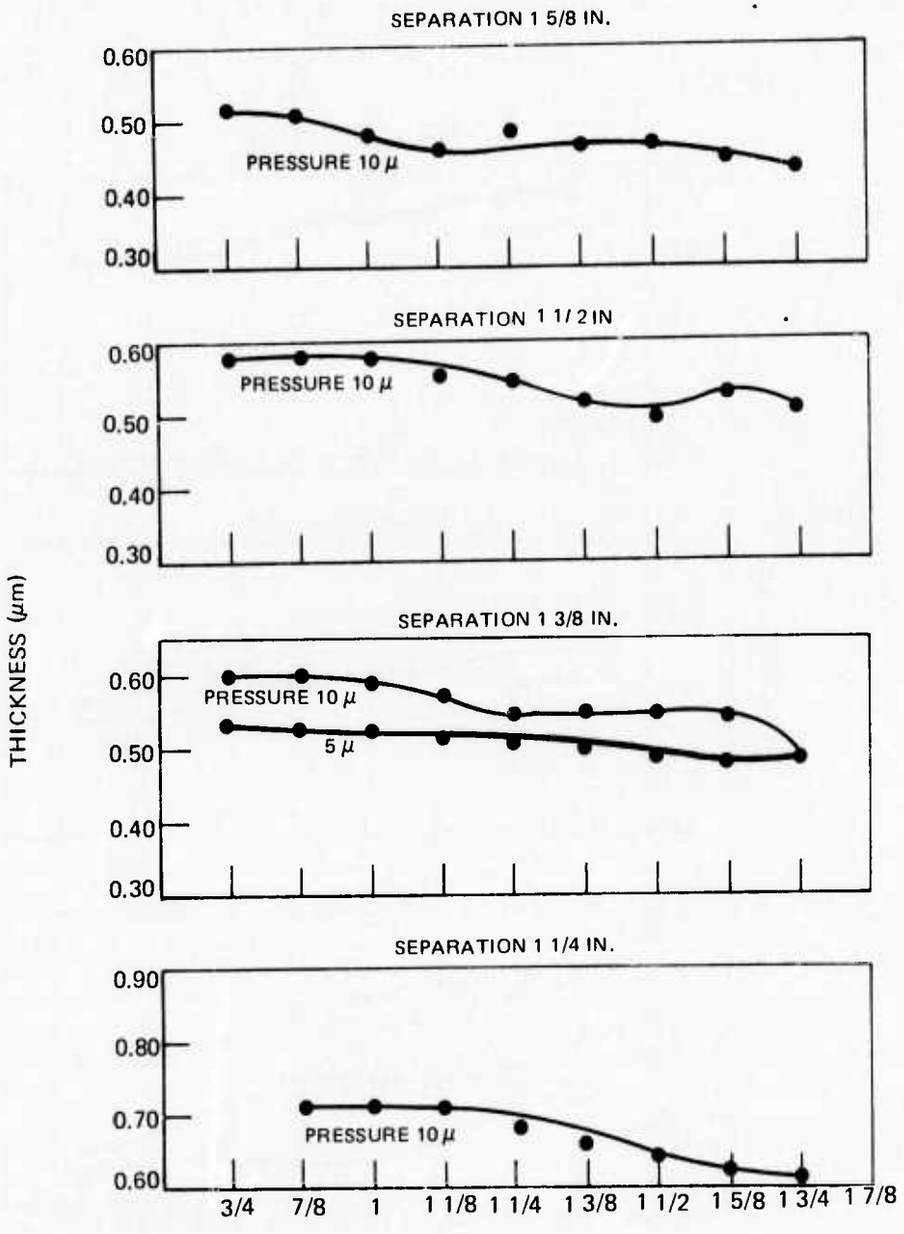
Figure 30(a), 30(b) and 30(c) show replication electron micrographs of the surfaces of aluminum films deposited at three pressures. Note the almost featureless character of the films deposited at 2.5 microns and at 25 microns of pressure. The metal atoms arriving at the substrate through a 25 micron ambient suffer enough collisions with the argon gas atoms to lose most of the energy acquired from the sputtering process to essentially freeze in place on striking the substrate. Grain growth and development of structure is greatly retarded. On the other hand, at the lower pressure the aluminum atoms arriving at the substrate have lost virtually none of their energy in transit and are able to disrupt any structure formation or grain growth in the aluminum already on the substrate. Note the detailed replication of a substrate defect shown in Fig. 30(c).

Because of the extremely small grain size in the aluminum films (all discussed in this report were deposited at room temperature), a series of surface etches were performed to delinate any structure present and to infer something of the grain size. Keller's Reagent, a 0.5% hydrofluoric acid etch and sputter etching were used and surface replicas of the etched films are shown in Figs. 31, 32, and 33. Both Keller's Reagent and the HF solution develop film structure rather strongly and imply, again, smaller grains and more homogeneous deposits for the higher pressure deposits. Sputter etching--the results of which are shown in Fig. 31--is far more demoncratic. The much more uniform, almost featureless, surface presented in Fig. 31 supports the use of sputter cleaning as a technique for removing residual insulator from the aluminum pad at the bottom of a feedthrough hole before depositing a contacting layer of metal. For virtually no change in deposition conditions from that employed in aluminum depositions, the alloy aluminum -4% copper yields smooth fine grained structures equal to aluminum. Figure 34 shows an optical photomicrograph of a

FIG. 28 (a) (b) (c) (d)

ALUMINUM FILM UNIFORMITY

POWER 500 W

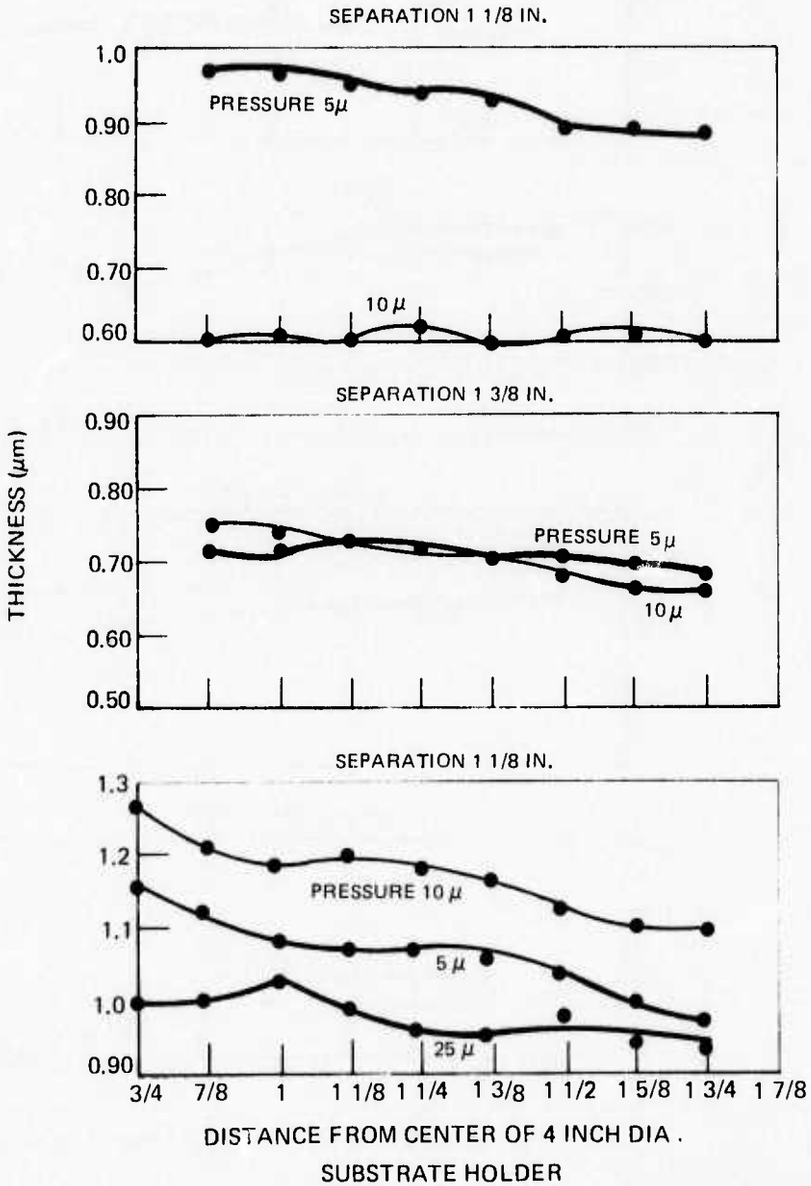


N07–34–1

FIG. 28 (e) (f) (g)

ALUMINUM FILM UNIFORMITY

POWER 500W

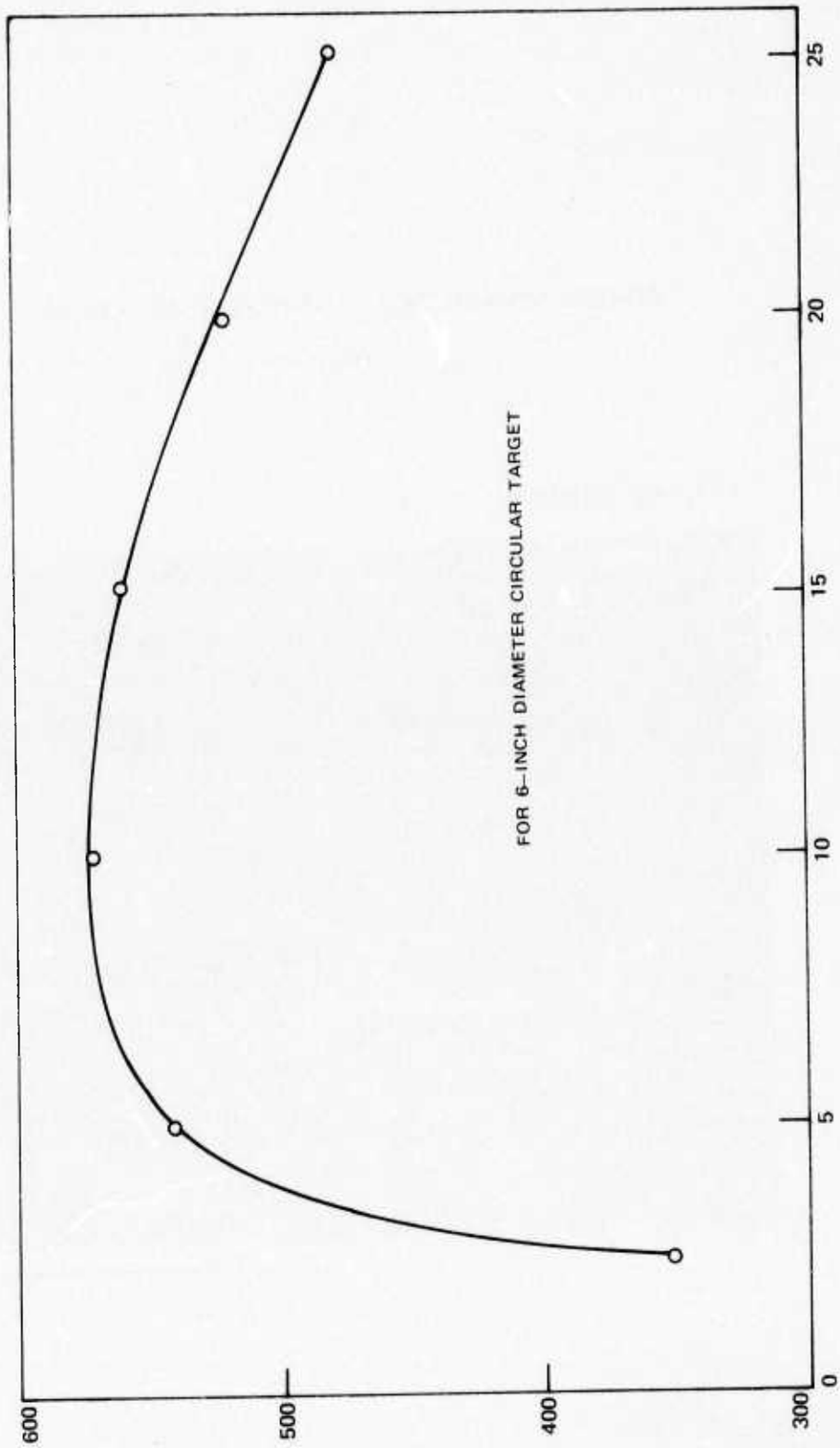


N07–34–3

FIG. 29

ALUMINUM DEPOSITION RATE VS. PRESSURE

TARGET TO SUBSTRATE SEPARATION 1 3/8 IN.
POWER 500 W RUN TIME 10 MIN



N07–34–2

FIG. 30 (a

SURFACE CHARACTER OF AS DEPOSITED Al FILMS

REPLICA ELECTRON MICROGRAPHS

(a) SPUTTERING PRESSURE 25 μ Ar

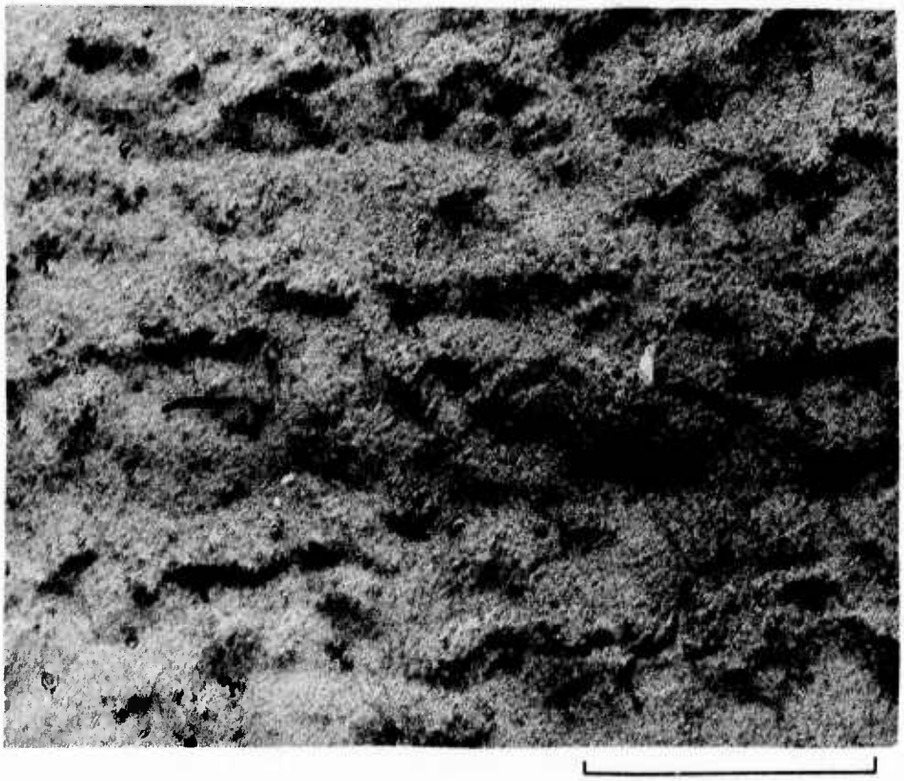
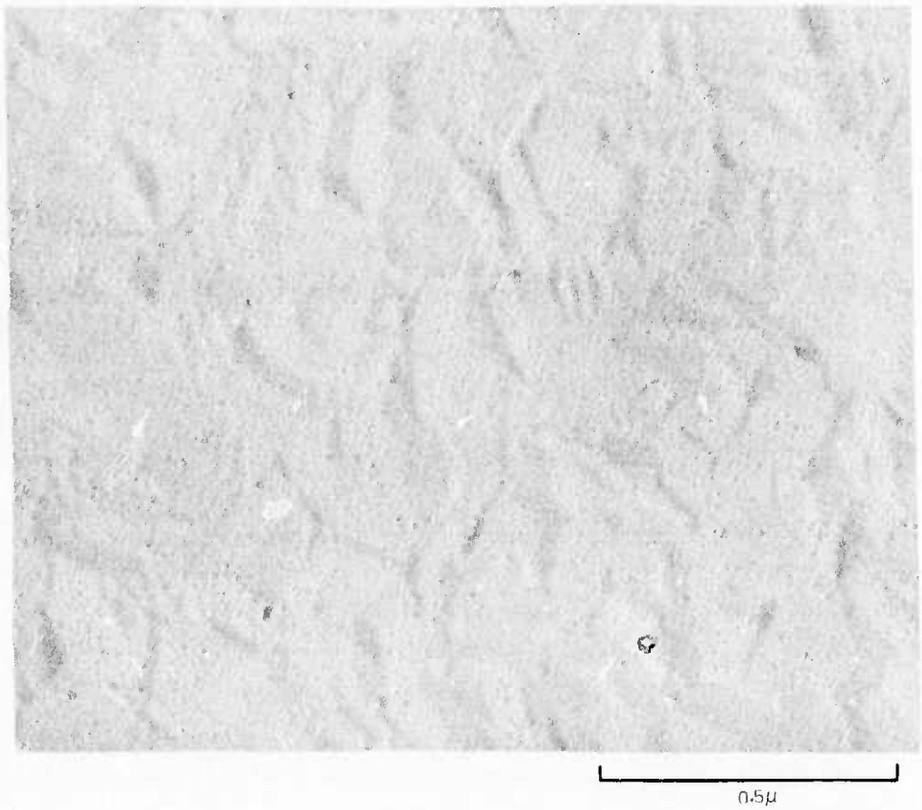


FIG. 30(b)

SURFACE CHARACTER OF AS DEPOSITED Al FILMS

REPLICA ELECTRON MICROGRAPHS

(b) SPUTTERING PRESSURE 10 μ Ar



N07–34–13

FIG. 30(c)

SURFACE CHARACTER OF AS DEPOSITED Al FILMS

REPLICA ELECTRON MICROGRAPHS

(c) SPUTTERING PRESSURE 2.5 μ Ar

NOTE REPLICATION OF SUBSTRATE IMPERFECTION

FIG. 31

COMPARISON OF STRUCTURE DEVELOPED BY VARIOUS ETCHING TECHNIQUES FOR 5μ AND 10 μ SPUTTERED Al FILMS

REPLICA ELECTRON MICROGRAPHS

SPUTTER 100W

5 μ Ar PRESSSURE

0.5μ

10 μ Ar PRESSURE

0.5μ

N07–34–4

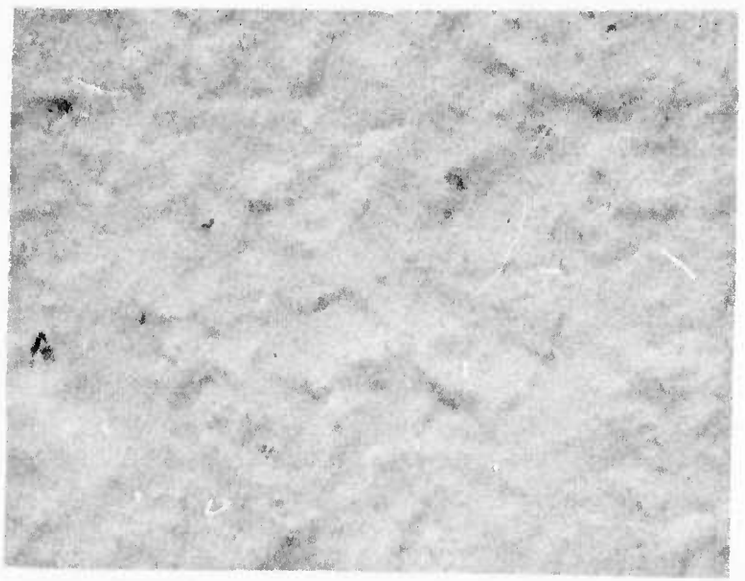
COMPARISON OF STRUCTURE DEVELOPED BY VARIOUS ETCHING TECHNIQUES FOR 5 μ AND 10 μ SPUTTERED Al FILMS

REPLICA ELECTRON MICROGRAPHS

0.5% HF

5 μ Ar PRESSURE

0.5μ



10 μ Ar PRESSURE

0.5μ

N07–34–11

N921820–4

COMPARISON OF STRUCTURE DEVELOPED BY VARIOUS ETCHING TECHNIQUES FOR 5 μ AND 10 μ SPUTTERED Al FILMS

REPLICA ELECTRON MICROGRAPHS

KELLER'S REAGENT

5 μ Ar PRESSURE

0.5μ

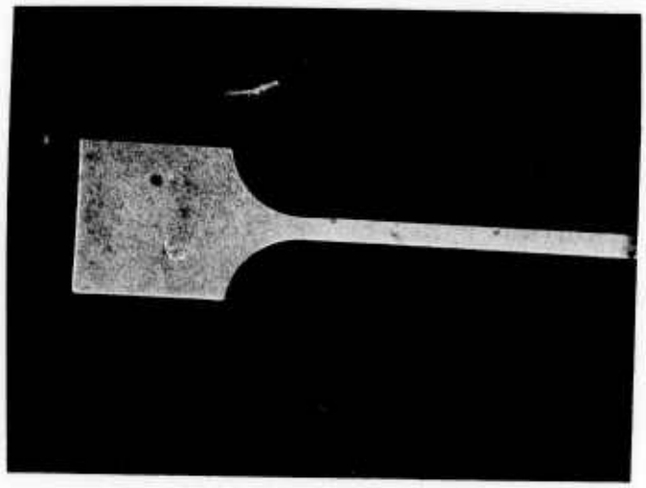
10 μ Ar PRESSURE

0.5μ

N07–34–12

FIG. 34

ELECTROMIGRATION TEST BAR



pattern etched in aluminum. Increasing the magnification to 1000x in Fig. 35(a) brings out structure developed due to the slightly elevated photoresist processing and etching temperatures. These "hillocks" grow in size and in number with further exposure to higher temperatures (200°C for 30 minutes) as shown in Figs. 35(b), 35(c), and 35(d). Note the spherical sections constituting the hillock geometry and the apparent depressions around the hillocks, possibly the result of metal migration into the hillock area from the immediate neighborhood.

It should be noted that the hillock growth is not a highly reproducible phenomenon. The numbers of these features per unit area and the size distribution vary from deposition-to-deposition. Some forty depositions were monitored by residual gas analysis of the vacuum chamber ambient just prior to initiation of the deposition and immediatly after its cessation. No specific constituent was seen to increase in concentration when hillock growth was observed. However, a general contamination background increase was always observed when hillock growth was most serious. In many cases hillock formation proceeded at room temperature in laboratory ambients. These observations strongly suggest local pollution levels will affect the surface topography of aluminum. The alloy system 4% copper in aluminum appeared to be somewhat less susceptible to the formation of the hillocks.

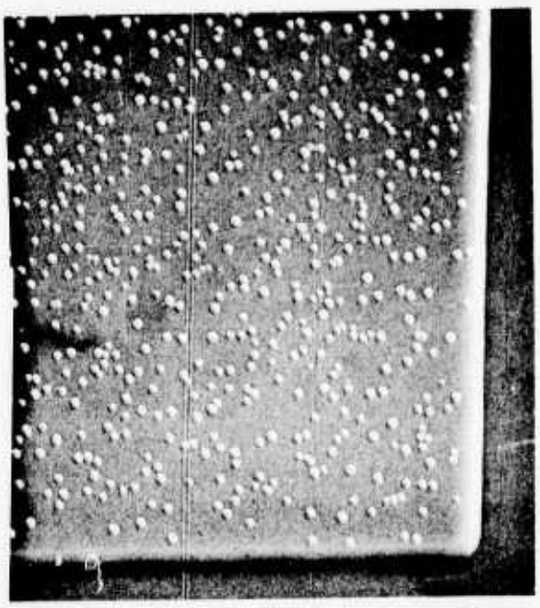
For comparisons sake, note the smooth texture of the aluminum-copper test bar in Fig. 36. This metal was deposited under the same conditions as the pure aluminum already shown and subjected to the same photoresist and etching procedures used for the aluminum. The lack of structure in the metal films is essential to smooth well defined metal edges and small geometries. On the other hand, the evaporated pure aluminum contact deposited at high temperatures and alloyed near 560°C exhibits characteristic fluting or serration of the etched edges in Fig. 37. Some of the sharp corners produced in this fluting will lead to difficulty in obtaining adequate insulator coverage of these points.

While Fig. 35 shows some of the effects of annealing aluminum at 200°C, even more dramatic changes are shown in Fig. 38 for films annealed at 535°C in nitrogen. Figure 38 shows the progressive roughening of the aluminum film and the development of some sharp edges on the large ($\sim$ 2μ diameter) hillocks formed. On the other hand, the alloy film shown in Fig. 39 does not develop the same kind of structure nor does one observe gross departures of the surface topography from the original plane.

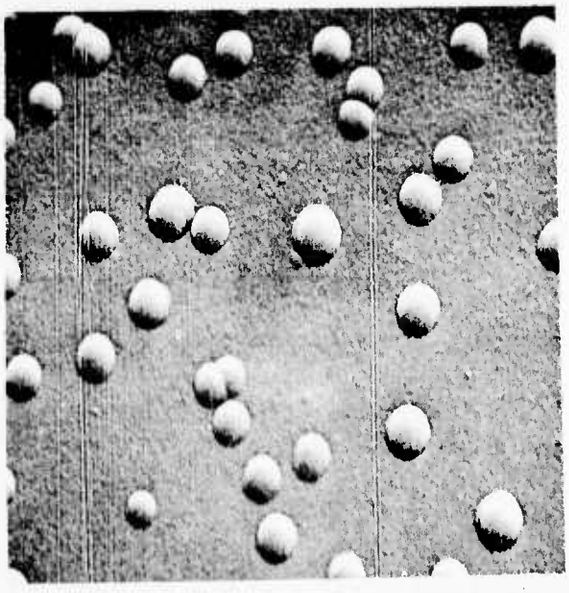
Thus, we see about the same effects of deposition parameters on aluminum -4% copper film properties as we observe for pure aluminum. A substrate temperature of 20-25°C, argon pressure during sputtering of 10 millitorr, and a source-to-substrate separation of approximately 1.12 inches produce best uniformity, smoothest films and fewest hillocks for 500 watts ($\sim$ 18 watts/inch^2) to the six inch diameter target.

SURFACE STRUCTURE IN Al

a) AFTER PHOTO–RESIST PROCEDURE 1000X SEM



b) SAME WAFER AFTER 30 MIN AT 200°C. 1000X SEM



c) SAME WAFER 5000X SEM

d) SAME WAFER, 80° TILT 5000X SEM

N10–88–7

FIG. 36

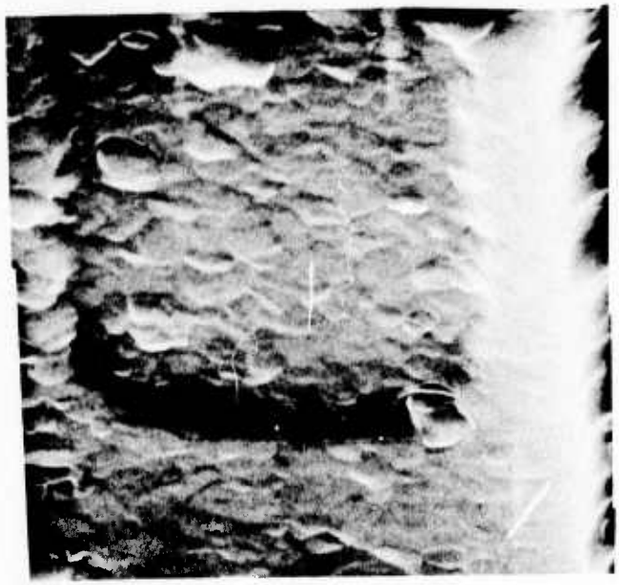
END OF TEST BAR

Al + 4% Cu 0.75 μ THICK

1000X SEM

EVAPORATED AND ALLOYED Al INTERCONNECTION

FLUTED EDGE CHARACTERISTICS OF EVAPORATED Al

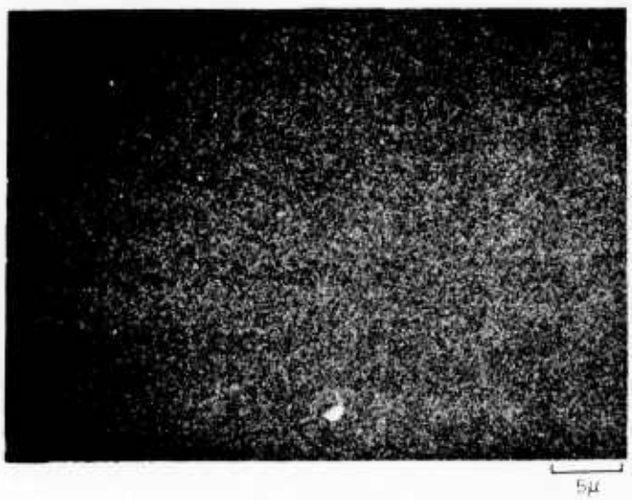


6000X SEM

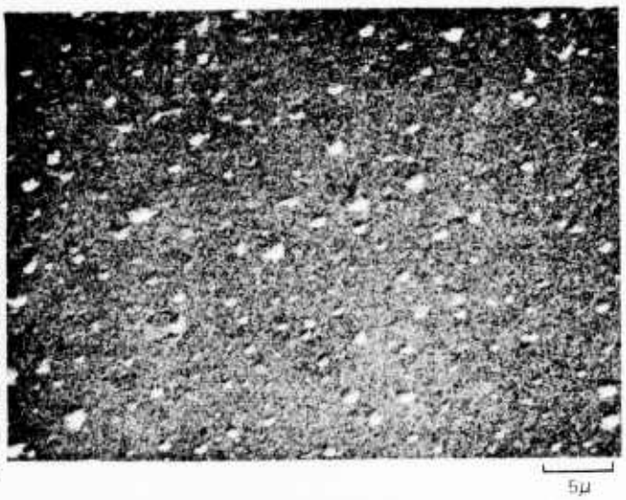
FIG. 38

Al FILMS

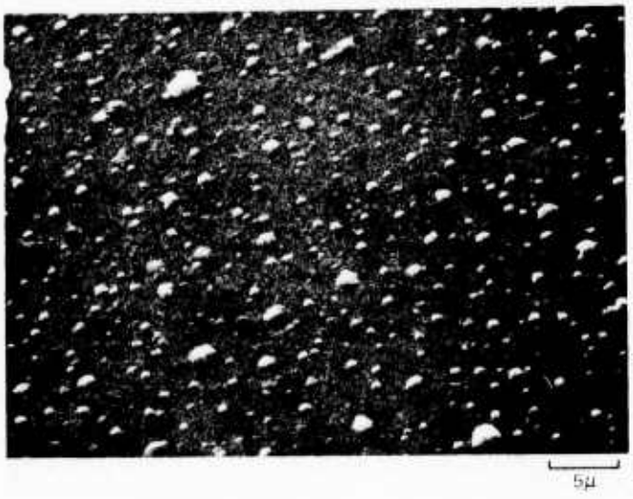
A. AS DEPOSITED – SEM



B. ANNEALED 5 MIN AT 535°C – SEM



C. ANNEALED 15 MIN AT 535°C – SEM

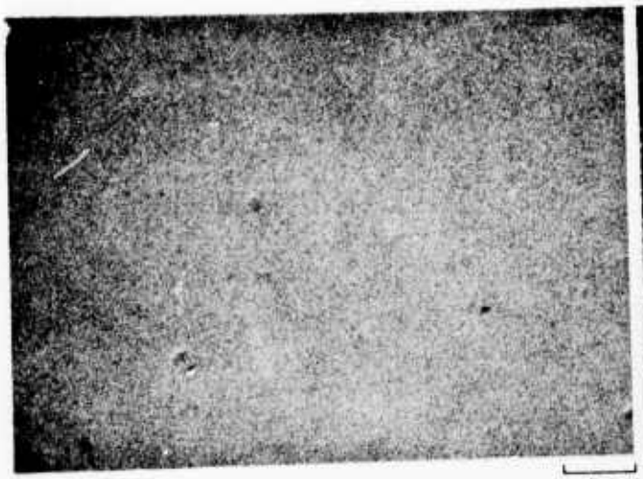


N11-170-11

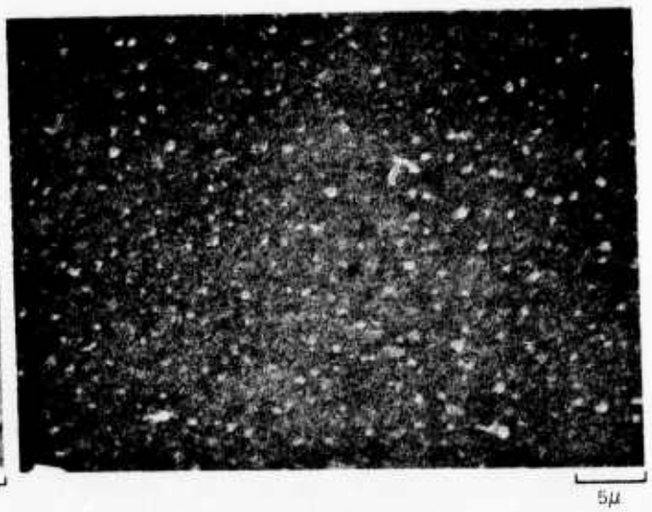
FIG. 39

Al + 4% Cu FILMS

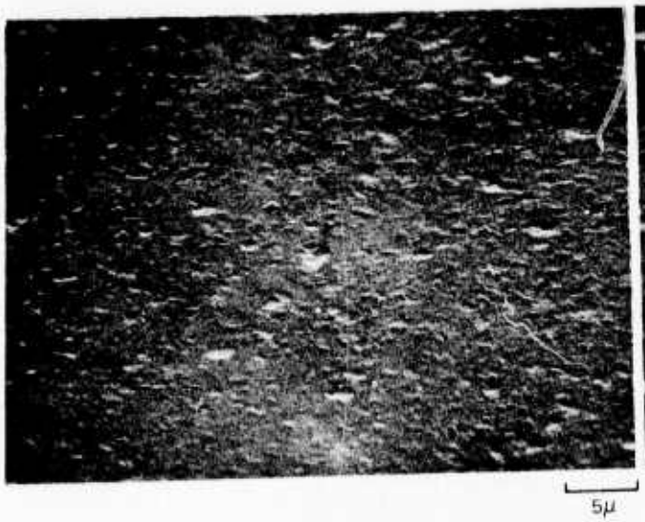
A. AS DEPOSITED – SEM



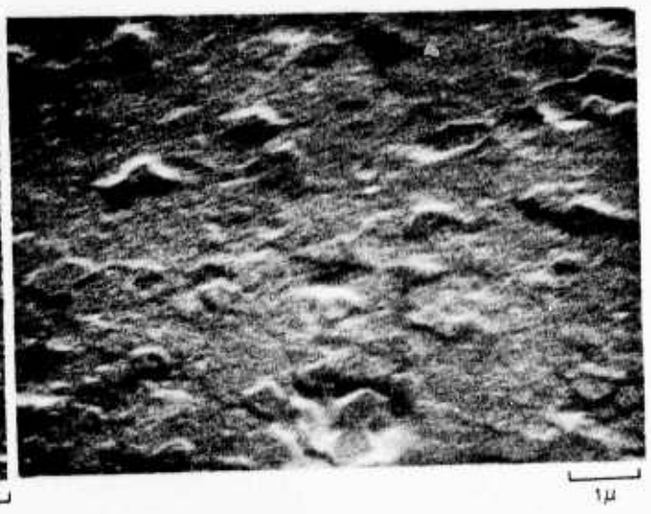
B. ANNEALED 5 MIN AT 535°C – SEM



C. ANNEALED 15 MIN AT 535°C – SEM



D. ANNEALED 15 MIN AT 535°C – SEM



N11–170–13

4.1.4 Electromigration Evaluation

Electromigration depends on both temperature and current density in the metal films. The near exponential dependence of life of a metal test piece on each of these parameters dictates that tests in limited time frames be conducted at high temperatures and at high current densities. Further, the phenomena associated with this mode of failure may be poly-mechanistic with one or the other mechanism predominating at different temperatures or current density levels. With these limitations in mind the evaluations of aluminum and 4% copper in aluminum were conducted at as low temperatures and as low current density as possible to still permit significant data accumulation during the course of this program.

In order to determine order of magnitude for current stress levels , a number of cells were stressed until one of the ten 0.001 inch by .010 inch bars in each cell failed (see Fig. 40). Cell dimensions were chosen to give large current density at reasonable currents. All cells were defined by chemical etching (see Appendix C) and the bars were then measured (thickness and width) to determine the true cross-sectional area. Figure 41 shows a portion of such an overstressed pure aluminum cell, one failed bar and two incipient failures. In the series of Figs. 42 through 48, we observe at higher magnifications both failed bars and incipient failures with attempts to remove the SiO_2 coating. These failures occurred within a matter of minutes at 2×10^6 amps-cm^2 at ambient room temperature with only convective cooling from a TO-type header.

A number of features of these incipient failures are well worth noting. The accumulation and depletion of aluminum (beginnings of failure) appear to occur in the wider tapered portions of the test bar. The overlayer of SiO_2 is pulled down or puckers up depending on the polarity of the bar end being examined. Figure 41 suggests a periodic widening and narrowing of the aluminum due to the stressing. Further, these Figs. 44, 45, 46 and 48 attest to the difficulty of selectively etching the SiO_2 over the highly stressed bars without introducing etching artifacts.

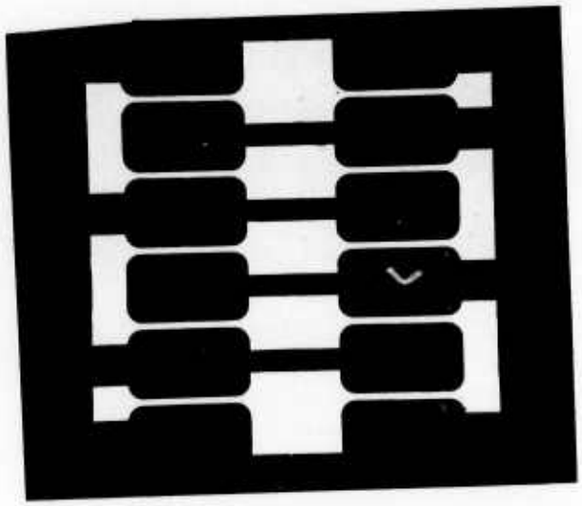
Two scanning electron micrographs of aluminum -4% copper test bars stressed to failure are shown in Figs. 49 and 50. The stress level was twice that for the failed aluminum and failure occurred at something over 500°C at the 4×10^6amp-cm^2 current density. Further, note that these bars were not yet overcoated with SiO_2 which at least stabilizes pure aluminum to electromigration failure. The failure of this uncoated alloy bar did not occur in the tapering portion of the bar and the entire test bar exhibits a striation parallel to the direction of current flow. To our knowledge this striation effect has not been reported in the literature. No explanation can be offered at this time.

Figure 51 exhibits the change in topography associated with the high current density at a large viewing angle with respect to the perpendicular. Figures 52 through 56 exhibit various features of failure under high current stress and have self explanatory captions.

Results are presented here for electromigration tests performed on both aluminum and aluminum -4% copper at a current density of 4.6×10^6amps/cm^2. This

FIG.40

ELECTROMIGRATION TEST PATTERN



TEST SECTION DIMENSIONS: 1 MIL X10 MIL

N10–88–5

FIG. 41

INCIPIENT FAILURES

NOTE DEPLETION AT CATHODE ENDS AND ACCUMULATION AT ANODE ENDS

ONE BAR HAS FAILED

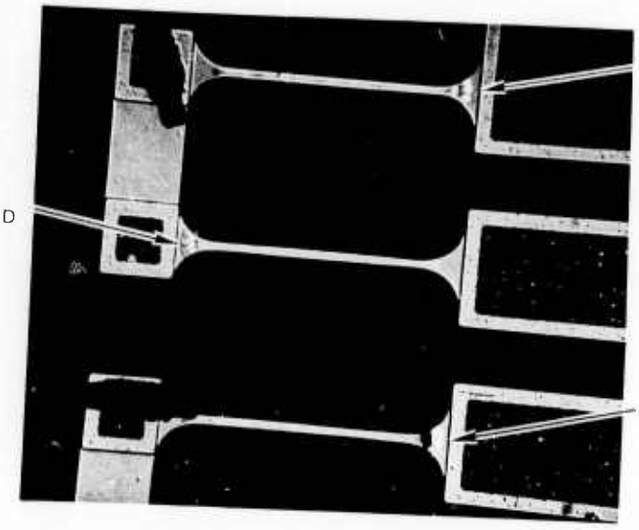
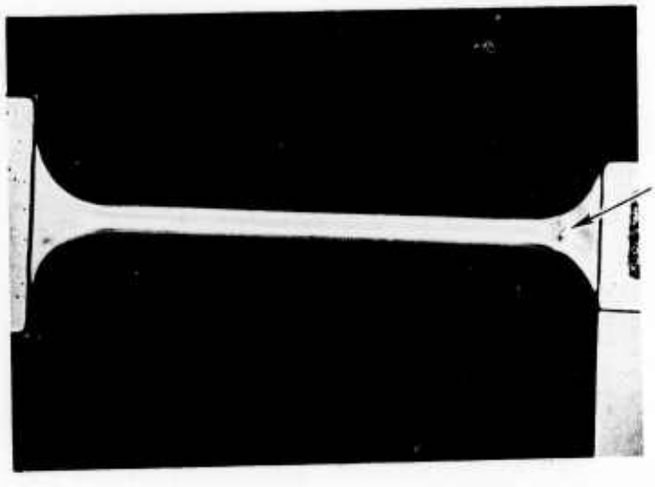


FIG. 42

INCIPIENT FAILURE

0.75 μ Al OVERCOATED WITH 1 μ SiO_2

DEPLETION AT CATHODE END AND ACCUMULATION AT ANODE END



N10–88–15

FIG. 43

INCIPIENT FAILURE AT CATHODE END

0.75 μ Al OVERCOATED WITH 1 μ SiO_2

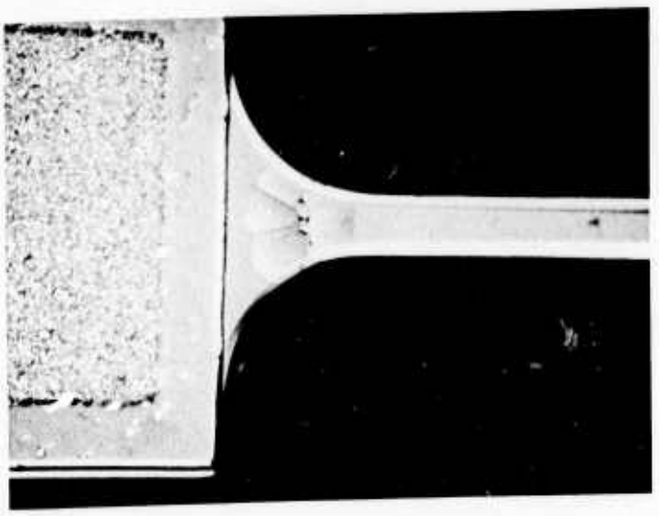


FIG. 44

INCIPIENT FAILURE

CATHODE END OF Al TEST BAR

1 μ THICK SiO_2 OVERCOATING PARTIALLY REMOVED

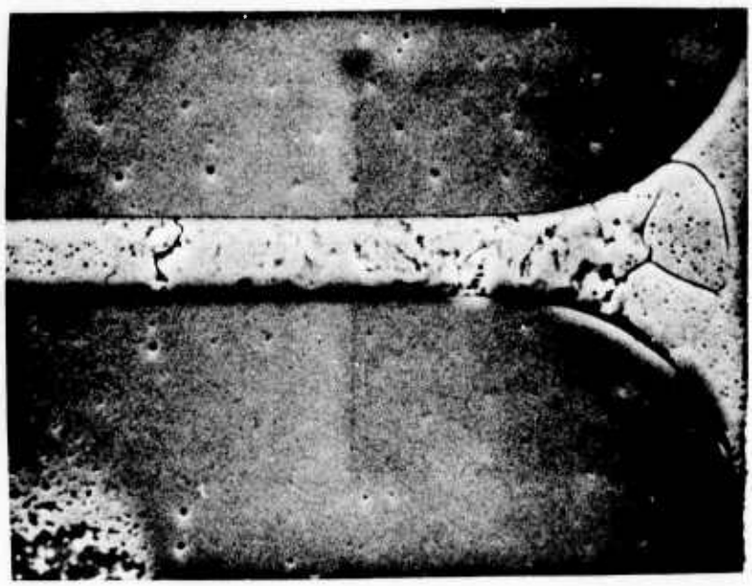
2000X

FIG. 45

INCIPIENT FAILURE

CATHODE END OF Al TEST BAR

SiO_2 OVERCOATING REMOVED



1000X SEM

FIG. 46

INCIPIENT FAILURE

CATHODE END OF Al TEST BAR

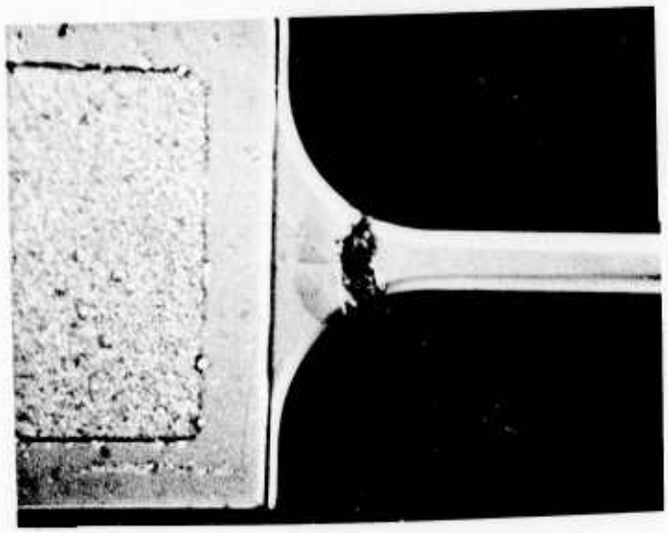
SiO_2 OVERCOATING REMOVED

2000X SEM

FIG. 47

FAILED TEST BAR, CATHODE END

0.75 μ Al OVERCOATED WITH 1 μ SiO_2



N10–88–8

N921820–4

FAILED TEST BAR CATHODE END

0.75 μ THICK Al

1 μ THICK SiO_2 OVERCOATING PARTIALLY REMOVED

2000X SEM

FIG. 49

FAILED TEST BAR

CATHODE END CLOSEST TO WIRE

Al + 4% Cu 0,5 μ THICK STRESSED AT 4×10^6 AMPS/CM^2

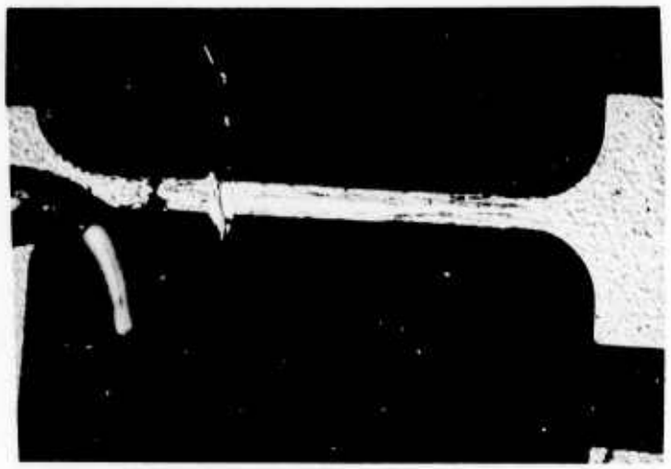


FIG. 50

ANODE END OF FAILURE TEST BAR

Al + 4% Cu NOT OVERCOATED WITH SiO_2

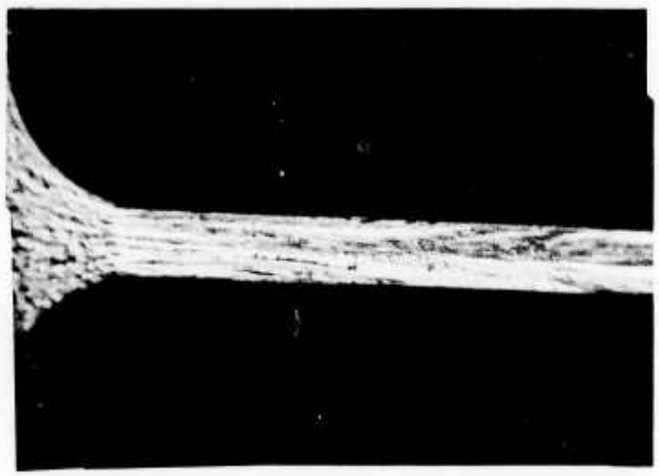


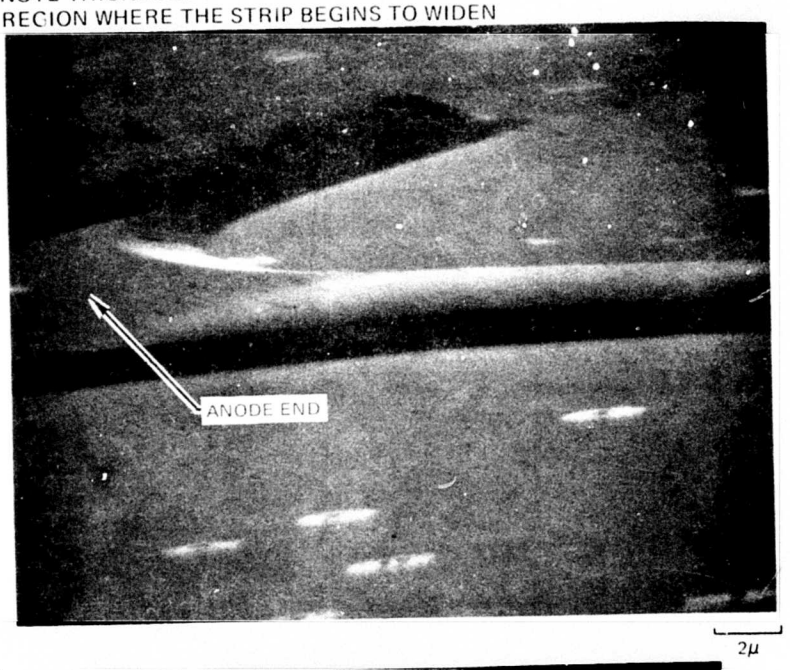
FIG. 51

FAILED TEST STRIP

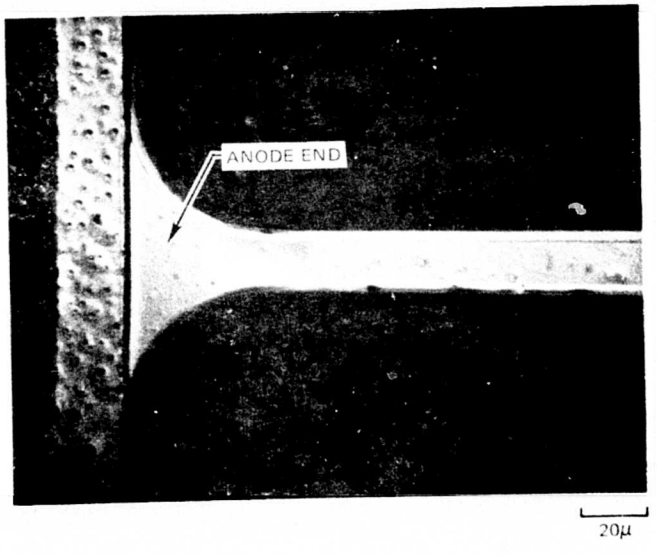
Al WITH SiO_2

HIGH ANGLE SEM

A. NOTE THICKENED REGION JUST AT THE REGION WHERE THE STRIP BEGINS TO WIDEN



B.



N11–170–8

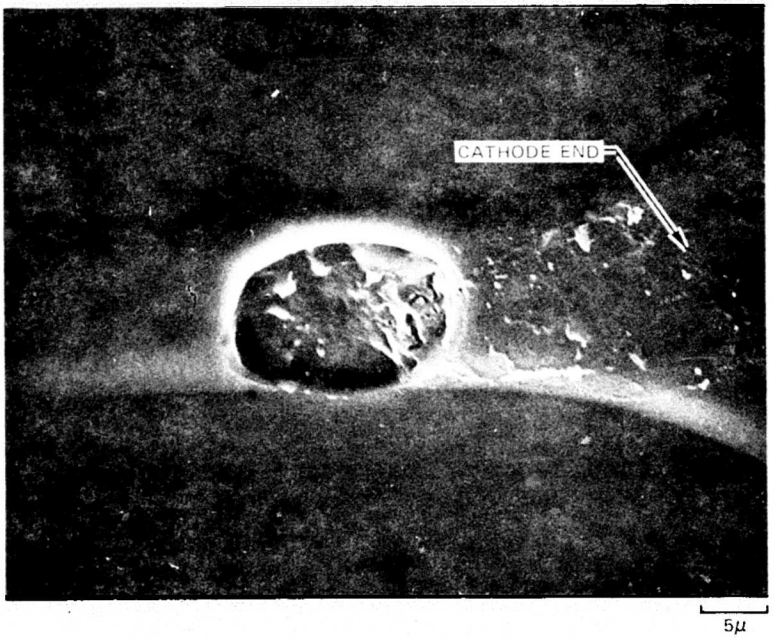
FIG. 52

FAILED TEST STRIP

OXIDE COVERING OVER FAILED AREA HAS BEEN EJECTED

Al WITH SiO_2

SEM

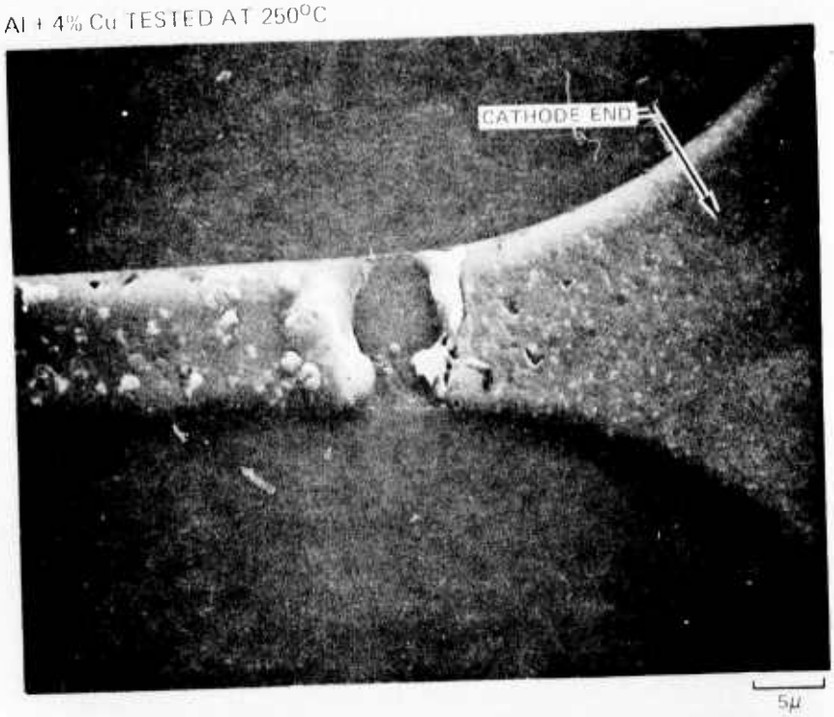


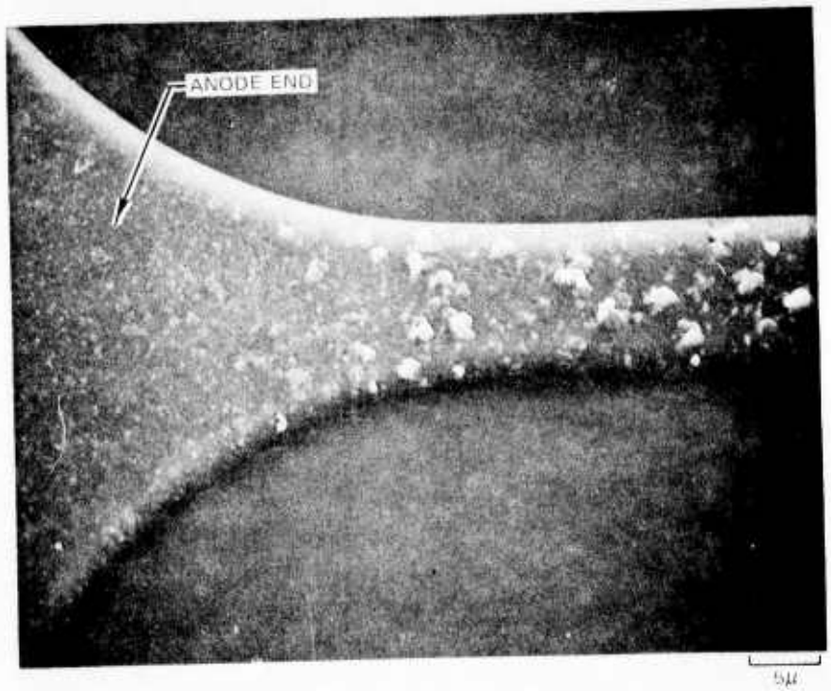
N921820–4

FIG. 53

FAILED TEST STRIP

A. Al + 4% Cu TESTED AT 250°C



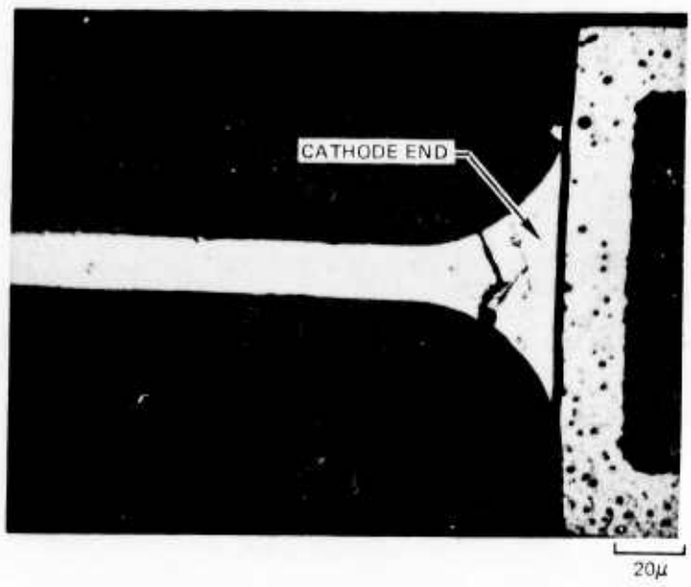


N11–170–7

FIG. 54

FAILED TEST STRIP

Al COVERED WITH SiO_2



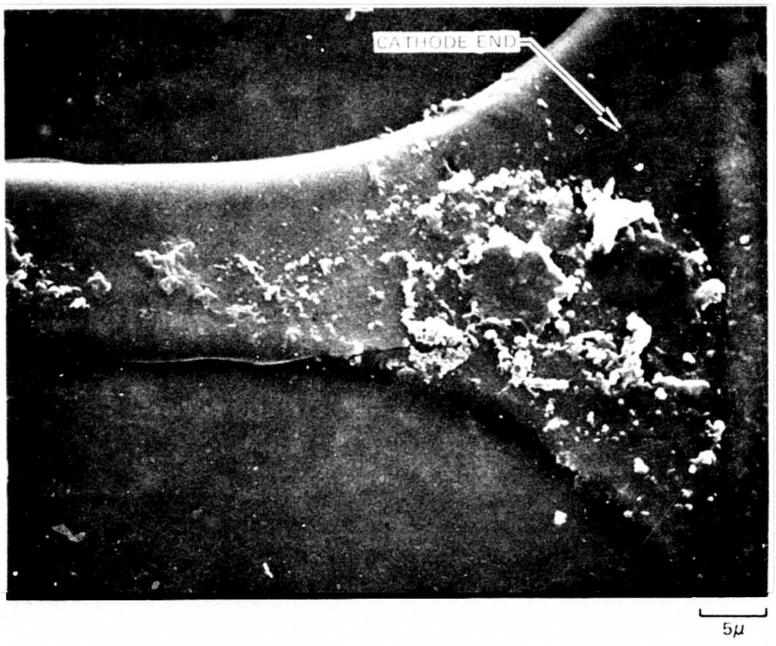
N11-170-1

FIG. 55

FAILED TEST STRIP

NOTE CRACKED OXIDE

Al + 4% Cu WITH SiO_2

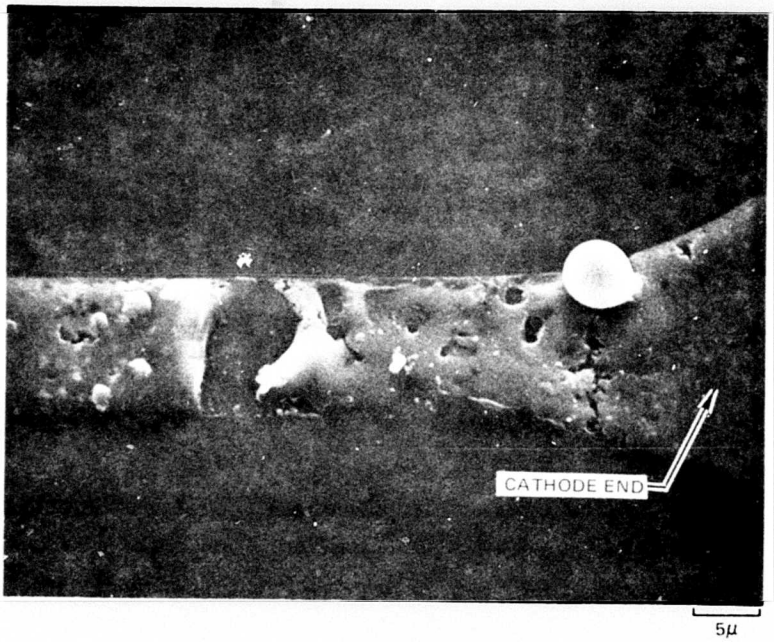


N11–170–12

FIG. 56

FAILED TEST STRIP

Al + 4% Cu TESTED AT 250°C



high value was chosen simply to accelerate the testing and permit data to be accumulated during a relatively short period, as already noted. Test bars were evaluated bare and with an overlayer of SiO_2.

Samples for these tests were eutectic chip bonded and ultra-sonic wire bonded in TO-5 packages. The uncapped packages were immersed in a temperature controlled bath of Dow Corning 704 silicone diffusion pump fluid. Thus, oil was in direct contact with the test chip but no evidence of chemical interaction was observed. The devices were used as their own resistance thermometers. A calibration curve of resistance versus temperature was prepared for each test and the temperature of the oil bath regulated to give the resistance corresponding to the selected device temperature (with the devices current loaded). Table I shows the temperature difference between the test links and the oil bath caused by ohmic heating.

TABLE I

Resistance Calibration Data

Test	Temperature, °C Device	Bath	ΔT
Al + 4% Cu	200	155	45
Al + SiO_2	250	95	155
Al + 4% Cu	225	185	40
Al + SiO_2	200	58	142
Al + 4% Cu	250	205	45
Al + 4% Cu + SiO_2	250	215	35

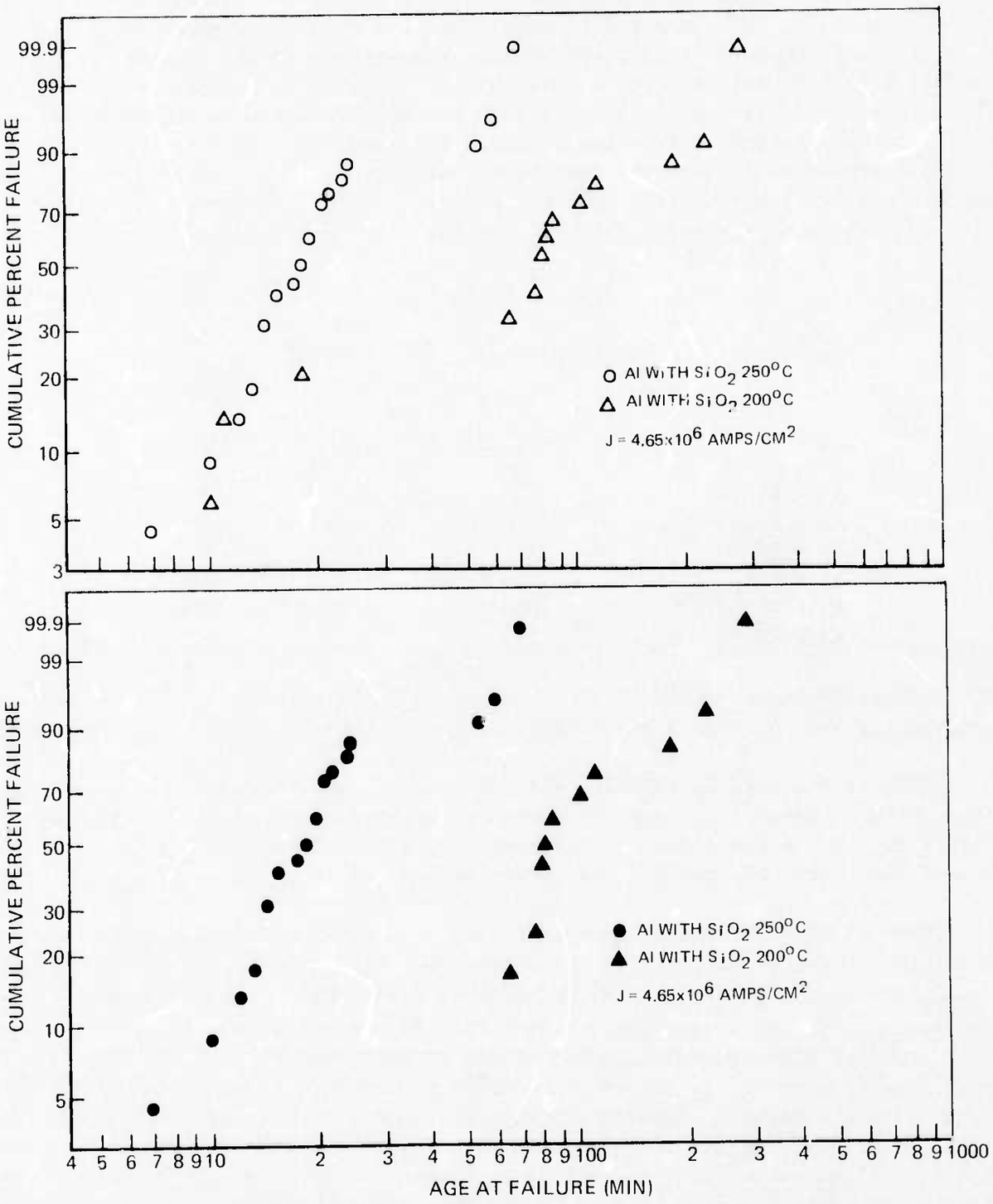
The results of these tests are presented in Figs. 57 through 60 plotted as Weibull Probability charts. For a short discussion of Weibull analysis see Appendix D.

Several features of the data are notable. Figure 60 shows more than an order of magnitude greater life for the coated alloy when compared to coated pure aluminum. Figure 59 shows a comparison of the coated with the uncoated alloy and verifies that, indeed, sputtered silicon dioxide offers an impovement in electromigration resistance.

Note in Figs. 57 and 58 apparently exhibiting two sets of data for the same conditions that the raw data of the upper plot exhibits a number of "sports" which represent "infant"mortality. A smooth curve fitting the data points has a pronounced hump in the lower region. This kind of behavior, departures from linearity, on a Weibull plot is generally attributed to more than one failure mode operating simultaneously. If the separate modes can somehow be identified with their data points, a Weibull analysis can be done for each set of points, deriving mean times to failure, activation energies, etc. for single mode failures. In some kinds of life tests, for example ball bearings, separate failure modes are readily identified after the fact, i.e. race failures and ball failures, and the Weibull

FIG. 57

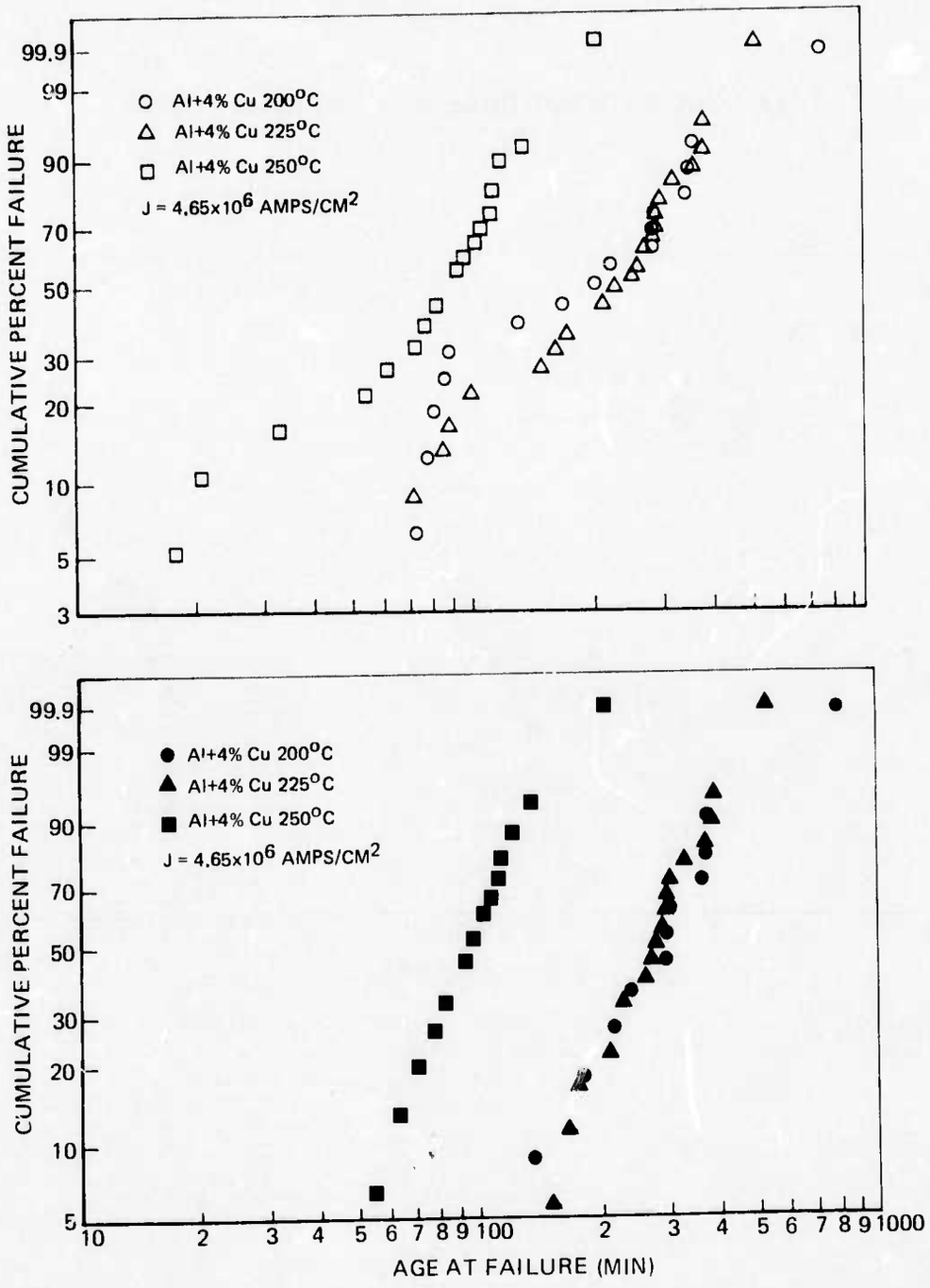
FAILURE RATE FOR COATED Al
TEMPERATURE DEPENDENCE



N11-170-4

FIG. 58

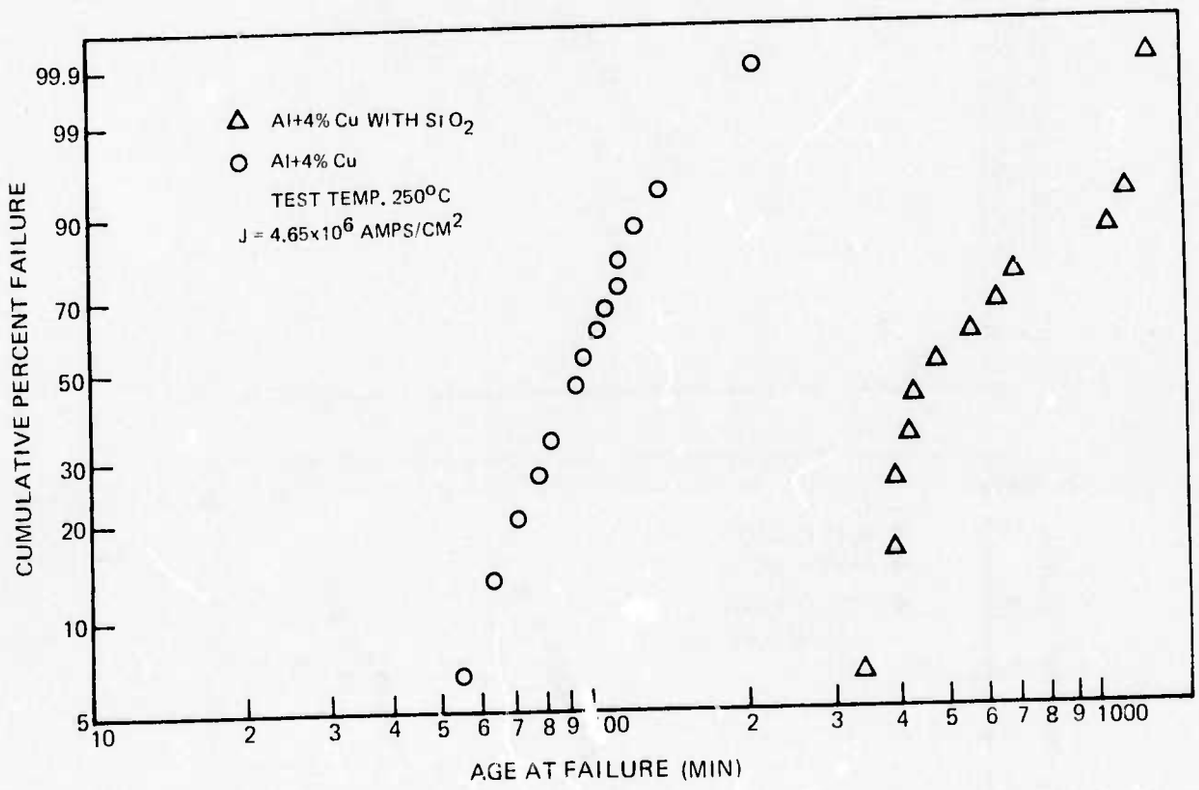
FAILURE RATE FOR AlCu
TEMPERATURE DEPENDENCE



N11–170–14

FIG. 59

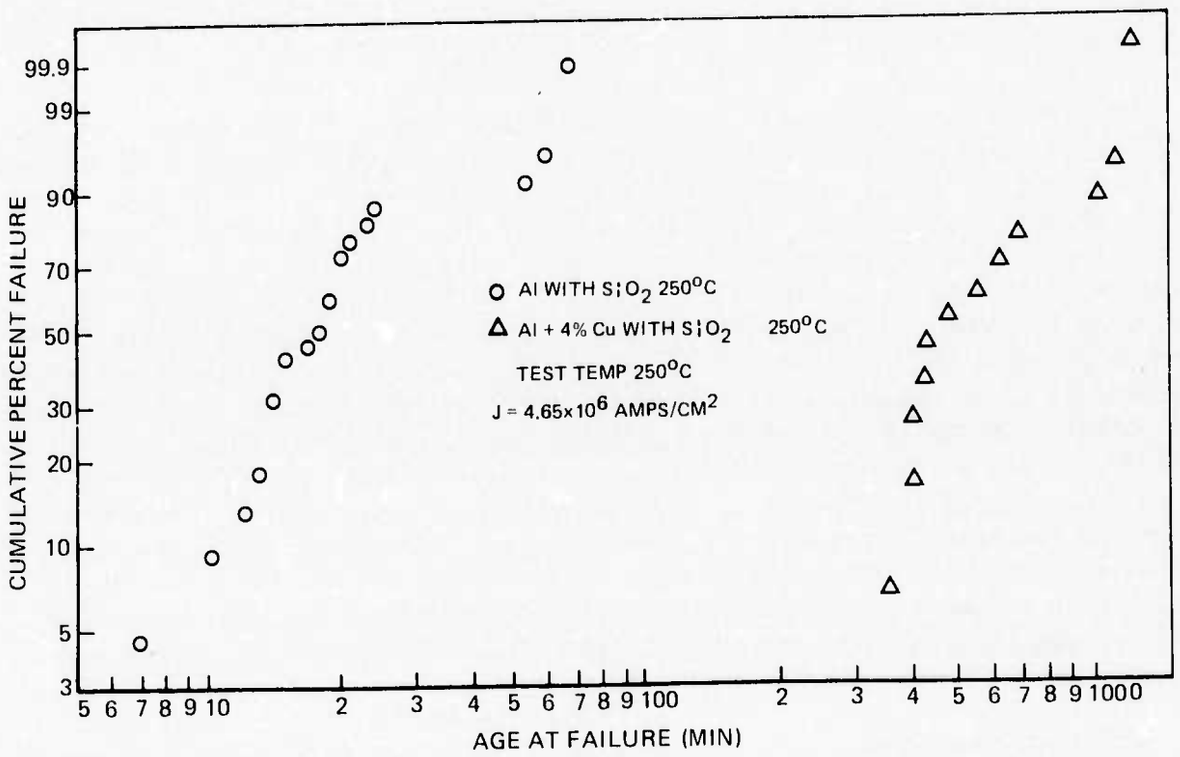
FAILURE RATE FOR BARE AlCu AND AlCu COATED



N11-170-3

FIG. 60

FAILURE RATE FOR COATED Al AND COATED AlCu



N11–170–5

analysis presents no problems. In the case of electromigration testing, however, at the moment of failure considerable damage occurs in the immediate vicinity of the failure and small defects such as metal voids, local contamination, passivation cracks or pinholes, may no longer be distinguishable. In fact, such defects may be difficult or impractical to identify prior to the test. The upper plots in Figs. 57 and 58 contain all data points taken for these tests. In the lower plots we excluded those data points (four or five at the most) which depart significantly from the straight line suggested by the large majority of longer lived samples. This exclusion does not significantly change the mean time to failure found from a Weibull plot for a given sample set but suggests a small population of short-lived samples within each set which exhibit failure mechanisms other than electromigration. One cannot, in general, separate two such populations by inspection of data alone. In most instances, other data would be required which would permit identification of the mode of failure for each member of the tested set.

As-deposited grain size in the sputtered films was "small", i.e., less than 2000Å (as inferred from electron micrographs, Figs. 31, 32, 33) for both aluminum and the alloy Al96-Cu4. The films were subjected to identical processing steps during photolithography but suffered variations in total time lapse between deposition and initiation of electromigration tests. Variations in length of exposure to the oil bath temperatures prior to initiation of the electromigration test also occurred. It was observed that grain growth and surface reconstitution were progressing at room temperature and that even slightly elevated temperatures accelerated these changes. It is very unlikely that much can be concluded regarding the effect of grain size on electromigration failure rate from these data. Similarly, only a few fortuitous instances of studies reported in the literature where preannealing at relatively high temperatures was part of the procedure for preparing the thin film alloys are likely to provide reliable grain size data. In those cases where layered structures of pure Aluminum alternating with pure copper were annealed to homogenize the films, grain growth probably proceeded until an equilibrium grain size was produced or, at the least, one which would not grow at the lower test temperatures.

The techniques used under this program could be modified to give a limited amount of data which might be sufficient to resolve the grain size vs. electromigration failure rate. A pre-anneal at or slightly above the temperature of interest would produce a grain size characteristic of equilibrium at this temperature. By experimentally determining the resistance of the stripes at temperature, the oil bath can be controlled to maintain the stripe resistance while developing the I^2R heating on the chip. This approach however will not entirely avoid the local temperature rise which will start when sufficient metal has migrated to significantly change the local cross section (and resistance) along the stripe.

Insufficient data are presented here to permit inference of an activation energy for the process or processes causing the electromigration failures. More data taken at lower temperatures and lower current densities would be required. Gathering these data would require much more time than was allowed under this program. The departures from linearity shown in the Weibull plots suggest more than one mechanism for the electromigration failure which means that an even more detailed examination of the process as a function of temperature and current density is required.

We can conclude, however, from the data given that substantial improvement in the reliability of metal interconnects can be achieved by the substitution of sputtered aluminum -4% copper for pure sputtered aluminum and that rf sputtered silicon dioxide overcoating either metal will further extend the life of metal interconnects subjected to the very high current densities producing electromigration.

4.1.5 Evaluation of Multilevel Test Cells

A total process for an integrated circuit must finally be evaluated for yields. Pinholes in films manifest as metal-to-metal shorts and feedthrough and metal interconnect continuity which result from all the processing steps must be taken into account in the form of yield of good devices or circuits. A test cell is required which is subjected to all the same processing steps as a circuit and can be tested for these significant faults. Since evaluation of total wafer processing is reported here, it should be pointed out that certain procedures resulting in low pinhole incidence in the films are important. Etch compositions are given in Appendix A and B. The gallium backing process and the associated special design of the substrate heater and holder are described in Appendix C along with the "taping procedure." The special moated pedestal design of the substrate holder avoids pinholing due to gallium expulsion from between the wafer and the holder to finally produce pinholes while the "taping" technique reduces praticulate contamination (and pinholing) to a low incidence.

The construction of the three layer test cell used in this program permits the four separate tests described earlier to be made to characterize every kind of fault. A test is the application of a voltage to a selected set of contacts and the detection of voltage at another set of contacts. A fault can be detected by either the presence or the absence of voltage, depending on the test and the contacts selected. A complete list of the twelve kinds of detectable faults is in Table II.

TABLE II

Fault Code

Fault Code	Fault
1	LOWER TO MIDDLE SHORT
2	MIDDLE TO UPPER SHORT
3	UPPER TO LOWER SHORT
4	THREE LAYER SHORT
5	UPPER METAL DISCONTINUOUS
6	MIDDLE METAL DISCONTINUOUS
7	LOWER METAL DISCONTINUOUS
8	UPPER VIA OPEN
9	LOWER VIA OPEN
A	VIA METAL TO UPPER METAL SHORT
B	VIA METAL TO MIDDLE METAL SHORT
C	VIA METAL TO LOWER METAL SHORT

The four tests are applied as follows: (see Fig. 2)

Test #1 - voltage applied to middle metal 1, upper metal 2 and upper via pads
voltage detected at lower metal 1, vias (common) middle metal 2,
upper metal 1

If the cell passes this test, we know that

1. all upper vias are good
2. the middle metal is continuous
3. the upper metal is continuous
4. the lower metal is not shorted to the middle or upper metals or to the via metal.

Test #2 - voltage applied to upper metal 2, lower metal 2, and lower via pads.
voltage detected at middle metal 1, vias (common), lower metal 1, and upper metal 1

Cells passing this test have

1. all lower vias good
2. lower metal continuous
3. upper metal continuous
4. no shorts from the middle metal to the upper or lower metals or to the via metal.

At this point, all those cells which do not have shorts are completely specified and need not be tested further.

Test #3 - voltage applied to vias (common)
voltage detected at, upper metal, lower metal 1, and middle metal 1

T is tests determines whether or not any of the crossover levels are shorted to the via metal.

Test #4 - (note: This test needs to be given only to those cells that indicate shorts in both Test #1 and Test #2)

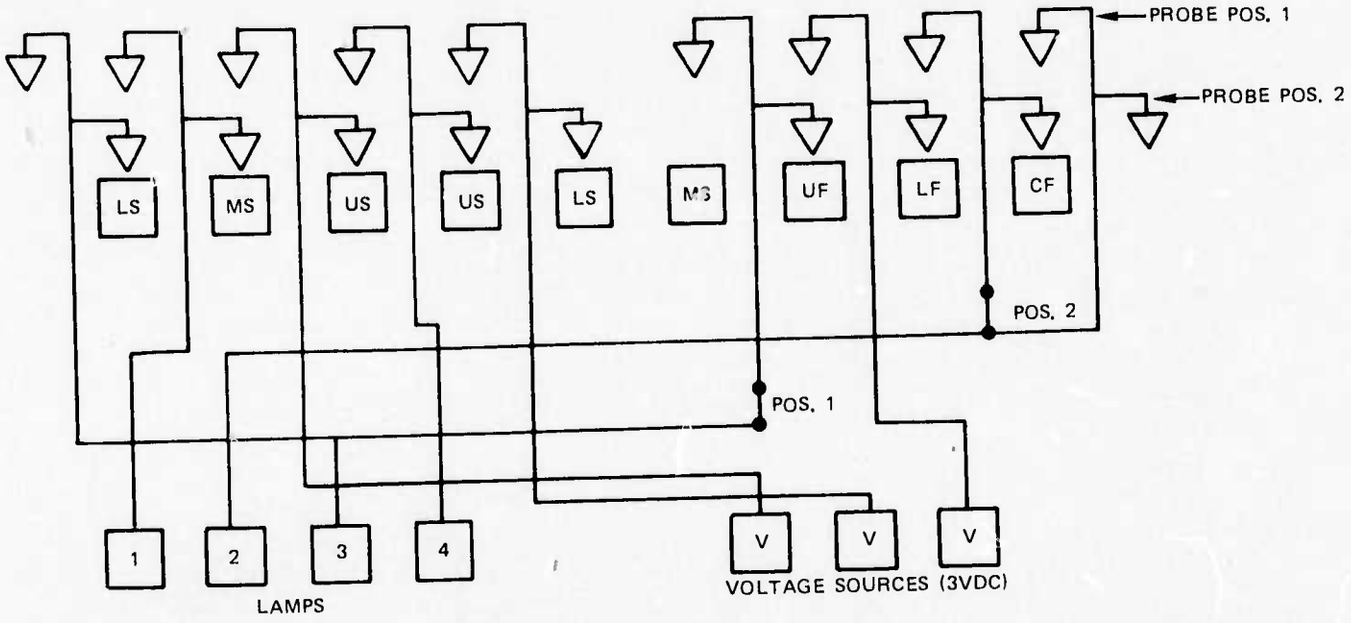
- voltage applied to middle metal 1
voltage detected at upper metal 1 and lower metal 1

This test will identify those cells in which all three metal levels are shorted together.

Referring to Fig. 61, Test #1 is performed with nine probes in position 1. Note that the probe on the extreme left does not touch a bonding pad and that the probe on the extreme right touches the pad labeled CF which is vias (common). The three boxes labeled VOLTAGE SOURCES (inputs in Fig. 62) supply 3VDC to the pads indicated. The four boxes labeled LAMPS are connections to the detector circuits (outputs in Fig. 62).

FIG. 61

3–LEVEL CROSSOVER TEST



POS. 1 V TO MS, US & UF

LAMP CONNECTIONS		ON MEANS
1	TO LS	SHORT LS TO MS AND/OR US
2	TO CF	UF CONT.
3	TO MS	MS CONT.
4	TO US	US CONT.

POS. 2 V TO LS, US & LF

LAMP CONNECTIONS		ON MEANS
1	TO MS	SHORT MS TO LS AND/OR US
2	TO CF	LF CONT.
3	TO LS	LS CONT.
4	TO US	US CONT.

LIGHT #1 FAULT CODE

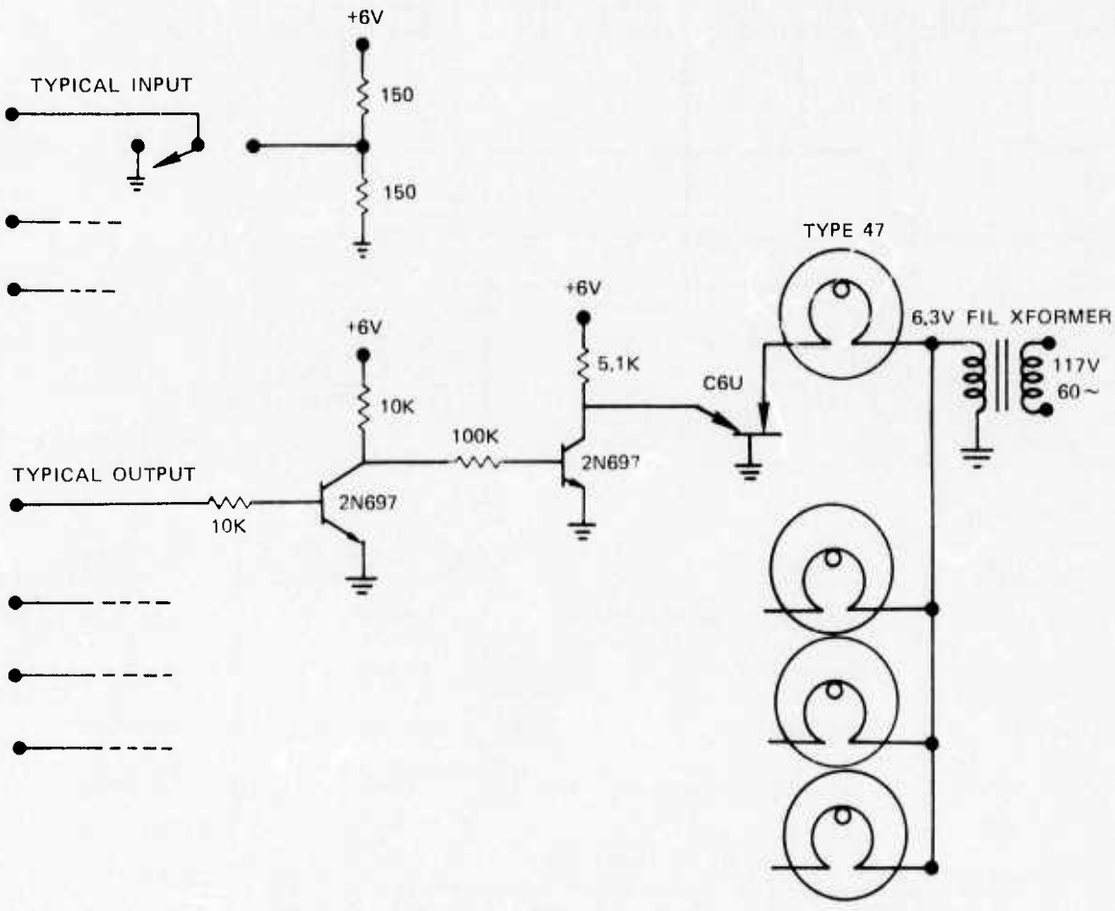
POS. 1	ON	OFF	ON	OFF
POS. 2	ON	ON	OFF	OFF
MEANS	LS–MS SHORT	MS–US SHORT	LS–US SHORT	GOOD
	AND/OR LS–US SHORT			

NOTE: A GOOD CELL WILL CAUSE THE SAME LIGHT PATTERN TO APPEAR ON THE TEST SET WITH THE PROBES IN BOTH POSITION 1 AND POSITION 2. LIGHT 1 OFF, LIGHTS 2,3, AND 4 ON

N12–15–2

FIG. 62

CIRCUIT FOR TESTING 3–LEVEL METAL TEST CELL



(LAMP GOES ON IF 3V SIGNAL APPEARS AT TYP. OUTPUT TERMINAL
BUT VERY LITTLE CURRENT IS DRAWN THROUGH TESTED DEVICE)

N12–15–1

Test #2 is performed in a similar manner with the probes shifted one pad location to the right. Now the probe on the extreme left touches the pad marked LS (LOWER METAL 1 in Fig. 2) and the probe on the extreme right does not touch a pad.

The two connections labeled POS. 1 and POS. 2 in Fig. 61 are present only for the corresponding probe positions. The table below the probe connection diagram in Fig. 61 indicates in detail the meaning of signals detected at the four outputs.

LIGHT #1 FAULT CODE table (Fig. 61) is used to interpret the lamp pattern indicating shorts between the various metal layers in the cell. The ambiguous situation indicated in the table where the lamp is on in both POS. 1 and POS. 2 is resolved in Tests 3 and 4 described earlier.

It is possible, of course, to perform all four tests in a single pass across the wafer by introducing a switch between the test set and the probes. We have found, however, that in the case where most of the cells are good, that it is considerably faster to use the TAC probe machine in semi-automatic mode and perform the tests sequentially.

Tabular data are presented in Table III for three typical wafers produced under this program. Average cell yields are 76%. Improvements in photoresist handling and more sophisticated mask making techniques could increase this yield to at least 81% by eliminating metal discontinuities and similar faults. Incidence of both shorts and feedthrough opens are less than 10 per 100,000 for a cell configuration which is probably far more complex in its interconnection pattern than the vast majority of contemplated LSI chips in the reasonable future.

TABLE III

Wafer Data Summary

FAULT	WAFER A	WAFER B	WAFER C	TOTAL	
1	19	11	4	34	LOWER-MIDDLE SHORT
2	13	14	13	40	MIDDLE-UPPER SHORT
3	0	0	1	1	UPPER-LOWER SHORT
4	2	2	0	4	UPPER-MIDDLE-LOWER SHORT
5	1	4	1	6	UPPER DISCONTINUOUS
6	3	2	1	6	MIDDLE DISCONTINUOUS
7	6	1	5	12	LOWER DISCONTINUOUS
8	1	2	0	3	UPPER VIA OPEN
9	1	3	1	5	LOWER VIA OPEN
A	0	0	0	0	VIA TO UPPER SHORT
B	1	0	4	5	VIA TO MIDDLE SHORT
C	1	0	1	2	VIA TO LOWER SHORT

TABLE III - Continued

	WAFER A	B	C	TOTAL
CELLS TESTED	157	169	158	484
FAULT FREE	113	130	127	370 (76%)
CELLS FREE OF OPEN VIAS&LEVEL TO LEVEL	122	137	132	391 (81%)

TOTAL LOWER-MIDDLE & UPPER-MIDDLE SHORTS - 82 (5.1 per 100,000 mils^2)
TOTAL VIA OPENS - 8 (7.7 per 100,000)

Wafer maps are shown in Figs. 63, 64, and 65 with the faults in each defective cell identified according to the alpha-numeric code shown in each figure. No particular distribution seem to prevail. In the absence of a non-random pattern, it is suggested that under the modest clean room conditions existing in this laboratory improvement beyond this level is not likely to follow. The particle count level of 10,000/ft^3 normally observed in the open areas, however, could be reduced by improved construction and discipline directed toward dust control and improvement in pinhole count should result. Some production environments are known to be characterized by lower particle counts and there is every reason to believe that the processes described here could be implemented with improved yields.

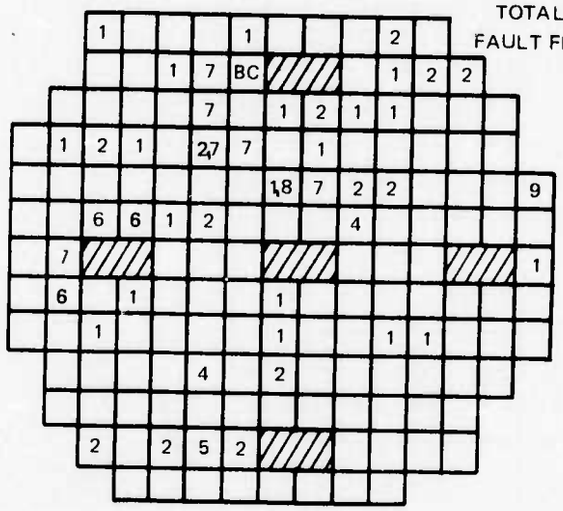
The tests described above were purposely done at very low voltages in order to avoid rupturing the insulator at weak spots between conductor layers. Insulator breakdown tests were done separately on a wafer for which the cell fault data (83% fault free cells) were quite similar to the wafers described above. Self-healing is observed as a high current pulse which is conjectured to vaporize the material in a filamentary conducting path which developed in the oxide. Direct observation of the phenomena is prevented by electrode geometry. This first current pulse through the insulator occurs at "first breakdown," that is the lowest voltage at which conduction occurs. The flaws characterized by "first breakdown" may be localized entrapped particulate matter or cracks in the oxide with absorbed gases or other matter along the walls of the cracks.

Continuous current flow probably results from the formation of conduction decomposition products from the oxide as it is locally heated by a runaway avalanche of carriers in the oxide. This conduction may or may not occur at the same site as a "first breakdown" phenomena.

A total of twenty-one good cells were tested, upper insulator and lower insulator. Most cells had a first breakdown at 200 volts or higher, with the highest near 400 volts and the lowest at 125 volts. The average first breakdown voltage was 275 volts. There was no significant difference between the upper and lower dielectrics which were both about 1.5 microns thick on this wafer.

FIG. 63

WAFER 102 A

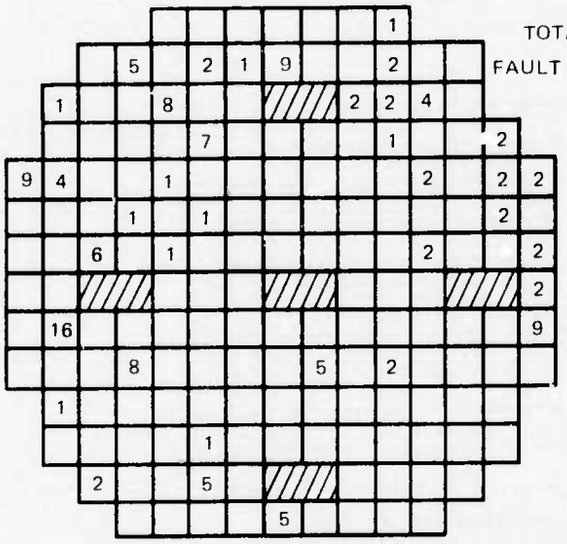


FAULT CODE	FAULT
1	LOWER TO MIDDLE SHORT
2	MIDDLE TO UPPER SHORT
3	UPPER TO LOWER SHORT
4	THREE LAYER SHORT
5	UPPER METAL DISCONTINUOUS
6	MIDDLE METAL DISCONTINUOUS
7	LOWER METAL DISCONTINUOUS
8	UPPER VIA OPEN
9	LOWER VIA OPEN
A	VIA METAL TO UPPER METAL SHORT
B	VIA METAL TO MIDDLE METAL SHORT
C	VIA METAL TO LOWER METAL SHORT

N11–204–3

FIG. 64

WAFER 102 B

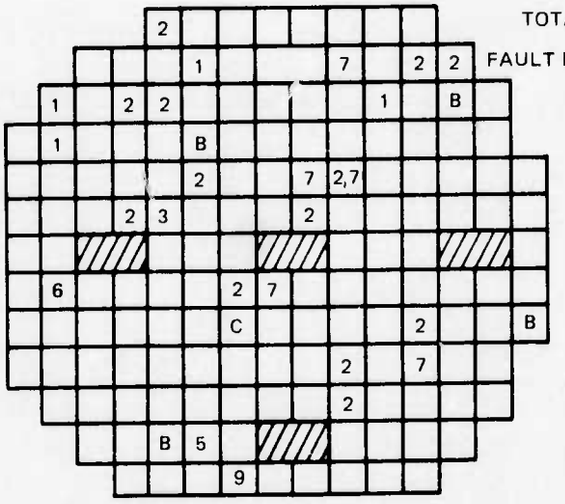


FAULT CODE	FAULT
1	LOWER TO MIDDLE SHORT
2	MIDDLE TO UPPER SHORT
3	UPPER TO LOWER SHORT
4	THREE LAYER SHORT
5	UPPER METAL DISCONTINUOUS
6	MIDDLE METAL DISCONTINUOUS
7	LOWER METAL DISCONTINUOUS
8	UPPER VIA OPEN
9	LOWER VIA OPEN
A	VIA METAL TO UPPER METAL SHORT
B	VIA METAL TO MIDDLE METAL SHORT
C	VIA METAL TO LOWER METAL SHORT

N11–204–2

FIG. 65

WAFER 102C



FAULT CODE	FAULT
1	LOWER TO MIDDLE SHORT
2	MIDDLE TO UPPER SHORT
3	UPPER TO LOWER SHORT
4	THREE LAYER SHORT
5	UPPER METAL DISCONTINUOUS
6	MIDDLE METAL DISCONTINUOUS
7	LOWER METAL DISCONTINUOUS
8	UPPER VIA OPEN
9	LOWER VIA OPEN
A	VIA METAL TO UPPER METAL SHORT
B	VIA METAL TO MIDDLE METAL SHORT
C	VIA METAL TO LOWER METAL SHORT

N11–204–1

4.1.6 Evaluation of Feedthrough Resistance

Etching of feedthroughs to permit level-to-level electrical continuity at desired points in a circuit has proven to be one of the more difficult technological problems. Metals tend to chemically react with oxides to produce new mixed oxide insulating films with new etching characteristics. These products are, at best, ill-defined in the metal film-oxide film case and vary in composition and thickness from point-to-point. This often requires a new etch or other insulator removal means than that used for the primary silicon dioxide etching step.

Figures 66 and 67 exhibit "properly etched" and "improperly etched" feedthrough holes in silicon dioxide over an aluminum -4% copper contact point. Note the granular texture where the oxide was removed from the metal. This is due to the already cited local chemical interaction between oxide and metal to produce products of non-uniform thickness and varying etch rate across the film. Figure 67 shows the results of over-etching in an attempt to remove this residue chemically-an undercutting of the oxide with the hazard now of an unsupported upper level of metal contacting the lower or, even worse, no bridging of the gap by the upper level metal to the lower level.

To avoid this problem and to produce low resistance contacts, sputter etching was used to clean substrates just prior to deposition of the metal. The substrate holder was insulated electrically from the vacuum chamber walls and RF power was then supplied to the substrate holder. After cleaning, power was supplied to the metal target and the substrate holder was grounded during the metal deposition. Only a very short time lapse was permitted during this change-over--perhaps one minute required--so that minimal adsorption from the ambient sputtering gas occurred before metal deposition on the cleaned surface began.

A thin layer of low vapor pressure vacuum grease was used on the slice backside to provide thermal contact between the wafer and the water cooled substrate holder. Apiezon N was found to be satisfactory for this purpose and was readily removed by thrichloroethylene.

A wafer was sputter etched for two minutes (at a power density of 8.0 watts/in^2-watts into a 4" target) prior to deposition of the second layer of Al - 4% Cu. A strip of devices from a diameter of the wafer was mounted by epoxy chip bonding and ultrasonic wirebonding in TO-5 headers. This strip of devices was oriented parallel to the radius of the substrate holder (cathode) during sputter etching.

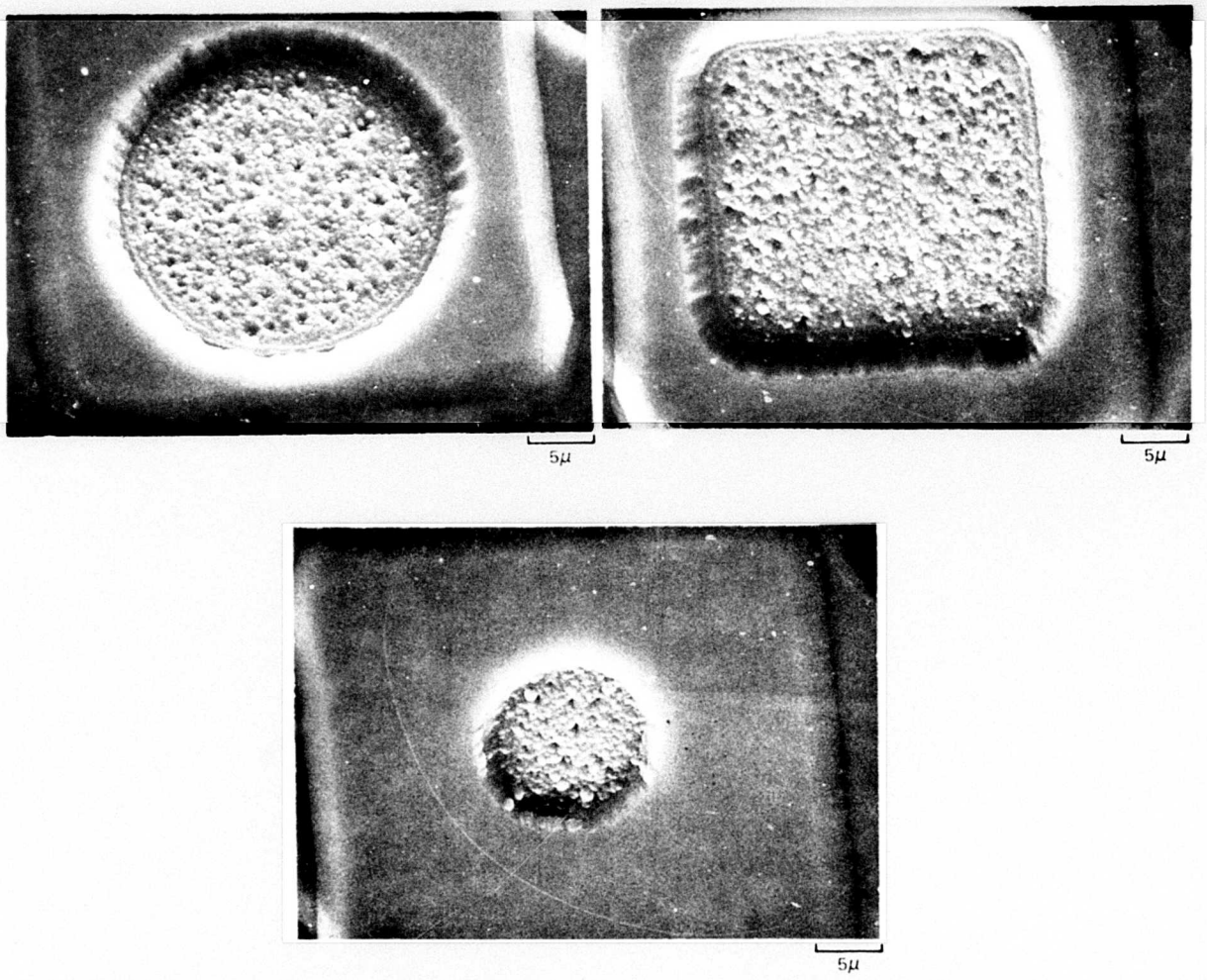
Resistance measurements were performed at as low current as possible to avoid altering any high resistance layers that might be present. The smallest reliably measureable voltages were three micro-volts, requiring currents of about one milliampere to be chosen, therefore, for this test.

The test pattern was a 4-point arrangement in the shape of a cross, with the via whose resistance was to be measured at the center. The two current contacts were opposite one another, one to the upper metal layer, the other to the lower

FIG. 66

GOOD VIA WINDOWS

NOTE SLOPING EDGES OF OPENING SECOND LEVEL METAL
IS PRESENT IN ALL CASES Al + 4% Cu



N11–170–9

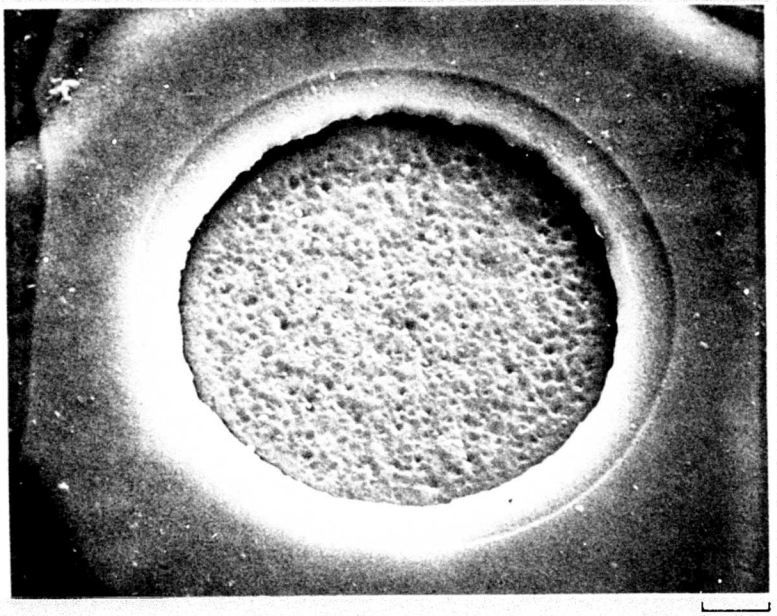
metal layer. The other two contacts were voltage measuring points. This configuration allowed the measurement of the voltage drop that occurred between the upper and lower metal layers (via resistance) independent of the resistive drop that occurred along the metal strips outside the area of the via. It can be seen from Fig. 68 that the measured via resistance was nearly independent of its position on the wafer and that it was about 3.5 millohms for a one square mil via. This is just about one tenth of the resistance of a one mil length of one mil wide, one micron thick aluminum. The lower two sets of points in Fig. 68 represent raw resistance measurements on vias of approximately one square mil and one quarter square mil areas. The upper set is a composite in which each point is obtained by multiplying the via resistance by the measured area of the via.

Thus, these data demonstrate that low resistance feedthroughs repeatedly result from a sputter cleaning procedure which also provides good metal-to-oxide adhesion.

OVER–ETCHED VIA

UPPER LEVEL METAL DOES NOT CONTACT LOWER LEVEL

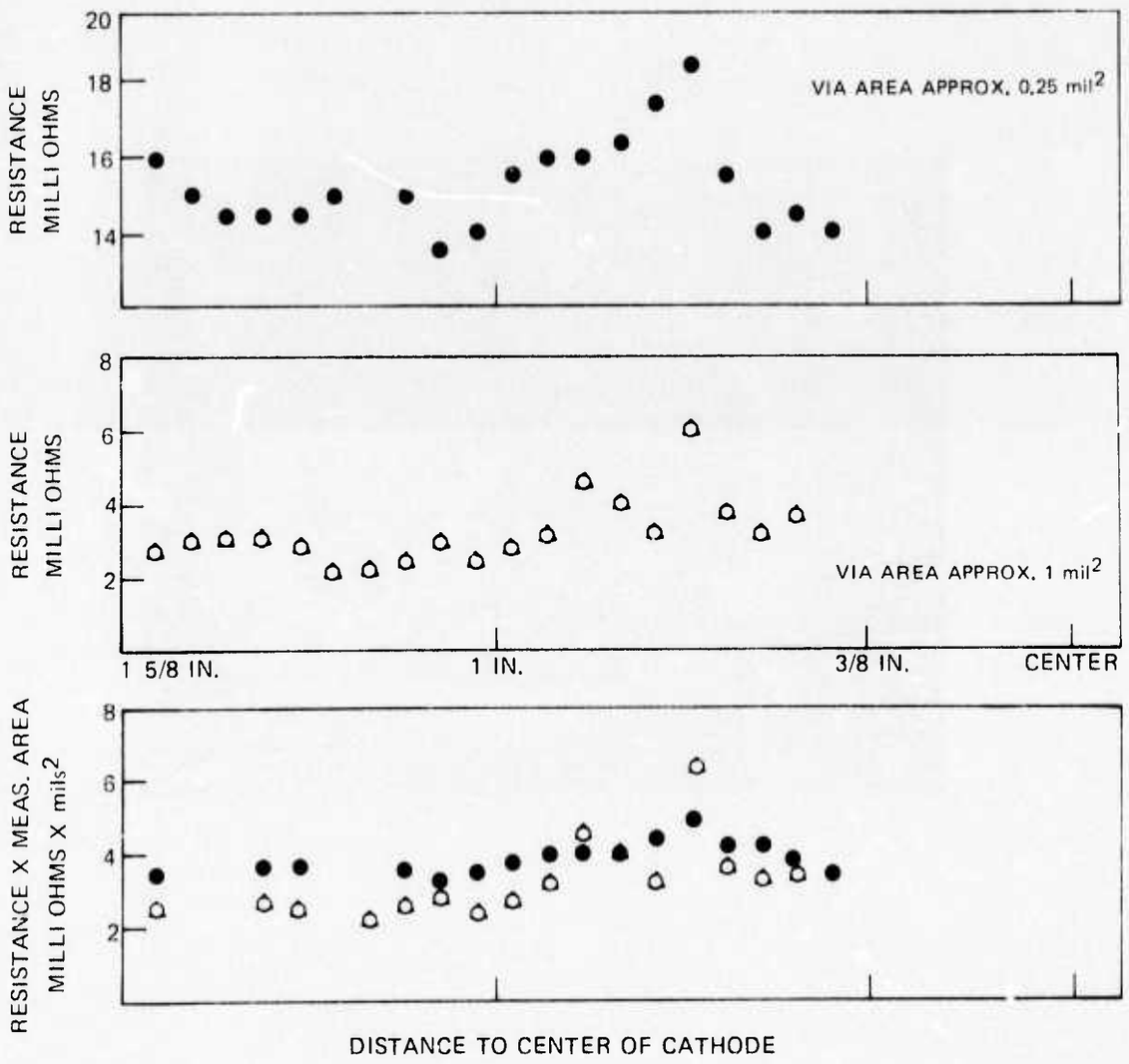
SEM



N11–170–2

VIA RESISTANCE

VIA RESISTANCE ALONG A WAFER DIAMETER PARALLEL
TO THE SPUTTER CLEANING CATHODE DIAMETER



N11-181-1

4.2 Phase II. Beryllium Oxide Sputtering

4.2.1 Statement of Problem

Thermal management has become one of the most important problems in the use of fast, high density integrated circuits. Many other solid state devices such as light emitting diodes and imaging charge coupled arrays require the removal of considerable quantities of heat during normal operation or, as in the latter case, even require cooling below normal room temperature in order to realize best performance (resolution and sensitivity in this instance).

One of the obstacles in the way of good heat sinking rests with the lack of many electrically insulating materials which have good thermal conductivity. Aluminum oxide is one of the common materials used in device package manufacture. It has a thermal conductivity low (0.37 watts /deg C-cm) compared to the metals (copper, for example, with a value of about 3 watts/deg C-cm).

Another difficulty in heat sinking of devices and device packages lies in the interface between device and package and in the package-heat sink interface. Commonly, devices in silicon are eutectic bonded or epoxy bonded to the package. Either technique associated with it has the hazard of void formation. The void in the epoxy is likely to form simply because of air inclusion. This case compounds the problem of poor thermal conductivity of the epoxies. On the other hand, the eutectics or solders used for die attaching tend to oxidize if improperly blanketed with an inert gas. The oxidation products will in general have much lower thermal conductivity than the solders and eutectics. Their formation and build-up degrades the cooling efficiency of the eutectic or solder bond. Void formation in this type of bond is also a common occurrence and is accentuated by the formation of oxidation products. Thus, the common die bonding techniques are seen to present serious drawbacks and to present both yield and reliability problems, ultimately contributing substantially to cost of manufacture and of ownership.

This program was undertaken to provide an improved alternative to heat sinking. Beryllium oxide has long been recognized as an electrical insulator with excellent thermal conductivity about the same as copper and some three times that of silicon. It was reasoned that a layer of beryllium oxide on the device surface bonded to the heat sink would significantly mitigate the effects of voids between the device and the heat sink provided a void-free interface between the device and the beryllium oxide could be produced. RF sputtering is known to produce such an interface with many other materials combinations. The thrust of this program was directed toward finding a set of sputtering parameters for deposition of an acceptable beryllium oxide layer on thermally oxidized silicon wafers.

4.2.2 Experimental Approach and Discussion of Results

The sputtering parameters which were chosen to be varied for this program were the usual ones of sputtering pressure, rf sputtering power, and substrate temperature. Thin layers (less than 0.5 micrometers in thickness) were deposited initially for rate determinations and observation of adhesion. During early depositions, the substrate temperature was not controlled by the usual gallium backing of substrates to temperature-controlled blocks. Rather, the substrates were allowed to "thermally float" and equilibrate with the glow discharge. This was a reproducible temperature at a given power level and was adequate for some of the determinations of rate. Other films were deposited using the gallium backing process in order to give more flexibility in the experiments.

Initially, adhesion problems were encountered when beryllium oxide was sputtered directly. This led to several film depositions by reactive sputtering-sputtering of beryllium metal in an oxygen containing ambient. Similar problems were experienced during the course of these depositions as well. It became clear that contamination problems could be significantly contributing to this adhesion problem. A thorough rework of the sputtering system including cleaning and readjustment of cathode-cathode shield spacing was instituted. The films deposited after the cleaning and rework adhered well and films in the 0.5 to 1.0 micrometer thickness range exhibited a refractive index of 1.72, virtually identical to the handbook bulk value.

One goal of the program was to determine feasibility of depositing thicker layers in the 5.0 to 25 micrometer thickness range for the more serious heat sinking problems. A number of depositions were attempted in this range of thickness but all were terminated after about 2 micrometers of beryllium oxide were deposited. Both reactively sputtered films and those deposited directly from a beryllium oxide target were sufficiently stressed to cause cracking of the substrates at this thickness of deposited BeO film. One substrate on which a beryllium oxide film somewhat less than 2 micrometers thick was deposited exhibited a pronounced curvature- $\sim$ 19 mils bow on a two-inch silicon substrate 13 mils thick. The direction of curvature corresponded to stresses in the film for compression and opposite to that expected for the relative thermal expansion coefficients of silicon and beryllium oxide. Others exhibited curvature commensuate with this observation.

Such large stresses have not to our knowledge been observed for rf sputtered insulators. Molybdenum, however, has been studied in some detail by the IBM group at Fishkill. They reported an almost complete elimination of stress from the molybdenum films deposited by bias sputtering. Their work was concerned with dc sputtering and a small negative dc bias was applied to the substrate holder to produce positive argon ion bombardment of the substrates. This suggests that an rf bias should be applied to the substrate holder so that the insulator covered substrates would be bombarded by positive ions during the deposition. This process apparently prevents trapping of lightly bound contaminants by an ion bombardment of the substrate less energetic than that required to produce sputtering of the target material.

TABLE IV

BeO Sputtering Rate Summary

Power, Watts	Pressure, O_2	Millitorr, A	Temperature, °C	Rate
1000 *	18	12	900°C	3000Å/hr
500 *	18	12	570°C	3800Å/hr
500 *	6	24	200°C	4000Å/hr
500	0	12	200°C	8000Å/hr
500	0	12	300°	6500Å/hr

* Reactively sputtered from pure Be target

In summary, the data presented in abbreviated form in Table IV gives the sputtering rates for several conditions. Highly stressed films are produced. The magnitude of the stress was found to be largely independent of gas pressure, gas composition and substrate temperature. The stress scaled approximately with film thickness. The rate of deposition was somewhat dependent on temperature. It should also be remarked that the rates observed were far slower than those observed for most insulators.

Scatter in these data was about ±15% in the sputtering rates for the beryllium oxide target (the last two data entries in the table). This scatter we believe to be attributable to a variation in the density of the sintered BeO target. This effect has been observed with other sintered targets and with metal targets which have been sputtered for several tens of hours. The metal targets developed a very rough mary-faceted polycrystalline surface with a real area far larger than the apparent geometrical area. Polishing the roughened metal surface resulted in higher rates essentially identical with the original rates observed over the early life of the target.

The conclusions deduced are that: (1) beryllium oxide sputters more slowly than most insulators; (2) in general, beryllium oxide deposited by rf sputtering from an oxide target or by reactive rf sputtering is highly stressed; (3) varying substrate temperature for either type of deposition has only a modest effect on deposition rate; (4) stress is relatively unaffected by substrate temperature; (5) varying oxygen-argon ratio during reactive sputtering has little effect on depositions rate; (6) varying oxygen-argon ratio has little effect on stress level.

5.0 SUGGESTIONS FOR FUTURE WORK

5.1 Multilevel Interconnect Technology

The data collected for this report only "scratches the surface" for the use of aluminum based metal alloys for interconnects. The metallurgists have investigated extensively literally dozens of binary as well as multicomponent systems based on aluminum. Many have been seen to be resistant to creep and fatigue. High values of hardness have been found to be characteristic of some of these alloys. Aluminum has been strengthened by small additions of iron to form a dispersed intermetallic phase. These alloys maintain reasonably good electrical conductivity at the same time as their strength increases. Because of the similarity between creep and fatigue behavior and the processes associated with electromigration, these alloy systems developed already for their improved mechanical properties should be evaluated in film form for their electromigration susceptibility. The sputtering process is uniquely suited for deposition of these multicomponent materials without changing composition. Just as sputtered 4% copper in aluminum was seen from the data in this report to exhibit marked reduction in electromigration susceptibility over pure aluminum, other copper additions in sputtered films can be expected to show the same kind of improvement. More data on sputtered aluminum-copper films is necessary over the range 1% to about 12% copper.

The relative importance of film thickness ratio to surface area has not been unequivocally established. A series of films with varying surface area but constant cross-section should be evaluated for electromigration susceptibility. That the overcoating of the metal film with silicon dioxide increases the life under high current density strongly suggests a surface migration effect inhibited by sputtered coatings.

5.2 Beryllium Oxide Sputtering Technology

Thicker layers of beryllium oxide must be deposited in order to have the broadest utilization in heat sinking. The stresses in the films of beryllium oxide limit use to 1.0 micrometer thick layers or less at present.

Bias sputtering has been shown to stress-relieve molybdenum films deposited by dc techniques. There is every reason to believe that a small rf bias on the substrate holder will also relieve stresses in beryllium oxide films. This technique should be applied to the beryllium oxide deposition under both reactive sputtering conditions and non-reactive conditions.

In the event stresses are eliminated by the bias sputtering process, an extension from thick film polycrystalline depositions to thick film single crystal films should be made. Much effort has already been expended on epitaxial growth of thin film single crystal semiconductors on single crystal beryllium oxide for heat sinking improvements. The same effect can be realized through a low temperature single crystal film deposition on the single crystal semiconductor. An investigation of this possibility has good potential.

With low stress polycrystalline beryllium oxide in hand, substrates other than silicon should be evaluated for beryllium oxide adhesion. Gallium arsenide, gallium phosphide, aluminum, gold, and aluminum oxide are all materials used in electronics device manufacture and should be included in such an evaluation.

Given success in these polycrystalline film deposition a program to develop etching techniques for various applications should be pursued. In particular, beryllium oxide for multilevel interconnects should be investigated for improvement in electromigration performance of metals overcoated with it. The improved thermal conductivity should result in lower metal interconnect temperature and a longer metal life under high current stress.

6.0 SUMMARY

This program in applications of rf sputtering to electronics was in two concurrent phases - one dealt with multilevel interconnect technology utilizing rf sputtering, the other dealt with rf sputtering of beryllium oxide for heat sinking applications.

For the multilevel interconnect technology, pure aluminum and a 4% copper in aluminum alloy were deposited by rf sputtering. These two metals were compared for electromigration susceptibility at temperatures of 200°C and greater and at a current density of 4.6×10^6 amps/cm^2. Specimens bare and covered with sputtered silicon dioxide were compared. Sputtered silicon dioxide about 1.5 micrometers. thick increased the mean life of the metal strips about 5 times. Addition of 4% copper to pure aluminum increased the lifetime more than a factor of 25.

A test cell was devised for evaluation of silicon dioxide in a multilevel configuration. Three layers of rf sputtered metal interconnections and two layers of rf sputtered silicon dioxide were incorporated in the test cell along with feedthroughs connecting first and second level metal and connecting second and third level metal. Perfect cell yield of 70-80% was observed. Fault identification show fewer than 10^4 metal-metal shorts between levels in 10^5 crossovers 0.001" x 0.001" and 1 in 10^4 improperly etched feedthroughs. Feedthrough resistance made a negligible contribution to a series of 140 feedthroughs produced in the pattern.

In sum a viable process for multilevel interconnects was developed. Silicon dioxide sputtered at a substrate temperature of 200°C controlled by gallium heat sinking to a heater block, at argon pressure of 5 millitorr, and at a power density of 14 watts/in^2 was demonstrated to have appropriate etching characteristics and to be virtually free of pinholes. Pure aluminum and 4% copper in aluminum were shown to be compatible with the silicon dioxide process and to give good level-to-level electrical contact at feedthroughs sputter cleaned just prior to the metal deposition.

Beryllium oxide was deposited by rf sputtering from a beryllium oxide target and by reactive rf sputtering from a beryllium target using oxygen-argon mixtures. In both cases stress levels in the films deposited were very high, producing pronounced bowing of substrates. Layers on the order of 2 micrometers thick shattered silicon substrates 5 centimeters in diameter and 325 micrometers thick. Reactively sputtered films deposited at about 3000Å/hour while films rf sputtered from a beryllium oxide target deposited at a rate of about 6500Å/hour for 500 watts into a 3.5 inch diameter target.

APPENDIX A

Wafer preparation prior to SiO_2 deposition

A. Particulate Contamination Removal

Clean substrates are placed face up on some clean, flat surface and one or two drops of acetone are applied near the far edge. A properly sized 5 mil thick sheet of cellusose acetate (electron microscopists replicating tape) is pressed against the flat supporting surface behind the substrate and rolled smoothly forward, sweeping the acetone across and completely filling the gap between the wafer and the tape. It is important here to use just the right amount of acetone because too much or too little will result in film contamination during the quartz sputtering operation. Too much acetone will overflow the substrate and carry dissolved acetate to the backside where it will deposit when the acetone evaporates. Too little acetone results in bubbles or incomplete coverage with a thin layer of acetate deposited at the edge of bubbles and the boundaries between covered and uncovered areas.

Drying time for the taped wafers is about ten minutes, after which the acetate film is peeled from the wafer.

This procedure is carried out twice on each substrate. After the second taping, however, the acetate is left in place during gallium application to permit wafer handling and protect the front against gallium contamination.

B. Gallium Application and Loading

In the following operations, it may be necessary to warm all of the components slightly above room temperature to prevent the gallium from freezing. (gallium container, substrates, and substrate holder).

Using the cellulose acetate applied previously as a handle, liquid gallium metal is brushed on to the back surface of the substrates. The area to be covered is a circle about three quarters of an inch in diameter centered on the back surface of the wafer. Care must be taken to completely wet the required area with as little gallium as possible.

Excess gallium (from the previous run) must be removed from the substrate holder and fresh metal applied. Here also it is important to completely wet the holder. However, a slight excess of the liquid metal should be applied to the center of the pedestal.

After the substrate and substrate holder are prepared the gallium coated surface of the substrates are placed in contact with the pedestals. Again using the acetate as a handle the wafers must be moved around on the pedestals (primarily rotary motion) until almost all of the air has been squeezed from under the wafers. Any lateral motion must be kept small enough so that the gallium is not spread beyond the spatter barrier on the substrate holder. Once all the wafers are in place on the holder, the acetate handles are removed and replaced with a single sheet of acetate. With this sheet in place as protection during transporting, the substrate holder is mounted in the sputtering system. Removal of this sheet is the last thing that occurs prior to closing the sputtering system.

All of the above operations should be performed in an area that is as dust free as possible. The tape application is best done in a vertical flow, filtered laminar exhaust hood and the sputtering system should be enclosed in a horizontal flow, filtered laminar clean station.

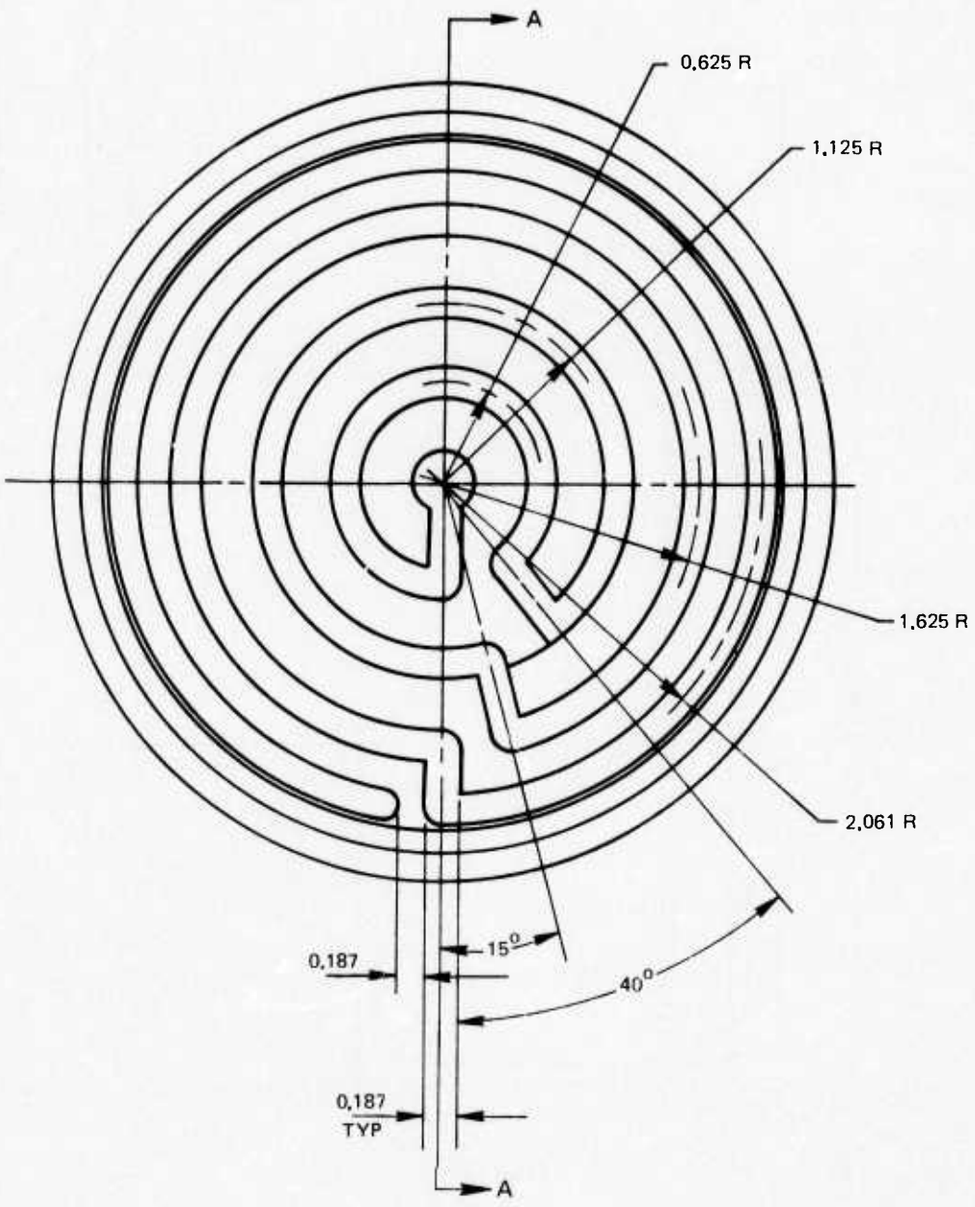
C. Vacuum System Hardware

R.F. cathodes used in this program whether functioning as substrate holders for sputter cleaning or as deposition sources, are constructed in a similar way. Figs. A-1 and A-2 show plan and sectional views of the parts of a five inch diameter cathode. The front and back sections are brazed together with a stainless steel disc separating the cooling channels. Simultaneously a quarter inch diameter pipe is brazed over a hole in the center of the stainless plate and a concentric half inch diameter pipe is brazed into the half inch socket in the cathode back. The cooling channel thus formed is continuous from the quarter inch input pipe, meandering through the front plate passing through a hole near the edge of the stainless steel disc, meandering through the back plate, to the half inch output pipe. The concentric pipes then pass through a vacuum seal and serve as both R.F. input and cooling water input/output (see also Fig. A-6).

The substrate heater used in the SiO_2 deposition system is assembled by brazing the substrate heater front (Fig. A-3) to the substrate heater clamp back (Fig. A-4) using the 0.750 stub as a guide. The quarter inch input and output pipes are brazed during the same operation. Assembly is completed by laying a 1/8 dia. heating coil in the groove on the substrate heater clamp back and clamping in place with a six inch diameter stainless steel disc and bolt. In use, the substrate holder (Fig. A-5) is bolted to the flat face of the substrate heater front.

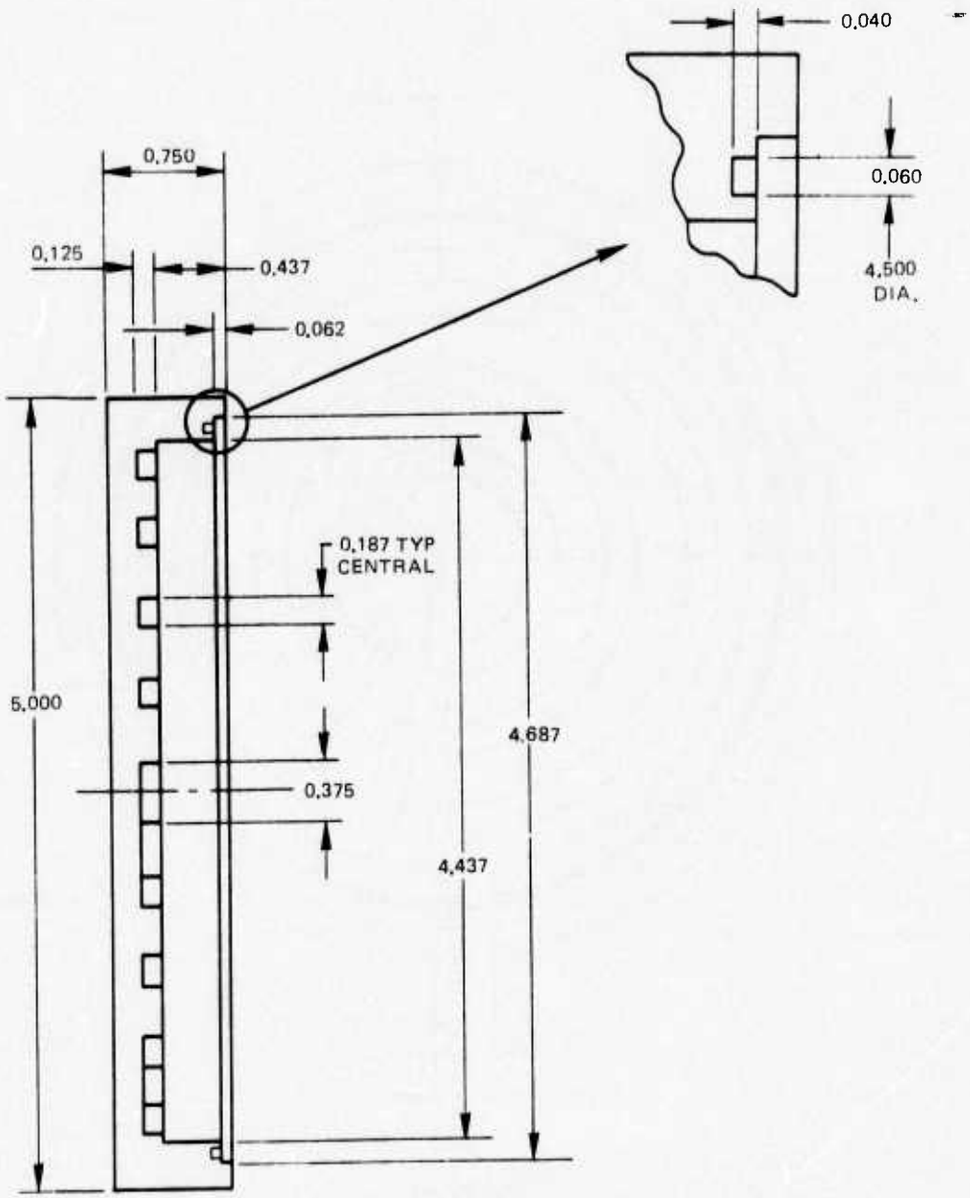
FIG. A –1

CATHODE FRONT



N12–114–1a

CATHODE FRONT (CONT.)

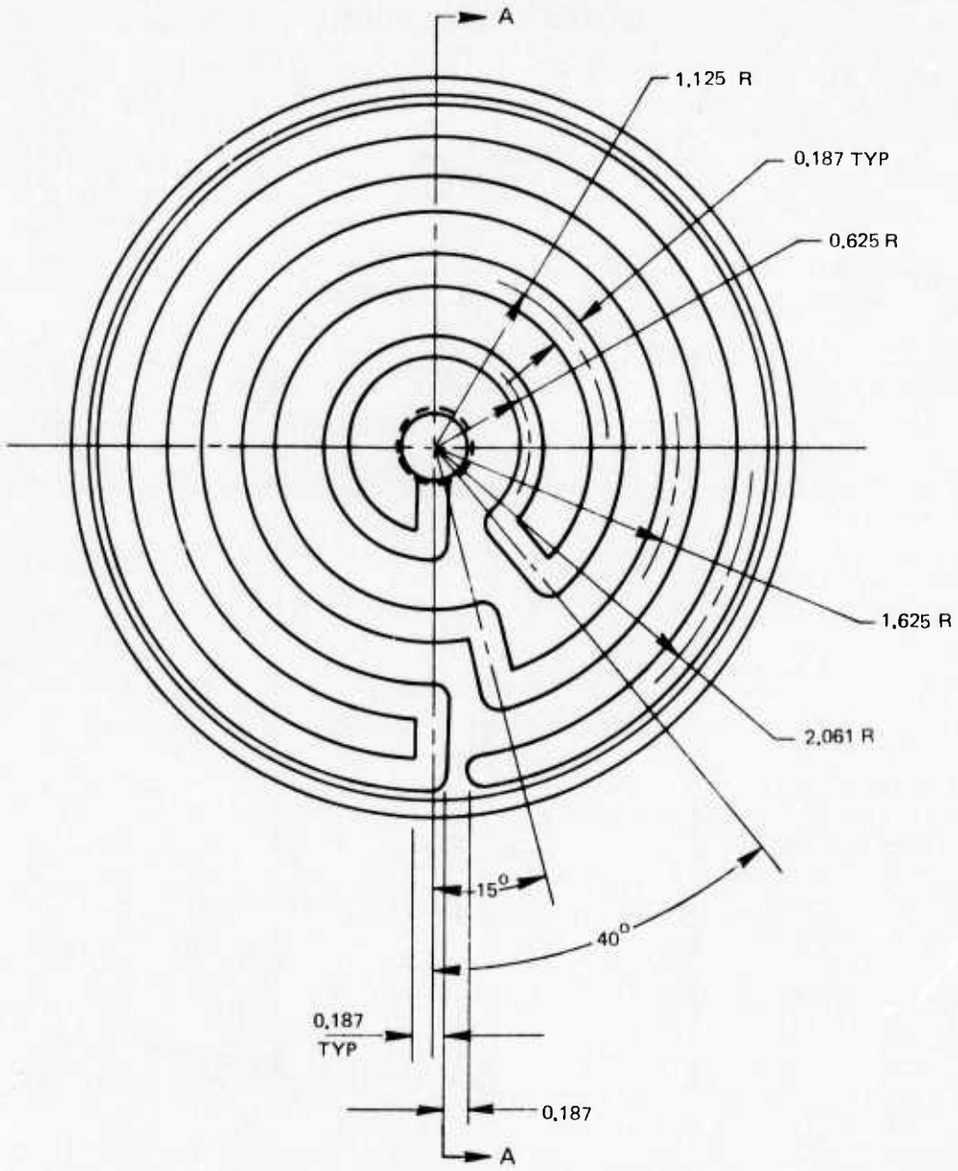


SECTION A-A

N12-114-1b

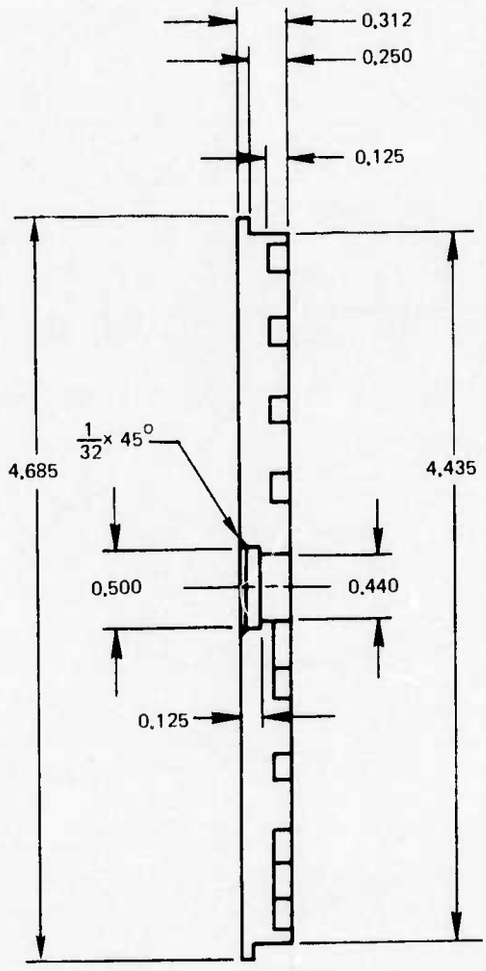
FIG. A–2

CATHODE BACK



N12–114–4a

CATHODE BACK (CONT.)

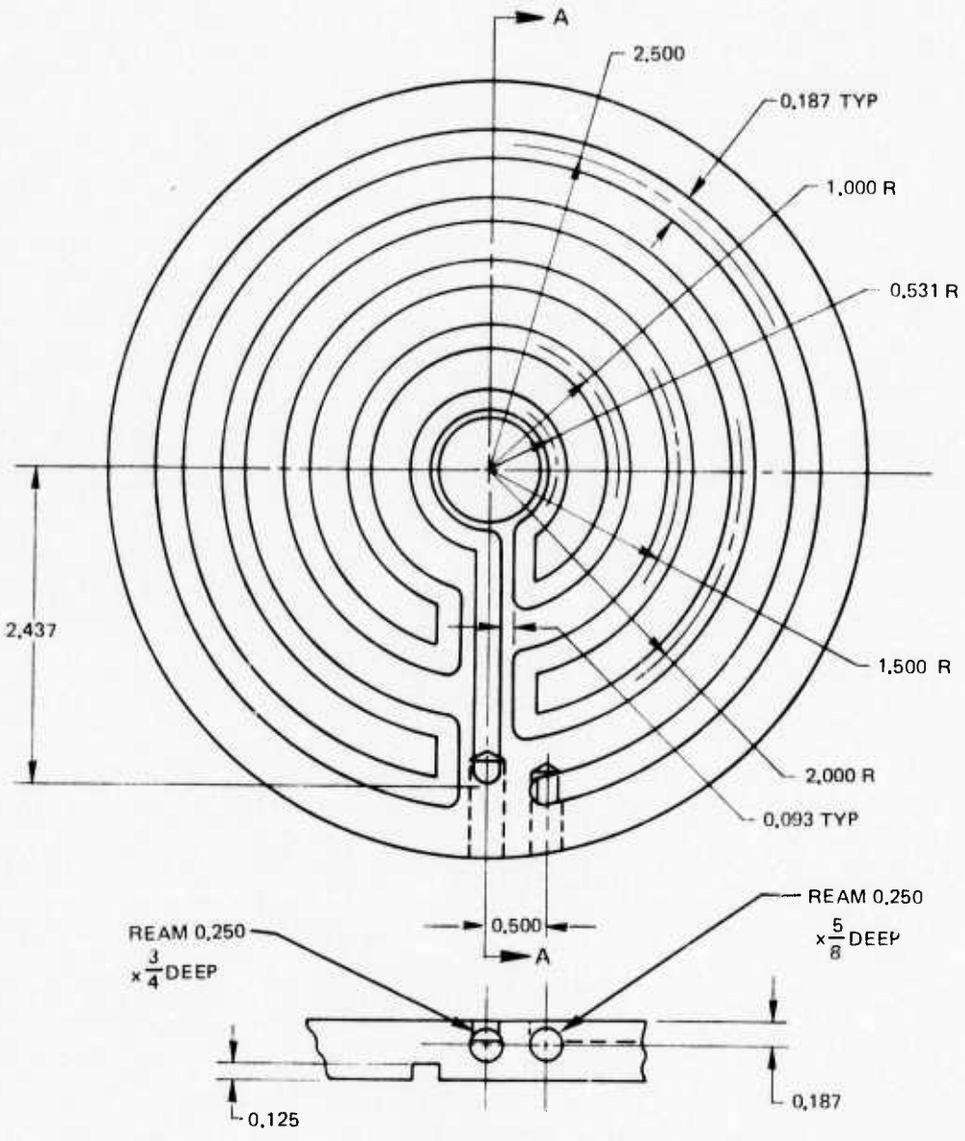


SECTION A–A

N12–114–4b

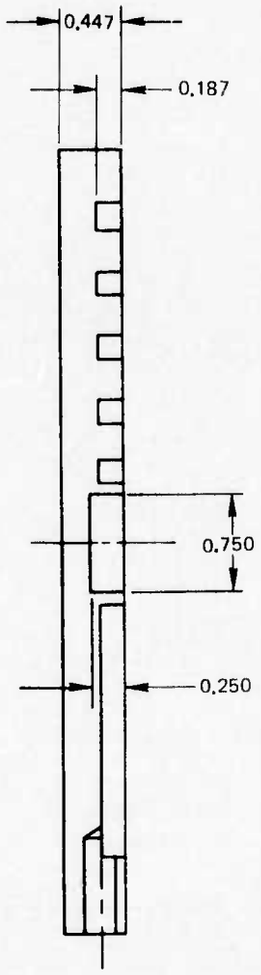
FIG. A–3

SUBSTRATE HEATER FRONT



N12–114–2a

SUBSTRATE HEATER FRONT (CONT.)

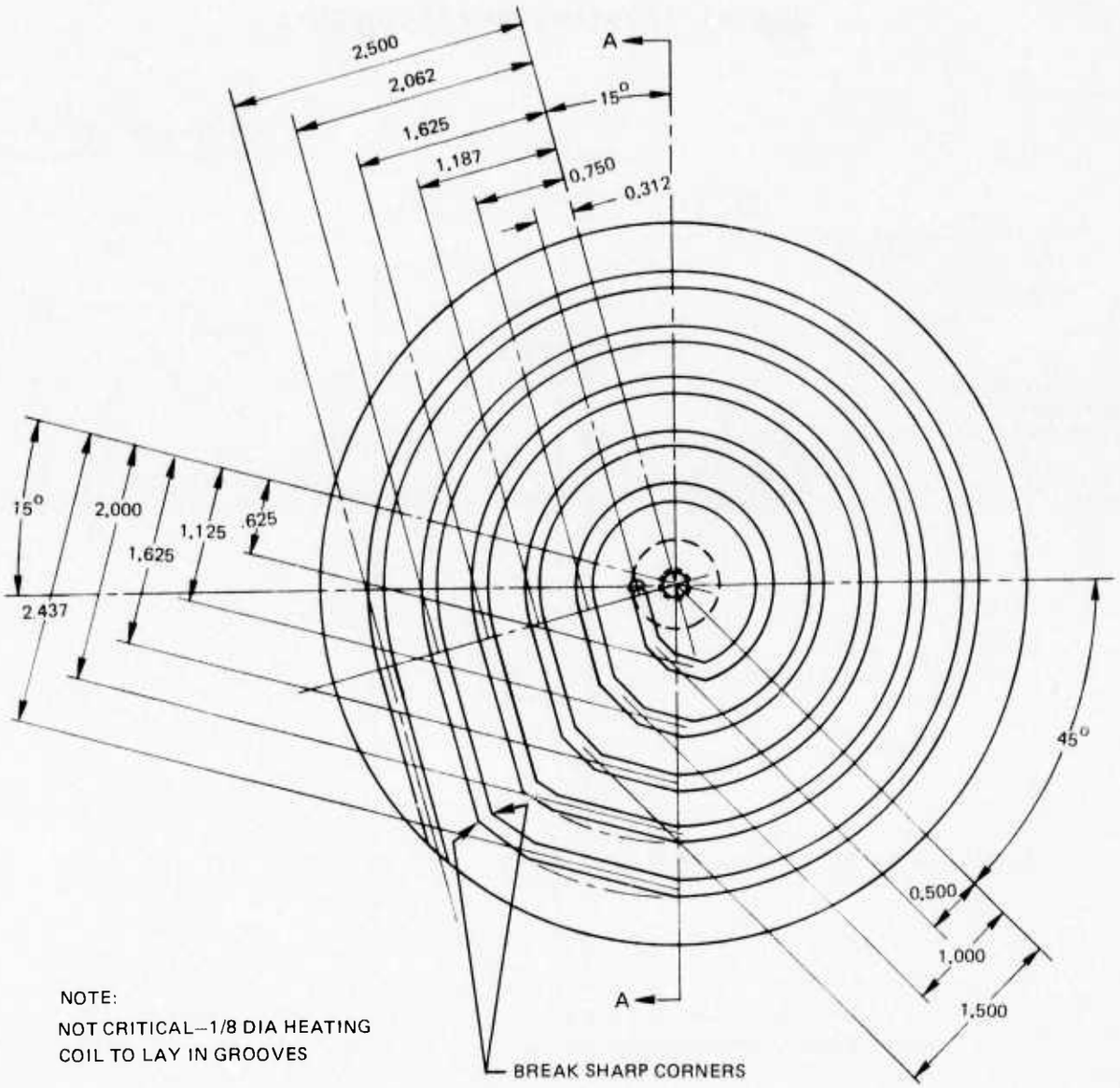


SECTION A–A

N12–114–2b

FIG. A–4

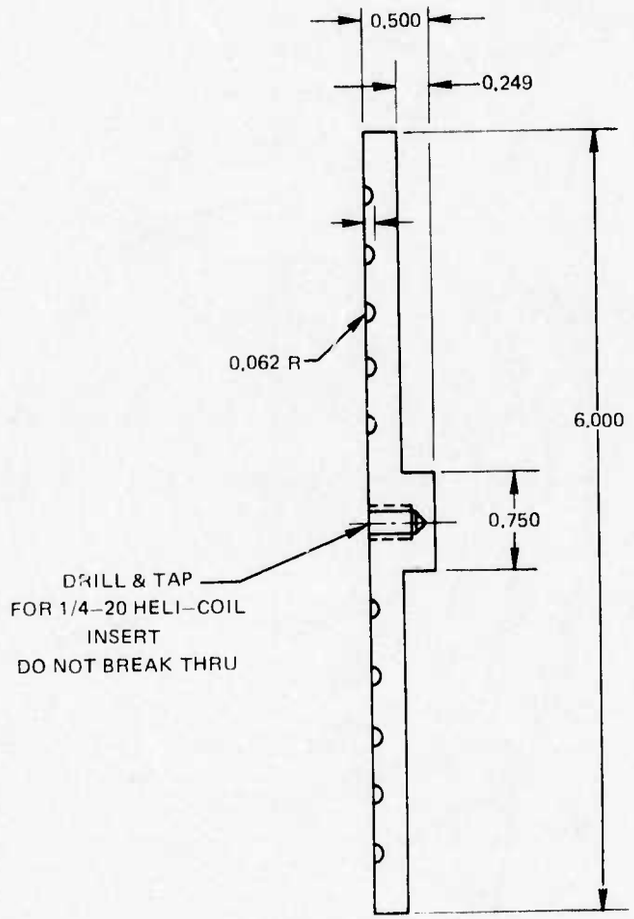
SUBSTRATE HEATER CLAMP BACK



NOTE:
NOT CRITICAL–1/8 DIA HEATING
COIL TO LAY IN GROOVES

N12–114–3a

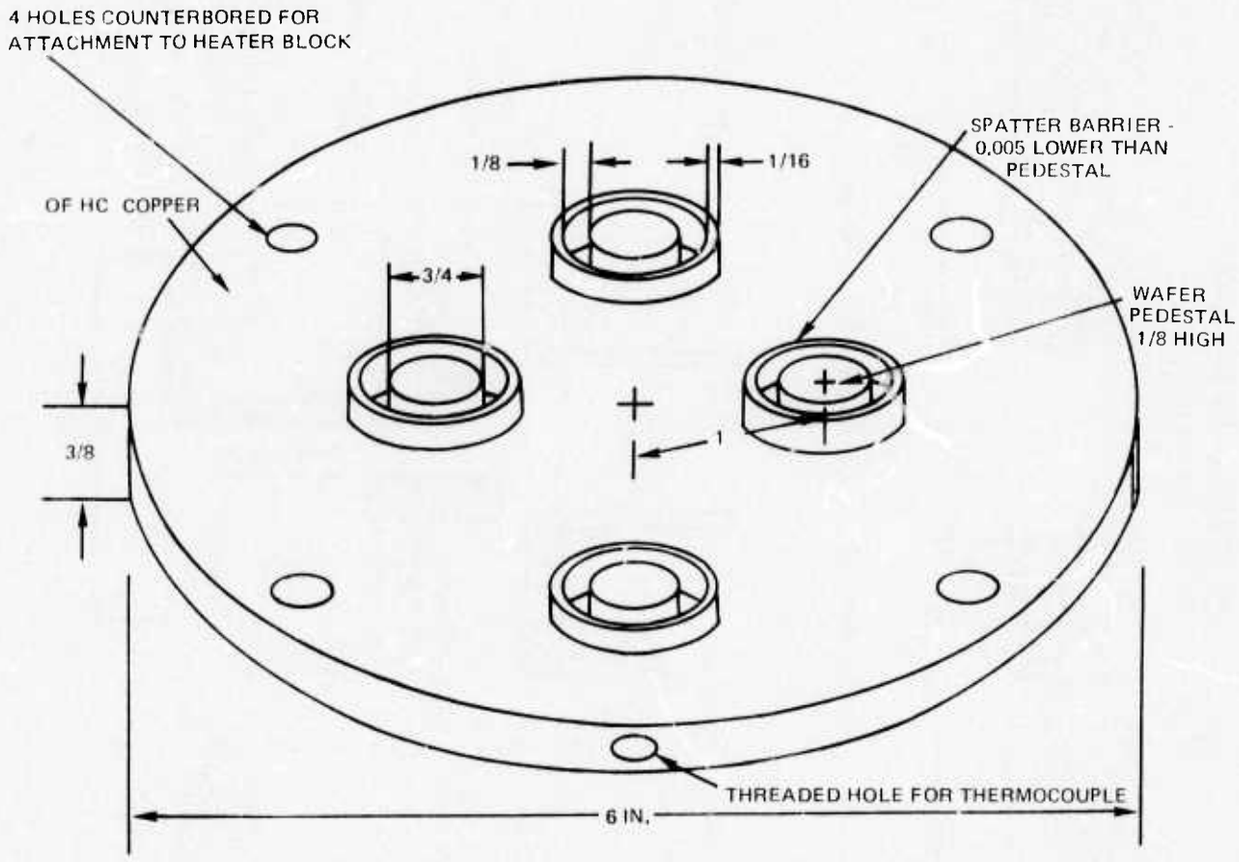
SUBSTRATE HEATER CLAMP BACK (CONT.)



SECTION A–A

N12–114–3b

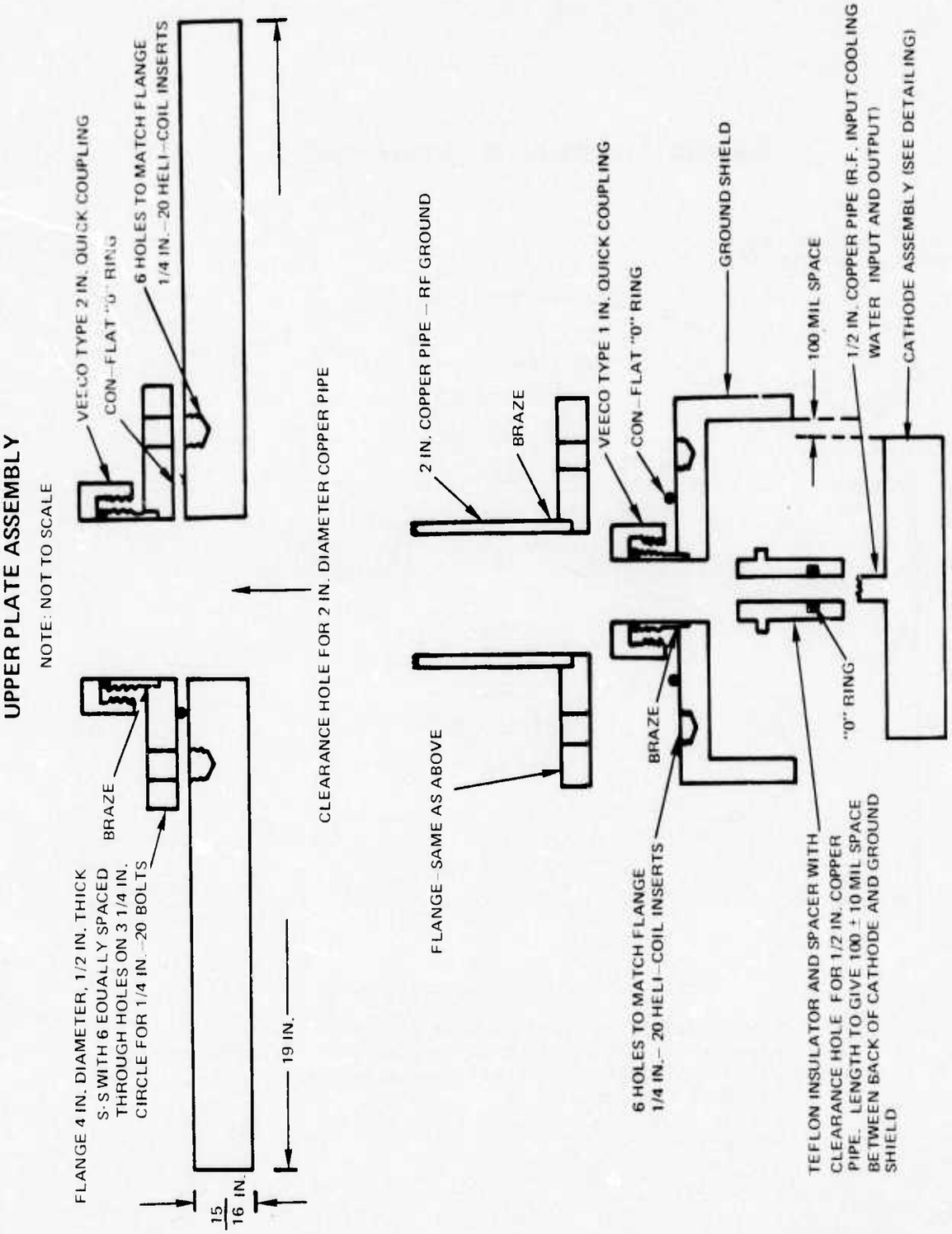
SUBSTRATE HOLDER FOR 1 1/4 DIA WAFERS



NOTE: 1. DURING S_1O_2 DEPOSITION, A 1/16 THICK S.S. SHIELD WITH 4 HOLES TO FIT OVER 1 1/8 DIA SPATTER BARRIERS AND WITH A STRAIN RELIEF SLOT FROM THE CENTER TO THE EDGE MUST BE USED
2. DRAWING NOT TO SCALE

N12–150–1

FIG. A-6



N12-150-2

APPENDIX B

Silicon dioxide was etched in a buffered hydrofluoric acid solution prepared by mixing 35 parts by volume of concentrated hydrofluoric acid with 215 parts of 40% ammonium fluoride solution.

Photoresist used for feedthrough etching in silicon dioxide is KTFR. Wafers coated with SiO_2 are dipped in a 1% solution of dimethyldichlorosilane in trichloroethylene and dried. Phenyldichlorosilanes may be used with equal if not better results. These materials act as bridges between the silicon dioxide and the photoresist to provide good adhesion between the two. Standard spinning, drying, exposure and developing conditions can be used for the photoresist. (See Appendix A, for example).

APPENDIX C

The etch for aluminum and for aluminum -4% copper used in this program and found to be entirely effective is a mixture of 10 parts by volume of concentrated nitric acid to 90 parts by volume of phosphoric acid. A few drops of Triton X (a 3M product) per 100 cm^{-3} of the mixture is added just before etching.

KTFR is the photoresist used diluted 1:1 with Kodak Thinner. The thinned resist is spun on at 2500 rpm for about 15 seconds to dry. A layer about 8000Å in thickness is produced. The KTFR is baked at 90°C for 10 minutes to remove last solvent. Patterns are produced in the resist by exposure through photomasks for up to 10 seconds while the plate and coated wafer are under a nitrogen blanket. After exposure, the resist is developed by dipping in KTFR developer and spray rinsed. A 30 minute bake at 90°C follows. The metal etching is effected at 90°C in the etch already described. The etch solution is agitated with a stream of gas bubbles. Rinsing with distilled water follows with spin drying. J-100 stripper is used to remove the KTFR.

APPENDIX D

WEIBULL ANALYSIS OF TEST DATA

When we analyze data we put it in order. The data may be placed in alphabetical groups, numerical ranks, or in some other order. We then examine the groups to see if there are simple or systematic relationships in order corresponding to the observed output. It may be possible to describe these relationships with a line on a graph, or with a few symbols. If we can establish and describe the relationships we can say the analysis has added to the meaning and usefulness of the original data.

Data points from tests or measurements can be plotted to show the frequency distribution with a selected independent variable, such as weight, length, or time. This histogram will show how many times each value of the variable is likely to occur. We may find we have an exponential distribution, or the familiar "normal" distribution, or something else. If the distribution curve were known, then we could define mathematically the product reliability, quality, or conformity. A very useful distribution curve was suggested by Waloddi Weibull in 1950. The analysis entails the plotting of data points on a specially prepared graph paper now called Weibull probability paper. A few simple measurements then directly provide the shape and position

parameters of the distribution curve. The scales on the Weibull probability paper are laid out to display the three parameters that define the distribution curve:

β , the Weibull Slope

η , the characteristic life

t_o , the starting point of the curve.

Direct measurements on the paper can be made to determine a product's reliability.

This system of analysis is based on a mathematical model known as the Weibull equation:

$$F(t) = 1 - e^{-\left(\frac{X}{\eta}\right)^{\beta}} \qquad (1)$$

where:

$F(t)$ = Cumulative probability of failure (the area under the distribution from t_o to t).

β = Weibull slope

η = Characteristic life

t = Random variable (time, stress, size, cycles, etc.)

t_o = Origin of the distribution

The probability density function f(t) is equal to $\frac{d\,F(t)}{dt}$, the ordinate of the frequency distribution.

$$f(t) = \frac{\beta\,(t - t_o)^{\beta - 1}}{\eta^{\beta}}\; e^{-\left(\frac{t - t_o}{\eta}\right)^{\beta}} \qquad (2)$$

Some of the possible distributions of f(t) are shown in Figure 1.

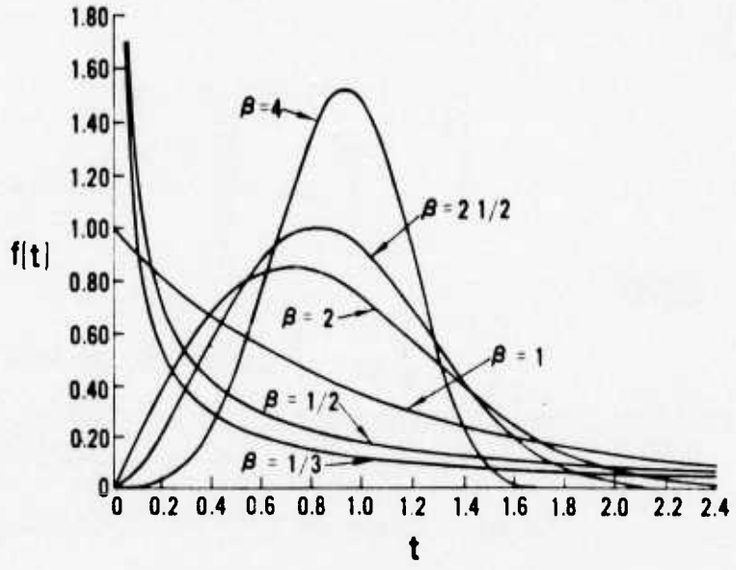


Figure 1 Possible Distributions of f (t).

DERIVATION OF THE RELIABILITY EQUATION

The flexible form of the Weibull equation can be understood by studying a rigorous, but general, mathematical model.

$$\text{Reliability (R)} = \frac{N}{N_o} = \frac{N_o - r}{N_o} = 1 - \frac{r}{N_o} \qquad (3)$$

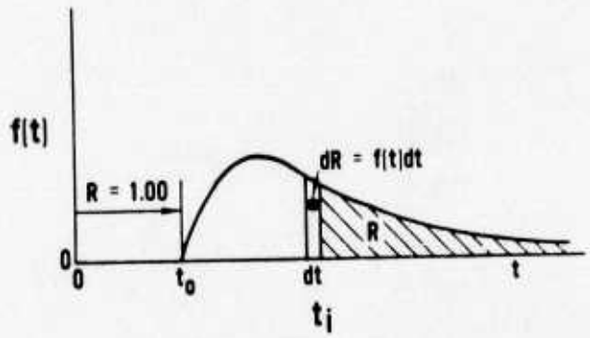
Where N_o is the number of units tested, r is the number failed and N is the number surviving.

In Figure 2 the unit cannot fail between 0 and t_o, hence R = 1.00; we

can say the product is 100% reliable before time t_o.

START

$$R = \frac{N}{N_o} = \frac{N_o - r}{N_o}$$



RESULT

$$R = e^{-\int_0^{ti} \lambda dt}$$

WHERE λ = FAILURE RATE

Figure 2 Picture of ony Distribution.

Taking the derivative of $R = 1 - \frac{r}{N_o}$ with respect to time

$$\frac{dR}{dt} = \frac{d}{dt}\left(1 - \frac{r}{N_o}\right) = \frac{1}{N_o}\frac{dr}{dt}$$

$$\frac{dr}{dt} = -N_o \frac{dR}{dt}$$

Dividing by N to get the rate of failure per unit still being tested:

$$\frac{1}{N}\frac{dr}{dt} = -\frac{N_o}{N}\frac{dR}{dt} = -\frac{1}{R}\frac{dR}{dt}$$

The rate of failure is referred to by a Greek symbol λ, called the instantaneous failure rate or the hazard rate.

$$\frac{1}{N} \quad \frac{dr}{dt} = \lambda$$

By substitution

$$\lambda = - \frac{1}{R} \quad \frac{dR}{dt}$$

$$\frac{1}{R} \quad \frac{dR}{dt} = - \lambda$$

$$\frac{dR}{R} = - \quad \lambda \quad dt$$

$$\int_1^{R_{t_i}} \frac{dR}{R} = - \int_o^{t_i} \lambda \ dt \qquad \text{when } t_o = 0,\ R = 1.00 \text{ and when } t = t_i,\ R = R_{t_i}$$

Integrating R

$$\ln R_i = - \int_o^{t_i} \lambda \ dt$$

$$R_{t_i} = e^{- \int_o^{t_i} \lambda \ dt} \qquad (4)$$

Equation (4) is a mathematical expression for the reliability of any failure mode at time t_i, but only useful if we know the equation for λ as a function of t. If λ is a constant, not a function of time, the $R_{t_i} = e^{- \int_o^{ti} \lambda \ dt} = e^{- \lambda t_i}$. This is the well known exponential expression for reliability. Weibull noticed that a great variety of data distributions seemed to fit an expression of the form $R_{t_i} = e^{- \left(\frac{t_i - t_o}{\eta} \right)^{\beta}}$ where $\left(\frac{t_i - t_o}{\eta} \right)^{\beta} \approx \int_o^{t_i} \lambda \ dt$ This is the Weibull model. His approximation of expression (4) has three parameters.

1. β describes shape of the distribution or the (slope on Weibull probability paper).
2. t_o = starting point or origin of the distribution
3. η = characteristic life

*NOTE: β and η must be greater than 0.

Figure (3) shows a distribution curve with a Weibull slope of 2 and two different characteristic lives. These distributions would appear as two parallel lines on Weibull probability paper with the line containing the greater η lying on the right. In these cases failure can begin to occur at $t_o = 0$. Be aware that some products like car batteries can fail before they are installed, and others, like a work-hardening material, can fail only some time after testing starts.

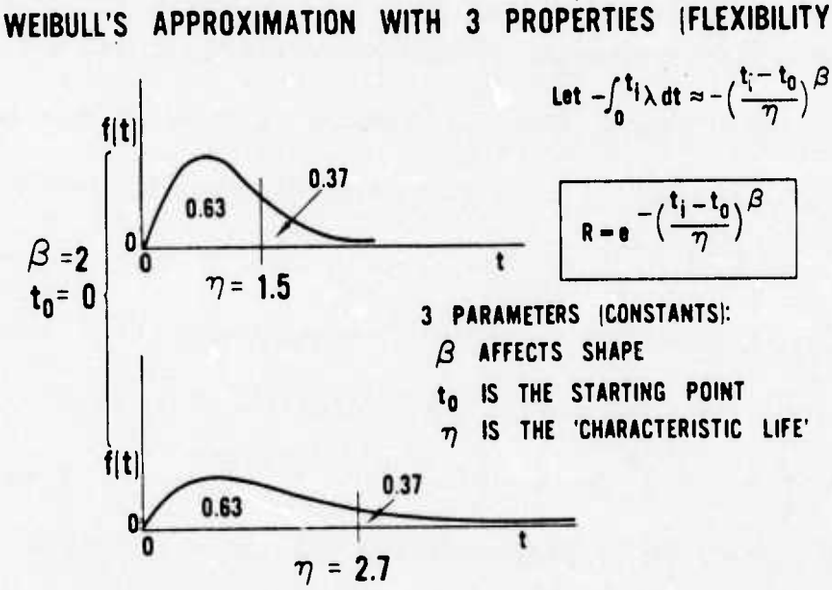


Figure 3 Effect of Characteristic Life on Distribution.

An interesting result occurs in the Weibull equation when $t_i - t_o = \eta$

$$R = e^{-\left(\frac{\eta}{\eta}\right)^{\beta}}$$

$$R = e^{-(1)^{\beta}}$$

$$R = e^{-1} = 0.37$$

The reliability is always 0.37 at the characteristic life. This is true for any value of β since 1 taken to any power is still equal to 1.

When test data is plotted on Weibull probability paper the three parameters can be estimated without involved mathematical calculations.

The basis for the design of Weibull probability paper is as follows:

$$R = e^{-\left(\frac{t_i - t_o}{\eta}\right)^{\beta}} \qquad \text{Let } t_o = 0$$

$$R = e^{-\left(\frac{t_i}{\eta}\right)^{\beta}}$$

$$\frac{1}{R} = e^{\left(\frac{t_i}{\eta}\right)^{\beta}}$$

$$\ln \frac{1}{R} = \left(\frac{t_i}{\eta}\right)^{\beta}$$

$$\ln \ln \frac{1}{R} = \beta \ln t_i - \beta \ln \eta \qquad (5)$$

$$y = A x + B$$

This last equation is in the form of a straight line where A and B are constants. Notice that the line's slope $A = \beta$. Using Weibull probability paper, the Weibull distribution will be represented by a straight line. Changes in the slope β correspond to changes in the shape of the Weibull distribution. On Weibull probability paper the slope of the

fitted straight line can be directly measured. From algebra we remember that the slope is $\frac{y_1-y_o}{x_1-x_o}$. By superimposing a sheet of regular transparent graph paper over the Weibull paper we can easily determine the slope.* Figure 4A shows that by moving 1 unit on the t axis and measuring the change in F, the slope is $\frac{2}{1}$ or 2. Figure (4B) shows the same method but with a slope of $\frac{5}{1}$ or 5. The corresponding failure distributions are shown above 4A and 4B

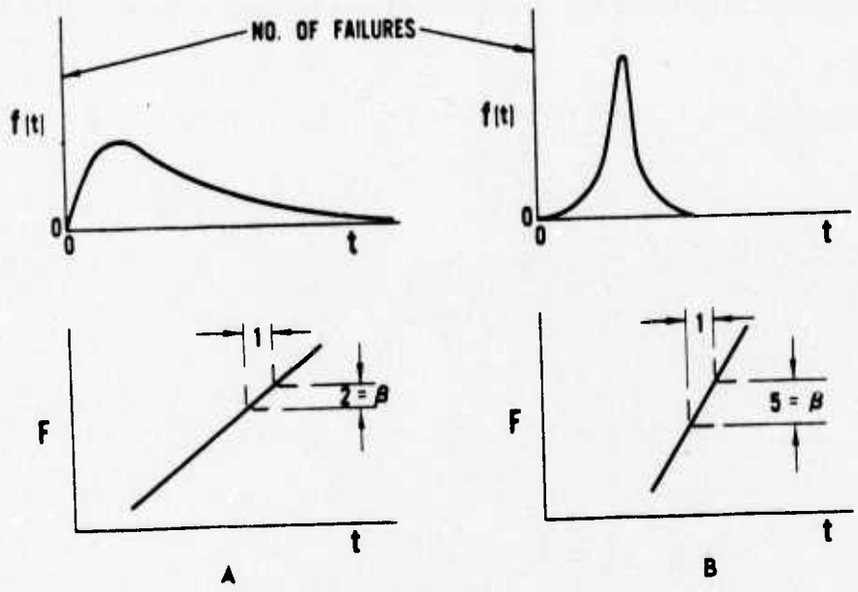


Figure 4 **Effect of Weibull Slope on the Distribution Curve.**

Characteristic failure distribution curves, defined by values of β are shown in Figure 5 For any value of β less than or equal to 1.0 the frequency distribution of failures is a curve which starts at a high frequency at t = 0 and approaches zero as t approaches infinity. Two

* This superimposition will only work when a β of 1 makes a 45° angle with the abscissa.

examples are shown with $\beta = 0.5$ and $\beta = 1.0$. When $\beta = 1$ we have the "exponential-life" distribution.

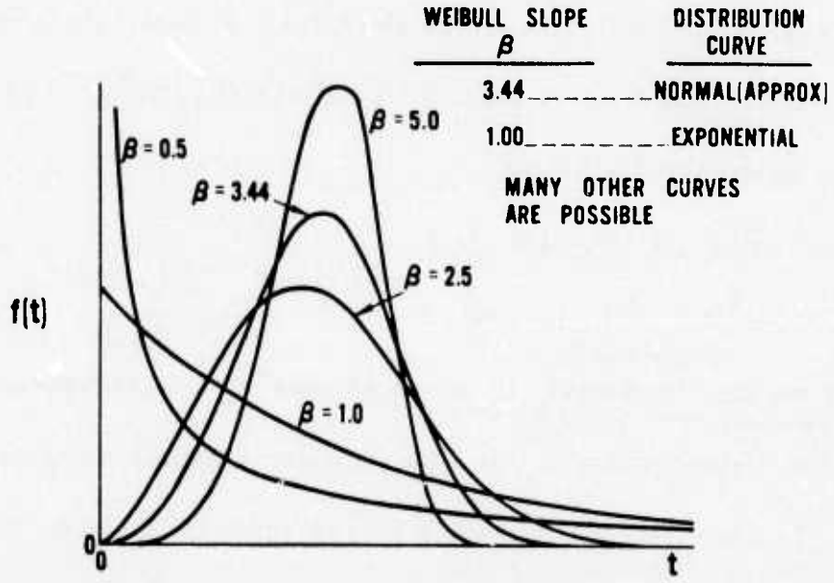


Figure 5 Characteristic Failure Distribution Curves.

When β is greater than 1.0, the origin of the distribution curve starts at a frequency of zero failures. For values of β slightly greater than 1.0, the frequency distribution is highly skewed with a long tail to the right. The distribution becomes essentially symetrical as β approaches 3.44 and becomes more sharply peaked with reverse skewness as β increases beyond 3.44. When $\beta \approx 3.44$ the values of the mean and the median of the distribution are equal and in this special case we have nearly a one-parameter normal distribution.

The two parameters β and η respectively identify the shape of the distribution and the point where 63% of the population will have failed. For other analytical studies, such as the t-test, F-test, etc., we must determine the average time to failure ($\bar{t}$) and variance (s^2). The general formula for each is given below.

$$\bar{t} = \eta \, \Gamma \left(1 + \frac{1}{\beta}\right)$$

$$s^2 = \eta^2 \Gamma \left(1 + \frac{2}{\beta}\right) - \eta^2 \left[\Gamma\left(1 + \frac{1}{\beta}\right)\right]^2$$

Previously we said that when $\beta \approx 3.44$, the median and mean are equal and the Weibull distribution closely approximates a normal distribution. To show this we replace t by $\bar{t}$ in equation 1 and calculate $F(\bar{t})$ for various values of β

$$F(\bar{t}) = 1 - e^{-\left(\frac{\bar{t}}{\eta}\right)^{\beta}}$$

or

$$F(\bar{t}) = 1 - e^{-\left[\Gamma\left(1 + \frac{1}{\beta}\right)\right]^{\beta}}$$

Figure 6 is a graph of $F(\bar{t})$ for various Weibull slopes. When $0 < \beta < 3.44$ the median is greater than the mean and the reverse is true when $\beta > 3.44$.

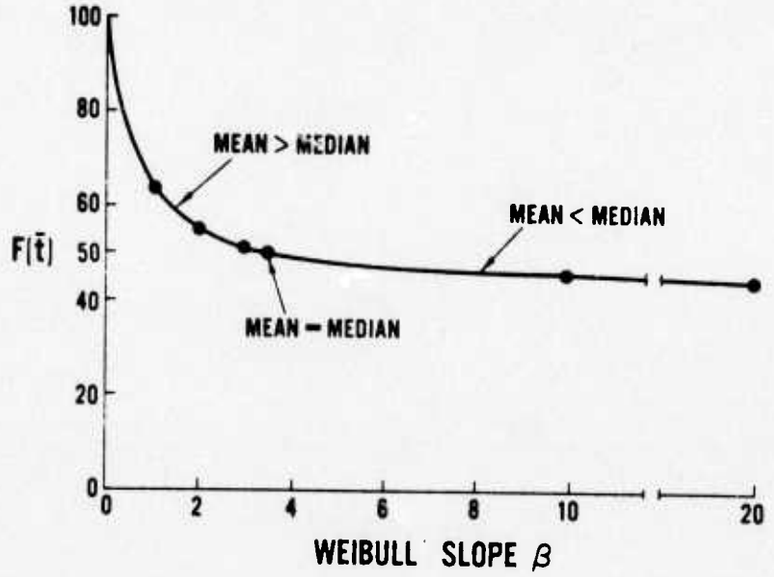


Figure 6 **Failure Probabilities with Varying Weibull Slope.**

ACKNOWLEDGEMENT:

The material in this section (Appendix D) is an excerpt from Pratt and Whitney Aircraft Division of United Aircraft Corporation, document PWA 3001, Introduction to Weibull Analysis by R. A. Mitchell, January 6, 1967.

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This report covers work under contract N00019-74-C-0256 for the period 1 January 1974 to 31 December 1974. A viable process for multilevel interconnects was developed. Silicon dioxide sputtered at a substrate temperature of 200°C controlled by gallium heat sinking to a heater block, at argon pressure of 5 millitorr, and at a power density of 14 watts/in^2 was demonstrated to have appropriate etching characteristics and to be virtually

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free of pinholes. Pure aluminum and 4% copper in aluminum were shown to be compatible with the silicon dioxide process and to give good level-to-level electrical contact at feedthroughs sputter cleaned just prior to the metal deposition.

Beryllium oxide was deposited by rf sputtering from a beryllium oxide target and by reactive rf sputtering from a beryllium target using oxygen-argon mixtures. In both cases stress levels in the films deposited were very high, producing pronounced bowing of substrates. Layers on the order of 2 micrometers thick shattered silicon substrates 5 centimeters in diameter and 325 micrometers thick. Reactively sputtered films deposited at about 3000Å/hr. while films rf sputtered from a beryllium oxide target deposited at a rate of about 6500Å/hr for 500 watts into a 3.5 inch diameter target.