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Final Technical Report
March 1975

# INTEGRATED SWITCHING/MULTIPLEXING/TECHNICAL CONTROL

Computer Sciences Corporation





Rome Air Development Center
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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This study is an investigation of the feasibility of combining the communication functions of circuit switching, multiplexing and technical control into a single transportable integrated communication complex suitable for use in a tactical environment. The communication system is intended for use in the 1980's when tactical networks will operate digitally. A tradeoff comparison is conducted to determine the relative merits of various candidate switch matrices with respect to size, weight, cost and power consumed and also

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the impact on the communication functions of transmission, common control, technical control, and signaling. The impact of integrating the technical control function into the communications complex is discussed with respect to quality monitoring and testing, fault isolation, alternate routing, and reporting and recordkeeping. Common processor requirements relating to the integration of technical control and switching functions are described. Program descriptions and memory sizing estimates are given for a baseline system for several different switch sizes.

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# 1.0 INTRODUCTION

## 1.1 OBJECTIVE

The objective of this engineering study is to investigate the feasibility of integrating the functions of switching, multiplexing, and technical control in order to decrease size, weight, and power requirements while increasing the operational reliability and mobility/transportability of a tactical communications complex. The communication system is intended for use in the 1980s when tactical networks will operate digitally. The ability to develop a self-supportable integrated communications facility of this type will decrease Air Force reaction time during contingencies and improve mission effectiveness by providing the Task Force Commander rapid and reliable communication in the tactical environment.

## 1.2 BACKGROUND

Switching, multiplex, and technical control equipments now in the military inventory and in the engineering development phase(s) will not fully and most effectively provide the Task Force Commander with a flexible and effective command control capability during tactical contingency deployments. One reason is that the equipment is not sufficiently selfcontained. The interoperation of the separate switching, multiplexing, and technical control facilities requires an excessive number of equipment shelters and associated interconnecting cables. The present approach to the problem is cumbersome and requires additional operation and maintenance support personnel and logistics support.

## 1.3 SUMMARY

### 1.3.1 Constraints and Assumptions

The work performed during this study program was based on the following set of constraints and assumptions.

1. The Integrated Switch/Multiplex/Technical Control (ISMTC) is to be used in the 1980 time frame when all-digital communications systems will be used. Thus, all input signals to the complex are assumed to be in a digital form.

2. Voice signals are digitally encoded using 32 kb/s Continuous Variable Slope Delta (CVSD) modulation exclusively. The use of PCM is not anticipated.

3. Terminal equipment data rates are expected to be $75 \times 2^n$ to a maximum of 9,600 b/s; higher rates will be 8000 x n b/s. "n" is an integral value in both cases.

4. The switch is expandable in increments of 150- to 300-line modules to a maximum of 2400 lines.

5. A maximum switch matrix blocking probability of 0.001 is maintained for average traffic loads up to 0.8 Erlangs per line.

6. The complex is transportable and designed for tactical use.

### 1.3.2 Summary and Conclusions

Based upon the above assumptions and constraints this study concludes that a transportable Integrated Switch/Multiplex/Technical Control (ISMTC) facility is feasible for the 1980 time frame. In fact the technology already exists which could support the development of such a communications complex.

The benefits to be derived from integration of the Technical Control (TC) function into the switch includes the elimination of the TC problems of separate siting, housing, power, processors, logistics, personnel, Red/Black areas, Tempest filtering, etc. The intercommunication facilities between TC and the switch are also eliminated. In addition, it should be noted that the integration of TC into the switch has little effect on matrix size, cost, and weight.

Matrix considerations are discussed in Section 2.0. Five candidate matrices are evaluated, one space division and four time division. Paragraph 2.1.1 describes a specific space division matrix fabricated from 4 x 4 four-wire matrix crosspoint integrated circuit chips. This provides the basis for the comparison of a space division array to the four time division approaches described in paragraph 2.1.2. A tradeoff comparison is conducted in paragraph 2.1.3 to determine the relative merits of each with respect to size, weight, cost, and power consumed and also the impact on the communication functions of transmission, common control, technical control, and signaling. It is concluded that the choice of a specific matrix type is relatively insensitive to the aforementioned communication functions and should be selected predominantly on the basis of cost, size, weight, and power requirements. A summary of the tradeoff results is given in Table 4 which indicates that Candidate 5 (Time-Space-Time) appears to be the favored choice. See paragraph 2.1.2.1.4 for a description of this candidate.

Various aspects of switch control such as common control, trunk barring, and line load control are presented in Section 2.2.

Section 2.3 describes the special service features of interest to the ISMTC control complex.

Section 3.0 deals with the multiplexing aspect of the ISMTC. It is concluded that time division switching and time division multiplexing should both be performed in an integrated time division matrix. The multiplexing scheme for the ISMTC is based on a bit-by-bit multiplexing of bit streams derived from CVSD subsets generating 32 kb/s per line. Groups are formed from the basic 32 kb/s line rate by a bit interleaving process.

A design approach is presented which distributes much of the multiplex equipment among the matrix, trunk group formatter, and line formatter. Multiplex/demultiplex equipment external to the switch is required for trunk groups greater than sixty channels and for groupings which are not certain multiples of 32 kb/s. Rates in the $75 \times 2^n$ category can be accommodated by the matrix after a retiming procedure performed by interface circuits.

In the technical control discussion of Section 4.0 it is assumed that the overall technical control structure is hierarchal in nature and is composed of the following four distinct elements:

1. System Planning and Engineering
2. System Control
3. Node Control
4. Equipment Support

This study is directed toward the analysis of the feasibility of incorporating the functions required of the Node Control and Equipment Support element into the common processor of the ISMTC.

A description of quality monitoring and testing applicable to the technical control function at nodes of a tactical communications network is included in Section 4.1. This description includes discussions related to:

1. Monitor Points and Parameters
2. Monitoring Regenerated Digital Signals
3. Monitoring of Non-Regenerated Digital Signals
4. Monitoring of Analog Parameters
5. Computer Processor Implications

Section 4.2 is directed toward the development of hardware considerations related to the fault isolation function of technical control. Emphasis is placed on the determination of the hardware required to isolate faults and system degradations of the transmission system. To illustrate the various concepts which may be used to implement the fault isolation function related to the transmission system, radio relay terminals are used for the purpose of discussion. The concepts described could be readily extended and applied to other types of terminals.

Several alternate routing schemes appropriate to the tactical Air Force Network are discussed in Section 4.3 for the purpose of evaluating processor implications.

Section 4.4 is devoted to the development of report formats for the technical control report and recordkeeping functions. Three types of reports are considered:

1. Maintenance Reports
2. Status Reports
3. Supervisory Reports

The section describes some of the factors which must be considered for the reporting and recordkeeping functions as well as typical report entries and formats.

Section 4.5 contains an investigation of the impact on switch design due to the integration of the technical control functions into the ISMTC. The analysis indicates that while the effects on the common processor are significant, impact on the switch matrix is moderate. The major effect is an increase in matrix size due to built-in matrix error detection equipment. An additional matrix impact could result from the implementation of a common transmission equipment monitoring scheme. It is concluded that the specific matrix type is relatively insensitive to technical control considerations and should be selected predominantly on the basis of switching and multiplexing factors.

Section 5.0 discusses the various aspects of an integrated complex. A system description of the overall nodal equipment configuration is given in Section 5.2. This includes a discussion of the various switch, technical control and input/output subsystem composing the ISMTC.

Section 5.3 discusses the type of orderwire to be used with the ISMTC. One 32-kb/s channel of a full 60-channel trunk group is sufficient to handle all signaling and supervision, remote status reports, continuous reporting to the Systems Control Element, and framing and synchronization. Periodic and aperiodic reports can be sent via "dial-up" lines when required. The 32-kb/s common channel is submultiplexed into four 8-kb/s subchannels as shown in Figure 55. This data rate capacity is more than adquate for handling the above-mentioned functions.

Common processor requirements relating to the integration of the technical control and switching functions are contained in Section 5.4. Program descriptions and sizing estimates are given for a baseline system for several different switch sizes. No specific processor(s) has been recommended but a section on desirable processor characteristics is included as well as a survey of applicable machines. In general, the conclusion reached from studying the various requirements indicates that current processor technology is capable of fully supporting the ISMTC. In fact, the risks involved in designing a processor from the operational characteristics viewpoint appear to be low. More risk appears in satisfying the stringent environmental and ruggedness specification. In this regard, the specifications of a presently available militarized minicomputer have also been included.

Section 5.5 presents a discussion on equipment procedural interfaces, internal and external interfaces, followed by descriptions of examples applicable to the interfacing of an ISMTC with the DCS. The worst case situation is considered, i.e., the basic systems will not be designed to be completely compatible. Therefore, the interface must be provided through the introduction of applique units which would be required at gateway interfaces.

The functions provided by the personnel assigned as switch operators, technical controllers, and installation and maintenance personnel are briefly described in Section 5.6. At present, most required actions are provided on a manual basis in tactical military communication networks. However, many of the required functions are readily adaptable to automation. Table 14 lists operation functions required in both manual non-integrated facilities and in an ISMTC applicable to the tactical networks of the 1980s and indicates which functions can be aided by automation.

A short discussion of Red/Black considerations is included in Section 5.7.

Transportability requirements are analyzed in Section 6.0. Preliminary estimates of ISMTC physical requirements indicate that it may be possible to house the complex in as few as one or two shelters.

## 2.0 SWITCHING CONSIDERATIONS

The main thrust of this part of the study is to determine the feasibility of integrating the switch, multiplex, and technical control into a single transportable communications complex designed for use in the tactical environment of the 1980s. In this section the switching aspect of the system is considered. Five candidate systems are compared as to their suitability for the Integrated Switch/Multiplex/Technical Control (ISMTC) application. Both space division and time division approaches are considered.

In order to aid the discussion, some tutorial material is included in the space division matrix section (paragraph 2.1.1) to familiarize the reader with switching concepts and terminology used in this report. Also included in this section is a specific space division matrix design which is used as the basis for comparison with the time division schemes described in paragraph 2.1.2. All candidate systems are compared to each other in paragraph 2.1.3 with respect to size, weight, cost, and power consumption as well as their impact on transmission facilities, signaling, common control, and technical control.

Section 2.2 includes discussions of switch control including common control, line load control, and trunk barring. Detailed discussions of processor functions and characteristics are deferred to Section 5.4.

An explanation of the various special switching services which may be required in a tactical environment is included in Section 2.3.

### 2.1 MATRIX TECHNOLOGY

#### 2.1.1 Space Division Arrays

In the past, space division arrays were not considered cost effective or sufficiently compact when compared to time division approaches. This section considers the possibility that the use of solid state crosspoints or future technological advances may change this view.

Paragraph 2.1.1.1 presents a brief review of space division network theory in order to introduce the reader to some of the switching terminology and concepts to be used in later sections. The properties of staged arrays and then folded staged arrays are discussed. This provides the background for the matrix design described in paragraph 2.1.1.3.

A specific circuit design is included in paragraph 2.1.1.2 for a 4 x 4 four-wire crosspoint matrix fabricated on a single integrated circuit. The possibility of integrating larger matrices on a chip is also considered. These integrated circuits are then used as the building blocks for a 2400-line three-stage folded space division array composed

of eight 300-line modules. This design is then used to calculate the quantity of chips required in such a system. The number of such integrated circuits determines the system cost, size, and reliability.

2.1.1.1 Theory

A switching network is that part of a switching system that establishes transmission paths between pairs of terminals. The most basic space division switching network is the N x N rectangular array depicted in Figure 1. The number of crosspoints (connecting devices) required is $N^2$. Note that at all times there is at least one available path between any pair of idle lines or trunks, regardless of the number of paths already occupied. Networks possessing this property are called "nonblocking".

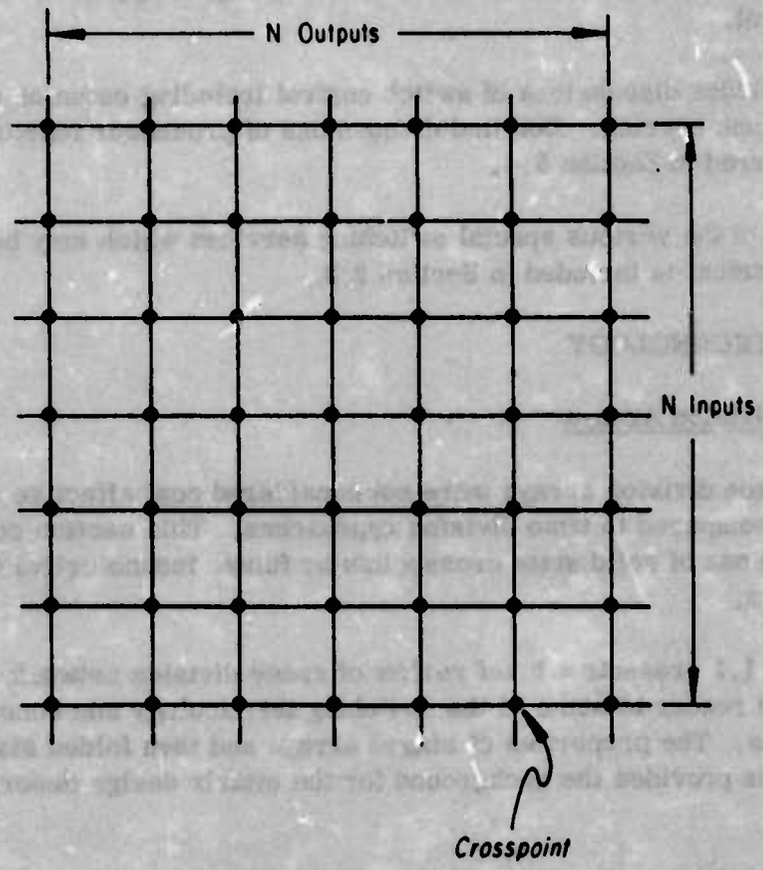


Figure 1. Space Division NxN Matrix

2.1.1.1.1 Staged Arrays

The number of crosspoints required for a space division matrix can be reduced through the use of staging. A three-stage array is shown in Figure 2. This approach replaces the large single matrix with a number of smaller matrices interconnected in stages. The first and third stages, as shown in Figure 2, have r modules each with n inputs and m outputs. The second stage has m modules, each with r inputs and r outputs. From Figure 2 it is clear that the total number of crosspoints, X(3), is

$$X(3) = 2\,nmr + mr^2$$

A nonblocking switch may be achieved by selecting $r = \sqrt{N}$ (assuming N to be a perfect square), and

$$m = 2\,N^{1/2} - 1$$

This yields a total number of crosspoints of

$$6\,N^{3/2} - 3\,N$$

which is less than $N^2$ for $N \geq 36$

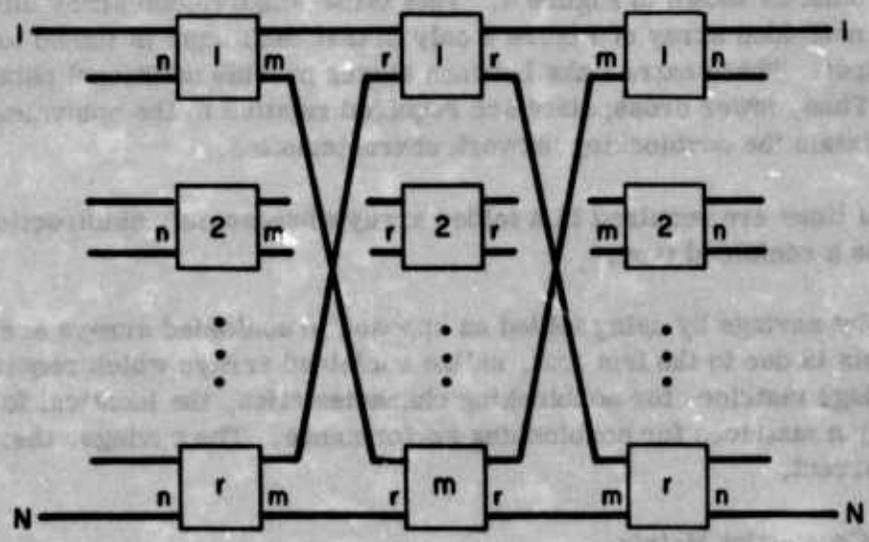


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Figure 2. Generalized Form of a N (m,n,r) Three-Stage Array

The three-stage switching array may be converted into a five-stage array by merely replacing each secondary stage rectangular array by a new three-stage array. Such a five-stage array is shown in Figure 3. Each input and output switch is assumed to have $N = N^{1/3}$ input or output lines. The total number of crosspoints is

$$X(5) = 2\,nmr + 2\,jksm + S^2km$$

For a nonblocking array $M = 2\,N^{1/3} - 1$ and $k = 2\,N^{1/3} - 1$. As in the three-stage array $j = r^{1/2} = N^{1/3}$. Therefore

$$X(5) = 16\,N^{4/3} - 14\,N + 3\,N^{2/3}$$

which is less than X(3) for $N \geq 160$.

For very large N it may be advantageous to use a seven-stage array. One such arrangement is possible by inserting a five-stage array for each secondary matrix of a three-stage array. The number of crosspoints contained in such a matrix can be shown to be (Reference 1)

$$X(7) = 36\,N^{5/4} - 46\,N + 20\,N^{3/4} - 3\,N^{1/2}$$

2.1.1.1.2 Folded Arrays

An alternative to staged arrays as discussed in the previous paragraph is the folded stage array such as shown in Figure 4. This three-stage folded array differs from the three-stage nonfolded array of Figure 2 only in that each input is linked to the corresponding output. These extra links between stages provide additional paths through the array. Thus, fewer crosspoints are required relative to the equivalent nonfolded array to maintain the nonblocking network characteristics.

Bidirectional lines are required in a folded array whereas only unidirectional lines may compose a nonfolded type.

The crosspoint savings by using folded as opposed to nonfolded arrays are quite substantial. This is due to the fact that, unlike nonfolded arrays which require 2 n - 1 secondary stage matrices for nonblocking characteristics, the identical folded matrix requires only n matrices for nonblocking performance. The savings, therefore, approach 50 percent.

2.1.1.2 IC Crosspoint Matrix

The cost, size, power requirements, and reliability of a space division array varies according to the number and size of the integrated circuit chips. Thus, in order to optimize the system and then determine these matrix parameters, one must first design or select a chip with maximum crosspoint density.

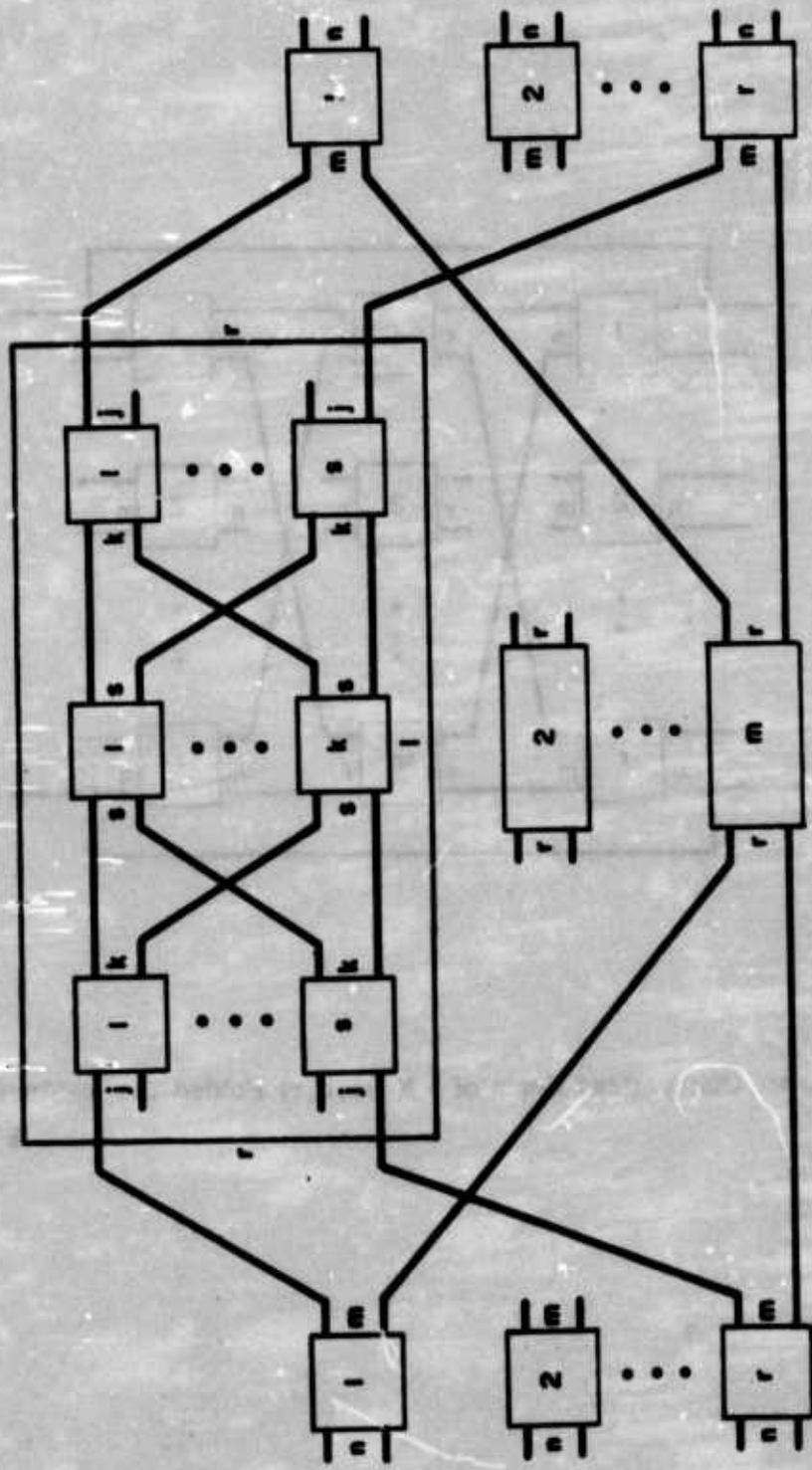

Figure 3. Generalized Form of a 5-Stage Array (Non-Blocking)

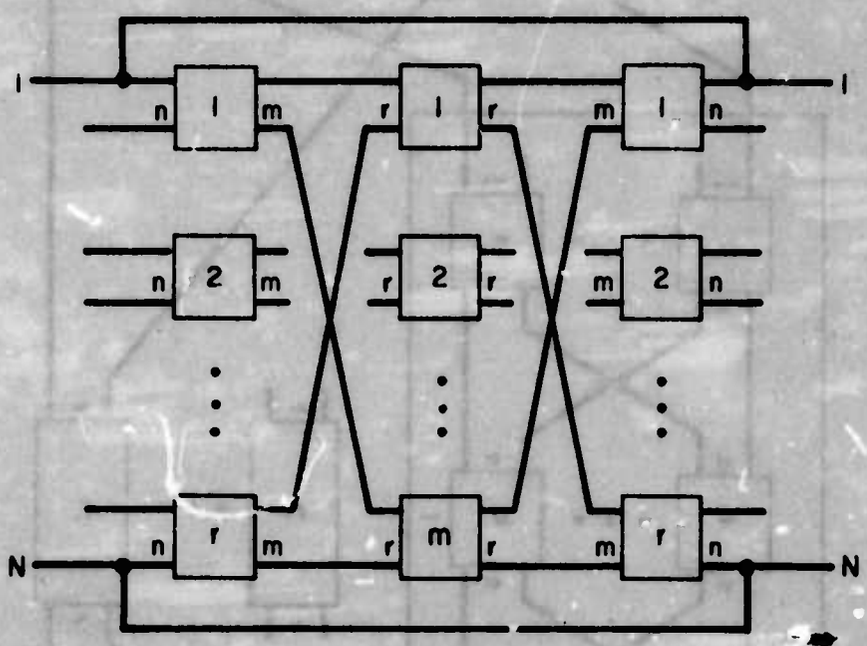


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Figure 4. Generalized Form of a N (m, n, r) Folded Three-Stage Array

2.1.1.2.1 Four-by-Four Crosspoint Chips

One possible type of digital crosspoint chip is shown in Figure 5. All input/output and control lines are shown for a four-wire 4 x 4 crosspoint matrix. Lines $X_{11}$, $X_{12}$, $X_{13}$, and $X_{14}$ are input lines, any of which may be switched to the outputs $Y_{11}$, $Y_{12}$, $Y_{13}$, or $Y_{14}$. Similarly, for the opposite transmission direction $X_{21}$, $X_{22}$, $X_{23}$, and $X_{24}$ may be connected to any of the output lines $Y_{21}$, $Y_{22}$, $Y_{23}$, or $Y_{24}$. Since the chip contains 16 four-wire crosspoints, a four-bit control word is required to select the proper crosspoint. An "open/close" signal is included to specify whether the selected crosspoint is to be opened or closed. In addition, a "chip select" pin is used by the connection control to enable the proper chip in the system.

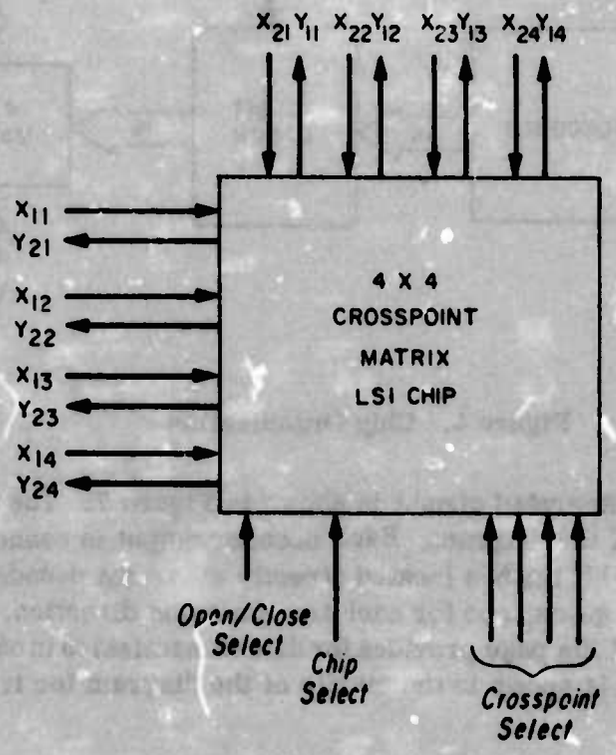



Figure 5. 4 x 4 Crosspoint Chip

The chip's functional organization is depicted in Figure 6. Note that the circuit is composed of the following three main parts:

1. Decoder Section - Selects one of the 16 latches according to the 4-bit input code.

2. Sixteen-Bit Latch - Flip-flops whose outputs hold each of the cross-points in their respective open or closed state until the new status is strobed in.

3. Matrix - The logic gates which actually provide the specified input/output connection.

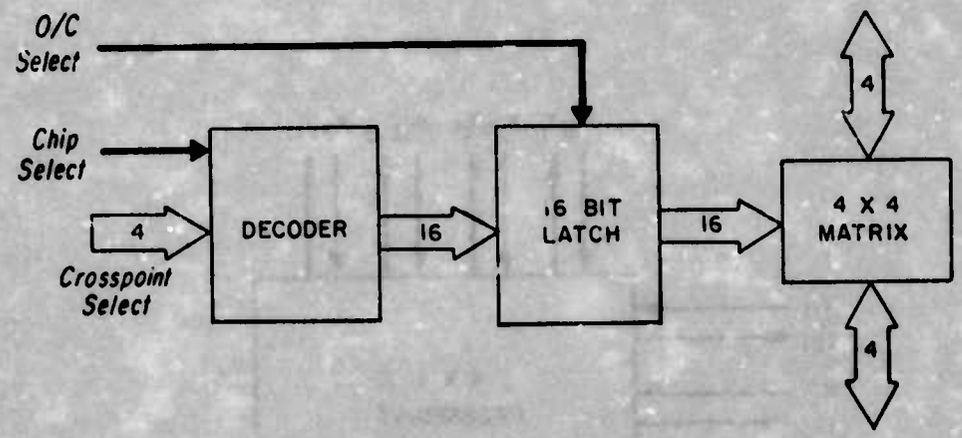



Figure 6. Chip Organization

A logic diagram for the integrated circuit is shown in Figure 7. The decoder section is located at the bottom of the diagram. Each decoder output is connected to the clock input of one of the 16 one-bit latches located directly above the decoder. Each latch output goes to two "AND" gates, one for each transmission direction. A twenty-gate array located at the top of the page provides for data transmission in one direction. An identical gating structure is shown in the middle of the diagram for transmission in the opposite direction.

The circuit operation will now be described by discussing a specific example. Suppose that it is desired to complete the following four-wire connection:

$$X_{12} \text{ to } Y_{13} \text{ and } X_{23} \text{ to } Y_{22}$$

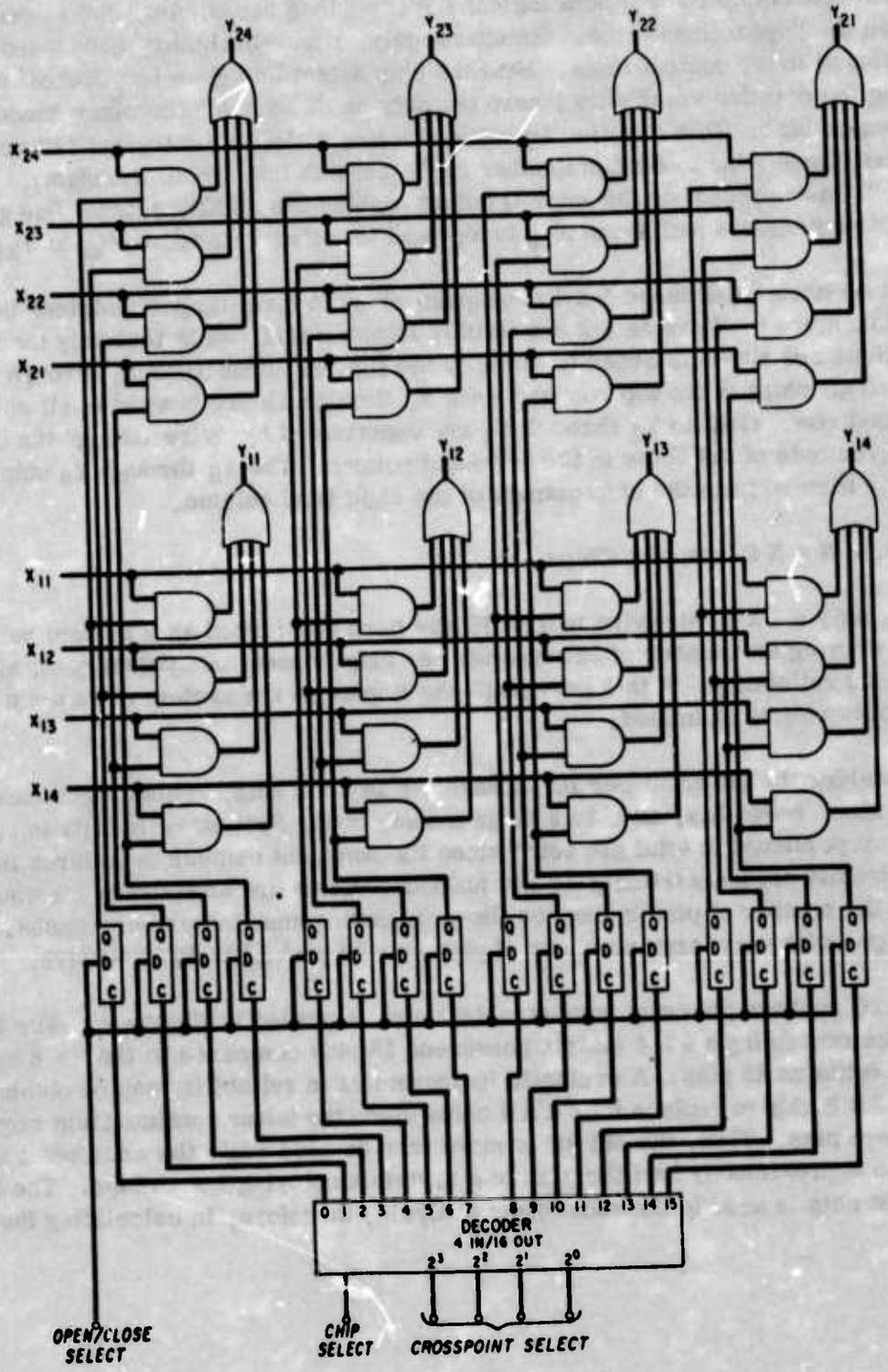



Figure 7. Logic Block Diagram - 4 x 4 Four-Wire Crosspoint Matrix Chip

First the connection control puts logical 1 ("1" = close crosspoint, "0" = open crosspoint) on the "open/close" line. Simultaneously, a four-bit binary code word (1001) is presented to the control lines. Next the chip select line goes low (logical 0) thus enabling the decoder which puts a zero out only on line 9. All the other decoder outputs remain high. This negative transition on line 9 clocks the logical "1" present on the "open/close" line into latch number 9 (the seventh latch from the right). The logical "1" now present on the latch Q output enables two "AND" gates. One gate provides a transmission path from $X_{12}$ to $Y_{13}$ and the other gate from $X_{23}$ to $Y_{22}$.

The interconnection of these 4 x 4 crosspoint chips to form larger matrices is illustrated in Figure 8. Here an 8 x 8 matrix is implemented. Note that only the two-wire connections are shown in order to simplify the figure. Input lines $X_1$ through $X_4$ are bussed to all chips in the top row and lines $X_5$ through $X_8$ are bussed to all chips in the second row. Outputs $Y_1$ through $Y_4$ are constructed by "wire ORing" the corresponding outputs of the chips in the left-hand column. The $Y_5$ through $Y_8$ outputs are similarly formed from the chip outputs of the right hand column.

2.1.1.2.2 N x N Crosspoint Chips

Thus far only a 4 x 4 four-wire matrix IC has been considered as a system building block. Varying the number of crosspoints per chip impacts on system cost, size, power, and reliability. In this paragraph the impact on the system of an n x n four-wire matrix chip is examined.

First consider the pin count per IC package for an n x n chip. This determines the package size, reliability, and, to a large extent, cost. System reliability is approximately proportioned to total pin count since the dominant number of failures in integrated circuits occurs in the chip-to-pin junction. Costs are affected by pin count since as the number of pins increases the yield during manufacture decreases. Thus IC packages with very large numbers of pins may be prohibitively expensive.

A plot of IC package pin count versus matrix size is plotted in Figure 9. Note than an IC package containing a 4 x 4 matrix possesses 25 pins compared to the 8 x 8 matrix IC which contains 43 pins. A dramatic improvement in reliability can be obtained by using an 8 x 8 chip to replace four 4 x 4 chips since the latter configuration requires 100 package pins. Thus, the MTBF is more than doubled while the crosspoint array shrinks to approximately half the size of a system employing 4 x 4 chips. The 8 x 8 crosspoint chip is used in the subsequent analysis, therefore, in calculating the

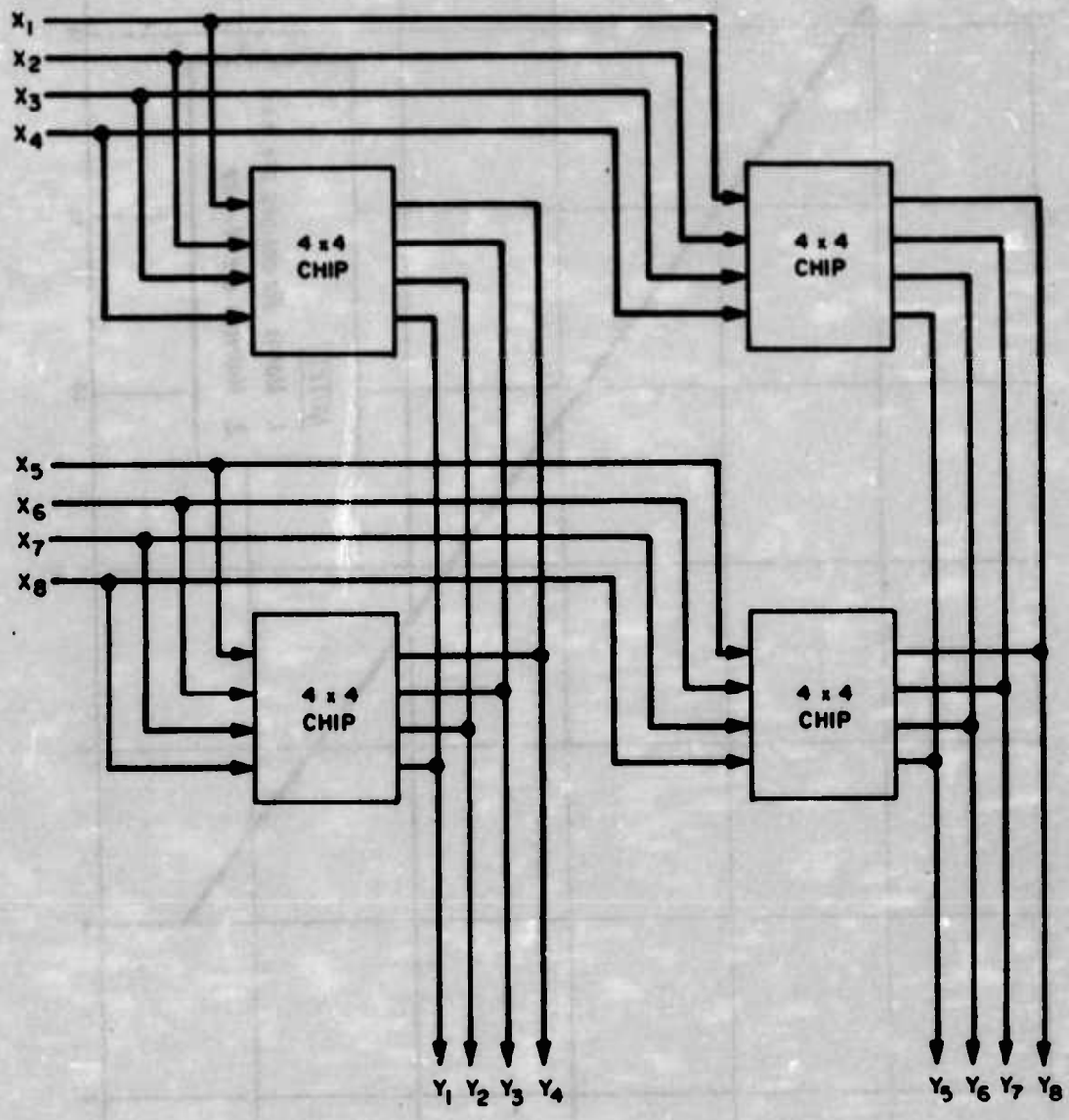



**Figure 8. Chip Interconnections for 8 x 8 Matrix**

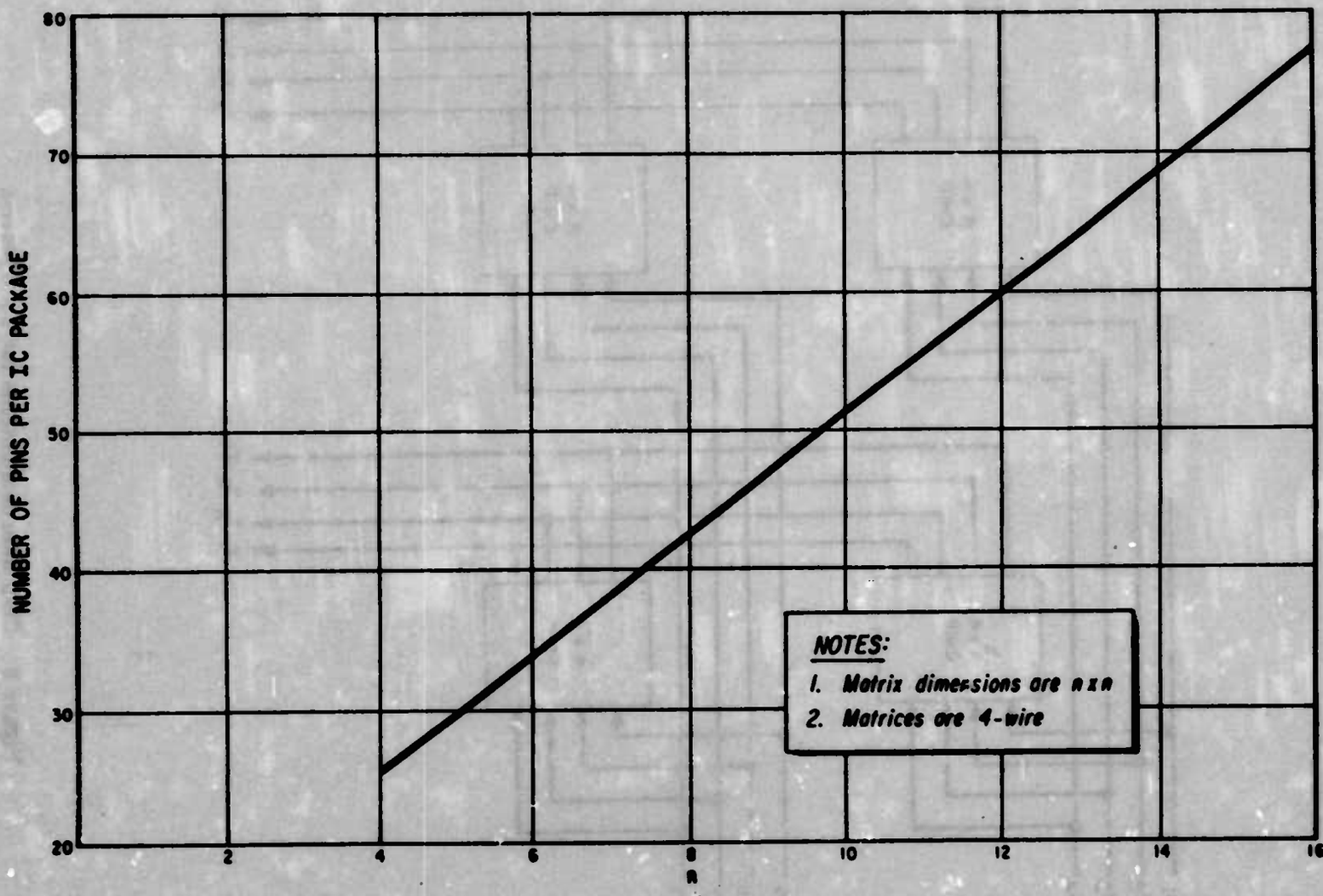



Figure 9. Pins per IC Package vs Crosspoint Matrix Size

tradeoff parameters of size, weight, power consumption, and cost for the space division candidate.[1]

2.1.1.3 Matrix Design

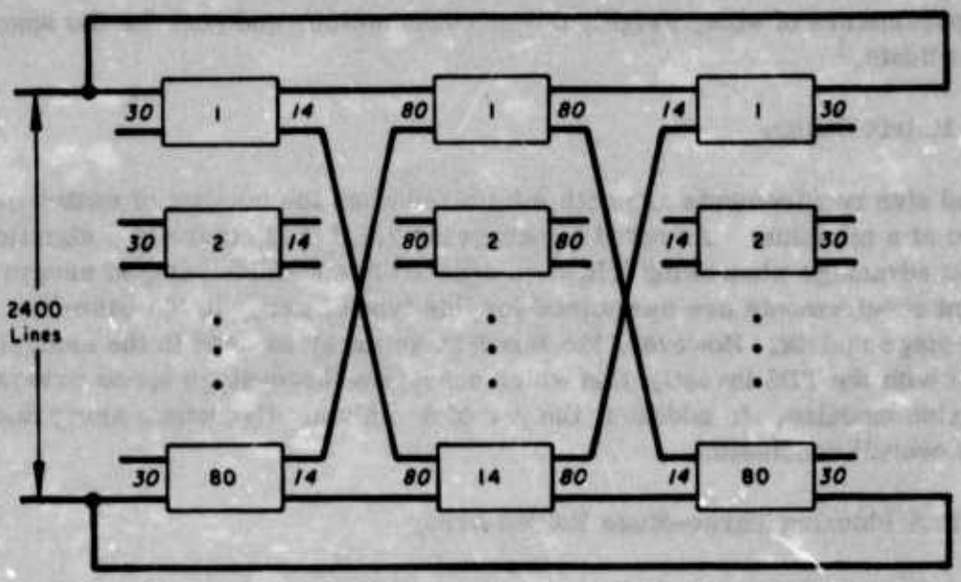
Power and size requirements are both minimized when the number of switch crosspoints are at a minimum. As noted in paragraph 2.1.1.1.2, there is a significant crosspoint advantage when using folded as opposed to non-folded staged arrays. Crosspoint requirements are minimized for this type of array in the 2400-line region by a five-stage matrix. However, the three-stage array as used in the analysis is consistent with the TDS investigation which considers three-stage space arrays of time division modules. In addition, the use of a minimum five-stage array does not affect the overall conclusion.

2.1.1.3.1 A Blocking Three-Stage Folded Array

Thus far only nonblocking arrays have been considered. Most space division switches economize on the number of crosspoints required by permitting a small amount of matrix blocking. Modern tactical switches such as the AN/TTC-39 specify a blocking probability of .001. Matrix blocking probability as low as this usually is insignificant when compared to trunk blocking. It is apparent that removal of a number of crosspoints will result in blocking. If the blocking probability is limited to 0.001 for 50 percent average total busy-hour occupation per line, the array is permissible. Thus, the switch of Figure 10 has been designed to fulfill the requirements of this study program. The three-stage folded array of Figure 10 contains a near minimum number of crosspoints for a 2400-line three-stage switch. The switch shown is a symmetrical array; that is, one which has an equal number of primary stage inlets and tertiary stage outlets. Note that the switch has eight 14 x 30 primary stage matrices, fourteen 80 x 80 secondary stage matrices, and a tertiary stage identical to the primary.

It is important to note that Figure 10 represents a blocking array. A totally nonblocking array would be realized if the switch possessed 30 secondary stage switches. The array has been transformed from an array with a zero blocking probability into a switch with a $0.69 \times 10^{-3}$ probability of blocking with 50 percent total occupation per trunk. This value is within assumed limits and the number of crosspoints has been cut by more than half over the equivalent nonblocking configuration.

[1] It should be noted that a 150-pin package has been manufactured by Texas Instruments and a 300-pin package has been developed for the Navy's AADC program. The suitability of constructing a crosspoint package of this pin size, however, has not been demonstrated from the viewpoint of cost, reliability and maintainability. As a result the more conservative approach of a 8 x 8 crosspoint design has been selected for analysis.




Blocking Probability = $0.691 \times 10^{-3}$ at 0.5 Erlangs
Number of Crosspoints $\cong$ 156,800

**Figure 10. 2400-Line Space Division Switch Three-Stage Folded Array**

At this point it is important to note that this particular design is totally inadequate for use as a tandem switch where the required grade of service is 0.001 blocking probability at 0.8 Erlangs per line. The probability of blocking for the matrix of Figure 10 for 80 percent total occupation per line is 0.456. The switch would have to be reconfigured to include 19 secondary stage matrices instead of the present fourteen to satisfy tandem switch requirements.

A further requirement which has been imposed on the system is that it be expandable in increments of from 150- to 300-line modules to a maximum of 2400 lines. This has been achieved by dividing the 2400-line system into eight identical 300-line modules (see Figure 11) in such a way as not to affect the blocking characteristics of the individual module. Note that each secondary stage is composed of fourteen 10 x 80 matrices of which only a 10 x 10 portion (1/8 of the secondary matrix) is used for the 300-line configuration. This inefficiency is progressively diminished as more modules are grouped together to form a larger system. These surplus crosspoints need not be supplied with the module unless the switch is to be used in an expanded configuration. However, adequate space and wiring must be provided for each module as if it were to be used in the maximum 2400-line configuration.

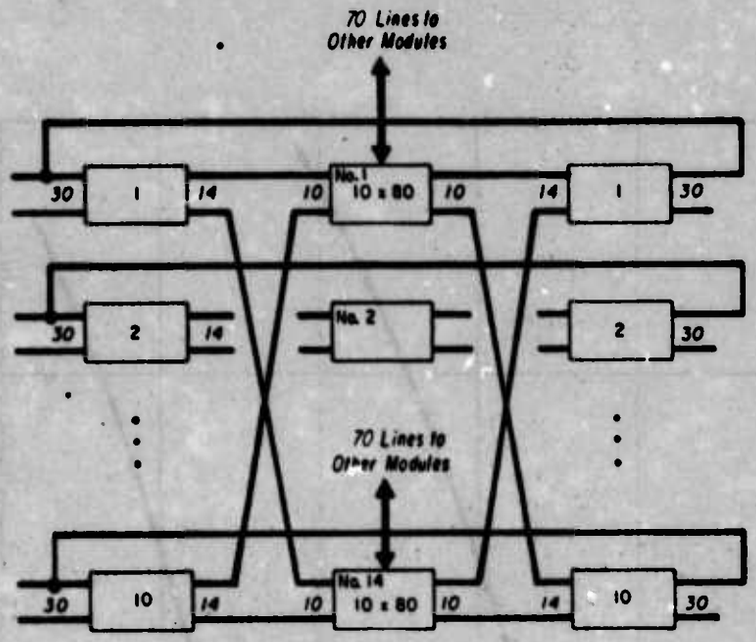



Figure 11. 300-Line Module

The modules are combined by attaching the 70 spare lines of each 10 x 80 matrix of one module with the corresponding matrix lines of another module to form a larger secondary matrix. For example, in forming a 600-line system, two 300-line modules are used. Ten spare lines from secondary matrix number 1 are connected to the ten corresponding lines of matrix number 1 in module 2, thus forming a 20 x 80 secondary matrix. Similarly, all fourteen 10 x 80 secondary matrices of module 1 are combined with the fourteen 10 x 80 matrices of module 2 to form fourteen 20 x 80 matrices. Thus, the new 600-line system contains twenty 30 x 14 primary matrices, fourteen 20 x 80 secondary matrices, and twenty 30 x 14 tertiary matrices. Again, note that only one quarter of secondary stage crosspoints are used. The full 2400-line system is formed by connecting the secondary stage matrices of eight 300-line modules to form fourteen 80 x 80 secondary matrices as shown in Figure 11.

2.1.1.3.2 Chip Requirements

The number of chips required for a 2400-line three-stage folded space division array versus the grade of service is plotted in Figure 12. Chip quantities were determined by dividing the total number of crosspoints by sixteen (for a 4 x 4 matrix chip) and then

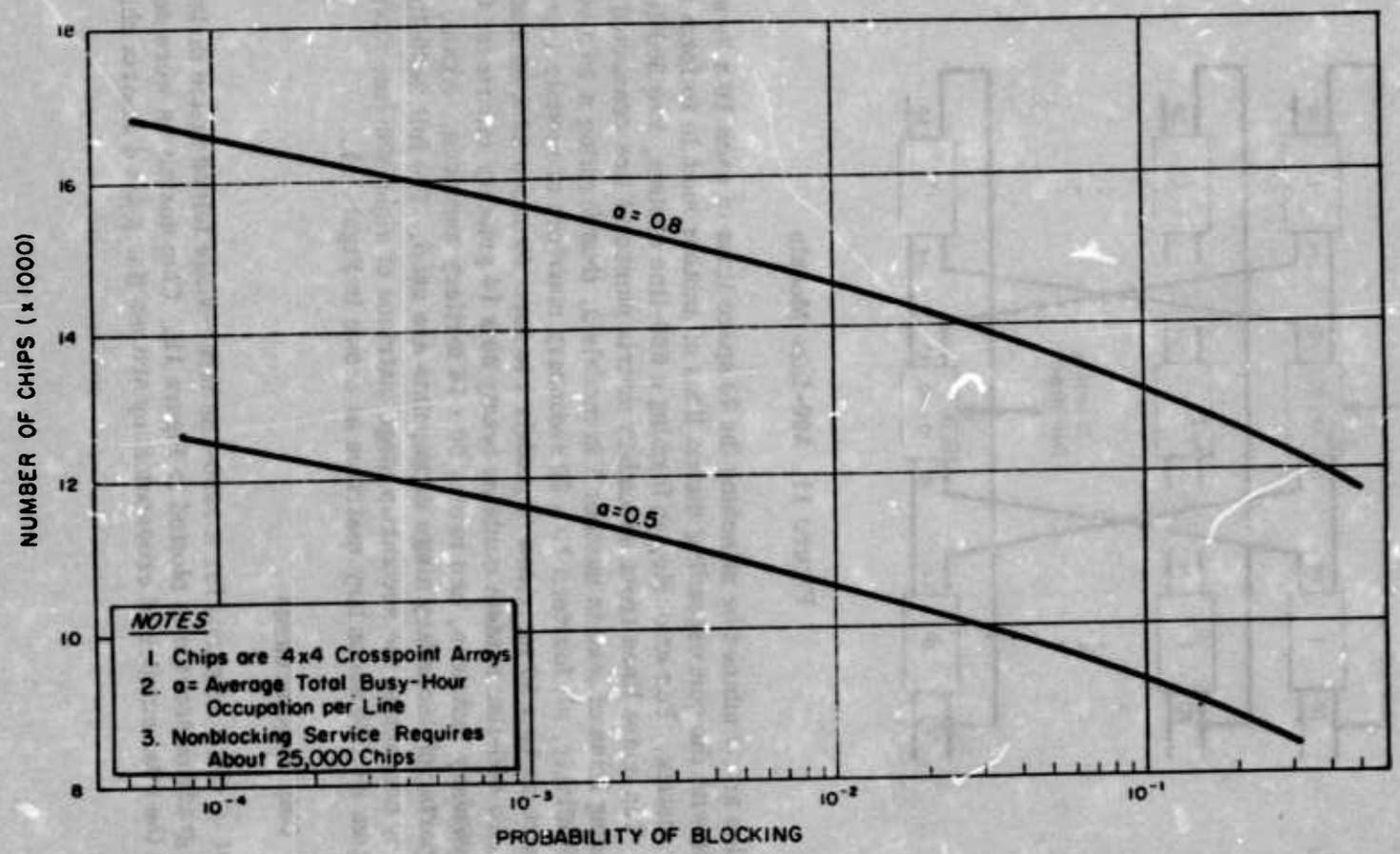



**Figure 12. Quantity of Chips Vs Grade of Service for a 2400-Line Three-Stage Folded Array**

adding 10 percent for unused crosspoints[2] and 10 percent for control circuitry. Curves are provided for both 50 percent and 80 percent average total busy hour occupation per line. In order to calculate the approximate number of chips required for a system composed of n x n matrix chips, merely divide the Figure 12 quantities by $(n/4)^2$.

Notice that about 12,000 chips are required for .001 blocking probability for a = 0.5 when 4 x 4 matrix chips are used. Such a system is clearly not competitive with time division systems in terms of cost, size, and reliability. The chip total grows to approximately 16,000 to satisfy tandem switch requirements (a = 0.8). Erlang loadings may exceed the assumed values for switches handling a high volume of data traffic with long holding times per line (e.g., measured in hours). To provide a non-blocking matrix requires 25,000 chips which would be the limiting case for traffic loading greater than that assumed above. The analysis assumes, however, that the predominant traffic type handled is digitized voice. As a result, loading factors (i.e., call introduction, holding times, etc.) based on present experience with circuit switches are judged appropriate for use in this analysis.

Although one could reduce all of the aforementioned chip quantities by a factor of four by using 8 x 8 matrix chips, the space division array would still be at a serious disadvantage when compared to TD systems (see paragraph 2.1.3).

2.1.1.4 Conclusions

The number of crosspoints which may be fabricated on a single chip is pin limited. A 4 x 4 four-wire crosspoint matrix chip is clearly realizable using present technology. An 8 x 8 four-wire crosspoint chip also appears to be feasible and is probably the largest matrix which may reasonably be expected to be fabricated on a single chip in the near future.

2.1.2 Time Division Arrays

The previous section discusses the possibilities of using a digital space division array as part of the ISMTC. However, multiplexing must be performed distinct from the matrix. In this section several time division approaches are considered in which the multiplex function is performed as an inherent part of the switching function.

[2]The term "unused crosspoints" refers to the fact that using 4 x 4 matrix chips to synthesize a rectangular crosspoint matrix possessing dimensions which are not multiples of four must waste some of the crosspoints available on the chips.

Reference 2 published in 1972 is a prior investigation performed for RADC of known digital switching techniques to determine the most suitable approach for future switching application. This work has been analyzed and evaluated in determining the nature of time division matrices considered for an integrated switch, multiplex, and technical control. A description of these systems follows.

2.1.2.1 System Descriptions

2.1.2.1.1 Time Division Module Array

The Time Division Module Array approach (referred to in the drawing as Candidate 2) is illustrated in Figure 13. The system shown is a 2400-line (3000 terminations) three-stage space division array which uses time division (TD) switching modules for each coordinate matrix. Note that each matrix is a 60 x 60 array composed of one fan-in and fan-out matrix. The fan-in structure is essentially a TD multiplexer which accomplishes the switching function by multiplexing the 60 input channels onto a single high-speed time division highway in any desired order. The fan-out portion performs the demultiplexing function.

Note that by splitting one of the output TD modules into its fan-in and fan-out portions, and placing the fan-out circuitry at the switch input, the array has been reconfigured to accept 2940 single channels plus one TDM 60-channel group (see Figure 14). It is important to note here that this change required no additional equipment (such as multiplex/demultiplex) and only minor rearrangement of existing modules. It can be seen that any combination of trunk groups and single channels may be implemented in the same manner with a reduced need for external multiplex.

2.1.2.1.2 Redundant Memory

The Redundant Memory approach (Candidate 3) is shown in Figure 15. The figure shows a 480-line portion of the switch. Notice the matrix inputs and outputs are 60-channel TDM highways while the former two approaches (space division and time division module array) were characterized by single channel input/output ports.

The Random Access Memory (RAM) stores an entire frame (60 bits) from each of the eight input 60-channel highways. The switching function is implemented by reading out of memory each of the 60 channels in any desired sequence. Each read-out command produces an eight-bit output (one bit for each of the eight highways) of which one bit is selected by a multiplex gate to be transmitted to the output highway. Note that the same eight highways are stored in all eight basic modules; thus, the name, Redundant Memory. The Connection Control (CC) supplies the 9-bit control words which determine the specific RAM memory cells read-out (6 bits) and which highway is selected by the multiplex gate (3 bits).

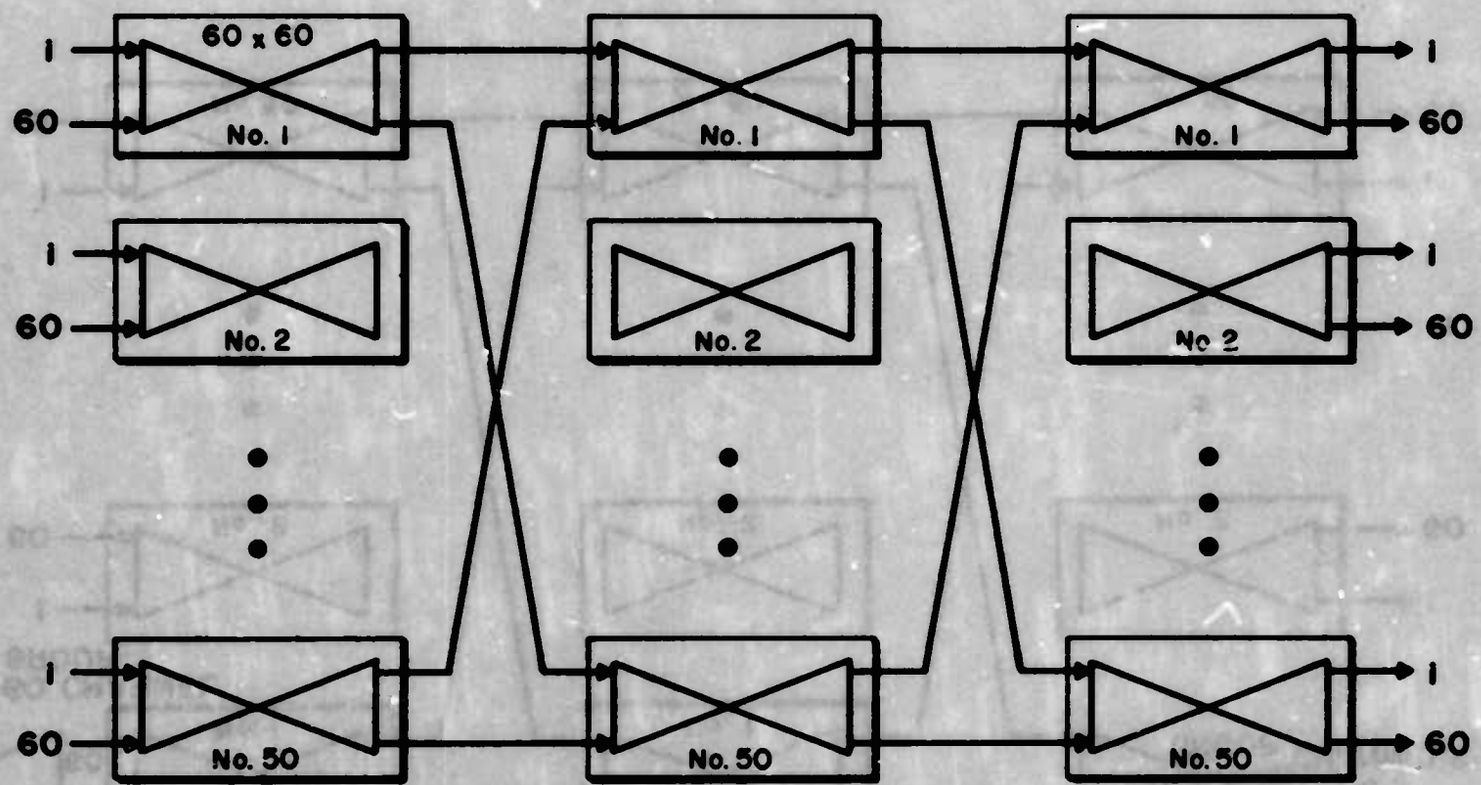



Figure 13. Candidate 2 - TD Module Array

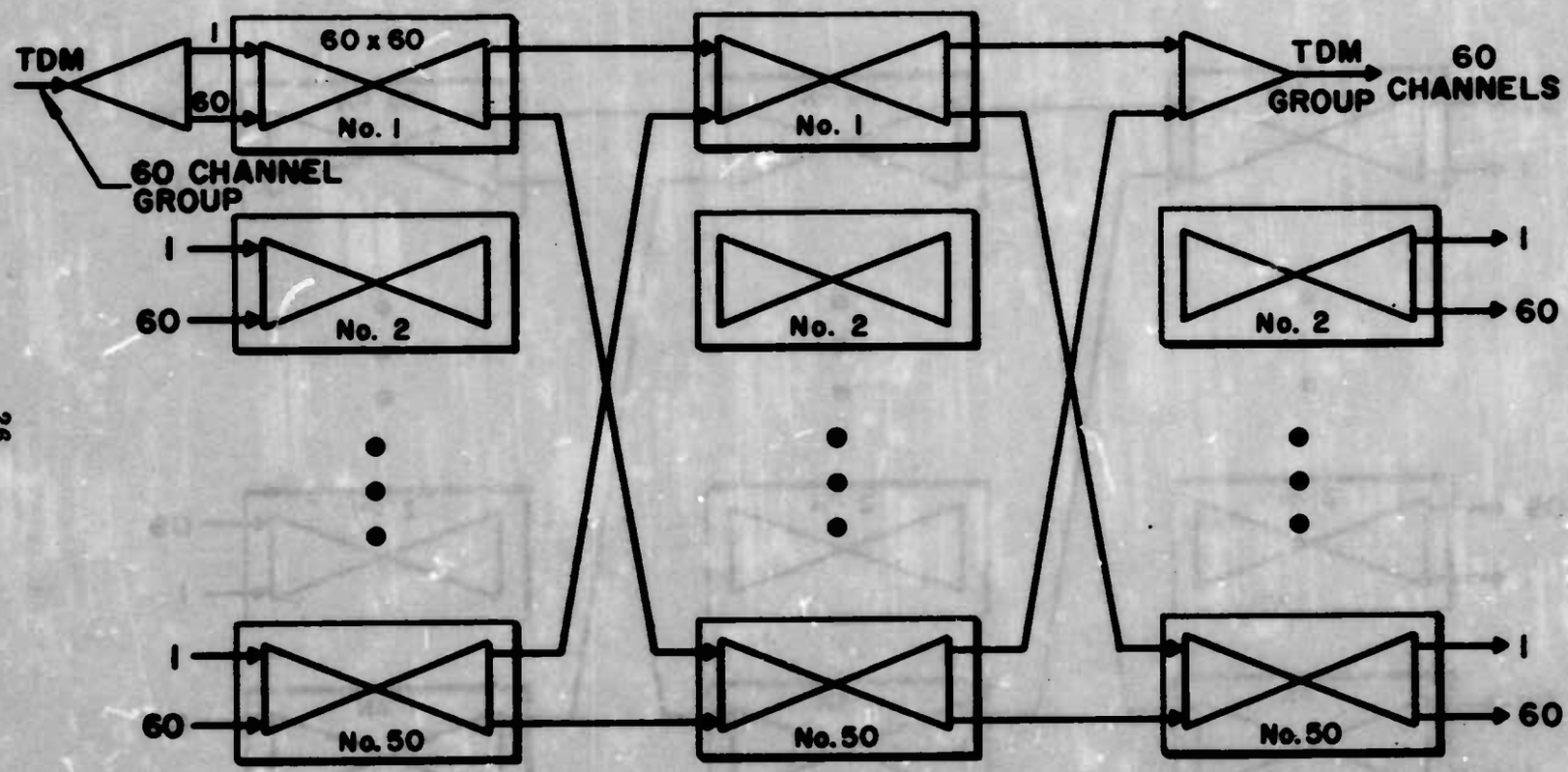



Figure 14. Candidate 2 Modified

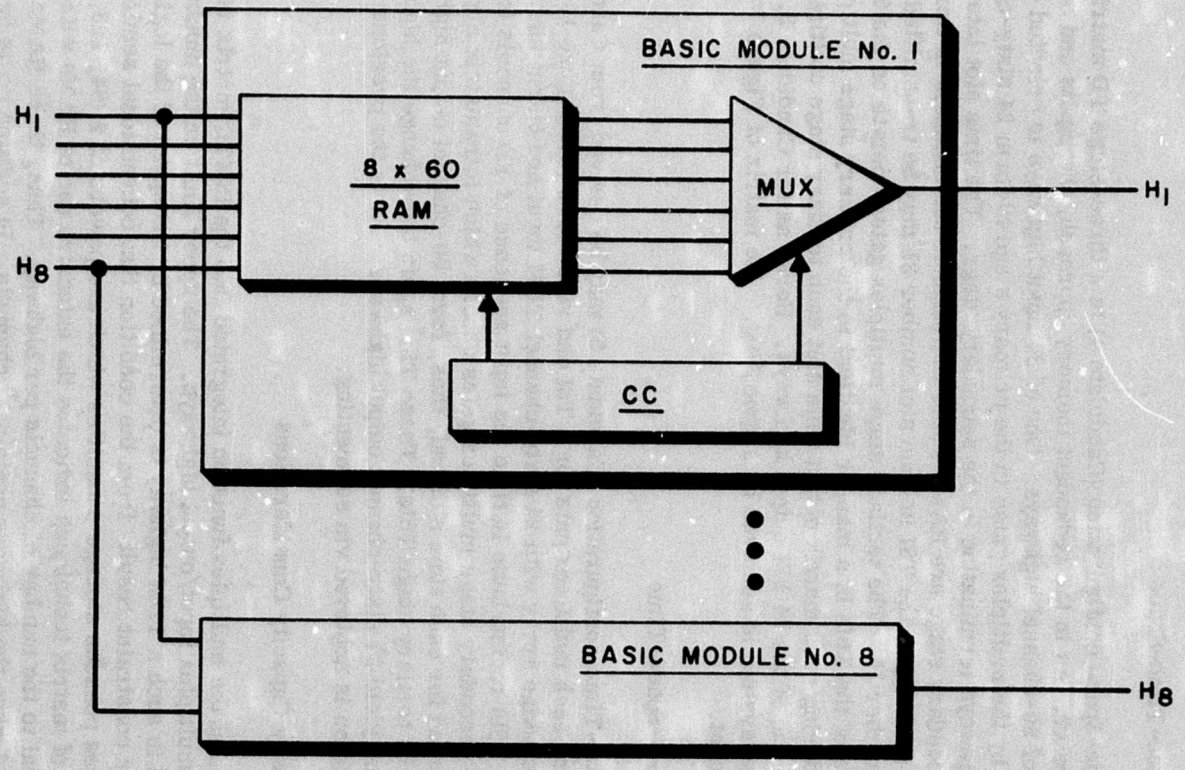



Figure 15. Candidate 3 - Redundant Memory

Expansion of the matrix shown in Figure 15 is accomplished by stacking three such systems to form eight tri-groups. Twenty-four such tri-groups, called a segment, are shown in Figure 16. Four such segments when interconnected compose a 2400-line switch. This segmenting is used to satisfy modularity requirements.

2.1.2.1.3 Space-Time-Space

The Space-Time-Space configuration (Candidate 4) is a three-stage TD matrix and is shown in Figure 17. As in the redundant memory approach, the inputs and outputs are composed of 60-channel highways. One of 24 input highways is selected during each time slot by the multiplex gates in the primary stage to form 24 sixty-channel intramatrix highways terminating in the secondary stage. The time slot interchanges (TSI) of the secondary stage are RAMs which redistribute the channels in time. For example, data arriving at the TSI in time slot number 31 may be transmitted in output time slot number 15. The tertiary stage multiplex gates operate on the 60-channel output highways of the TSIs in a manner identical to the primary stage multiplex equipment. Thus, during each matrix output time slot each tertiary stage multiplex gate transmits only one of the 24 TSI output highways. Here, as for Candidate 3, modular expansion of the system is achieved by segmenting. The matrix of Figure 17 represents one segment.

2.1.2.1.4 Time-Space-Time

The Time-Space-Time configuration (Candidate 5) may be derived from Candidate 4 by interchanging each multiplex gate for a TSI and vice versa (see Figure 18). Again, one has a three-stage array with 24 sixty-channel TDM input and output highways. The primary stage TSIs redistribute in time the input sequence of TD channels for each highway. The secondary stage multiplex gates choose which intramatrix highway input will be enabled for each time slot and, thus, form 60-channel output highways which are routed to the tertiary stage TSIs. These TSIs again interchange the highway channels in time and yield 24 sixty-channel output highways. As in the previous two candidates, expansion is achieved via segmenting.

2.1.2.2 Highway Capacity Considerations

It is assumed that the multiplex function integrated into the ISMTC matrix results in time division multiplex input/output highways. The upper limit on the number of channels contained in such a TDM highway is determined by the speed of the logic circuitry used. Another constraint results from the condition that conventional semiconductor memory devices possess storage capacities which are powers of 2 (64, 128, 256, etc.). CSC's survey of matrix techniques indicates the extensive use of RAMs with storage capacities equal to the number of channels per highway. Thus, these RAMs are most efficiently used when the highways contain $2^n$ channels. In addition costs decrease as the number of channels per highway increase (see Figure 19).

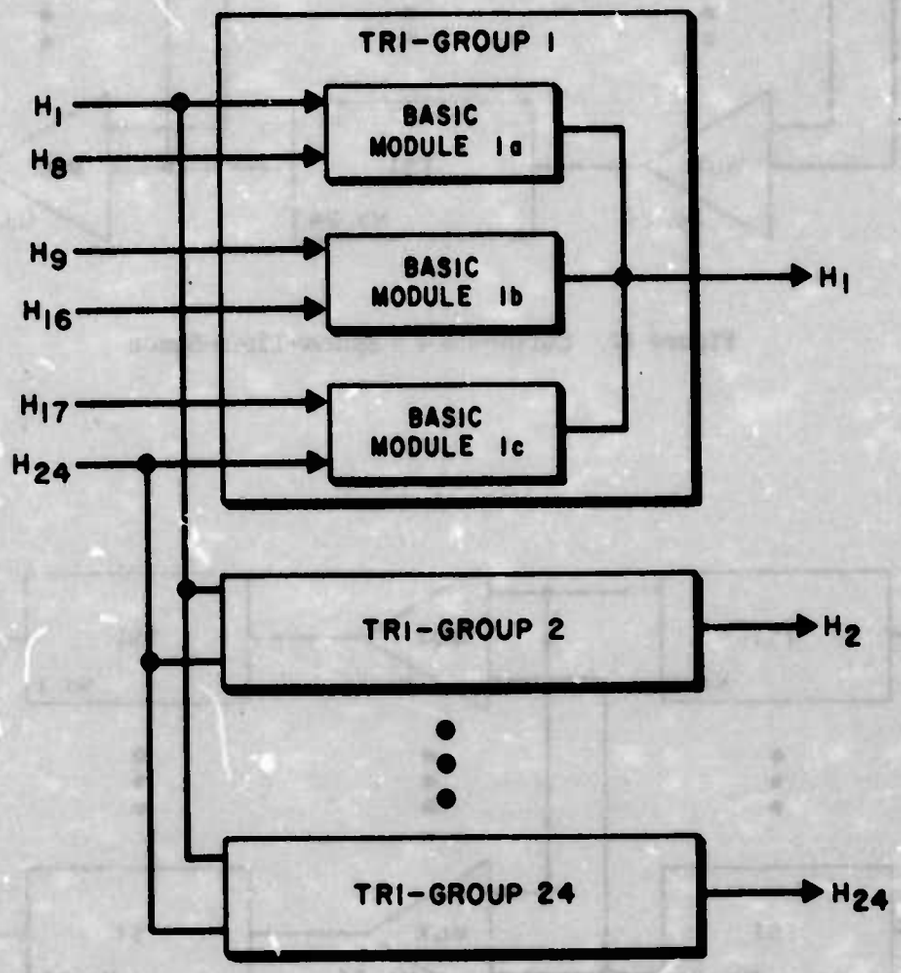



Figure 16. Redundant Memory Segment

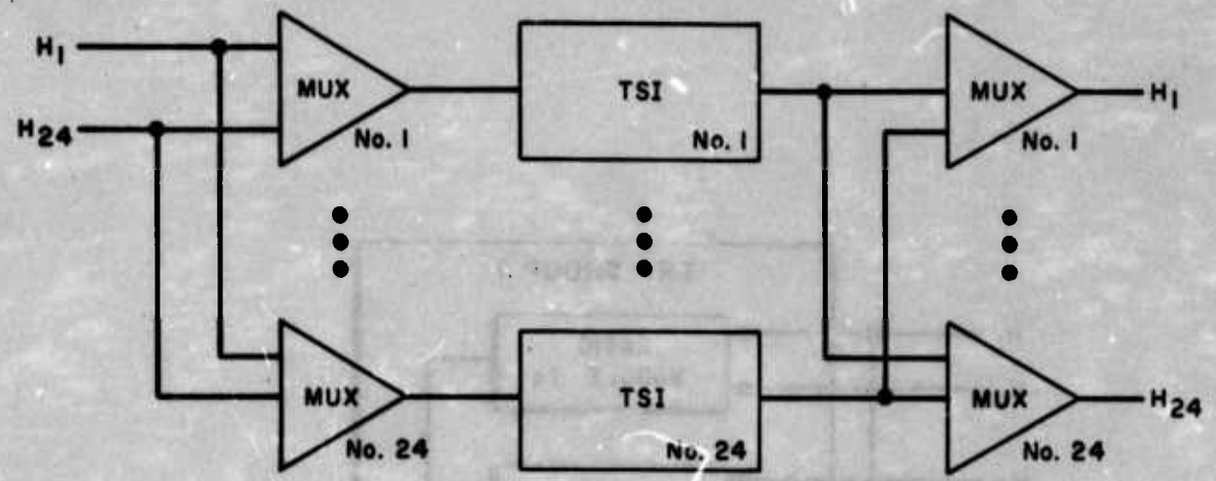



Figure 17. Candidate 4 - Space-Time-Space

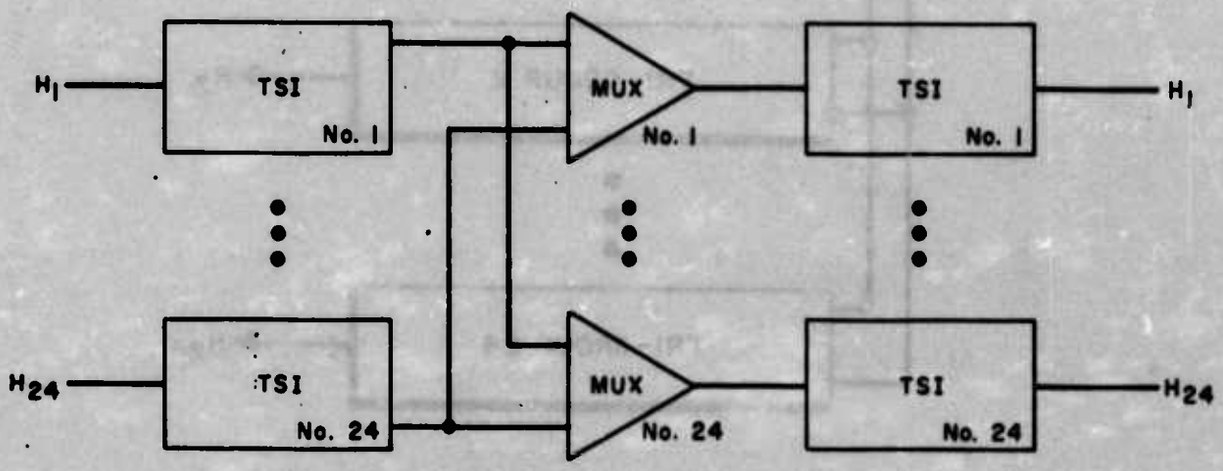



Figure 18. Candidate 5 - Time-Space-Time

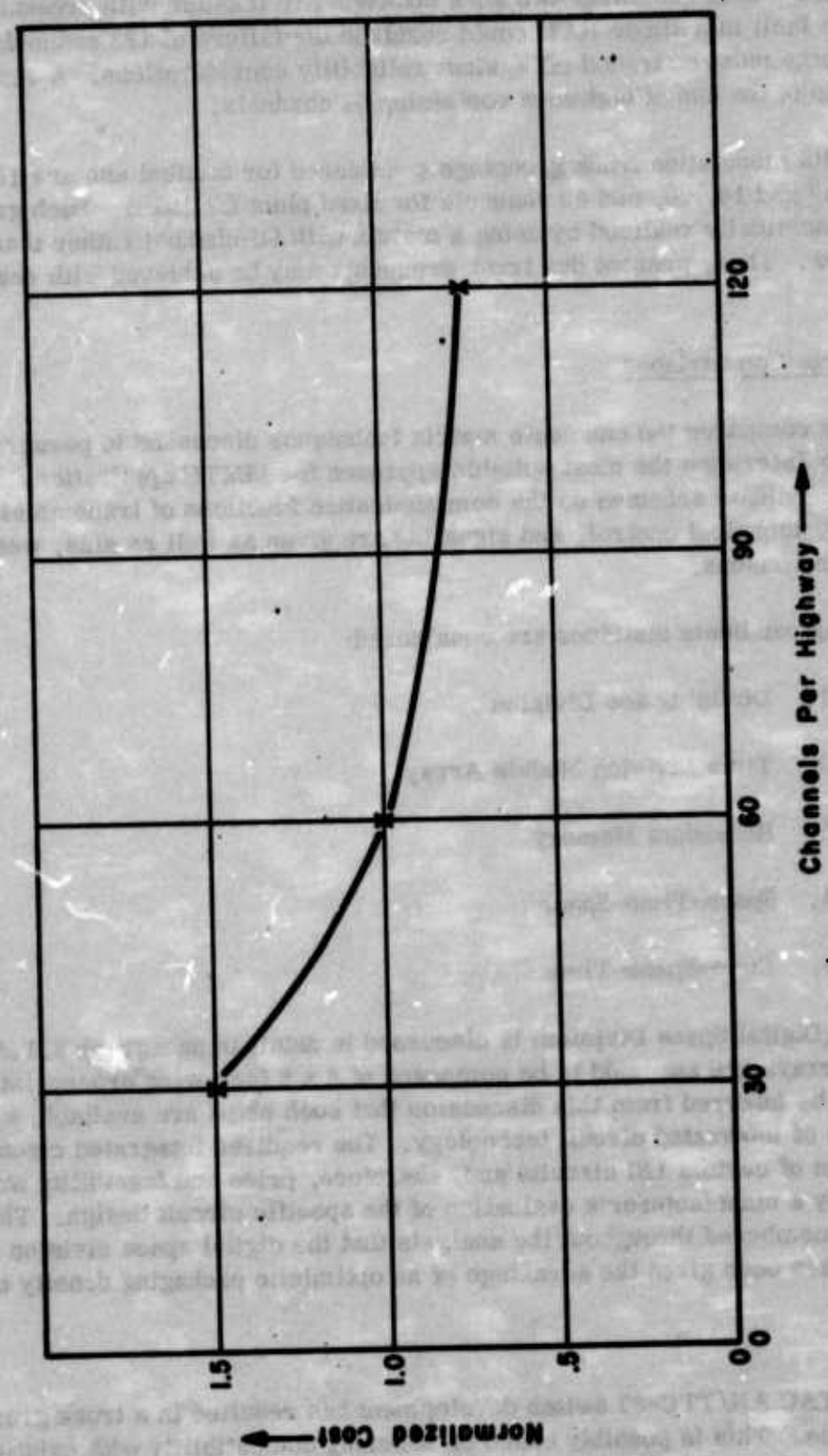



Figure 19. Cost Vs Number of Channels Per Highway

Highways containing 128 thirty-two kb/s channels are feasible with present technology. However, a fault in a single RAM could result in the failure of 128 channels. Therefore, economy must be traded off against reliability considerations. A reasonable compromise is the use of highways containing 64 channels.

Present delta modulation trunk groupings considered for tactical use are 15, 30, and 60 channels[3] and 10, 20, and 40 channels for fixed plant facilities. Such groupings may be economically realized by using a matrix with 60-channel rather than 64-channel highways. Thus, present day trunk groupings may be achieved with reasonable economy.

### 2.1.3 Matrix Comparisons

This section compares the candidate matrix techniques discussed in paragraphs 2.1.1 and 2.1.2 to determine the most suitable approach for ISMTC applications. The impact of the candidate schemes on the communication functions of transmission, common control, technical control, and signaling are given as well as size, weight, power, and cost comparisons.

The following candidate matrices are considered:

1. Digital Space Division
2. Time Division Module Array
3. Redundant Memory
4. Space-Time-Space
5. Time-Space-Time

Candidate 1 (Digital Space Division) is discussed in detail in paragraph 2.1.1. The crosspoint arrays are assumed to be composed of 8 x 8 four-wire crosspoint chips. It should not be inferred from this discussion that such chips are available within the present state of integrated circuit technology. The required integrated circuits fall into the realm of custom LSI circuits and, therefore, price and feasibility would be determined by a manufacturer's evaluation of the specific circuit design. Thus, it should be remembered throughout the analysis that the digital space division candidate may have been given the advantage of an optimistic packaging density compared

[3]Note: TRI-TAC AN/TTC-39 switch development has resulted in a trunk group size of 72 channels. This is possibly based on assuring compatibility with existing Army 48 kb/s per channel PCM equipment (i.e., AN/TTC-44, -45, -46 and -47 series equipment).

to the other candidates which are realizable with existing integrated circuits. It is the belief of the authors, however, that a 8 x 8 four-wire digital crosspoint integrated circuit is achievable for use in tactical switching matrix for use in the 1980s through LSI production technology.

Note that the Space Division network described in paragraph 2.1.1.3.1 contains 2400 terminations. TD arrays of paragraph 2.1.2 contain approximately 3000 terminations for a 2400-line switch. Thus, in order to establish a valid basis for the comparison of the two techniques the number of crosspoints for Candidate 1 will be increased by 40 percent.

2.1.3.1 Size/Weight Comparison

Matrix size and weight calculations have been performed for all five candidate systems for 300-, 600-, 1200- and 2400-line arrays. A preliminary step in the determination of size/weight of electronic equipment is the estimation of the number of integrated circuits required. Tables 1 and 2 yield the results of such a chip count for each candidate matrix. The space division matrix (Candidate 1) will be presumed to be composed mainly of 40-pin chips while the composition of the remaining candidates will consist predominantly of 16- and 18-pin chips.

The volume of a typical 18-pin IC package is approximately 0.054 cubic inches while a 40-pin chip occupies approximately 0.252 cubic inches. Reference 3 estimates equipment volume by using a stacking factor of 0.5. Thus space requirements may be calculated by multiplying the chip quantities of Tables 1 and 2 by 0.108 for the time division candidates and 0.504 for the space division candidate.

Although such packing densities may be achievable, for reasons of maintainability and cooling this extremely dense component packing may not be desirable. Present commercial packaging techniques yield packing densities approximately one tenth of those indicated in Reference 3. For the purposes of this analysis a more conservative approach than that presented in Reference 3 is deemed appropriate and volume estimates of Reference 3 are increased by a factor of ten to make the estimates more consistent with packing densities achievable with best current commercial practice. Thus the volumes shown in Figures 20 and 21 were derived by multiplying the chip quantities of Tables 1 and 2 by 1.08 and 5.04 for the time and space division matrices, respectively. The results are shown in Figures 20 and 21 assuming an average trunk occupancy of 0.5 and 0.8 Erlangs, respectively. An important feature of the curves is that the space division array (Candidate 1) occupies from 4 to 7 times the space required by its nearest time division counterparts (Candidates 2, 3, 4, and 5). Note that for systems with less than about 400 or 500 lines the smallest matrix is Candidate 3. However, throughout the remainder of the range Candidate 5 is the most compact. In Figure 20 Candidate 3 is actually the largest of the TD systems for matrices greater than about 2000 lines. Thus the choice of the most compact system is strongly dependent on the distribution of switch line capacities expected.

Table 1. Chip Quantities for Candidate Matrices (a=0.5)

| # Lines / Candidate | 300 | 600 | 1200 | 2400 |
|---|---|---|---|---|
| 1 | 515 | 1029 | 2058 | 4116 |
| 2 | 414 | 897 | 1794 | 3588 |
| 3 | 120 | 520 | 1280 | 4560 |
| 4 | 243 | 405 | 972 | 2160 |
| 5 | 168 | 364 | 896 | 2128 |

Table 2. Chip Quantities for Candidate Matrices (a=0.8)

| # Lines / Candidate | 300 | 600 | 1200 | 2400 |
|---|---|---|---|---|
| 1 | 687 | 1373 | 2748 | 5495 |
| 2 | 483 | 1035 | 2070 | 4140 |
| 3 | 120 | 520 | 2280 | 5280 |
| 4 | 324 | 702 | 2052 | 4752 |
| 5 | 196 | 420 | 1176 | 2688 |

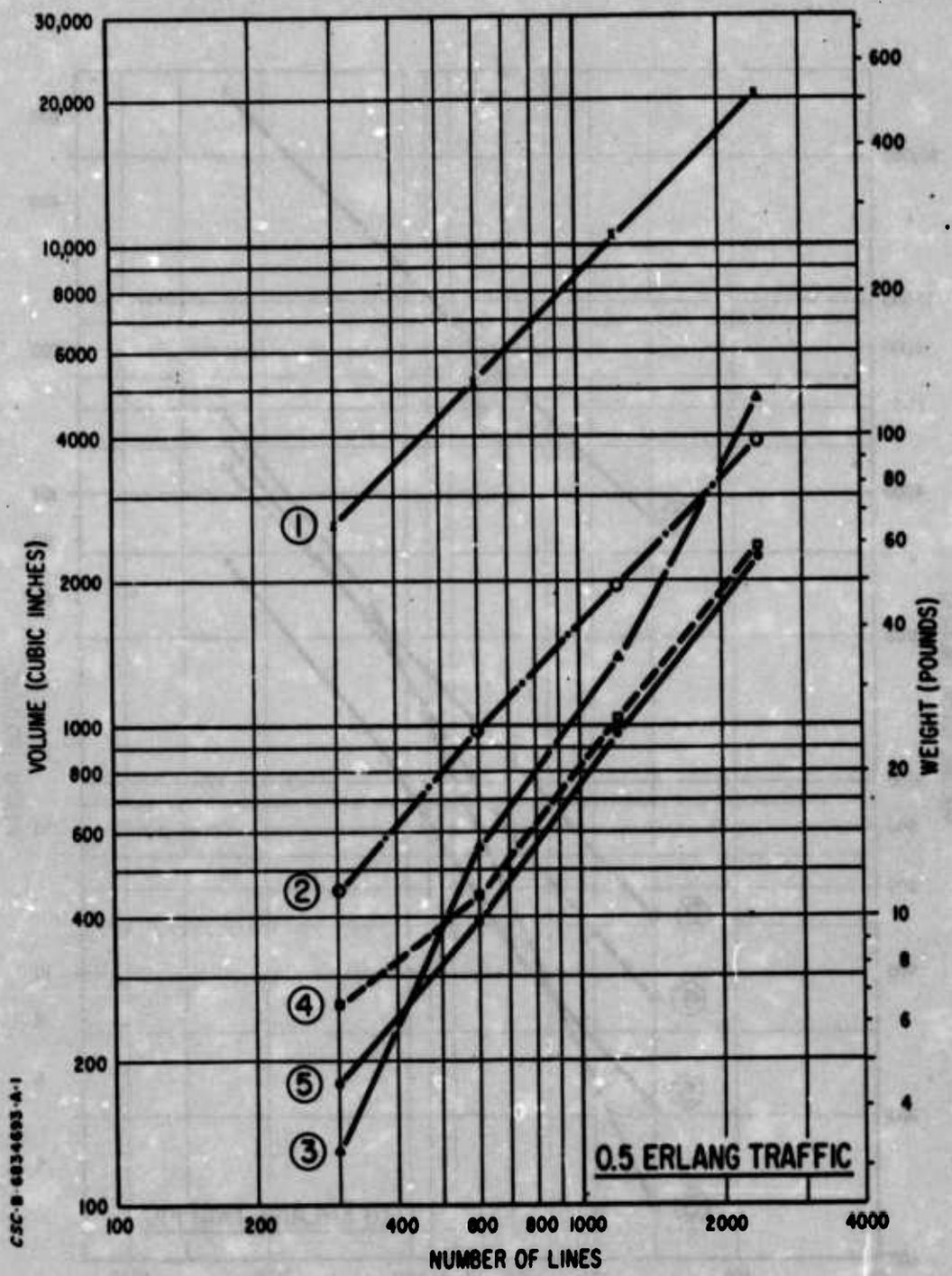



Figure 20. Matrix Size/Weight Vs Number of Lines (0.5 Erlang Traffic)

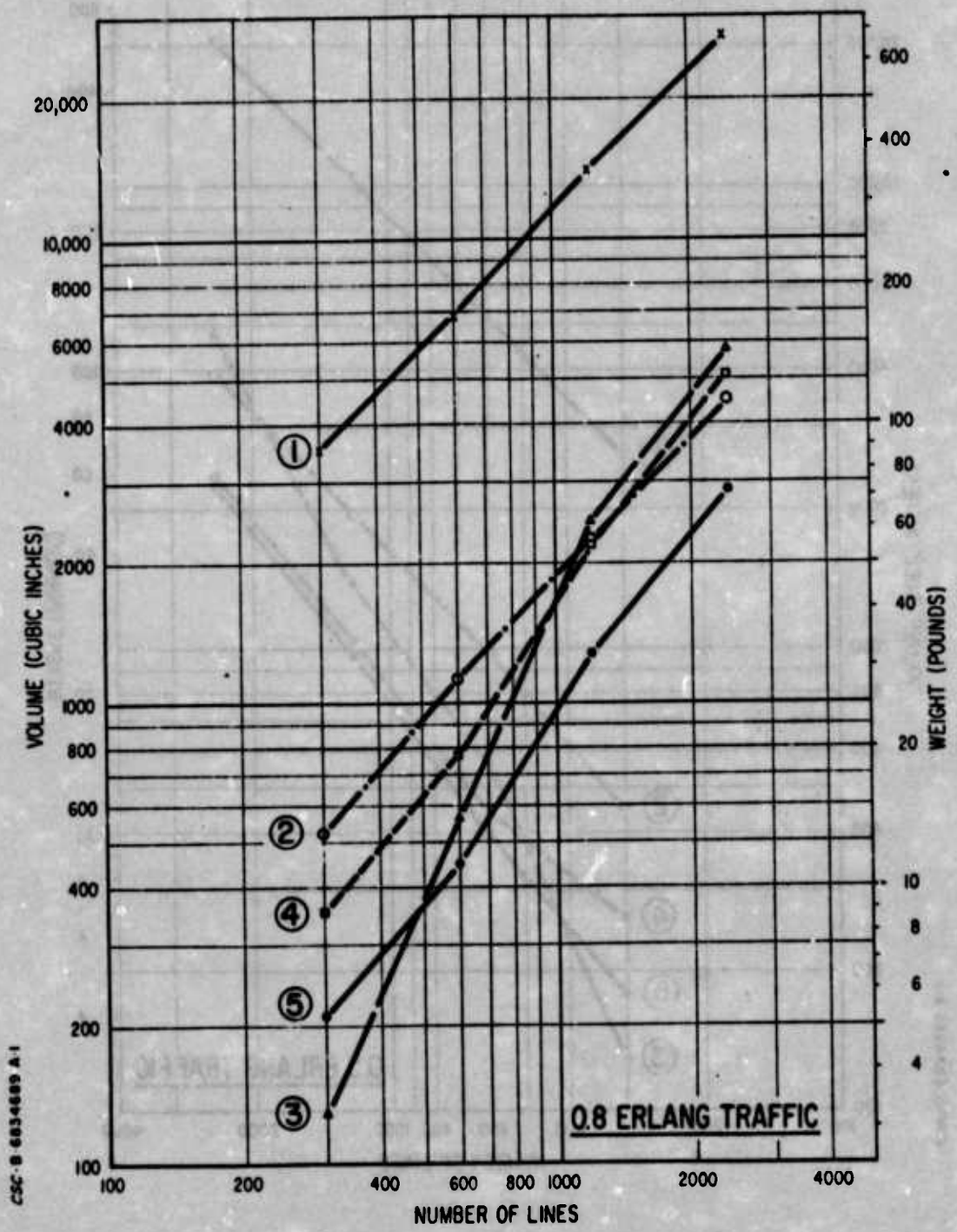



**Figure 21. Matrix Size/Weight Vs Number of Lines (0.8 Erlang Traffic)**

In order to develop a tradeoff parameter to compare ISMTC matrix candidates on a size and weight basis, it is desirable to adjust the values by the distribution of switch line capacities expected in field operation. The AN/TTC-39 specification (Reference 4) provides guidance in this respect. The anticipated distribution of AN/TTC-39 switches is given by Table 3. Note that 96 percent of the switches have a capacity of 600 lines or less. A single figure of merit which may be more indicative of a candidate's overall space requirements is a weighted average of the range of switch volumes. This is obtained for a specific candidate by multiplying the volume for each line capacity by the corresponding percentage of switches (given in Table 3) of that capacity and summing the results for all switch capacities. These calculations were performed and the results obtained are shown in Table 4 for all five candidate systems. Average volumes are given for both 0.5 and 0.8 average trunk occupancy. Table 4 indicates that the average matrix volume in a typical network composed of Candidate 5 matrices designed to handle 0.5 Erlang traffic loading is 310 cubic inches. This weighted average for the volume parameter is less than that for any of the other candidates.

2.1.3.2 Power Consumption

A plot of power consumption versus number of lines for the candidate matrices at 0.5 and 0.8 average trunk occupancy (i.e., Erlangs) is given in Figures 22 and 23, respectively. Calculations were based on 300-, 600-, 1200-, and 2400-line configurations.

The power consumption for each of the TD matrices was determined by first tabulating the number of chips of each type (e.g., RAM, Multiplexer, Shift Register, etc.) in each candidate. The power dissipation for each chip type was determined by referring to recent (1973) catalogs for comparable chips. The total power consumption for each matrix was then calculated by multiplying each chip dissipation by the quantity of chips required and then summing the results for all chip types.

The results of the above analysis are projected for 1976 by multiplying by 0.8. This 0.8 figure is derived from Reference 3 which projects an average 7.7 percent decrease per year in bipolar gate dissipation between 1971 and 1975 and a 3.7 percent decrease per year during the 1975 to 1980 time frame.

Power consumption calculations for the space division matrix are based on the assumption that the crosspoint chips are CMOS integrated circuits and the maximum data rate is 32 kb/s. CMOS gate power consumption is proportional to frequency. Presently a typical CMOS gate dissipates approximately 50 $\mu$W at 32 kb/s. Of the approximately 800 gates on each 8 x 8 crosspoint chip only a maximum of 32 gates are operating at the 32 kb/s rate. This analysis yields 1.6 mW per chip for 1.0 Erlang occupation per line. The corresponding figures for 0.5 and 0.8 Erlangs are 0.8 mW/chip. The maximum number of chips carrying 32 kb/s traffic in the 2400-line space division switch of Figure 10 is about 560. Thus, the maximum power dissipation

Table 3. AN/TTC-39 Switch Distribution

| Subscriber Loops and Trunks | Percent of Total Switches |
|---|---|
| 150 | 1 |
| 300 | 55 |
| 600 | 40 |
| 1200 | 3 |
| 2400 | 1 |

Table 4. Matrix Tradeoff Parameters (Average for 300 to 2400 Lines)

| | Size ($in^3$) | | Weight (lbs) | | Cost (Normalized) | | Power (Watts) | |
|---|---|---|---|---|---|---|---|---|
| Candidate | a=0.5 | a=0.8 | a=0.5 | a=0.8 | a=0.5 | a=0.8 | a=0.5 | a=0.8 |
| 1 | 4046 | 5404 | 101 | 136 | 9.0 | 12.0 | 367 | 498 |
| 2 | 730 | 850 | 18 | 21 | 2.0 | 3.6 | 124 | 157 |
| 3 | 390 | 430 | 10 | 11 | 1.4 | 1.5 | 94 | 103 |
| 4 | 380 | 620 | 10 | 16 | 1.2 | 2.4 | 78 | 127 |
| 5 | 310 | 370 | 8 | 9 | 1.0 | 1.2 | 67 | 79 |

anticipated for a 2400-line space division matrix due to the CMOS crosspoint chips is approximately 728 mW (560 x 1.3 mW).

In addition to the crosspoint chips the space division matrix requires line drivers to interface the 300-line modules to form a 2400-line matrix. Assuming 75 mW/line driver and 33,600 drivers yields about 2,500 watts for 2400-line matrix designed to handle 0.8 Erlang traffic.

An interesting aspect of these curves is that on a power consumption basis the space division matrix is more competitive relative to the TD candidates in comparison to the results obtained in the size tradeoff. Although on a weighted average basis the space division technique is about 5 to 15 times the size of the TD schemes, the power consumption is only 3 to 6 times that required for those systems. It should be noted that virtually all power consumed in the space division matrix is due to the line drivers required to interconnect the 300-line modules which are the building blocks for larger switch sizes. This is because the crosspoint chips are assumed to be fabricated with CMOS for which the switching power consumption is proportioned to frequency. The 32 kb/s maximum rate required for the digital space division approach results in very low power requirements. An inherent feature of all space division arrays is that only a small fraction of the total number of crosspoints are closed at any time, even for peak traffic loads. This factor, combined with the CMOS power consumption characteristics, results in an estimated maximum power requirement of less than one watt for the total number of crosspoints necessary for a 2400-line space division matrix exclusive of line drivers. Thus, if it were deemed advisable to remove power from the unused line drivers of the smaller switch configurations, then space division matrices below 1200 lines would be quite competitive from a power consumption point of view. For example, the power requirement for a 1200-line matrix would be cut in half by removing power from the unused line drivers.

Figures 22 and 23 indicate that, below the 400-line region, Candidate 3 uses the minimum power of all the candidates. For larger switches the best choice from a power requirement point of view is Candidate 5. Again as for size, an overall tradeoff figure of merit reflecting the distribution of switch capacities is the weighted averages of power consumption for each candidate as shown in Table 4. This table indicates that minimum power consumption results from a switched network composed of Candidate 5 type switches.

2.1.3.3 Cost

Figures 24 and 25 represent the relative costs of the various candidate systems using certain results obtained in Reference 2. The present costs have been normalized relative to the least costly matrix (Candidate 3 at 300 lines). It is expected that the costs of each candidate with respect to one another will not change appreciably in the near future.

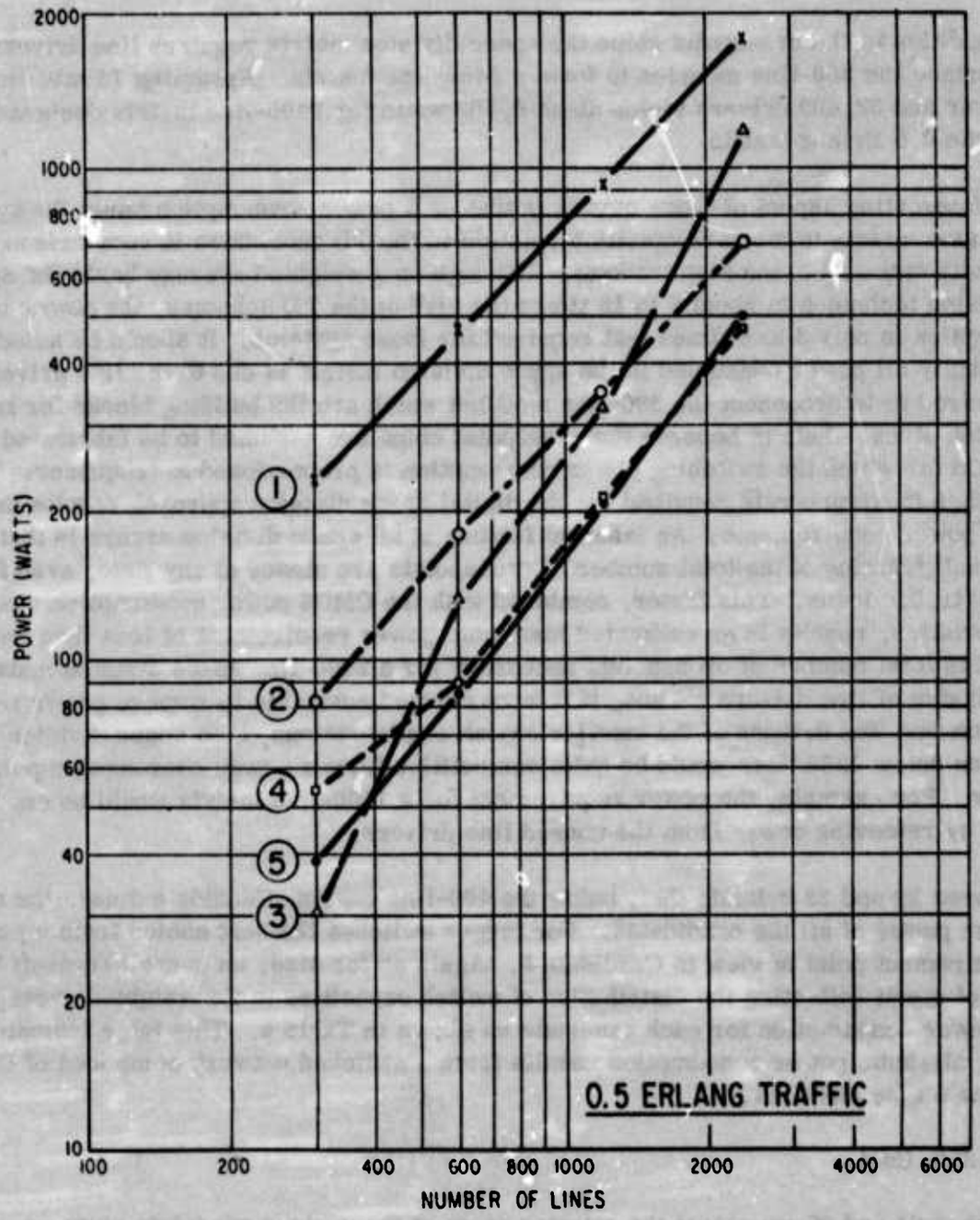



Figure 22. Power Consumed vs Number of Lines (0.5 Erlang Traffic)

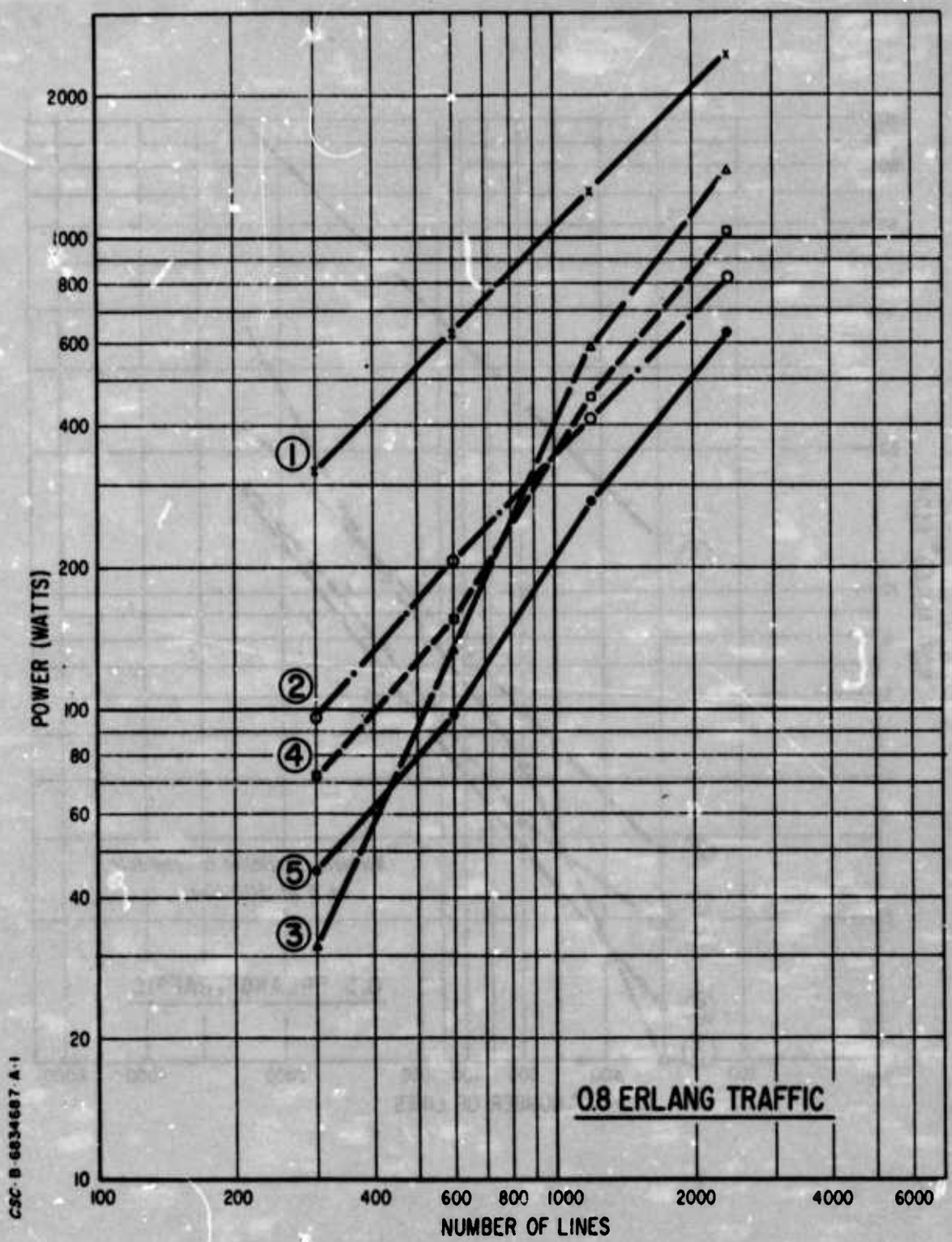



Figure 23. Power Consumed Vs Number o' Lines (0.8 Erlang Traffic)

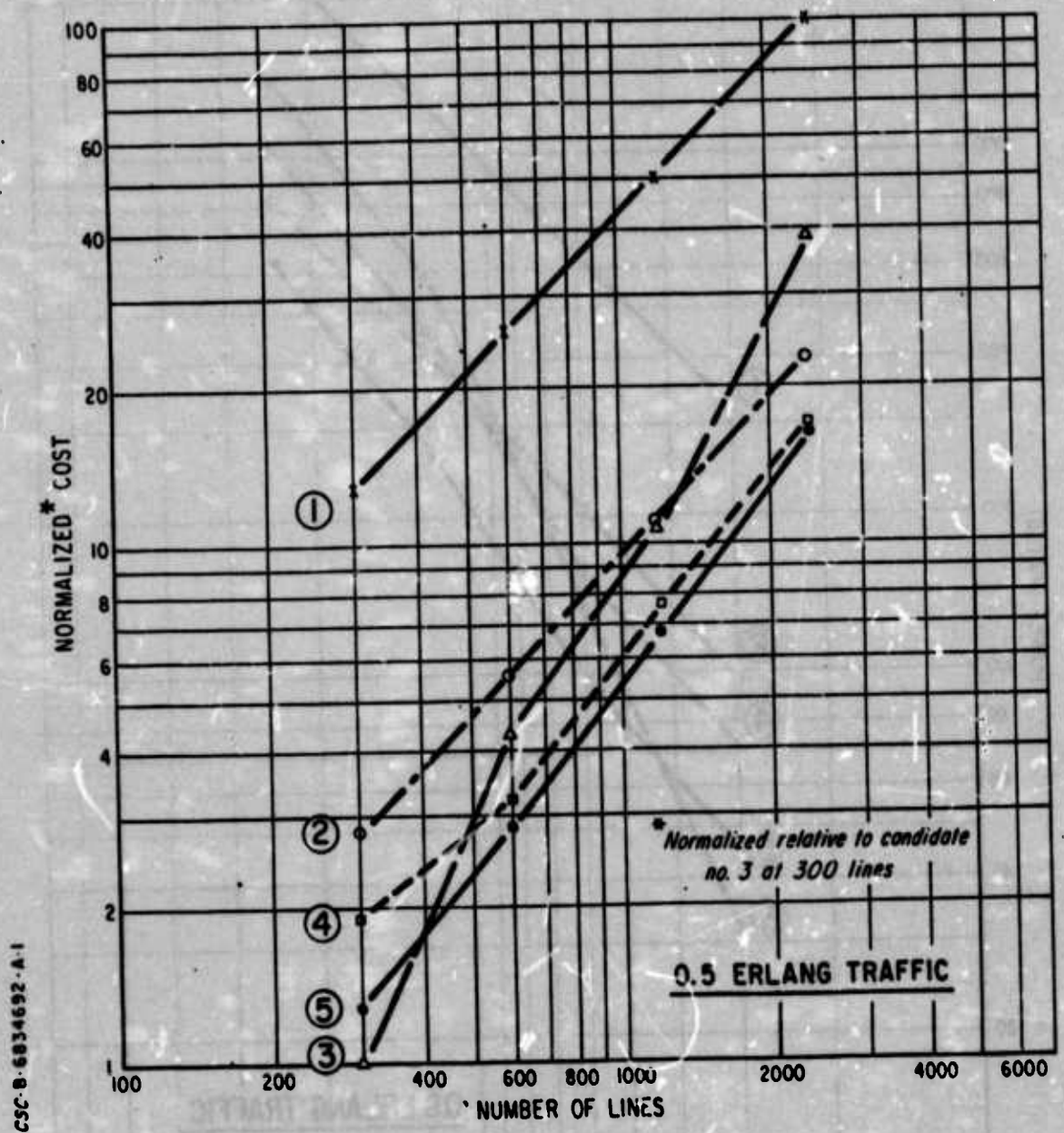



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**Figure 24. Relative Cost Vs Number of Lines (0.5 Erlang Traffic)**

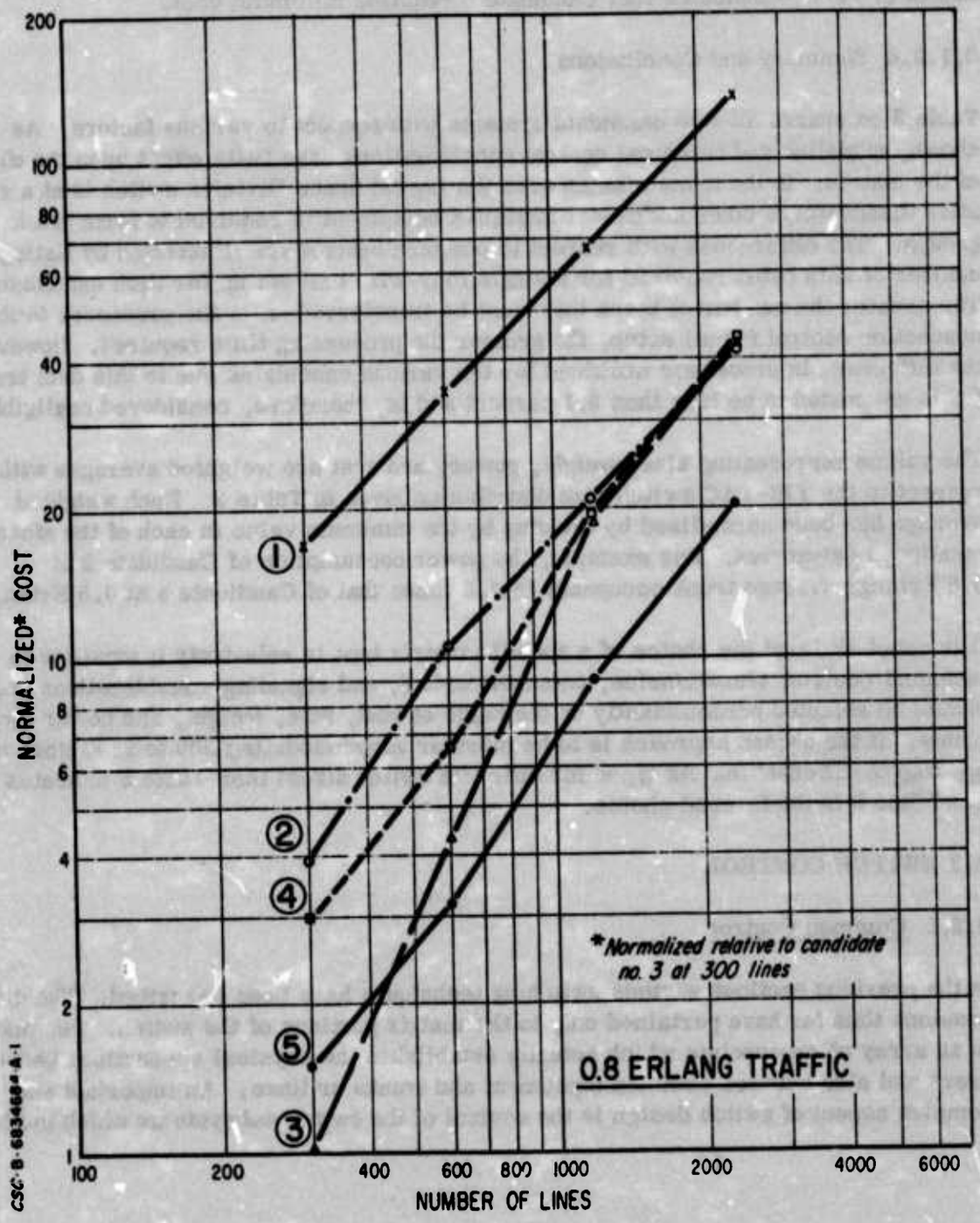


**Figure 25. Relative Cost Vs Number of Lines (0.8 Erlang Traffic)**

Again Candidate 5 is the least expensive approach for larger systems and Candidate 3 is the most economical for small systems. The weighted average for all system sizes shown in Table 4 indicates that Candidate 5 requires minimum cost.

2.1.3.4 Summary and Conclusions

Table 5 compares all five candidate systems with respect to various factors. As shown, signaling and technical control considerations have little effect upon the choice of the matrix. In the transmission area the Digital Space Division switch is at a relative disadvantage since additional multiplex equipment is required to form trunk groups. The differences with respect to common control are illustrated by listing the number of data bytes required for a single four-wire call set up for each candidate. The greater the number of bytes that must be transferred from the processor to the connection control for all setup, the greater the processing time required. However, the difference in processor workload for the various candidates due to this data transfer is estimated to be less than 0.1 percent and is, therefore, considered negligible.

The values representing size, weight, power, and cost are weighted averages with respect to the TRI-TAC switch size distribution given in Table 3. Each weighted average has been normalized by dividing by the minimum value in each of the aforementioned categories. For example, the power consumption of Candidate 2 at 0.8 Erlangs average trunk occupancy is 2.3 times that of Candidate 5 at 0.5 Erlangs.

It is concluded that the choice of a specific matrix type is relatively insensitive to technical control, transmission, common control, and signaling considerations and should be selected predominantly on the basis of cost, size, weight, and power requirements. If the chosen approach is to be modular accommodating 300 to 2400 lines (as opposed to different matrix types for different switch sizes) then Table 5 indicates that Candidate 5 is the favored choice.

## 2.2 SWITCH CONTROL

### 2.2.1 Common Control

In the previous sections various switching techniques have been described. The discussions thus far have pertained only to the matrix portions of the switch. The matrix is an array of crosspoints which actually establishes the physical connections between users and also between common equipment and trunks or lines. An important and complex aspect of switch design is the control of the switch subsystems which include:

Table 5. Matrix Tradeoff Table

| Candidate Matrix | Transmission | Signaling | Common Control (bytes/call set-up) | Technical Control | Size/Weight | | Power Consumption | | Cost | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | a=0.5 | a=0.8 | a=0.5 | a=0.8 | a=0.5 | a=0.8 |
| 1. Digital Space Division | * | NE | 9 | NE | 13.0 | 17.5 | 5.5 | 7.4 | 9.0 | 12.0 |
| 2. TD Module Array | NE | NE | 18 | NE | 2.4 | 2.8 | 1.8 | 2.3 | 2.0 | 3.6 |
| 3. Redundant Memory | NE | NE | 8 | NE | 1.3 | 1.4 | 1.4 | 1.5 | 1.4 | 1.5 |
| 4. Space-Time-Space | NE | NE | 18 | NE | 1.2 | 2.0 | 1.2 | 1.9 | 1.2 | 2.4 |
| 5. Time-Space-Time | NE | NE | 18 | NE | 1.0 | 1.2 | 1.0 | 1.2 | 1.0 | 1.2 |

* = Requires MUX

NE = Negligible Effect

a = Average Per Line Occupancy

1. Matrix

2. Digit Receiver (DR)

3. Trunk Send Buffer (TSB)

4. Trunk Receive Buffer (TRB)

5. Conference Bridge (CB)

6. Supervisory Tone Generator (STG)

Matrix connections are controlled by the processor via the connection control (CC). For both space and time division arrays the CC serves as the memory for the matrix in which the status of each crosspoint is recorded. In this way the matrix operates independently of the processor unless a connection is to be altered. The setup or release of a connection is initiated by the processor by transferring connection data into the CC. Once this data is stored the CC acts to control the matrix in such a way as to implement the new connection.

The following paragraphs deal with the mechanisms by which the processor controls items 1 through 6 above. Processor functions and characteristics are described in detail in Section 5.4.

2.2.1.1 Connection Control

The CC provides the control words to the matrix for switching any channel input to any channel output. The CC possesses a memory which contains the information needed to specify all current connections through the matrix. For the most part, the CC operates independently of computer control. The central processor intercedes only to change call connections by transmitting new data to the CC memory. It should be noted that the CC may be segmented and distributed among the basic modules and even among the space division crosspoint chips. Thus, although functionally separate, the CC may physically be an integral part of the matrix.

2.2.1.1.1 Space Division Array Connection Control

The CC memory of the space division array described in paragraph 2.1.1 is the 16 flip flops on each chip shown in Figure 7. Each bit represents the status of one crosspoint. The status of the crosspoint is changed by clocking a new binary state into the flip flop.

A block diagram illustrating one possible method of space division matrix control is shown in Figure 26. Each 4 x 4 four-wire matrix chip requires six control inputs; four determine the crosspoint, one selects the chip, and one defines the new crosspoint

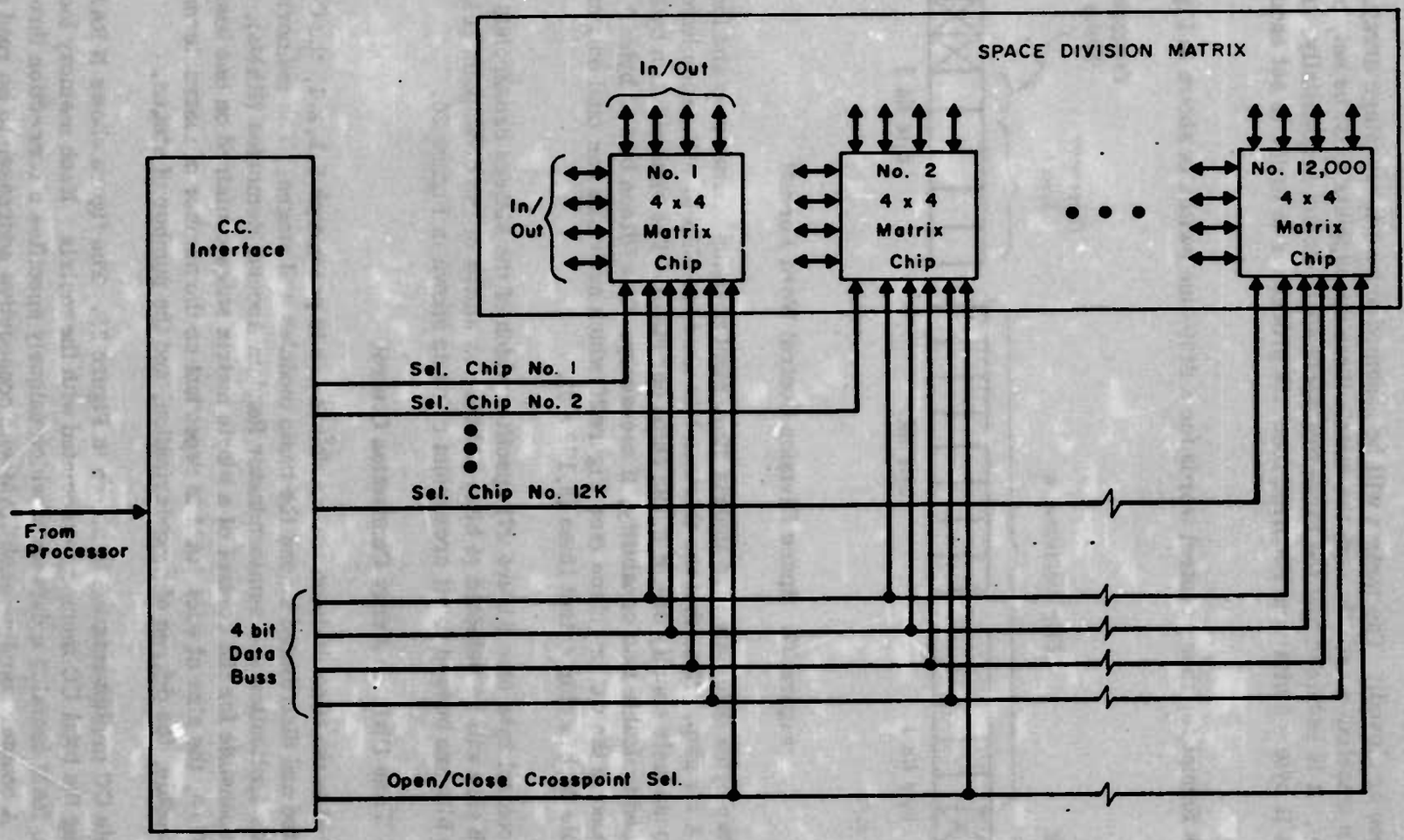


Figure 26. Space Division Matrix Control Block Diagram

status (open or closed). The matrix will be assumed to be a three-stage array. Thus, in order to establish a path through the matrix three crosspoints must be set, one for each stage. It is assumed that the three crosspoints will be set sequentially. Three data bytes (1 byte = 8 bits) are required from the processor in order to set each crosspoint.

A possible format for these control words for a 2400-line switch is shown in Figure 27.

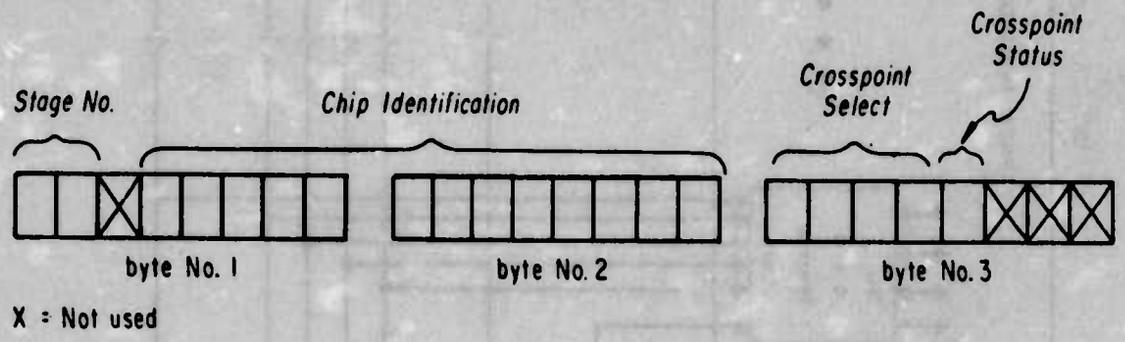


Figure 27. Space Division Control Word Format

The first two bytes determine the matrix stage number being operated on and identify the actual 4 x 4 chip. Note that the thirteen bits used for chip identification have the capacity to uniquely specify one of 8,192 chips per stage. The unused bit in byte #1 could be used to double this capability, if necessary. The fifteen bits of bytes 1 and 2 are decoded in the CC interface (see Figure 26) which activates one (and only one) of a possible 24,576 chip select lines (8,192 x 3).

The third control byte (see Figure 27) specifies which of the sixteen crosspoints within each chip will be selected (4 bits) and the new status of the crosspoint (1 bit). These five bits are bussed to all crosspoint chips as shown in Figure 26.

2.2.1.1.2 Time Division Array Connection Control

As described in the time division matrix discussion in paragraph 2.1.2.1, the CC may be segmented and distributed among the basic modules and stages. The memories used for this application are semiconductor Random Access Memories (RAMs). Each RAM is responsible for the control of a single matrix stage contained on one basic module. Thus, the size of each RAM is dependent on the number of matrix terminations per module, the degree of modularization, and the number of stages.

One possible CC implementation is shown in Figure 28. The figure shows N RAMs representing the total CC memory associated with the matrix. Each memory location within a CC RAM contains a data word which uniquely specifies a connection through one stage. A counter supplies each RAM with consecutive addresses to be read out.

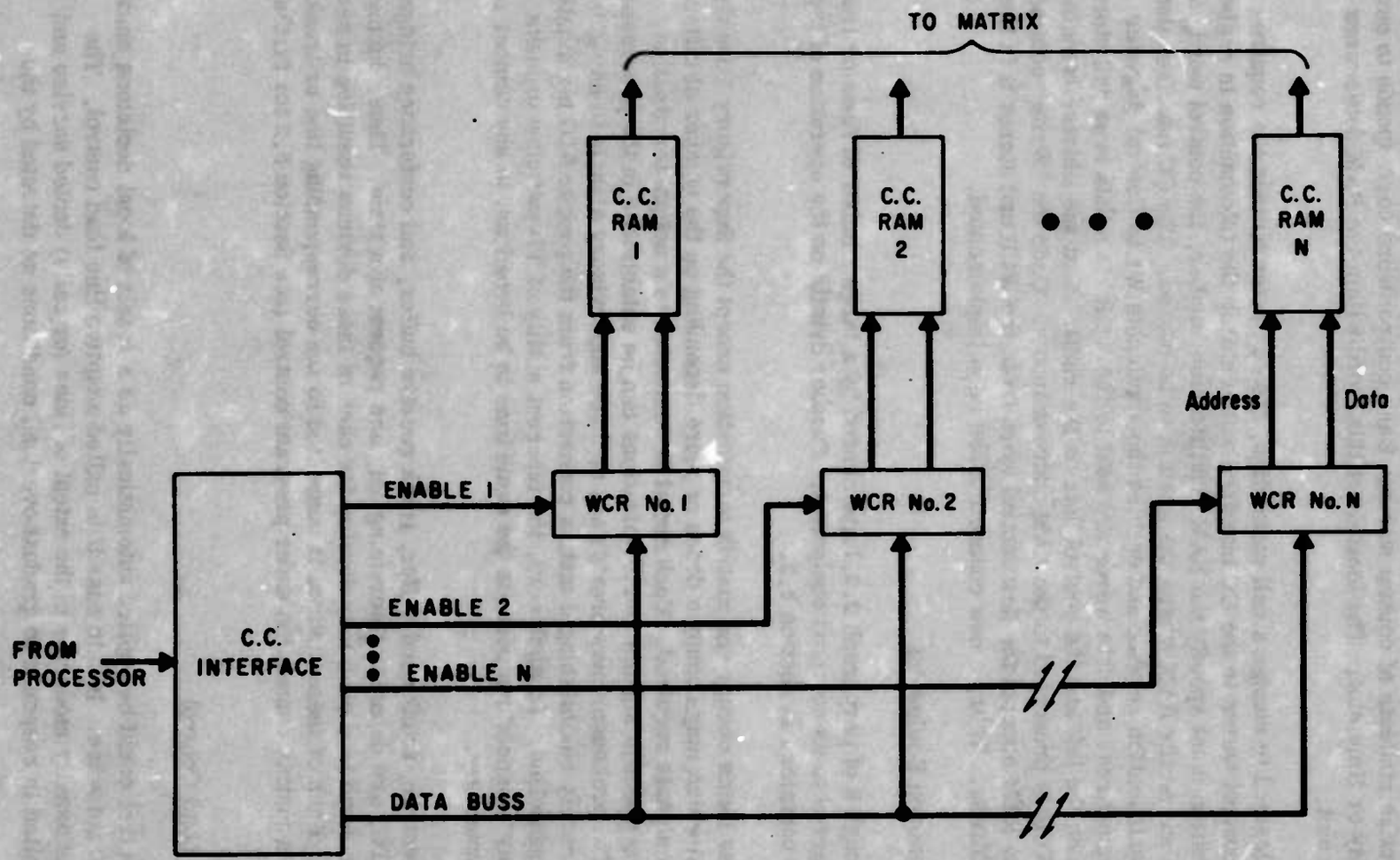


Figure 28. Time Division Matrix Control Block Diagram

The counter is allowed to cycle repeatedly, thus causing the RAM to periodically output its entire contents of control words. Each control word corresponds to one input highway or time slot. The location of this word within the RAM determines the output time slot.

When it is desired to change a call connection, the computer outputs the required number of control words to the CC interface which stores the information in registers. This information must specify the RAM identification number, the control word, and the address within the RAM where the word is to be stored. The CC interface decodes the RAM identification number and enables the applicable Write Control Register (WCR). The address and data words are sent to the WCR via a data buss and stored, the address on the left and the control data on the right. Next the address contained within the WCR is presented to the RAM address inputs. Once the "Write" command is given, the RAM accepts the new control word from the WCR and stores it in the specified address. Thus, a new connection has been implemented.

2.2.1.2 Common Equipment

Items 2 through 6 of paragraph 2.2.1 are shared by a large number of lines or trunks and are referred to as common equipment. Further details on the operation of these devices are contained in Section 5.2.

Each of these items occupy one matrix termination except the Supervisory Tone Generator (STG) which may occupy a dozen or more depending on the number of different supervisory signals required. Each signal is connected to a unique termination. A table relating specific signals and terminations can be established in the processor memory. The processor may provide any of these supervisory signals to any subscriber by merely establishing a matrix connection from the proper STG termination to the applicable line. Furthermore, the inherent ability of TD switches to make "one-to-many" connections permits the same tone to be broadcast to any number of lines simultaneously.

The digit receiver, trunk send buffer, trunk receive buffer, and conference bridge, unlike the STG, are capable of servicing only one request at a time. Thus, during heavy traffic service queues may develop for each of these devices resulting in service delays. Each of these devices is connected to the corresponding line or trunk by means of a matrix connection under program control (see Section 5.2 for further details).

2.2.2 Line Load Control

Line load control could be applied automatically as a result of local decisions made in the ISTMC software. In this case it is called adaptive line load control. The application is usually moderate in the extent of lines (or calls) denied service and would be applied in response to gradual overload conditions as detected by the

technical control traffic monitoring routines. Where overload is rapid and excessive, a more extensive denial of service to a large number of line groups is required and will be controlled by the Systems Control Node responsible for that tactical area. This procedure is called drastic line load control. The Systems Control Node can have available to it a more moderate denial of service through selective line load control as well as a number of subsidiary techniques to limit call duration and duration of the ringing signal.

2.2.2.1 Adaptive Line Load Control

The adaptive line load control could be achieved by denying service to routine and perhaps low priority users on a class of service or priority basis. As this is a random application, all lines in this category will be denied service equally during overload periods without any one line or group being singled out.

This control would deny service to routine users and the number of denials would increase with the degree of overload. Again, this control may be applied only under overload conditions as determined by the thresholds set in the traffic monitoring software routines. This service denial by class and type of service requires a modification of the translation tables to indicate the class of service to be denied. This would be indicated to the common control processor which in turn would deny any request for service by action of the input dial digit receivers.

Figure 29 shows a functional flow diagram of the interactions required between the switch processor and the sensing and control hardware. Following the sequence of events one through seven as shown on the figure, the processing of the service request (off-hook signal) would be the same as a normal request up to the translation stage at which point the class of service would show a service denial and so indicate to the originating register. The originating register cancels dial tone and forwards a Forced Service Denial request to the translation program.

In this manner of disposing of the service requests, dial tone is never applied to the line by the common control call setup routine and, therefore, congestion in the switch matrix is avoided. In order for the line load control procedure to be adaptive to the degree of overload, the application of the procedure is automatic and based on logic inputs from the main traffic load monitor. As overload continues or increases, the number of classes denied service increases. As the load diminishes, the number of classes denied service decreases until the normal load is reached as indicated by a threshold setting contained in software. As shown in Figure 29, it would probably be advisable to provide a manual entry key to initiate line load control under operator control. The manual start key may take the form of a command generated at the operator command console.

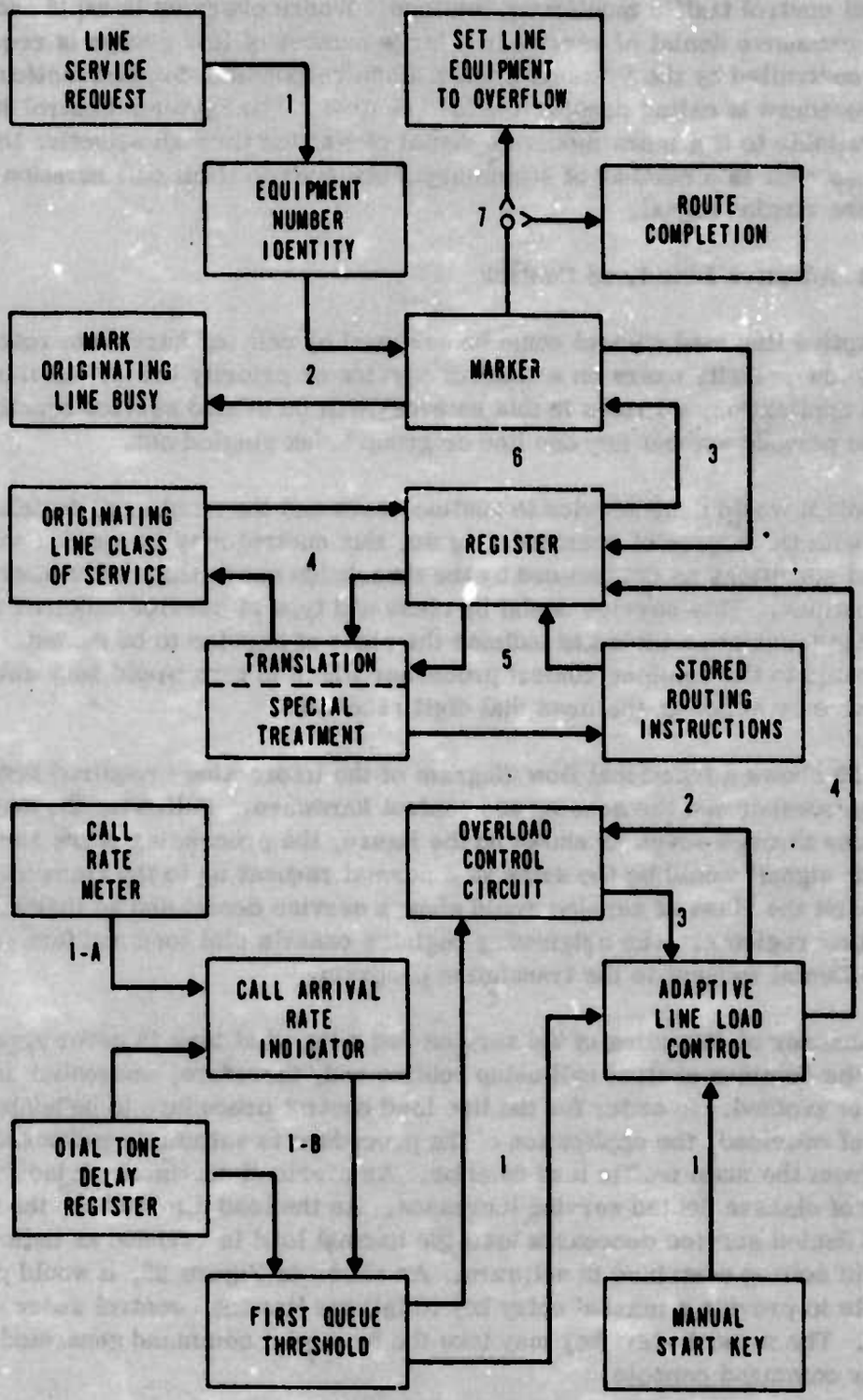


Figure 29. Adaptive Line Load Control Automatic/Manual Start

#### 2.2.2.2 Drastic Line Load Control

Drastic line load control should be under the command of the System Control Element based on area-wide traffic data supplied automatically by the ISMTC traffic monitors. It is invoked under the conditions of rapidly building and extensive overload as indicated by excessive call delay and high call arrival rate.

Drastic line load control is applied directly to specific line groups by the manual action of the local switch operator or automatically by the program intervention of the ISMTC processor or Communication System Control Element (CSCE) processor. In either case hook scanner recognition of call requests is denied system users. Drastic line load control differs from adaptive line load control in that the degree of denial of service is not varied with traffic load conditions. The denial of originating (out-going) service can be accomplished without restricting the ability to receive (incoming) calls.

### 2.2.3 Trunk Barring

Barred trunk access, or trunk load limiting, is a technique whereby certain users of the network are denied access to the trunking system but are permitted interconnection to other users homed on the same switch. Barred trunk access can be either adaptive or fixed. In either case, initiation and/or coordination of the control function is required from the CSCE due to the effect on other system nodes resulting from the disturbance to the internode trunk connectivity. Adaptive control adjusts trunk barring action to the degree dictated by the network congestion. Fixed trunk barring schemes generally drastically reduce the number of trunks available to the routine user in a way which is unresponsive to short term improvements in the congestion situation and, therefore, is often referred to as "ruthless" barring.

### 2.2.4 Call Limiting

Other methods of limiting traffic congestion can be implemented by the System Control Element short of the denial of service results from line load control or trunk barring. These involve processor imposed restrictions on call duration and ringing time.

#### 2.2.4.1 Call Duration Restrictions

Call duration restrictions can be imposed on lines by class and/or type of service by the addition of an Automatic Disconnect Routine (ADR). This routine times calls initiated on marked lines and, when the preset interval expires, causes call disconnect. If this technique is used, it is generally recommended that a warning tone be inserted on the line shortly before disconnect occurs.

In addition to providing the ADR, modifications are required in the network control and call disconnect programs. Also, class marking additions have to be built into either the line termination hardware or the control software.

2.2.4.2 Limited Ringing Duration

Limit control of ringing time can provide some lessening of congestion by decreasing trunk seizure overhead time. Provision of a timed ringing control routine would permit the monitoring of each call initiation attempt and provide a forced ringing disconnect at the end of the preset timed interval (e.g., one minute). Use of this procedure can be restricted to routine calls if desirable. This procedure, however, would have little effect during severe congestion.

## 2.3 SPECIAL SERVICES

Tactical network switching centers are generally required to provide special services in addition to call connect and disconnect. As a minimum, priority recognition and preemption are provided. The advent of flexible processor controlled switches permits the introduction of other special services to make the communication system more responsive to the needs of its users. Some switch services are accomplished in software, placing an increased load on the processor, while others are accomplished in hardware, increasing the equipment complexity. An integrated facility supporting tactical communications for the 1980s should supply the following special services as a minimum: priority recognition, preemption, conferencing, off-hook (hot-line) service, and attendant recall. In addition, consideration should be given to providing abbreviated or compressed dialing, call transfer, call forwarding, and camp on. The special service features of interest to the integrated switch/multiplex/technical control complex are discussed in the following paragraphs.

### 2.3.1 Precedence and Preemption

A priority (precedence) rating is generally assigned to military users to reflect the relative importance of their communications. Preemption is the action of interrupting an established connection between two users of lower priority and reseizing the access line or trunk when there is no idle circuit available to complete a higher priority call. The specifications for the TRI-TAC switch (AN/TTC-39) recognizes five levels of priority for the users of the circuit switch in descending order of precedence as follows: Flash Override (FO), Flash (F), Immediate (I), Priority (P), and Routine (R). The DCS AUTOVON switches also use a five-level precedence scheme with precedence designations consistent with those given above. It would be desirable, therefore, for the integrated facility to employ a precedence scheme consistent with the above.

The implementation of the priority and preemption plan must be considered in the ISMTC design. The switch actions required are as follows.

If a user selects his allowable priority or a lower priority, the call setup proceeds in the normal fashion. If a user is not permitted the call priority requested, the switch must automatically notify the user that he is not entitled to that priority. Flexibility would be enhanced by implementing the line priority identification by means of the stored program approach rather than hardwired. By this means the switch operator can reassign priority classes through the command console.

Before preemption takes place, a disconnect (preempt) signal must be sent in both directions to notify the users that they are to be disconnected. The switch must then disconnect the line from the existing call, connect the higher priority call, and return an identifiable signal to the disconnected user or users. Generally a busy signal is satisfactory for this purpose preceded by a distinctive tone to permit the user to identify the type of disconnect.

### 2.3.2 Conference

The ISMTC must provide the capability for both random and preset conference calls. A random, or progressive, conference is based on the technique whereby the conference initiator sequentially dials each desired conferee into the conference. The conference initiator generally waits to verify the success or failure of each conferee connection before proceeding to dial the next conferee on the conference list. Generally, access to the random conference service is obtained by dialing, or keying, an assigned digit at a predetermined position in the dialing sequence. A preset, or preprogrammed, conference is initiated by dialing a preset code which is related to a preset list of conferees; that is, the code is translated into a preprogrammed list of outgoing codes and the switch automatically establishes a connection to the conferees associated with the codes.

A major distinction exists between the two in terms of the switch implementation. The preset conference implies the use of software routines and conferee address tables stored in the switch. The amount of storage capacity required is a function of the number of preset conferences permitted and, therefore, this capability should be restricted as much as possible. The response time requirement for preset conference setup would permit the use of auxiliary storage such as drums or discs to store the address of each conferee. Space and weight requirements should be considered, however, before the number of preset conferences are assigned per switch.

Progressive or random conferences are primarily a function of switch hardware since conference addresses are supplied sequentially by the user or switch operator. The common control can treat call setup in the manner it does for ordinary calls. Limitations are imposed by conference bridging hardware.

### 2.3.3 Broadcast

Broadcasting provides the means for a calling party to reach a number of predesignated users simultaneously. The broadcast service is similar to the random and preset conference with the exception that transmission is one way, i.e., unidirectional from broadcast originator to the called parties. The impact on the switch and its storage requirements is similar to that discussed in the conferencing paragraph above. Tactical requirements usually place greater emphasis on the preset broadcast capability to handle rapid command dissemination to the affected echelons. As a result, response requirements in some cases will be more severe than the conferencing requirement.

### 2.3.4 Abbreviated Dialing

Abbreviated dialing, or keying, consists of making special arrangements to place calls to a number of predetermined addresses by dialing a two- or three-digit code. The two- or three-digit code is translated in the switch processor to the full address. The switch processor stores the full address required to establish the interswitch call and, therefore, the load on the processor is a function of how many users are permitted to use the abbreviated dialing procedure. Naturally this procedure should be limited to those users requiring rapid emergency response.

Repertory dialers can be used if the requirement for speed is not essential but rather the ability to remember the number of the called party. In this case the equipment complexity is moved from the switch to the user's end instrument. Both mechanical and electrical repertory dialers are available to serve this function. Mechanical dialers are usually achieved by insertion of a prepunched card while electrical dialers generally have magnetic memories.

### 2.3.5 Call Transfer

This service provides the user with the capability to transfer an incoming call to another directory number. When an incoming call is answered by the called party, that party is able, by switch hook or button operation, to place the existing call on hold and obtain connection to a register. A new number is then dialed and the party on hold is automatically transferred to the new number when the transferring party goes on hook. This is basically implemented in hardware with little impact on the stored program.

### 2.3.6 Call Forwarding

With this service a user can have all incoming calls automatically transferred temporarily to a different telephone by dialing a unique code followed by the number to which he wishes his calls transferred. The information he dials in is used to update the directory table to permit connection to the new location. This condition exists until

the reverse transfer is made. This service has more impact on the processor portion of the switch than does call transfer, since software changes to the user-line address table must be performed in response to the user's request. The hook scanning routine is required to recognize a call forwarding request and notify the operating program which in turn is required to call upon a special application program which alters the user-line address table.

### 2.3.7 Hot-Line Service

Hot-line service can be provided on both full period and demand basis. On the demand basis, when the hot-line is not being used, the trunking is used for lower precedence traffic. If a hot-line subscriber uses the same instrument for hot-line calls as that for conventional calls, the service request must be accompanied by a special off-hook signal denoting request of the hot-line. The switch then immediately establishes the call to the previously stored number. The automatic sole-user call setup routine can preempt all other calls to assure virtual hot-line service. The call setup delay can be well under one second and, therefore, appear to be negligible to the user. An advantage to this approach is that the "dedicated" hot-line has the full alternate routing and restoral capability of the switched network and is monitored by the technical control portion of the node.

Full period hot-line service requires a permanently established connection. It is recommended that the ISMTC handle this on a wired-through basis but with the user line terminated on the TDS/TDM matrix to obtain the advantage of the technical control rearrangement, fault, and quality monitoring routines.

### 2.3.8 Camp On

The camp-on service eliminates the need for a calling user to redial the called party if the called party is presently busy; that is, the calling party can remain off hook and wait until the called party goes on hook. When this occurs, the switch automatically completes the connection. Implementation of this feature is not difficult from a hardware and software standpoint, but has a serious network disadvantage for interswitch calls. The originating and intermediate switches will be required to seize trunk and matrix connections in anticipation of eventual call setup. During busy conditions this offers a substantial phantom traffic load to the system. For this reason, camp-on capability is generally not implemented in switched networks. Camp on can have utility as a user service for intraswitch calls and for interswitch calls if procedural arrangements are programmed into the processor to preempt camp-on calls for all other call requests.

## 3.0 MULTIPLEXING/DEMULTIPLEXING

A major objective of this study is the incorporation of the multiplex function into the switch as an integral part, or as distinct elements, of an integrated design. The advantages of such an approach include:

1. Simplification of fault and quality monitoring.
2. Decreased size, weight, and power requirements.
3. Simplified field setup (cabling, interconnections).

An important consideration in the switch/multiplex design is that a sufficiently high degree of flexibility be maintained to accommodate the required range of trunk groupings. Although the precise trunk group sizes have not as yet been specified for the 1980s, a design approach is presented in the following paragraphs which will likely provide the desired flexibility.

### 3.1 MULTIPLEXING TECHNIQUES

#### 3.1.1 Frequency (Space) Division Multiplex

In frequency division multiplex systems, each channel of the system is assigned a unique portion of the frequency spectrum. The total amount of bandwidth required per channel is dependent upon the type of modulation plan used to place each channel into its assigned portion of the frequency spectrum. There are basically three types of modulation plans used in FDM systems. They are:

- Single Sideband, Suppressed Carrier (SSB-SC)
- Double Sideband, Emitted Carrier (DSB-EC)
- Double Sideband, Suppressed Carrier (DSB-SC)

There are specific applications where one type of modulation is already preferable to the others, not so much from a performance standpoint but from an economic point of view. For example, when considering the cost of multiplex equipment alone, the cost of the SSB-SC modulation systems is higher than that of the other two. This is primarily due to the cost of the additional filtering required to remove the unwanted sideband and carrier. However, for this additional cost, voice frequency channels can be placed adjacent to each other, each occupying 4 kHz of the frequency spectrum. When the number of channels involved is large or where the transmission path is long, the additional cost of the terminal equipment is more than offset by a fuller utilization of the bandwidth available in the transmission path. For example, in a radio path having a baseband bandwidth of 2.5 MHz, 600 SSB-SC channels can be accommodated.

This same radio facility could accommodate only 300 DSB channels. As a result SSB-SC has become the predominant method of frequency division multiplexing.

The same basic considerations as outlined above will apply to a coaxial cable system where the cost of the cable and the associated repeaters forming the transmission path may be significantly larger than that of the terminal equipment.

Double sideband, emitted carrier, provides the least expensive circuitry on a per channel basis. Transmitting the carrier on each channel has the disadvantage that the repeater is called upon to handle a larger amount of power. This disadvantage is somewhat alleviated with the DSB-SC method, but at the expense of complicating the terminal equipment since means must be devised to recover (re-insert) the carrier at the receiver. The DSB-EC and DSB-SC approaches are very seldom used in modern multichannel FDM design.

It should be noted that existing FDM equipment was designed primarily for optimum transmission of voice frequency signals. Since voice and data signals differ appreciably, digital transmission via FDM is far from optimum. In addition, FDM does not permit functional integration with the switch as does a TDM/TDS approach (i.e., switch and multiplex in one equipment unit). Also, advances in LSI circuitry favor the digital or time division techniques to achieve cost, size, and weight advantages. Thus, FDM is not recommended for ISMTC applications.

### 3.1.2 Time Division Multiplex

Time Division Multiplex (TDM) is a technique used in transmitting two or more digital signals over a common path by using different time intervals for different signals. When TDM is applied to digital communications systems, data bits from different users are interspersed in time and transmitted sequentially over the same data communication channel. In other words, the communications channel is "time shared" by the users. In operation, the TDM equipment sequentially scans (samples) each incoming line and simultaneously connects the line being sampled to the output line. A framing pattern is inserted by the transmitting TDM unit to permit synchronization. This framing pattern is used as a reference to enable the receiving equipment to distribute the received data to the proper output line.

The essential requirement for TDM equipment is that the time division plan be compatible with the bit rates of the inputs. Although TDM equipment is primarily used for the purpose of transmitting digital data signals, analog signals (voice, analog facsimile, quasi-analog data, etc.) can also be accommodated provided they are preprocessed via analog-to-digital conversion equipments, e.g., pulse code modulation (PCM) or delta modulation equipment.

An extremely important advantage of TDM is that the objective of integrating the multiplexing and switching function is readily and economically achieved. Paragraph

2.1.2.1 describes four time division switch systems which utilize time division multiplexing and demultiplexing to perform the switching function. In each of these schemes TD highways are accessible for use as TDM trunk groups without the aid of external multiplex equipment.

Another advantage of employing TDM techniques is that bulk encryption could be used rather than having to encrypt each channel separately, as would be the case if all digital sources were fed directly through modems into an FDM system.

3.1.3 TD-968 ( )/G

The multiplexer TD-968 ( )/G converts 3, 6, 12, or 24 four-wire voice-frequency channels to a time-division-multiplexed, pulse-code-modulated (TDM-PCM) signal for use in a digital transmission system. This multiplexer provides a link between existing analog users and the expanded digital transmission facilities of the Defense Communication System (DCS). The TD-968 ( )/G is designed to accommodate analog telephones, data modems, and facsimile equipment. This multiplexer is compatible with the AN/GSC-24 (V).

However, the present planning for the all digital tactical environment of the 1980s provides for the accommodation of analog signals via delta modulation. The use of PCM is not anticipated and, thus, the TD-968 ( )/G would not be applicable to the ISMTC.

## 3.2 MULTIPLEX DESIGN APPROACH

A major objective of this program is to integrate to the maximum possible extent the multiplex function into the ISMTC complex. Of vital importance to tactical systems is the requirement that the multiplex schemes be sufficiently flexible to easily accommodate a wide range of local trunking requirements.

In order to formulate a complete multiplex design approach for the ISMTC, the specific trunk groupings envisioned for the 1980 time frame are required. For tactical networks, 32 kb/s delta modulation (CVSD) will likely be the means of digitally encoding voice signals[4]. Unfortunately, no trunk grouping standards presently exist for 32 kb/s delta modulation derived signals. Trunk group sizes have been assumed in the following discussion which are consistent with those discussed in the section on matrix considerations.

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[4] Based on recent voice digitization developments, there has been some indication that 16 kb/s or even 8 kb/s, digitized voice equipment may be practical in the time frame of concern to this study (i.e., 1980s). This study, however, uses 32 kb/s since this rate is the presently accepted tactical line rate.

### 3.2.1 Matrix/Trunk Group Formatter Interface

Trunk group sizes of 15, 30, and 60 trunks are used in this discussion for the tactical trunking configuration. Surveys done during prior work (Reference 2) have indicated the suitability of this sizing. In addition, trunk group sizing of 10, 20, and 40 trunks per group are desirable for interfacing with the strategic network. Figure 30 is an example of how such trunk groupings may be accommodated by a switch matrix with 60 channel input/output highways. Note that the 60-channel highways have been multiplexed/demultiplexed into 20 (or 15) channel highways. These lower capacity highways may now be combined or split in the trunk group formatter (TGF) to form the aforementioned trunk groups (see paragraph 3.2.2).

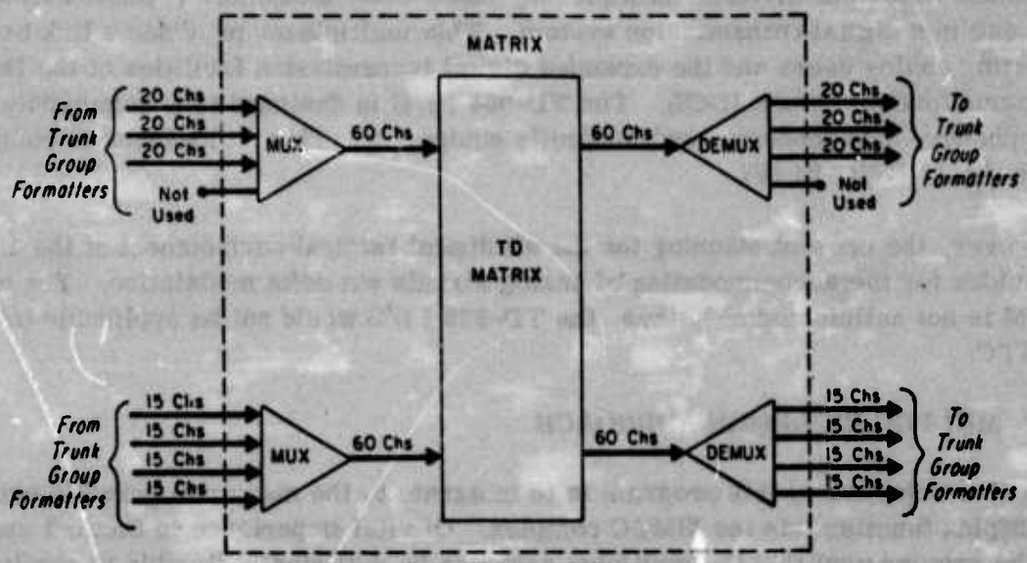



Figure 30. Trunk Group Combining/Decombining

It is important to note the flexibility achieved for handling tactical or strategic trunk group sizes. The same four-input multiplex chip is used for 20- or 15-channel inputs. The only difference between the two applications is the timing signals supplied and the fact that one input is not used for the 20-channel application. Thus, the matrix can now accept almost any combination of 20- and 15-channel highways depending upon which timing signals are supplied to which multiplexer/demultiplexer. Also note that with suitable modifications other trunk group sizes which are submultiples of 60 channels (i.e., 12 channels) may also be accommodated in a similar manner.

The group combining/decombining function has been assigned to the matrix for several reasons. First, all the high speed signals are confined to the matrix. Thus, interface with external components is possible at lower bit rates. Furthermore, the addition of these multiplex/demultiplex functions to the matrix is trivial to implement

since all incoming signals are already synchronized by the TGF. Reliability is a further factor to be considered. It is desirable to minimize the vulnerability of the system to a single fault which may affect an entire 60-channel highway. If the group combining/decombining were implemented elsewhere, 60-channel highways would at some point be transmitted to (or from) the switch matrix through a single integrated circuit. However, by integrating the function into the matrix (see Figure 30) the reliability of critical points may be increased through the use of appropriate redundancy techniques.

### 3.2.2 Trunk Group/Trunk Group Formatter Interface

The multiplex/demultiplex at the interface between the trunk groups and the TGF must also be considered. In the above paragraph, the advantages of combining/decombining several smaller size trunk groups into a 60-channel highway within the matrix was discussed. The result was a matrix with lower rate trunk group input and outputs (e.g., 15- or 20-channel trunk groups) instead of high speed 60-channel highways.

Consider the case where the switch must accommodate trunk group sizes of 10, 20, and 40 channels. The matrix would contain 20-channel input/output groups. These groups must be multiplexed/demultiplexed outside the matrix to form the desired 10-, 20-, and 40-channel groups. The TGF could provide for this function.

The output combiner/decombiner functions of the TGF are shown in Figure 31. The inputs are from the matrix in the form of two 20-channel groups. Both groups are multiplexed to produce a 40-channel group which is sent to the selector gate. One 20-channel group is split into two 10-channel groups and transmitted to the selector gate along with the original 20-channel group. A two-bit control word at the selector gate is used to determine if the output is a 10-, 20-, or 40-channel group.

## 3.3 SWITCHING OF NON-32 kb/s SIGNALS

Terminal equipment data rates planned for the future long haul and tactical communication systems are (Reference 5)

"a. $25 \times 2^{-m}$ Bds or b/s

b. 50.0 Bds or b/s

c. $75 \times 2^{m}$ Bds or b/s, up to and including 9600 Bds or b/s, where M is a positive integer 0, 1, 2 .... 7.

d. The modulation rates (expressed in Bds) and the data signaling rates (expressed in b/s) above 9600 Bds or b/s are based on 2400 x N....."

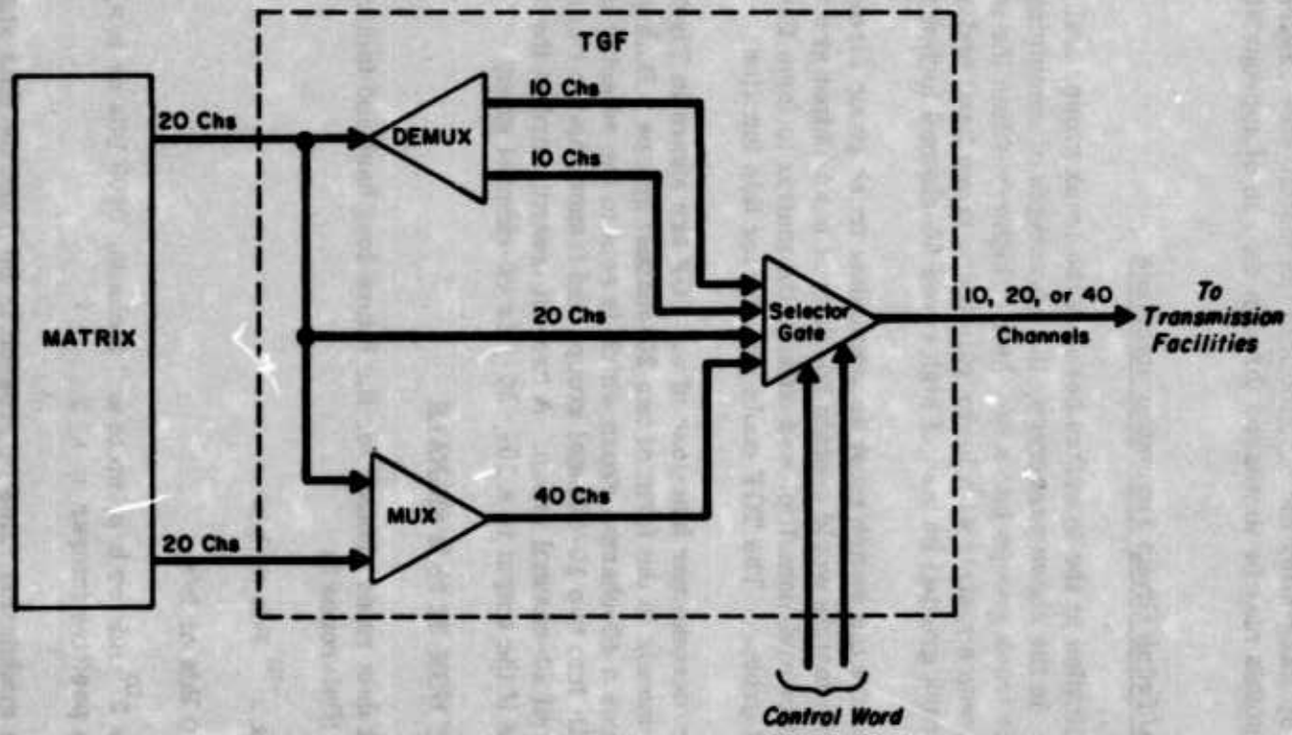



Figure 31. Trunk Group Formatter Output - Multiplex/Demultiplex Function

The handling of the very low bit rates in categories (a) and (b) above is inefficient in a high speed system such as the ISMTC unless the individual channels are multiplexed prior to introduction to the main TDS/TDM matrix. Thus, the rates described by (a) and (b) should be multiplexed external to the ISMTC with a low data rate (telegraph) submultiplexer to achieve necessary transmission efficiency.

Rates which are multiples of 8000 b/s are multiplexed/demultiplexed external to the TDS/TDM matrix to satisfy interface requirements. Using present techniques this should be a fairly straightforward procedure for integral submultiples of 32 kb/s. However, the handling of $75 \times 2^m$ b/s signals by a matrix switching 32 kb/s channels is not accomplished as easily.

Note that the maximum rate in the $75 \times 2^m$ b/s family of speeds is 9.6 kb/s. It is possible to accommodate 9.6 kb/s inputs on the 32 kb/s TDS/TDM matrix lines by using signal processing circuits to assure synchronism between the matrix line and the 9.6 kb/s user input. For example, Figure 32 illustrates the timing for one such scheme. Note that ten 32 kb/s pulses form a frame (Waveform A) which is precisely the same duration as three 9.6 kb/s pulses (Waveform B). The 9.6 kb/s subscriber line can be buffered at the switch input to synchronize the 32 kb/s and 9.6 kb/s frames and then retimed as shown for Waveform C. Note that the result is to compress each of the three 9.6 kb/s pulses to the width of a 32 kb/s pulse and place them in time slots 1, 4, and 7 of the 32 kb/s frame. Thus, Waveform C contains the information from the 9.6 kb/s line but is compatible with the 32 kb/s rate required at the switch. Assuming synchronism between the 9.6 kb/s and 32 kb/s frames can be achieved at the output of the destination node, Waveform C could be sampled only at the first, fourth, and seventh bit of each frame. These bits could then be buffered and reclocked at a 9.6 kb/s rate and transmitted to the subscriber.

Synchronism must be achieved, however, between the 32 kb/s and 9.6 kb/s frames at the destination node. For local calls this is no problem since the frames are already synchronous. This is not the case at foreign nodes. However, since only three of the 10 time slots per frame contain data, the remaining slots could be used to supply inband synchronization information. A Barker Code could be inserted into the time slots of each frame to uniquely identify a specific time slot. For example, a 1, 1, 0 sequence inserted into slots 8, 9, and 10 respectively yields sufficient synchronization information provided that all other unused slots are set to zero. Five- and seven-bit Barker Codes may also be used for this application.

The penalty one pays for such a design is in the inefficient utilization of the data throughput capacity of the switch, especially for rates well below 9600 b/s. Whenever possible, all signals with a common source and destination and with rates below 9600 b/s should be multiplexed together to form a common channel. Accomplishing this is a function of the switch trunking and multiplexing plan based on actual traffic requirements.

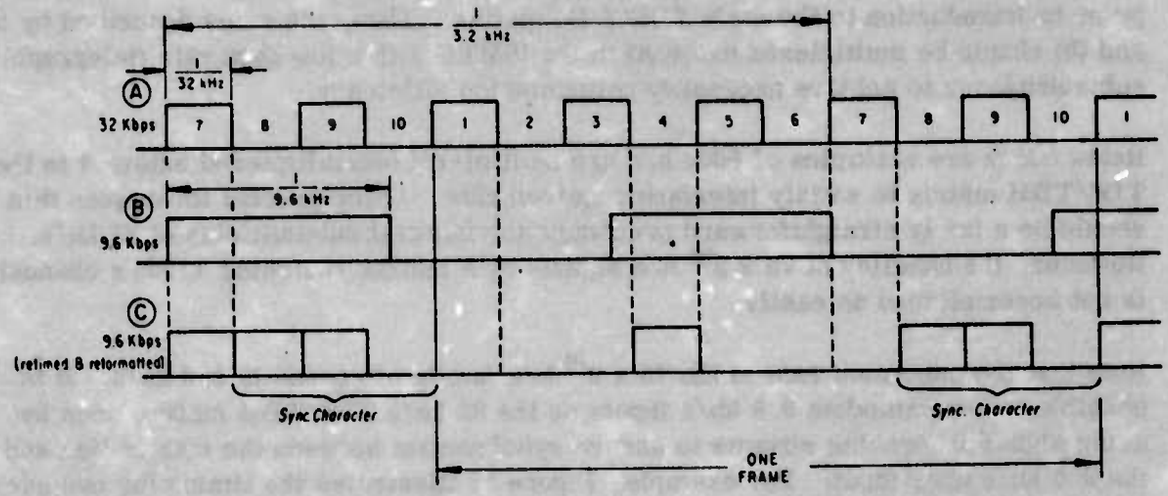



Figure 32. Conversion of 9.6 kb/s Signals to 32 kb/s Format

An alternate approach to switching $75 \times 2^m$ signal rates might be to have a separate matrix especially dedicated to handling such signals. Within this matrix, provision might be made for switching subchannels in order to increase data throughput when dealing with low rates. Such an approach would only be cost effective if the number of $75 \times 2^m$ b/s channels serviced by the ISMTC node was a substantial proportion of the total traffic load.

## 3.4 CONCLUSIONS

Time division switching and time division multiplexing should both be performed in an integrated time division matrix.

The multiplexing scheme for the integrated switch/multiplex/technical control is based on a bit-by-bit multiplexing of bit streams derived from CVSD subsets generating 32 kb/s per line. Groups are formed from the basic 32 kb/s line rate by a bit interleaving process.

Bit-by-bit multiplexing has an advantage in the tactical network over character multiplexing since it provides a "transparent" transmission system. Characters have no real meaning within the Air Force tactical network since there is no standard character format requirement specified for the terminals. While character multiplexing and character switching offer a means of reducing highway speed, the highway speed as configured for the ISMTC does not present a problem. Highway speeds of 1.92 Mb/s (60 lines x 32 kb/s/line) are planned which are well within the capability of bipolar logic anticipated for use in the integrated time division switch/multiplex.

It is probable that the AF tactical system will be required to serve low speed users in addition to the 32 kb/s CVSD channels and high speed data users. Distributions of users, network configuration, and operating doctrine will dictate the method of accommodating low speed users in a manner which will be cost effective for the overall system.

The multiplex system design approach discussed in this section has little impact on the design of the technical control signaling and common control schemes. It should be noted, however, that transmission equipment carrying greater than 60 channels require external multiplex equipment. In addition, subscriber loops must be multiplexed into groups compatible with the matrix input/output groups. This function could be performed in the line formatter.

## 4.0 TECHNICAL CONTROL

Technical control encompasses the coordination among, and operational control over, associated facilities of telecommunications systems. The prime purpose of technical control is to provide the broad degree of system flexibility essential for maximum and consistent effective utilization of available communications resources. This requires the capability to selectively use various combinations of available transmitters, receivers, terminal equipment, frequencies, and propagation paths. The decision process required to implement this capability is dependent upon many factors, foremost of which is the current operational status of each station, or node, in the network with respect to both equipment and traffic. Based on the knowledge of the current status of each station in the network, effective decisions can be made at various levels within the overall technical control structure. In our analyses, it is assumed that the overall technical control structure is hierarchal in nature and is consistent with the preliminary TRI-TAC concept for Tactical Communications Control Facilities (TCCF). In this concept, the TCCF is composed of four distinct elements:

- System Planning and Engineering
- System Control
- Node Control
- Equipment Support

Figure 33 illustrates the hierarchal structure of the TCCF concept including the functional flow of information between the TCCF elements. With reference to Figure 33, it should be noted that the links between the various TCCF elements are information links, and not necessarily the communications links required to support transfer of the information. Before describing the types of information required to be passed between TCCF elements, a brief description of the major functions of each element is presented below.

1. System Planning and Engineering - The major functions of the System Planning and Engineering (SP&E) element include:

   a. Overall network planning including trunk sizing and routing.

   b. Analysis and selection of required equipment and radio frequencies.

   c. Development of implementation plans.

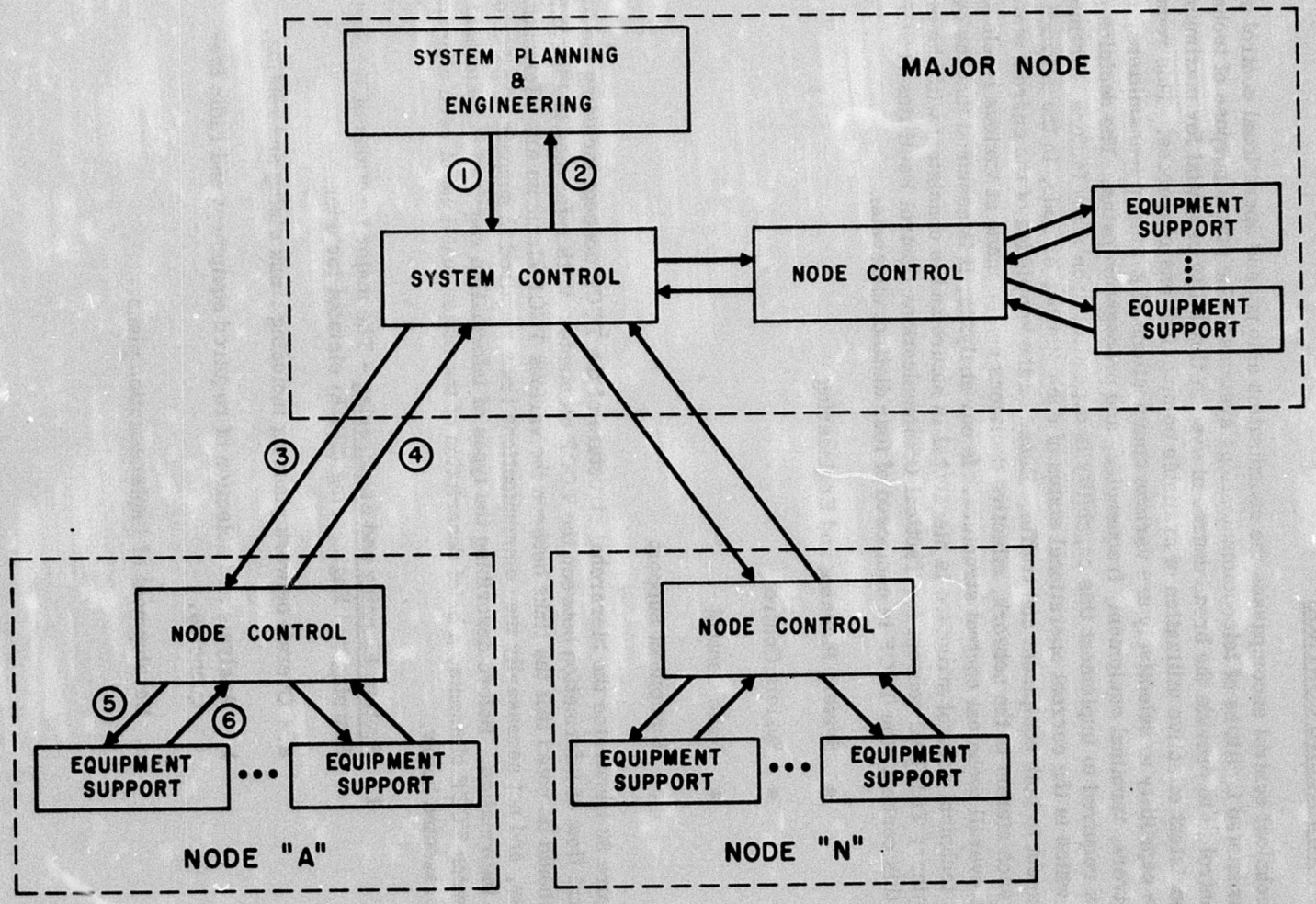



Figure 23. Hierarchal Structure of TCCF Concept

In our concept, in order to provide these functions the SP&E element must develop and maintain a large data base. The data base must contain up-to-date information related to equipment inventories, available radio frequencies, geographic location of nodes, current network configuration (after system deployment), etc. In addition, the SP&E element must have the capability to manipulate the data base in order to arrive at optimum solutions to overall network problems, i.e., processor assistance is required to support the SP&E element.

2. System Control - The prime function of System Control (SC) is to provide real-time management and control of all communications resources within the communications network. In this capacity, SC must have the capability to continuously optimize performance and service throughout the system during both stressed and non-stressed conditions; that is, the SC element must be capable of evaluating overall network performance with respect to traffic handling capacity, directing changes in circuit routings based on this evaluation, and instituting other traffic control techniques as required to maintain optimum communications throughout the system. In addition, SC must have the capability to isolate faults related to particular nodes in the system. This latter capability must be based on the analysis of equipment and traffic status reports received from the nodes of the system. To effectively provide all of the required SC capabilities, the SC element must be provided with processor assistance and the necessary software to support the SC function.

3. Node Control - The major function of the Node Control (NC) element is to provide real-time technical control at each switching node within the communications network. This element is responsible for management and operational control of all communications equipment associated with the node, including equipment at repeater sites for which the NC element has been assigned responsibility. To provide effective real-time technical control over the node, the NC element must have the capability to automatically:

   - Monitor equipment alarms and signal quality.
   - Isolate "in-station" faults.
   - Restore circuits which have failed.
   - Generate reports and records related to both equipment and traffic status.

4. Equipment Support - The Equipment Support (ES) element provides for the installation, operation, and maintenance of communications equipment at the node. In general, an ES element will be associated with each unit of communications equipment, including the switch, at the node.

5. TCCF Integration - This study is directed towards the analysis of the feasibility of incorporating the functions required of the Node Control element into the common processor of an Integrated Switch/Multiplex/Technical Control Facility. The processors required for the System Control and the System Planning and Engineering elements will require software and operating characteristics unique to their specific functions. Furthermore, since one SC and one SP&E element can handle more than one node, it is not practical to provide their required capabilities into the ISMTC processor at each node of the network.

With reference to Figure 33, the type of information required on the links between the various TCCF elements is presented below.

Link 1 - SP&E to SC

- Node locations including repeater sites
- Node-pair frequency assignments
- Network connectivity
- Routing tables
- Switch sizes
- Data base updates

Link 2 - SC to SP&E

- Requests for additional trunks and/or switches
- Data base updates
- Status of nodal equipment and traffic
- Network traffic status summaries

Link 3 - SC to NC

- Frequency assignments
- Routing tables
- Fault isolation reports
- Fault reports

Link 4 - NC to SC

- Traffic status reports
- Equipment status reports
- Fault reports
- Sensor (monitor point) information (for system control fault isolation on a node-pair basis)

Link 5 - NC to ES

- Frequency assignments
- Fault reports

Link 6 - ES to NC

- Equipment status
- Fault cleared report
- Sensor and alarm information

Section 4.1 presents the parameters which are pertinent to providing the technical control functions for the Node Control element of a TCCF. Basically, there are four major functions associated with technical control at nodes of a communications system. They are:

- Circuit quality monitoring and testing
- Fault isolation
- Alternate routing
- Reporting and recordkeeping

## 4.1 QUALITY MONITORING AND TESTING

The major purpose of quality monitoring and testing is to provide indications of network and station equipment degradation prior to complete failure. This function, monitoring and testing, also provides the basis for the initiation of fault isolation and circuit restoral procedures. Quality monitoring of both the transmission and switch/multiplex subsystems is a definite requirement for the ISMTC.

In planning for the ISMTC and later in implementing the overall communication system, the problems related to monitoring at key locations must consider:

- What to monitor (selection of key parameters)
- Where to monitor (selection of key points)
- How to monitor (selection of monitor equipment and techniques)
- How often to monitor (measuring and reporting frequency)
- Actions to be taken in response to sensing of degradations.

The discussion which follows presents some of the above considerations.

### 4.1.1 Monitor Points and Parameters

In the tactical environment of the 1980s the trunks between switching centers will be provided by various types of transmission equipment, including communication satellites, transponders aboard remotely piloted vehicles (RPVs), tropospheric scatter radio, line-of-sight radio, and cable transmission systems.

A block diagram of a typical transmit/receive station identifying possible equipment and signal monitoring points is shown on Figure 34. Typical equipment to be monitored by the signal quality monitor function include all equipment through which the signals pass and those support equipments and/or subsystems which, if malfunctioning, would affect system performance. Equipments and subsystems to be monitored include:

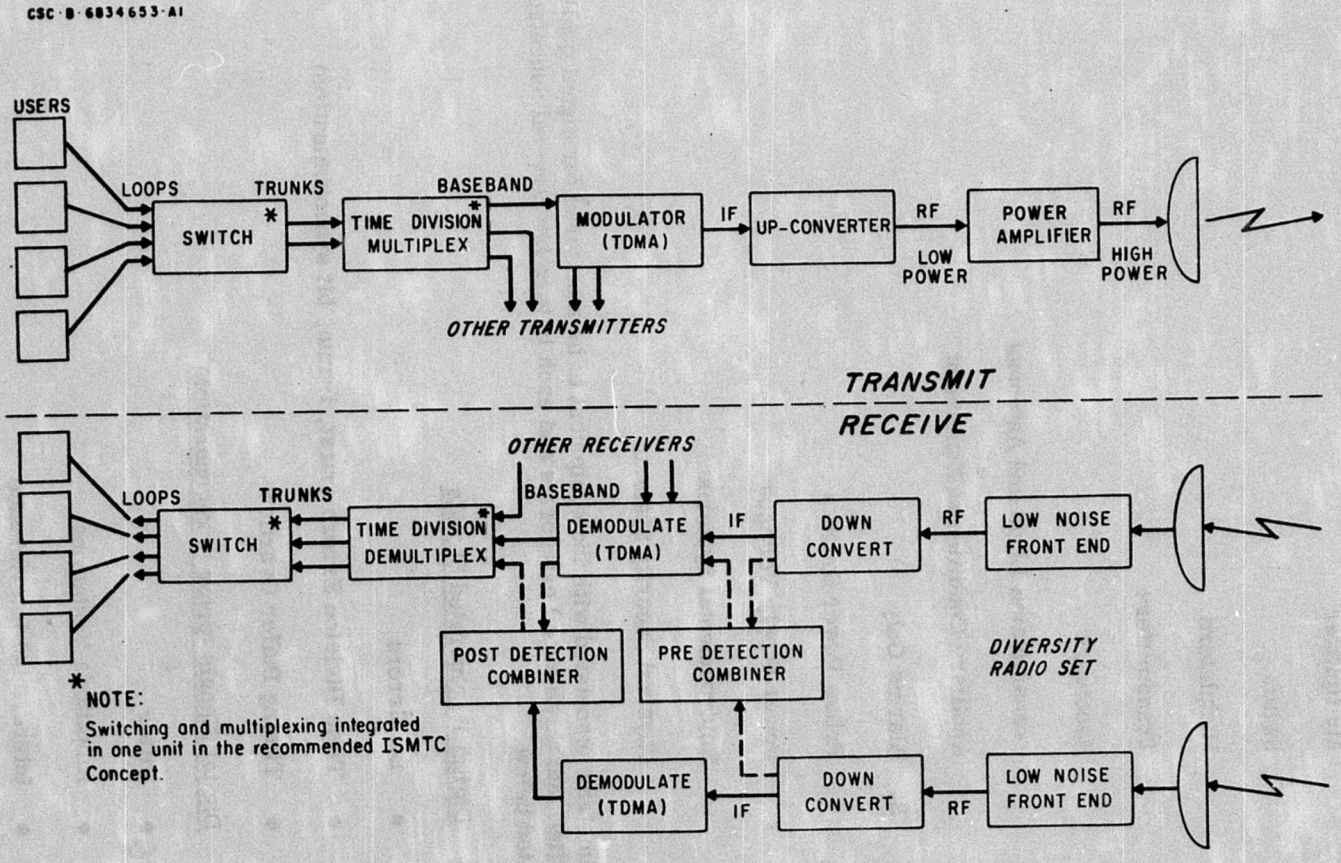



Figure 34. Typical Monitoring Point Block Diagram

1. Signal Quality and Alarms

   Multiplexer

   Switch

   Modulators

   Transmitters

   Receivers

   Transmission Lines and Antennas

   Ancillary Conditioning Equipment

2. Alarms Only

   Prime Power Sources

   Power Supply Voltages

   Environmental Systems

   Physical Security Systems

The parameters associated with the equipment to be monitored for signal quality can be classified into three broad categories and each in turn into several subcategories as indicated below.

Digital Regenerated Signals

- Bit Errors
- Time Division Errors (burst, frame, bit synchronization)
- Timing Buffer Overflow

Digital Signals (prior to regeneration)

- Jitter
- Amplitude Variations
- Intersymbol Interference

Analog Parameters

- Transmit
  - Baseband
  - Intermediate Frequency
  - Local Oscillator
  - Low Power RF
  - High Power RF
  - Reflected RF
- Receive
  - Receiver Noise Figure[5]
  - Received Signal Level[5]
  - Local Oscillator[5]
  - Baseband[5]
  - Combined Baseband

A discussion of the nature of the signal parameters to be monitored is presented below.

4.1.1.1 Monitoring Regenerated Digital Signals

Various portions of the system including the switching, multiplexing, and delay buffering equipment, deal with fully digital signals which have been locally re-timed and have locally preset amplitude (i.e., regenerated digital signals). Monitoring at these points in the system is needed, especially for failure recognition, but may not provide any indication of approaching failure until the degradations become severe enough to cause binary errors. This occurs because of the sharp threshold in the relationship between error rates and signal-to-noise ratio for gaussian additive noise in a non-fading channel. For other types of noise and channel disturbances, or for a fading

[5]For each diversity branch if diversity is used.

signal, the threshold is not as abrupt and error rate may possibly be used to indicate channel degradation.

With respect to the monitoring of digital signals, the following parameters can be sensed.

- Bit Errors - Binary errors and error patterns can be measured between input and output of a switch or multiplex equipment, or node to node by cooperative action between two contiguous nodes.

- Time Division Errors - The effect of small errors in timing (i.e., digital distortion) tends to appear in the form of bit errors in one or more channels. Larger errors (greater than one half of a highway bit time) will result in incorrect identification of time slots, so that all the channels of a given TDM highway will be slipped and directed to incorrect users (i.e., loss of frame synchronization).

- Timing Buffer Overflow - Clock drift between two nodes, or large unexpected shifts in time delay, can cause buffer overflow or underflow in the circuits provided for bringing separately received channels into common frame timing (for multiplex and switching).

Monitoring for digital errors may be accomplished on circuits which are either idle or are in-use.

4.1.1.1.1 Idle Circuits

If a predetermined known pattern is transmitted on all idle channels (the digital counterpart of the idle channel tone), it can be monitored and its presence used to indicate circuit continuity. All circuits can be tested rather rapidly by sequential scanning. The sampling time for each channel can be made long enough to monitor performance but not long enough to measure bit error rate. When errors are detected the circuit should be remeasured and, if confirmed, corrective action taken.

Somewhat less frequently the bit error rate of idle channels should be tested and the results recorded. Degradation in error rate versus time provides a measure of circuit degradation.

When errors are measured on a circuit the error pattern and/or statistics can be analyzed by the processor for diagnostic purposes. If the errors occur in bursts or are random, or if they occur one or two at a time or in larger groups, analysis of the patterns could provide information for fault isolation. Also, by inserting a test pattern generator at the transmitter, the test pattern may be varied to stress different system parameters. For example, by varying the number of "1s" and "0s" the clock recovery circuits may be tested.

#### 4.1.1.1.2 In-Use Circuits

When a circuit is in use its performance may be monitored by making use of any known redundant information associated with the digital signal. This technique is referred to as Code Violation Monitoring. Several examples illustrating this approach are given below:

1. Forbidden Patterns - Based on existing analysis and documentation, it is likely that digitized voice will be handled by a CVSD process. In most CVSD encoders/decoders, certain forbidden characters occur inherent to the delta modulation scheme. For example, the typical CVSD process described in the TRI-TAC specifications excludes the possibility of four consecutive zeros. If at the receive switch end a simple modulo-type detector were used, an error could be indicated every time four consecutive zeros were detected. A determination would have to be made concerning how soon an alarm should be sent; that is, one may not wish to send an alarm based on the first error detected. One may wish to average over a certain time period and extrapolate a line error rate and, based on a line error rate threshold preset in the processor, send an alarm.

2. Frame Pulse Monitor - In some digital systems the framing pulse(s) is the only unique signal which is always transmitted. This signal may be monitored at the receiving node and also telemetered to the transmitting node to indicate failure. A frame monitor can also be used to indicate loss of crypto synchronization.

3. Other Code Violation Monitors - Other examples are: on the Bell T-1 only 14 consecutive "0s" are permitted; T-2 is limited to six consecutive "0s"; and the T-4 is limited to two consecutive "0s". Any variation from this would indicate fauity operation. If forward error correction, ARQ, or parity is used, relatively simple sensors and algorithms may be devised to monitor circuit performance.

#### 4.1.1.1.3 Duplicate Transmission

Another method of circuit testing is to transmit some (or all) of the bits of the message in an order wire or idle channel and to cross correlate the received bit streams to test for bit errors.

### 4.1.1.2 Monitoring of Digital Signals (Prior to Regeneration)

Signals in digital format, after transmission over a noisy or disturbed path, may exhibit perturbations such as intersymbol interference, noise, timing jitter, and

timing drift. These disturbances can be sensed as a measure of signal degradation even before they are large enough to cause measurable error rates, at a subsequent fully-digital point in the system.

The following parameters can be sensed.

- Jitter
- Amplitude Uncertainties
- Intersymbol Interference

Multipath or filter dispersion can cause intersymbol interference, which will in general appear as a combination of jitter and amplitude fluctuation. In these cases the perturbations will be found to correlate with the bit pattern of earlier and later bits of the data stream.

#### 4.1.1.3 Monitoring of Analog Parameters

Although the systems considered are wholly digital, the problem of localizing faults and degradations will involve making analog measurements of the degradation in radio signals, wire lines, etc.

For this purpose, conventional analog measurements (such as signal power, noise, interference, VSWR, fading, multipath, delay distortion, slot noise, etc.) will usually make it possible to establish whether a signal is being degraded at the source (transmitter), in the radio or wire-line path, or in the receiving system. This kind of fault localization is needed to determine which site needs maintenance, or whether the problem is propagation disturbances between sites.

Before the analog monitoring function can be effectively automated some means must be provided to make the required measurements and to transmit the results to the common communications processor at the ISMTC facility. For the 1980 time frame, transmission equipment should be designed to provide the required measurement capability, including the means to communicate the resulting data to the ISMTC. The latter will require analog to digital conversion of the measurement and the ability to insert the data into an order wire between the transmission facility and the local and remote ISMTC facilities.

### 4.1.2 Computer Processor Implications

Monitoring of digital parameters is basic and provides knowledge of channel failure. This is used for indicating channel status, for control of alternate routing--either directly by the processor (if automatic alternate routing is desired and if a standby

routing choice has been made) or by manual intervention--and to initiate various messages to echelons concerned with traffic and systems management and with maintenance.

Non-regenerated digital signals will have to be monitored to provide indications of system and circuit degradation prior to failure and to ensure detection of channel failure (where encryption would otherwise prevent observing digital errors) and to assist in fault localization.

It is expected that monitoring of analog parameters will also be required, in order to distinguish between degradations at the sending end, in the path, and at the receiving end of a hop (for guiding maintenance and alternate routing). Further localization of faults to subsystems will be useful for maintenance purposes.

A major consideration in planning to integrate technical control functions into the circuit switch at each node will be the added burden on the processor controlling the switch.

A significant impact of integrating the equipment support function into the switch processor appears to be in digital monitoring of switch and multiplex failures. Very fast reaction is needed here, since a switch or multiplex failure, or an error in framing, can result in failure of a very large number of channels. To provide quick reaction to failure and rapid fault localization (for automatic replacement of a switch module), the technical control function will require rapid access to the computer, an infrequent but sizable peak computing burden, and will probably also use a significant amount of external special-purpose monitoring logic. A preliminary examination of this aspect of the technical control monitoring has been undertaken (see paragraph 4.5.1.1).

The remote monitoring of digital and analog parameters at key points between each pair of switching nodes is expected to use special-purpose hardware in order to minimize the channel capacity used for signal quality status reporting, which could otherwise become a significant traffic burden. Thus, the main impact on the ISMTC processor at a given node is expected to lie in the extra program capacity used for fault localizing, and in originating appropriate failure reports. The speed of response needed for these functions will be relatively low (several seconds can be used) so that extra computing speed will not be needed.

## 4.2 FAULT ISOLATION

One of the most complex processes in present day technical control operations is that of fault isolation. The complex pattern of actions involved in the interval between failure and restoral encompasses monitoring, testing, and coordination. The ability to perform the fault isolation process is, therefore, very dependent upon the skill level and experience of individual technical controllers. The problem is one of providing the technical controller with the tools that will help him perform this complex process more effectively.

There are two basic approaches that should be considered depending on the type of fault isolation desired. In-station fault isolation provides for the isolation of faults within the node and is a station-oriented function. System fault isolation provides for identification of faults as in-station or out-of-station and, if out-of-station, localization of the trouble to a specific station or stations in the transmission path.

The degree of fault isolation will be dependent upon two major factors:

- Hardware - The type, number and configuration of the signal and equipment sensors used for recognition of degradation and failures both in the transmission and switch/multiplex subsystems.

- Software - The designed capability of the common communications processor whereby the degradation and failure indications are collected, compared, and correlated in order to validate and isolate the problem areas.

Considerations related to hardware are presented below.

### 4.2.1 Hardware Considerations

The basic technique applicable to the implementation of the fault isolation function of technical control is that of comparison of measurements; that is, to isolate faults in a system, comparisons must be made with respect to the quality of input and output signals of key elements within the overall system. If, for instance, the quality of an input signal to one of the key elements is within its acceptable range, and the quality of the associated output signal is out of tolerance, the fault in the system can be isolated to that element or the following element. The ambiguity as to which is the faulty element occurs if the input stage to the following element has malfunctioned (e.g., short circuited). In this case an additional diagnostic is required to enable isolation to one element.

As noted previously, monitoring of both digital and analog signals will be required for optimum fault isolation capability. This section is directed toward a discussion of hardware considerations related to the analog monitoring and fault isolation functions, i.e., monitoring and fault isolation of the transmission system.

The problem of localizing transmission faults and degradations will require analog measurements of key parameters of the transmission subsystem. Before the analog monitoring and fault isolation functions can be effectively automated, some means must be provided to make the required measurements and to transmit the results to the common communications processor system at the ISMTC facility for correlation. There are several basic concepts applicable to providing for this capability, all of which require special purpose hardware for their implementation. The complexity of the hardware required will be dependent upon the type of terminal, the number of monitor points, and the type of orderwire available to transmit the monitor information to the ISMTC.

To illustrate the various concepts which may be used to implement the fault isolation function, radio relay terminals will be used for the purpose of discussion. The concepts described could be readily extended and applied to other types of terminals.

There are two types of radio relay repeaters that must be considered, baseband repeaters and IF (or RF) repeaters. The type of repeater used will affect the type of channel required to transmit the monitor point information back to the ISMTC. For instance, with baseband repeaters, the monitor point information could be inserted and transmitted on the 32 kb/s digital orderwire channel of a trunk group.

With IF (or RF) repeaters, the monitor information cannot be inserted in one of the trunk group time slots without special provisions being made for demodulation of the baseband signal. Therefore, other means must be used to transmit fault detection and quality monitor information to the ISMTC. The following paragraphs describe techniques which are applicable to the implementation of the fault isolation function for both types of repeater terminals. The fault isolation techniques described are based on monitoring a minimum number of points but can be extended to encompass many more points. In actual practice it may be desirable to monitor a larger number of key points so that the degree of fault isolation capability could be extended. The actual number of monitor points that will be incorporated into the transmission equipment supporting the ISMTC during the 1980 time frame will be dependent upon the specific design of such equipment. It is strongly recommended that the development of specifications for the ISMTC and network-wide transmission equipment be done on an overall system-oriented basis in order to obtain maximum interoperability; that is, there should be close coordination and liaison between those responsible for the development of transmission, switching, multiplexing, technical control, and end instrument subsystems of the overall tactical communications equipment.

4.2.1.1 Baseband Repeaters

The typical complement and configuration of major equipment at a baseband repeater terminal for one direction of transmission is illustrated in Figure 35. As a minimum, the inputs and outputs of each functional element shown in Figure 35 should be monitored for signal quality and/or level.

The overall process of monitoring and fault isolation, as applied to the transmission system supporting an ISMTC, consists of several steps:

1. Analog signal detection and measurement
2. Analog-to-digital conversion
3. Message formatting
4. Message transmission to the ISMTC

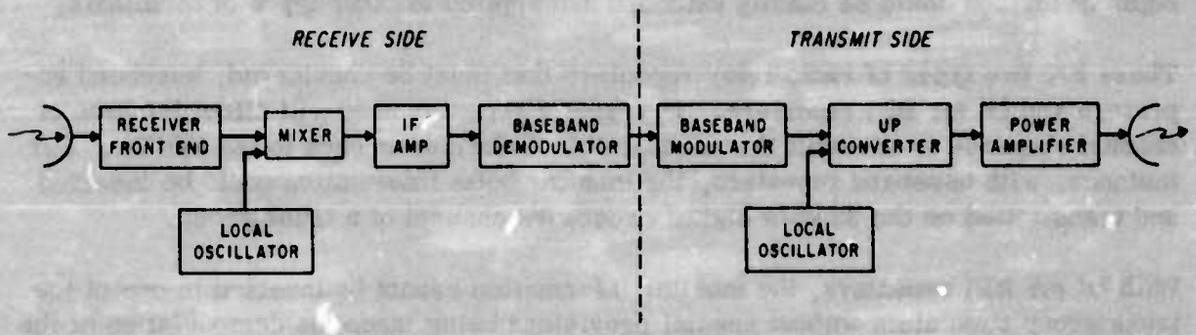



Figure 35. Typical Configuration of Equipment at Baseband Repeater Terminals

4.2.1.1.1 Signal Detection and Measurement

Signal detection and measurement will require sensors capable of detecting and measuring the specific parameters to be monitored. It is recommended that consideration be given to the incorporation of these sensors into the transmission equipment to be used during the 1980 time frame. Consideration should also be given to optimizing the number of key points to monitor through detailed tradeoff analyses during the specification preparation phase of the transmission equipment design.

4.2.1.1.2 Analog-to-Digital Conversion

Analog-to-digital (A/D) conversion will be required to convert analog measurement signals into digital signals in order to provide for proper message input to the digital ISMTC processor. There are two basic methods which may be used to provide for A/D conversion. One method incorporates an A/D converter as part of the monitor sensor equipment at each monitor point, i.e., one A/D converter per monitor point. The second method involves the use of a single A/D converter fed by a scanning device which sequentially connects each analog monitor point in the system to the A/D converter. Figures 36 and 37 illustrate the multi- and single-A/D converter approaches. The figures also show the equipment required to format and transmit the monitor point information to the ISMTC processor.

4.2.1.1.3 Message Formatting

Message formatting is required to insert the monitored data into a message for transmission to the ISMTC processor. The length and format of the message is dependent upon:

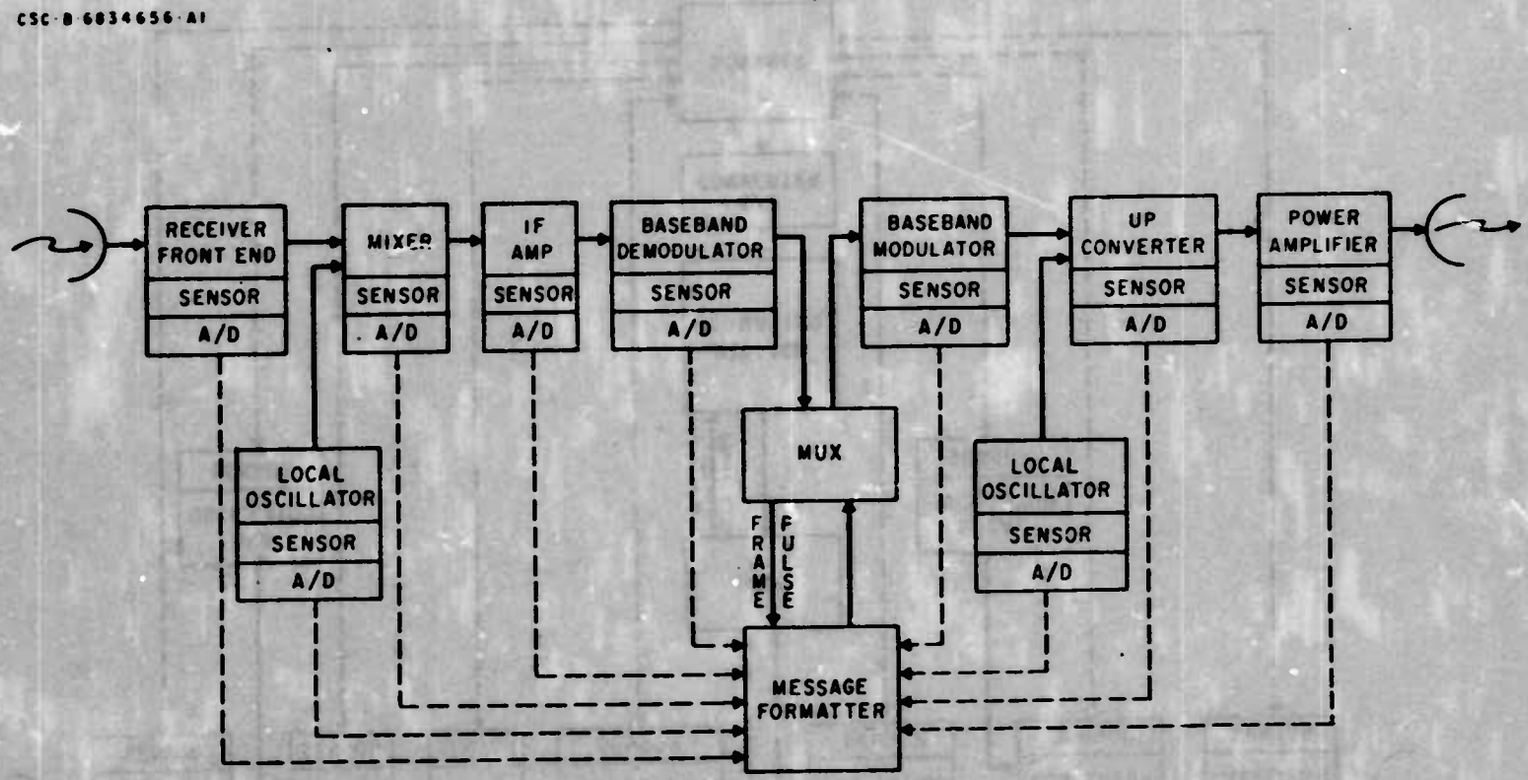



**Figure 36. Multi-A/D Converter Approach to Monitoring at Baseband Repeater Terminals**

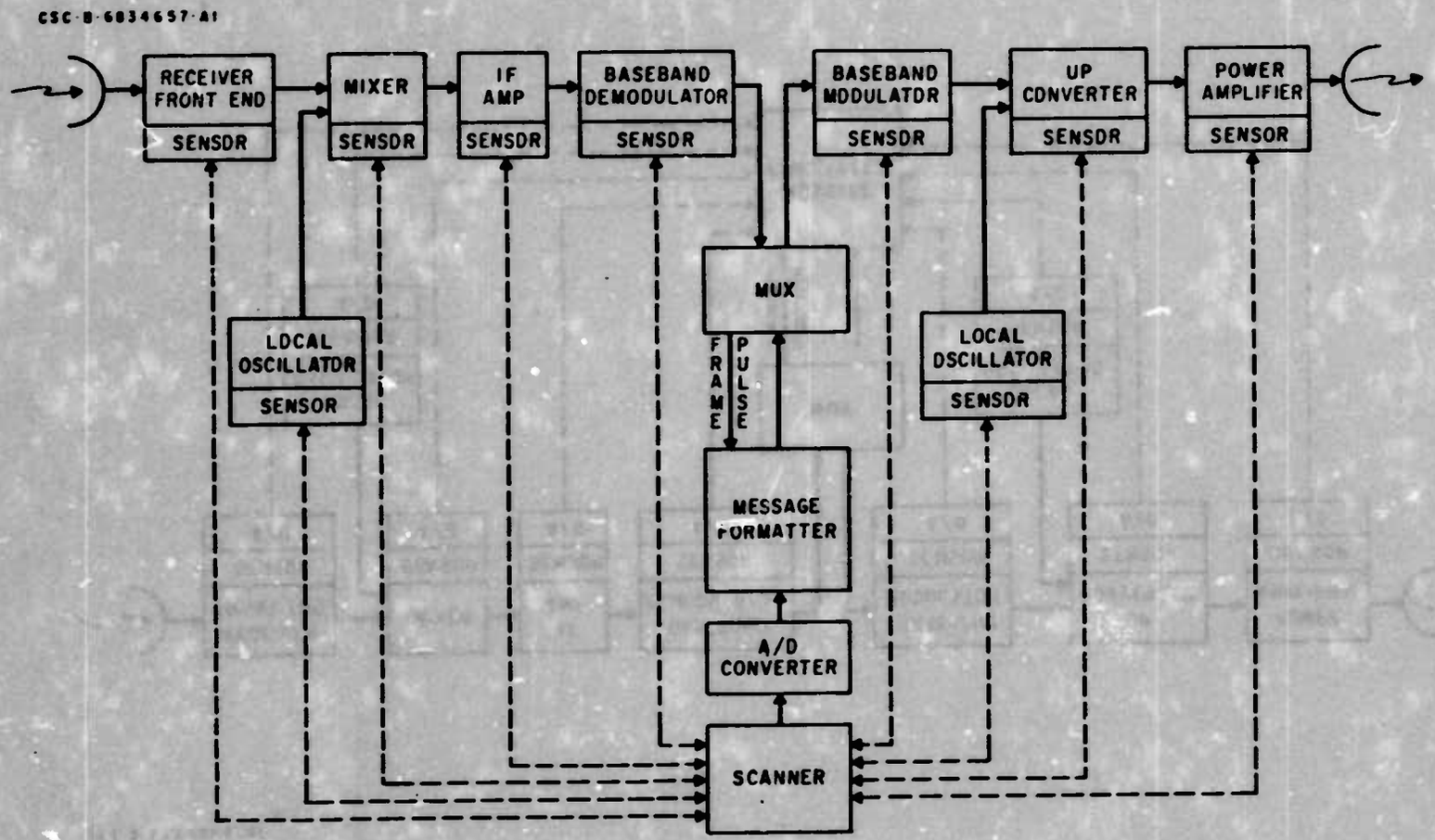



**Figure 37. Single-A/D Converter Approach to Monitoring at Baseband Repeater Terminals**

1. The number of monitor points.

2. The length of the bit sequence used to code the monitor point data.

3. The type of reporting used, e.g., continuous, periodic, or aperiodic reports.

The length of the bit sequence used to code the data will be dependent upon the number of discrete quantized measurement levels available from the A/D converter. The greater the number of levels, the greater the accuracy of measurement. In a simple three-level (green, amber, and red) monitor and alarm system, only two bits would be required and the A/D converter is a simple four-state device. The two bits could be used to code the signal condition as follows:

- Space-Mark (0-1) Green Condition - Signal level/quality is within acceptable operating tolerances.

- Mark-Space (1-0) - Amber Condition - Signal level/quality has crossed a pre-established threshold causing system degradation. The system is still operable but cannot provide optimum performance.

- Mark-Mark (1-1) - Red Condition - Signal level/quality has deteriorated to the point where the system becomes inoperable.

The dibit Space-Space (0-0) would not be required. In order to minimize false alarms due to errors caused by the transmission system, it is desirable to transmit the monitor point condition more than once, possibly up to four times, thus making an eight-bit byte for transmission to the communications processor.

In a more sophisticated system where trending of system performance is desired, the measurements at the monitor points would be quantized to many more than two levels. The actual number of levels will be dependent upon the measurement accuracy required to develop trends in system performance ($2^N$ discrete measurement levels require N bits for transmission).

An additional factor affecting the length and format of monitor point sensor messages is the method of reporting. The three basic types of reporting that could be used to transmit sensor data back to the ISMTC processor are:

- Continuous Reporting - With this type of reporting the condition at each monitor point in the station is continuously transmitted in sequence to the ISMTC processor. Each monitor point is allocated a specific time period within the full status condition message. Figure 38 illustrates the basic format of the continuous report message

not including overhead characters such as framing, start-of-message (SOM), end-of-message (EOM), error control, etc. It should be noted that every report contains the status of all monitor points in the station. Also, by assigning a time period to each monitor point there is no need to identify the monitor point by a discrete address.

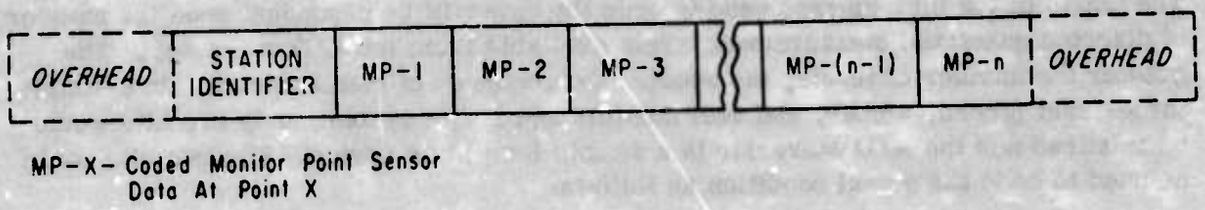



Figure 38. Continuous Report Format for Monitor Point Sensor Data

- Periodic Reporting - This type of reporting is similar to continuous reporting with the exception that the status condition message is transmitted on a periodic basis (e.g., once a minute) instead of continuously.

- Aperiodic Reporting - This type of reporting would be used for "exception" reporting of fault conditions; that is, monitor point sensor condition message would not be generated except when a change of condition exists. The format for an aperiodic report of this type is illustrated in Figure 39. It should be noted that this type of reporting requires the address (identity) of the monitor point at which the faulty condition exists. Aperiodic reporting results in minimum loading of the ISMTC processor, whereas in comparison continuous reporting results in a relatively high loading.


Figure 39. Aperiodic Report Format for Monitor Point Condition

4.2.1.1.4 Message Transmission

Once the monitor point message is formatted, it must be transmitted to the processor of the ISMTC for correlation. At baseband repeater stations and at an ISMTC node, the message is inserted directly into the digital orderwire channel of a trunk group. With reference to Figures 36 and 37, the message formatter receives frame pulses from the demodulated trunk group for synchronization and therefore is able to locate the time slot assigned for transmission of remote status information. At the proper time, the message formatter outputs the message to the multiplexer where the message is inserted into the trunk group.

4.2.1.1.5 Correlation of Monitor Point Data

Correlation, or comparison, of monitor point sensor data is basic to the process of fault isolation. The correlation of monitor point status is accomplished by setting up tables for storage of monitor point sensor data for each station under control of the local ISMTC processor. For each station, locations in the tables are permanently assigned to specific monitor points in the stations. The tables are updated periodically depending upon the type of reporting technique selected for reporting the data. Through comparison of related input/output conditions of the points being monitored, faults could be isolated.

In a three-level monitor point alarm system, the correlation of data for fault isolation is usually relatively straightforward. For instance, if the received signal level (RSL) at a repeater station is reported to be in the "amber" condition, and the power input to the antenna of the corresponding transmitter at the node station is reported to be in the "green" condition, the fault could be isolated to the antenna and feed system, assuming there has been no signal perturbations caused by the propagation media.

In a system where trending of system performance is required, correlation of monitor sensor data is accomplished in the same basic manner as described above for a three-level monitor point alarm system. However, instead of making comparisons of "green", "amber" and "red" conditions, comparisons are made between reported measured values of signal level/quality and preestablished values for each monitor point. The processor keeps track of the difference between the two values (measured and optimum) and develops trends with respect to system performance. Also, if the difference between the two values exceeds a predetermined value, a trouble report warning of system degradation or potential system failure is generated.

4.2.1.2 IF Repeaters

The typical complement and configuration of major equipment at an IF repeater terminal is illustrated in Figure 40. The overall process of monitoring and fault isolation at such a terminal is very similar to that described above in paragraph 4.2.1.1,

Baseband Repeaters. The only difference is the technique used for message transmission. Sensors for signal detection and measurement, A/D converters, message formatter, and the function of correlation of monitor point sensor data is the same as that described for the baseband repeater case.

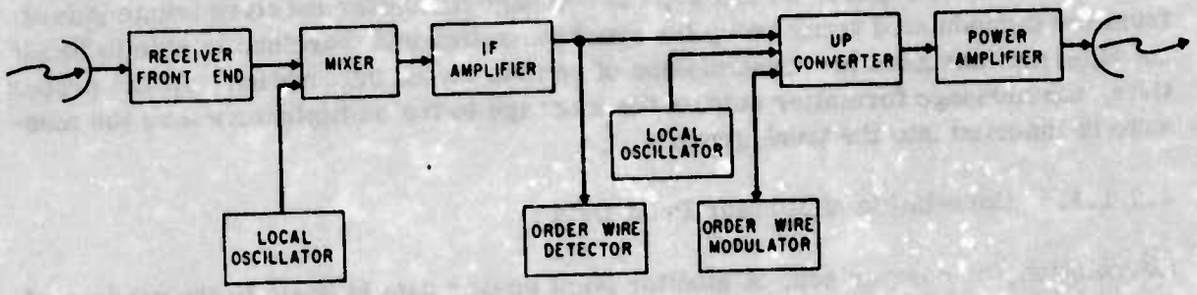



Figure 40. Typical Configuration of Equipment at IF Repeater Terminals

Figures 41 and 42 illustrate the equipment required to implement the monitoring function at an IF repeater terminal for the multi- and single-A/D converter approaches. Since the digital baseband is not available, access to the digital orderwire of the trunk group cannot be obtained directly. Therefore, the orderwire channel must be provided by some other means and a number of techniques are available and are commonly used in existing transmission systems. Among the techniques available are:

1. Use of a special orderwire demodulator and remodulator.
2. Use of a separate orderwire RF carrier.
3. Low level phase modulation of the local oscillator.
4. Use of a different means of transmission for the orderwire.

## 4.3 ALTERNATE ROUTING

Many military networks currently in operation generally perform circuit rearrangement at the technical control position and alternate trunk/line selection at the switching center. This method of operation has evolved from the operational separation of the individual dedicated user networks and the backbone transmission system serving the networks. In most cases, little or no switching was provided and users were served primarily by dedicated lines.

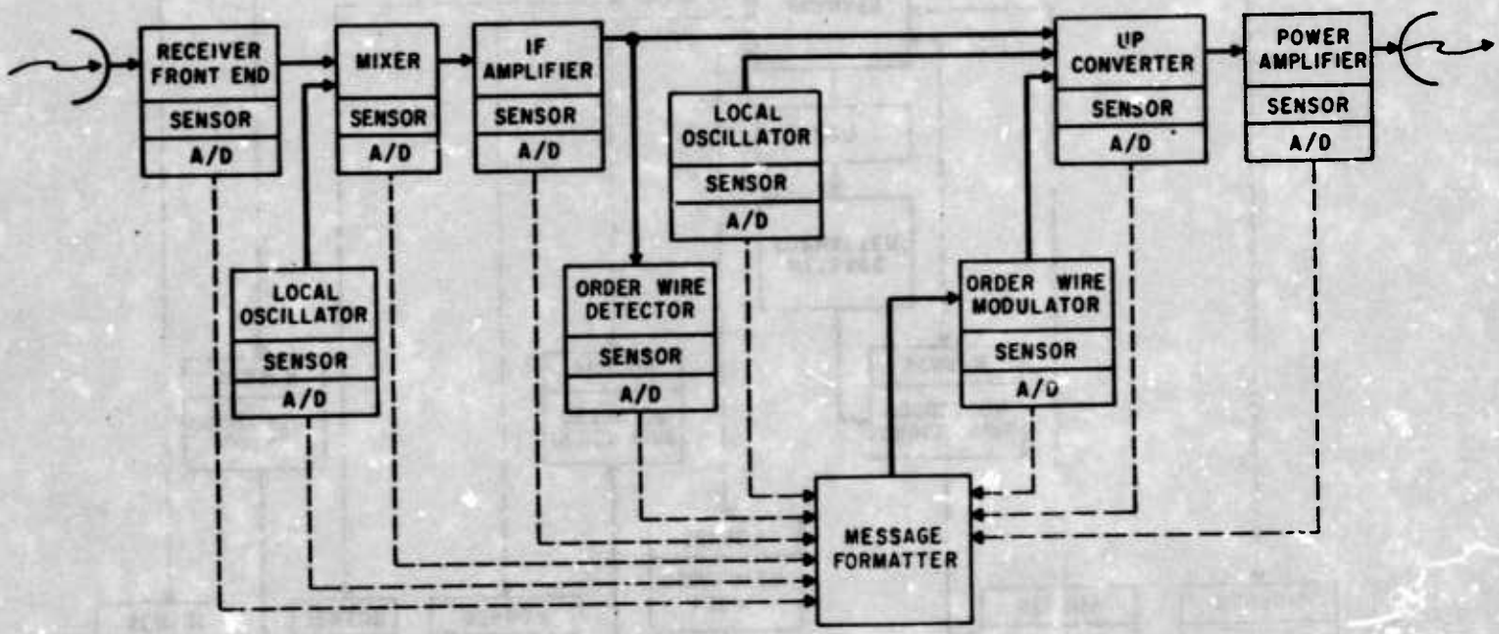



**Figure 41. Multi-A/D Converter Approach to Monitoring at IF Repeater Terminals**

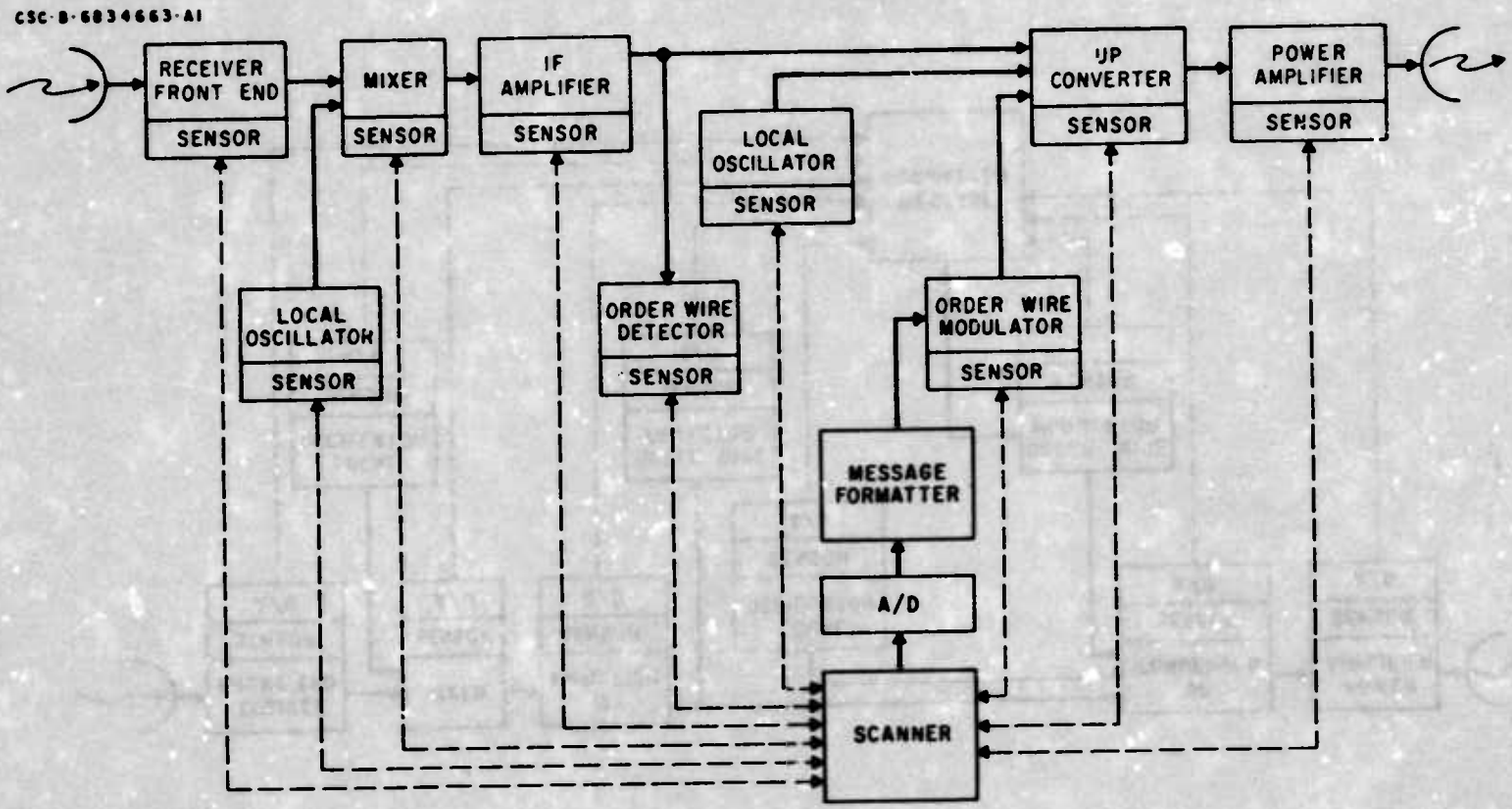



**Figure 42. Single A/D Converter Approach to Monitoring at IF Repeater Terminals**

In this environment a Technical Control facility is required to restore service to users when circuit outages occur since the advantage of alternate trunk selection at the switch is unavailable. The means of providing this circuit restoral is accomplished manually at a technical control patching facility. In this type of operation the technical controller is required to detect the trouble (e.g., circuit outage), locate the fault, determine the users affected, and select the alternate route to restore communications for the affected users.

Recognizing the inherent flexibility, survivability, and cost savings that can be realized by the implementation of common user switching systems, military communications engineers have been implementing switched communication networks to support strategic and tactical communication needs. AUTOVON and AUTODIN are prime examples of the trend towards increasing network survivability and flexibility while taking advantage of the cost savings of a common user network.

In recent years tactical communication planners have also put a great deal of effort into the development of new communication networks to support the tactical environment. It has been determined that the needs of tactical users can be efficiently and economically consolidated into digital switched networks.

Advances in the technology have made it practical to consider integration of switching, multiplexing, and technical control under the operational control of a common processor complex. Many of the technical control functions which are usually accomplished manually and remote from the switch can be done as part of this system. For example, the process of circuit rearrangement can be accomplished by alternate routing schemes which are integrated into the switch processor. This integration comes about by making use of the technical control quality monitoring sensors which are used to determine circuit outages and circuit performance inherent to the technical control function. These sensor outputs can be brought directly into the processor portion of the switch control and used to update adaptive routing tables which will determine the routes selected for newly initiated calls.

In the present method of operation the tech controller basically works independently of the switching center. The tech control function is to determine circuit outages and circuit quality and to provide alternate means of communications--in essence, alternate trunks--in order to reestablish communications when outages occur. Trunk capacity, therefore, is restored to the switch without intervention on the part of the switch. The tech controller has provided an alternate transmission means to serve the purposes of that trunk. In the ISMTC complex, the sensor information would be passed to the processor which also performs the switch control function. The switch's trunk selection mechanism, therefore, would satisfy the normal circuit restoral function that is accomplished by the tech controller.

Means for accomplishing this adaptive routing or circuit restoral in the technical control sense will be discussed below. The selection of the most appropriate method, or the most appropriate route selection algorithm, depends upon the nature of the network; that is, the quantity and distribution of nodes, traffic density and distribution, priority considerations, and survivability constraints are among the factors that must be considered.

### 4.3.1 Routing Procedures

In networks subject to the stresses, complexity, and fluidity of modern tactical warfare, the choice of a routing method is critical. Survivability, efficiency of trunk usage, speed of response, grade of service, and complexity of the nodes are only a few of the major considerations of network design which are directly influenced. In addition, a tactical communication node which integrates the technical functions of circuit rearrangement with the switching function of trunk group assignment and trunk selection provides a ready means to automate this activity.

The need for integration and automation by means of the common processor system at the node derives primarily from two basic considerations:

1. The need for fast recovery of the network after severe damage.
2. The high mobility of individuals, military units, and the communications plant itself.

It appears that while satisfying the prime military requirements for survivability and mobility, an advanced routing system can perhaps compensate for a major fraction of its own cost by permitting more efficient use of the trunking system. Two factors related to an ISMTC for the 1980s contribute to this conclusion:

1. The Air Force tactical network for the 1980s is digital, thereby removing the limitations on the number of links traversed that apply to analog transmissions.
2. The state of the art of digital telecommunications equipment and processors has progressed to a point to which relatively complicated functions involved in automated fault detection and isolation, circuit management and circuit switching can be performed relatively inexpensively and with compact reliable units.

There are many possible approaches to providing a routing system appropriate to the tactical Air Force Network. A few of these are discussed next.

#### 4.3.1.1 Search Routing

Because of its ability to locate users in the network without maintaining large updated directories, and because it can find best routes in a network of changing topology, search routing from an operational viewpoint offers many advantages. Variations of this approach have been studied by a number of investigators (at CSC, North Electric, Sylvania, IBM, and RCA, to name a few) and each of these variations has advantages and disadvantages in dealing with the basic problem of network overload by the search signals during stress and with other problems of search routing.

A CSC-developed approach called quick-trace routing provides a method of dealing with these problems. The approach avoids complicated processing at the nodes for purging the system after the search has been completed and combines the advantages of search routing with many of those of stored directory routing.

#### 4.3.1.2 Quick-Trace Routing

The quick-trace system is an austere version of saturation routing that appears especially well adapted to a multi-node tactical environment requiring tandem switching. It attacks the classic problem of network overload during search, by the following features:

1. Out-of-band search by means of a special signaling or orderwire time slot not used as a user traffic channel. This procedure confines the search traffic to a single channel.

2. Search messages are passed from node to node very promptly and rapidly, greatly reducing the time of propagation and, hence, the number of messages in the system at any one time.

3. Trunk capacity is not seized or reserved during the search; the speed of search permits retrace rapidly, assuring that trunk availability is unlikely to have changed between search and setting up of the call.

4. A short search sequence is possible. This may be used to limit the portion of the network searched for a large proportion of the calls.

Avoidance of trunk reservation speeds up the search and eliminates the task of later releasing those reservations which were not used. Even more important, calls and search messages seeking to use a desirable route are not turned away because of reservations held by other search messages which will not actually make use of the reserved trunks.

The quick-trace routing method can look through an "all trunks busy" link to find a subscriber without preempting trunks during the search procedure. Positive control for call status signaling can be obtained by locating the called party even though the path searched included a link in the "all trunks busy" condition.

Dual handling of priority searches is provided so that when preemption is required the best alternate not requiring preemption is also presented. Thus, in contrast with search systems using inband search on the trunks, a preemptive search need not disconnect a low priority call unless that trunk is needed in the actual call setup. In the quick-trace method search is initiated at the originating node, but the final call connection is extended on a "spill back" basis from the called party's node.

1. Out-of-Band Search Channel

A separate out-of-band search channel (i.e., orderwire time slot) in each link is set aside for the search process. Since a 32 kb/s time slot is set aside for signaling and technical control functions of fault and quality reporting, it is possible to make use of this facility. Determination of the data rate required by the routing procedure is a function of the network size in terms of number of switching nodes, the switch and trunk sizing, and the network configuration. Generalized calculations indicate that the size range to accommodate routing data is approximately one-third to one-half of the 32 kb/s channel.

2. Search-Message Format

When the originating node processor receives a call request to a user not homed on the originating switch, it assembles the search message into a prearranged format. A format suitable to a large tactical network (e.g., accommodating up to 256 nodes which can be considered a worst case condition) is shown in Figure 43.

| | CALL IDENTIFICATION | | |
|---|---|---|---|
| Search Limit<br>4 bits | Priority<br>2 bits | Original Node<br>8 bits | Called Number<br>24 bits |

Figure 43. Typical Search Message Format

The search message is launched via the search channel to all contiguous nodes whose links to the originating node are not fully occupied by calls of higher or equal priority. Each priority call is handled as if it is two separate calls--one of the appropriate priority, and one treated as routine. The result is that for

priority calls whose best path requires preemption, there is also available an alternate choice indicating the best path available without preemption. If the paths are not significantly different in length, the alternate can be chosen to avoid unnecessary exercise of preemption.

Each node scans the full search message (less than 2.5 milliseconds long for the search message shown in Figure 43 when framing and error control are included) before deciding whether to store the message, store it and pass it on, or eliminate the message. The search does not have to be held up while the switch determines whether or not it has the called number; as a result, very rapid dissemination of the search takes place, even if the scanning process by which the switch determines whether the called number is present is relatively slow. If the switch design permits rapid scanning it may be better to wait for the search for the called number at the switch before deciding to pass on the search message. With reasonable care in the design of the scanning equipment, the whole process of read in, scan and decision, and reinsertion back onto the search channel, where required, will take less than 10 milliseconds when estimated on a worst case basis.

A search message for a particular call arriving at a node is passed on to all contiguous nodes to which trunk capacity at the priority level of the call exists, provided that this has not already been done for that call in response to a search message coming into the node by a shorter route, and provided that the message has not exceeded its search limits. Any search message that is passed on, or that would be passed on if it had not just reached its search limit, is also placed in storage at the node in a temporary memory accessible under the call identifier together with a record (4 bits) of the link on which the search message entered the node. The information necessary to permit the decision to store and/or pass on the search message resides in the priority and search limit numbers discussed next.

### 3. Search Limit

The search limit number is inserted by the originating switch for two purposes: limiting the length of the search, and providing an indication of the number of handovers in each path. The latter information is useful to technical control network monitoring. The information is passed on to the System Control Node via the orderwire time slot assigned this function. Each subsequent search node, before passing the message on, will reduce the inserted number by one count. A node receiving a message with a search limit number equal to zero may perhaps store the message but will not pass it on. Thus, if the originating node inserts the number 2, the search will penetrate the network to a depth of 3 nodes distant from the origin. A search to the depth of two or three nodes is referred to as a short search in large multi-node networks with much tandem switching. Under the general recommended procedure, except perhaps in the case of a limited number of special users, the originator switch first attempts a short search and automatically reinstates the call as a long search only if the called party is not located within the search depth of the short search.

The length of the short and long searches may be varied adaptively depending on the node, the deployment, or the immediate tactical situations. For example, plans for the Air Force Combat Theater Ground Communication Network indicate that communication satellites and remotely piloted vehicles (RPV) may form the primary means of internodal communications. Tropospheric scatter radio, line-of-sight radio, and cable will serve as a secondary source of trunk interconnects. In this network, the technical control function of circuit rearrangement can be accomplished adaptively as follows:

The primary means of call interconnect is tried by means of a short search message assuring that the initial call setup attempt will be made by means of a satellite or RPV link. If this attempt is unsuccessful, the alternate routing can be accomplished through the secondary terrestrial network by launching a second attempt using the long search format (perhaps six to ten nodes). Under these conditions about 85 percent of the calls are expected to be limited to short searches with consequently less loading on the search channel and less processing in the network.

The search limiting feature described above also serves the useful function of giving the switch some control over limiting trunk usage during stress conditions. A form of trunk barring can be instituted in response to the traffic monitoring function by limiting certain users to call connects which can be accomplished by means of short searches. In this case the secondary terrestrial network can be held in reserve for essential calls.

This technique primarily bases circuit routing on the minimum number of links traversed by the search signal. Minimum overall delay in propagation of the search signal can be used as an alternate technique. This procedure, however, has the disadvantage of penalizing trunks derived from satellite systems. Since satellite transmission is considered an important method of communication in the future tactical theater, overall delay does not appear to provide appropriate criteria for most call set-up situations. Certain special users such as message switching systems using ARQ techniques, however, may not be able to tolerate circuits having relatively long transmission delays. In these cases, special class marking of user access lines are required.

4. Call Identification

The call identification consists of a N bit number, M bits of which identify the originating node and P bits identify the called number. For example, a large network may use eight bits for node identification and twenty-four bits for address identification. Together with the priority indicator, which serves to differentiate between priority and routine searches, the total N bit call identification word uniquely tags each search.

The call identifier word (CIW) is stored at each node before the search message is sent to the subsequent nodes. The CIW of an incoming search is scanned against those currently in store at a node and used to terminate searches arriving at a node that have accumulated handover counts higher than that of a previously processed version of that search message. A "scratch-pad" type memory can be set aside in the common processor to store the volatile CIWs since the search procedure is brief and there will be only a few searches in progress at any one time. A call not exceeding its search limit, and not found in the "searches in progress scratch pad", is passed to the next nodes after updating the stored information.

5. Path Establishment

When a node determines that it serves the called number, a brief delay is established to permit the arrival of possible better paths that may have been queueing for transmission. In the case of priority calls, this delay also permits receipt of both the preemptive and routine paths. The terminating node then signals back along the link stored in its memory. This link corresponds to the last step in the path by which the search message following the best route entered the node. The next node in turn, after consulting the call identifier, signals the previous node and the process is repeated until the originating node is reached.

6. System Purging

The search message in the scratch-pad storage at the ISMTC node must be retained in the system until the selected path has been established. After the path has been established the stored search messages for that call must be purged. This can be accomplished by a time-out procedure under control of the common processor software; that is, a message is stored for a fixed time at the node after which it is assumed that the call lock-in has occurred via some other path and the message is erased. The advantage of this procedure is that the need for retracing of paths to purge memories is avoided. Additional system speed is obtained by permitting fast time out for short searches.

7. Processor and Traffic Loading Estimates

The main purpose for describing in some detail a possible routing scheme which can serve the combined functions of switch routing and technical control circuit alternate routing is to provide sizing estimates for the common processor. In order to do the required calculations, assumptions on network sizing must be made and are as follows:

A population of 12,000 users (i.e., subscribers) are assumed, each generating four three-minute calls during the busy hour. The number of calls generated in the entire network amounts to 13.3 calls per second. For the purposes of the calculation, it is further assumed that 10 percent of the calls have priority status and are launched as double searches and, therefore, a reasonable approximation for

total search traffic is 15 calls per second for the complete network. Each link is occupied by each long search message approximately once and the short searches will occupy perhaps a third of the links. Assuming that 85 percent of the traffic is handled with short searches results in an average traffic of 6.45 search messages per second in each link. Since the search message duration is about 2.5 milliseconds (a conservative estimate) the traffic loading on the average link during the busy hour will be only 0.016 Erlangs. The resultant probability that the search message will wait in queue for transmission out of the node is 0.016, and the mean wait in queue for each search message will be only 40 microseconds.

This indicates that the traffic loading on the search channel time slot is light. When processing times are added at the nodes a reasonable cross office (within node) time of 10 milliseconds per search is obtained. A best path will generally be found, therefore, in about 0.1 seconds and complete call setup (except possibly for final seizure of the trunks) should be obtained in less than 0.2 seconds in the case of terrestrial links. In the case of satellite links, a minimum transmission time of 440 milliseconds is required for combined up link and down link transit time (including return time). Thus, if a maximum of two satellite paths (both up link and down link) is assumed, transmission delays approach 1 sec and, therefore, in this worst case call set-up delay is dictated by transmission delay and not node processing constraints.

4.3.1.3 Deterministic Routing

Another possible method of providing an alternate routing capability in the integrated complex is by using "deterministic routing". The term "deterministic routing" refers to routing techniques in which status information about the links and subscribers is circulated throughout the network, and route selection is based on this knowledge. In contrast to search routing, in which the direction the call will take is not known until after the search is complete, deterministic routing implies planning the intended route in some detail. This planning may be done at the originating switch, or on a link-by-link basis at each switch in the path.

To provide the flow of status information, transmission capacity must be supplied by the network either through the signaling on available links or by means of a separate status channel (out of band). The latter approach was chosen for the discussion below. Calculations indicate that the transmission requirement for this scheme is not large--a fraction of a 32 kb/s channel--but the impact on the common processor is severe in terms of memory capacity and processor load. Based on a maximum of 130 nodes and 12,000 subscriber numbers, a number directory of approximately 400,000 bits will be required at each node. This constitutes a major limitation of this class of routing because of the disadvantage it will impose on the tactical limitations on size and weight. The practicability of this approach, therefore, depends heavily on technological advances in memory storage devices.

The call may either be set up from the originating node by originating register control or by step-by-step procedures. If originating register control is used, the

originating switch selects the complete route, from origin to destination, based on its up-to-date awareness of link status conditions. The step-by-step procedure requires each tandem node to make a route decision to the next contiguous node. At the next node a new decision is made on direction for the next handover. Both procedures require the same type of status information described in this paragraph. The advantage of originating register control is that only route computation or table look-up is required for each call. However, the step-by-step procedure permits the network to react to possible changes in status during the time the call is being set up, and thus permits slower status updating cycles.

The deterministic routing method has the advantage of providing full network status information at each node. In addition to its use in routing each call, this data can be used for technical control of the network by providing real-time network status data for the System Control Function.

## 4.4 REPORTING AND RECORDKEEPING

Technical control operations oriented records systems are required to provide the information necessary for maintaining a continuous awareness of the operational status of circuits, equipment, and the associated network. In present day systems, considerable effort and manpower are required to maintain such records systems. Studies have shown that the major portion of the recordkeeping workload is spent in collecting, recording, formatting, and generating reports, with a very small portion attributed to the analysis of the recorded data.

The logical solution for providing an efficient recordkeeping system lies in the use of processor-controlled records. This would provide an ideal base to eliminate the time and workload restrictions existing in the reporting and analysis of operations activities. In addition, an analysis output could be readily generated from the master file of the day's activities and could provide higher echelons with guidance by identifying developing trouble areas. Corrective measures could thus be applied to situations long before they reach proportions that would be identified by the present manual analysis effort.

It should be stressed at this point that the information used in compiling and generating reports is a product of the recordkeeping system. It is the maintenance and analysis of the recordkeeping system that are time consuming. Thus, while automation of only the reporting function may increase the quantity and accuracy of the reports to higher headquarters, it cannot ease the recordkeeping workload of technical controllers, which provides the basis for the formal reports. Therefore, automation must inolude both the reporting function and the recordkeeping function for maximum overall effectiveness and reduction of workload.

The flexibility and scope of an automated reporting and recordkeeping system are only limited by the available inputs and the control program sophistication. Input sources include measured data from signal and equipment monitors, manual operator entries,

circuit technical data concerning the routing and operational characteristics of circuits and channels, circuit rerouting assignments, maintenance actions, and similar operational data inputs required in the day-to-day operation of the technical control.

An automated system containing this type of information should satisfy existing and future reporting requirements, and the outputs could be provided with little human intervention. Furthermore, definitive listings could be produced for specific staff action, eliminating the requirement for managers to sift through large amounts of data to identify action items relating to this activity.

There are several approaches to automating the reporting and recordkeeping function. Each ISMTC could be provided with its own processor-controlled record system and would be responsible for generating reports on all circuits appearing at the ISMTC and performing analysis for all circuits under its control. This approach is not recommended because redundant trouble reports could be generated from several ISMTC nodes on the same circuit problem, thus providing redundant data at management level.

In the second approach, selected switch nodes could be designated as reporting stations and provided with processor-controlled reporting and recordkeeping systems. Other switch nodes would be designated as reported-on stations and provided access to the records systems of a reporting station. In this way, a single automated system could serve several nodes. Each reported-on station would be provided automated access to the processor of a reporting station for submission or retrieval of relevant data. The reporting station would be responsible for the reporting, recordkeeping, and data anlysis for both itself and each associated reported-on station. This approach minimizes redundant reports at management level and provides reported-on stations with the benefits of an automated recordkeeping system.

A third approach is simply an extension of the previous approach, with the addition of a central reporting location for controlling and directing the reporting stations. In this approach, the reporting stations are grouped by communities of interest, and each group is assigned a control center equipped with a processor-controlled reporting system. The control centers would be responsible for all report generation for the reporting stations under its control. It would automatically receive status change information from all subordinate reporting stations, thus enabling it to process and generate reports on circuit status for faults occurring within its area of responsibility and to provide a consolidated system analysis of the data submitted by each reporting station. The control center would be responsible for compiling, correlating, and comparing the input from each reporting station and generating reports for management. This centralization of reporting responsibility for a community of interest will effectively eliminate redundant reporting and reduce the time spent on inter-ISMTC coordination in compiling reports. It will also reduce the possibility of redundant reports at management level.

There are basically three types of reports which may be considered: (1) Maintenance Reports, (2) Status Reports, and (3) Supervisory Reports.

The factors which must be considered for the reporting and recordkeeping function are discussed next. In these paragraphs typical report entries and formats are described. It should be emphasized that the reports, report entries, and report formats discussed were developed as an input to the analysis of the impact of report generation and distribution on the ISMTC common processor. The complete development of the ISMTC reporting and recordkeeping function should be based on an approved TRI-TAC TCCF plan. A preliminary plan incorporating the operational concept of the TRI-TAC TCCF has been developed but is still in the review cycle of the three military services. It is entirely possible that the approved TCCF plan will require several different types of reports within each of the three categories of report noted above. Furthermore, the report entries and formats described below may have to be modified to conform to the approved TCCF plan.

### 4.4.1 Maintenance Reports

Maintenance reports must be generated on a near real-time basis and transmitted to the associated maintenance function for immediate action. Two types of maintenance reports should be generated automatically: (1) a fault report upon completion of all required fault isolation procedures; and (2) a fault-cleared report upon circuit restoral. As a minimum, the fault report should include:

1. Fault report number/date/time
2. Location of fault
3. Circuit number
4. Faulty element (reason for outage or system degradation)
5. Remarks

The fault-cleared report should include, as a minimum, the following items:

1. Fault report number/date/time.
2. Time fault cleared/total time of outage.
3. Reason for outage (code or narrative description of action taken to clear the fault. This would be entered into the report at the maintenance facility, tagged onto the processor-generated report, and stored for the preestablished report retention period).

To minimize storage requirements, specific codes should be assigned, whenever possible, to each of the items noted above. Fault reports and fault-cleared reports are described next in more detail.

4.4.1.1 Fault Reports

It should be noted that the fault reports and fault-cleared reports described below are for use by the maintenance function at a particular node.

1. Fault Report Number/Date/Time - All fault reports should be numbered sequentially beginning with number 1 at the start of each day. The date/time group should follow the fault report number, e.g., FR001/12-10/0015.

2. Location of Fault - As noted above, fault reports are generated for use by the maintenance function at a particular node. To expedite the dispatch of maintenance personnel to clear the fault, the report must include the location of the fault at the affected node. There are two basic methods by which the location can be specified on the fault report, viz:

   a. Van/shelter equipment function, i.e., tropo transmitter, tropo receiver, switch center, etc.

   b. Van/shelter pre-assigned number designations correlated with locations on a map of the nodal area.

   Of the two, the location by equipment function appears to be the better method since maintenance personnel will in general be familiar with the location of all functional equipment at a node without reference to maps and tables. In the following discussion it will be assumed that the location method of specifying equipment function on the fault report will be used. Table 6 lists examples of location codes and descriptions for typical equipment functions.

3. Circuit Number - This entry on the fault report will indicate to maintenance personnel the number of the faulty circuit of the location indicated by the previous entry. It is anticipated that circuit numbers will not require more than ten digits or combinations of ten letters and digits (alphanumerics).

4. Faulty Element - This entry will indicate to maintenance personnel the particular modular equipment element which caused an outage or start of system degradation. There are basically two classes of equipment which must be monitored to determine (fault isolate) faulty elements which may be causing system problems: (1) major transmission subsystems; and (2) ancillary support equipment, e.g., air-conditioning, prime power sources, etc. In many instances the failure or degraded performance of ancillary support equipment will lead

Table 6. Location Codes and Descriptions

| Location Code | Description |
|---|---|
| TT-X | Tropo transmitter number "X". (A number must be assigned to most location/function codes since there may be more than one set of equipment providing the same basic function.) |
| TR-X | Tropo receiver "X" |
| LT-X | Line-of-sight transmitter "X" |
| LR-X | Line-of-sight receiver "X" |
| HT-X | High-frequency transmitter "X" |
| HR-X | High-frequency receiver "X" |
| ST-X | Satellite ground terminal transmitter "X" |
| SR-X | Satellite ground terminal receiver "X" |
| RT-X | Remotely piloted vehicle ground terminal transmitter "X" |
| RR-X | Remotely piloted vehicle ground terminal receiver "X" |
| MS | Major switch (ISMTC) |
| US-X | Unit level switch "X" |

to failure of a major transmission subsystem. The system, therefore, must be capable of correlating many measurements from the monitoring function in order to determine the correct faulty element. Table 7 lists some typical faulty element codes for major transmission subsystems and ancillary support equipment. It should be noted that mnemonics are used as faulty element codes in order to minimize "table look-ups", i.e., the mnemonic codes can be easily remembered by maintenance personnel. In general, it is recommended that mnemonic codes be used whenever possible. The number of codes required is related directly to the desired degree of automated fault isolation. As noted previously, the degree of fault isolation capability is dependent on the number of key points monitored within the system. The analysis and selection of which points should be monitored and how they should be monitored (including frequency of sampling) must be an integral part of the design of communications and ancillary equipment to be used in the time frame under consideration; that is, future equipment should be designed using a systems-oriented approach taking into consideration the overall requirements for equipment monitoring as it relates to the total technical control function.

#### 4.4.1.1.1 Fault Report Format

Figure 44 illustrates the format of a typical fault report. This type of report should be generated by the common processor of the ISMTC if the fault is isolated at the local node, or by the processor associated with the system control element if the fault is a system (network) problem. In any event, the report should be distributed to the equipment support element at the affected node immediately after the fault is isolated.

| Line | Contents |
|---|---|
| 1 | SXXX/FR01/12/16/0015 |
| 2 | AAANNNNAAA/OUT/0014 |
| 3 | TT-02/PAM |

**Figure 44. Typical Fault Report Format**

Table 7. Faulty Element Codes and Descriptions

| Faulty Element Code | Element | |
|---|---|---|
| PAM | Power Amplifier | Major Transmission Subsystems |
| UCO | Up Converter | |
| DCO | Down Converter | |
| MOD | Modulator | |
| DEM | Demodulator | |
| TDM | Time Division Multiplexer | |
| PRE | Preamplifier | |
| COM | Combiner | |
| DUP | Duplexer | |
| EXC | Exciter | |
| ANT | Antenna | |
| IFA | IF Amplifier | |
| OSC | Oscillator | |
| REC | Receiver | |
| TRA | Transmitter | |
| ⋮ | ⋮ | |
| ACO | Air Conditioning | Ancillary Support Equipment |
| HEX | Heat Exchanger | |
| LOP | Low Oil Pressure | |
| FFS | Faulty Fuel System | |
| GOL | Generator Overload | |
| GUV | Generator Undervoltage | |
| GOV | Generator Overvoltage | |
| TRF | Transformer Failure | |
| ⋮ | ⋮ | |

With reference to Figure 44, the following is a description of each line entry in the report:

Line 1 - Station XXX reporting/first fault report of the day/date-time group.

Line 2 - Circuit AAA NNNNAAA/complete outage/detected at 0014.

Line 3 - Fault isolated to tropo transmitter at site 2/defective power amplifier.

NOTE

The entry OUT on Line 2 signifies a complete outage as noted above. Another possible er'ry in the same position could be SD (system degradation) to signify that action must be taken to prevent a complete outage.

4.4.1.1.2 Fault-Cleared Report Format

A typical fault-cleared report is illustrated in Figure 45. This type of report should be generated by the processor which generated the original fault report and distributed to the equipment support element. For each fault-cleared report, personnel at the equipment support element should enter the equipment designation or part number of the element which was replaced to clear the fault. This type of information would be useful for the correlation and analysis of equipment failures to develop trends.

| Line | Contents |
|---|---|
| 1 | SXXX/FCR03/12/16/0100 |
| 2 | FR01/0059/44M |
| 3 | PAM Type 954 (P/O AN/MRC-98) |

Figure 45. Typical Fault-Cleared Report Format

With reference to Figure 45, the following is a description of each line entry in the report:

Line 1 - Station XXX reporting/third (3rd) fault-cleared report of the day/ date-time group.

Line 2 - Reference FR01/fault cleared at 0059/total time of outage was 44 minutes.

Line 3 - Replaced power amplifier Type 954 which is part of the AN/MRC-98.

NOTE

Lines 1 and 2 generated by the appropriate processor. Line 3 would be entered interactively via keyboard at the equipment support element.

4.4.2 Status Reports

Status reports should be generated by ISMTC nodes either on a periodic basis or upon demand by the system control element. With regard to status, the system control element must be aware of the status of both equipment and traffic at each node under its control. If all fault and fault-cleared reports generated by the switch nodes were transmitted to the system control element processor, equipment status at each node could be readily determined; that is, the system control element processor through correlation and analysis of the fault and fault-cleared reports could develop the following types of information:

- Faults not cleared
- Total time of outage by circuit
- Failures by type of transmission media
- Failures by type of equipment

Therefore, an equipment status report would not have to be generated by each ISMTC node since the maintenance reports described previously contain the necessary information to generate these reports at system control. However, each ISMTC must be capable of generating traffic status reports for transmission to system control. The traffic status reports should include those traffic statistics deemed necessary to obtain maximum operational effectiveness of the system control element. The traffic status report should include:

- Reporting station/report no./date-time group
- Link occupancy
- Busy hour/busy hour load/average call hold time
- Trunk barring (on) line load control (on)

| Line | |
|---|---|
| 1 | SXXX/TSR03/12/16/1100 |
| 2 | AAA 12345/75% |
| 3 | AAB 12345/90% |
| . | . |
| . | . |
| . | . |
| N | AAX12345/85% |
| (N+1) | 0845-0945/0.80E/1.5M |
| (N+2) | TB-1H35M/LLC25M |

Figure 46. Typical Traffic Status Report

Figure 46 illustrates a typical traffic status report format. With reference to this figure, the following is a description of each entry in the report:

Line 1 - Station XXX reporting/traffic status report number 3/date-time group.

Lines 2 to N - Link occupancy by link number.

Line (N+1) - Busy hour was 0845 to 0945/busy hour load was 0.80 Erlangs/average call hold time was 1.5 minutes.

Line (N+2) - Trunk barring was on for 1 hour 35 minutes/line load control was on for 25 minutes.

NOTE

With respect to Line (N+2), this entry may have to be expanded to include which trunks were barred and for what time period. In addition, other entries such as calls by precedence level, error rate/trunk, etc., may be required.

4.4.3 Supervisory Reports

Supervisory reports, as used here, refer to those reports which are required and generated by the system control and planning elements. These reports are used as the basis for maintaining optimum system connectivity and operational effectiveness at all times, i.e., during stressed and non-stressed conditions. Examples of stressed conditions include rapid redeployment of forces resulting in relocation of nodal equipment, outages due to equipment failure, outages due to action by the enemy, and unanticipated changes in traffic loads over certain trunks. During stressed conditions the network will have to be reconfigured as quickly as possible. This reconfiguration may require the following actions:

- Reassignment of alternate routes for each node in the network.
- Initiation of trunk barring on specific trunks.
- Changes to satellite/RPV time-slot assignments.
- Any other actions which may affect overall network connectivity.

To accomplish the above actions will require a processor with a large data base and having the capability to perform scientific calculations, e.g., calculation of optimum alternate routing tables for each node, calculation of path losses for radio links, selection of non-interfering frequencies, etc. The processor must also be capable of generating and disseminating supervisory reports containing the information required to implement the actions noted above at all affected nodes. Many of the inputs required to perform the necessary calculations and report generation would not be available at ISMTC nodes. However, the information required would be derivable at the system control element from each ISMTC-generated report (fault, fault-cleared, and traffic status). Based on our analysis, it does not appear to be practical or feasible to include the capability for scientific calculation and the generation of supervisory reports into each ISMTC node. However, each ISMTC must provide inputs to this function via the maintenance and traffic status reports described above in paragraphs 4.4.1 and 4.4.2, respectively.

This system has the disadvantage in that overall network reconfiguration is dependent on the survival of the supervisory node. Possible methods to alleviate this problem are: (1) the assignment of alternate supervisory nodes to assume reconfiguration responsibility after a certain delay period; (2) manual reconfiguration by switch operators

and technical control personnel; and (3) supervision and control provided by a contiguous nodal system.

## 4.5 TECHNICAL CONTROL IMPACT ON SWITCH DESIGN

This section investigates the impact on switch design due to the integration of the technical control functions into the ISMTC. The analysis indicates that while the effects on the common processor are significant, the impact on the switch would be moderate. The major effect is an increase in matrix size due to built-in matrix error detection equipment. Additional matrix complexity results if the common transmission equipment monitoring scheme described in paragraph 4.5.2 is implemented. It is concluded that specific matrix type is relatively insensitive to technical control considerations and the matrix should be selected predominantly on the basis of switching and multiplexing factors.

Further switch design considerations resulting from the order wire implementation are discussed in Section 5.3.

### 4.5.1 Technical Control Considerations on Matrix Design

This section discusses the various aspects of technical control associated with the switch matrix. More specifically, the topics covered include fault detection, fault isolation, and automatic cutover to spare modules. An effort has been made to keep the discussion as general as possible in order not to restrict the study to any one matrix type. However, in order to bound the problem several assumptions have been made which reflect the properties of those switch arrays expected to be the most applicable to this study. Therefore, for the purpose of this discussion, the matrix will be assumed to be a time division array with N input and N output highways each containing M channels. It should be noted that Candidate matrices 1 and 2 described in Section 2.1 do not possess the above properties. However, these matrix approaches were not preferred in the matrix comparison of paragraph 2.1.3 due to cost, weight, and power considerations.

#### 4.5.1.1 Fault Detection

##### 4.5.1.1.1 Out-of-Service Matrix Testing (Candidate A)

Figure 47 shows a possible matrix monitoring technique. A matrix output highway is selected by a multiplex gate and demultiplexed into individual channels. A single channel is routed to the processor I/O interface via another multiplex gate. Each channel may now be monitored on an individual basis.

This monitoring technique could be used to check continuity or bit error rate on idle trunk group channels and check for "forbidden" characters on occupied channels. The processor could also check the trunk group common channel framing pattern for bit errors.

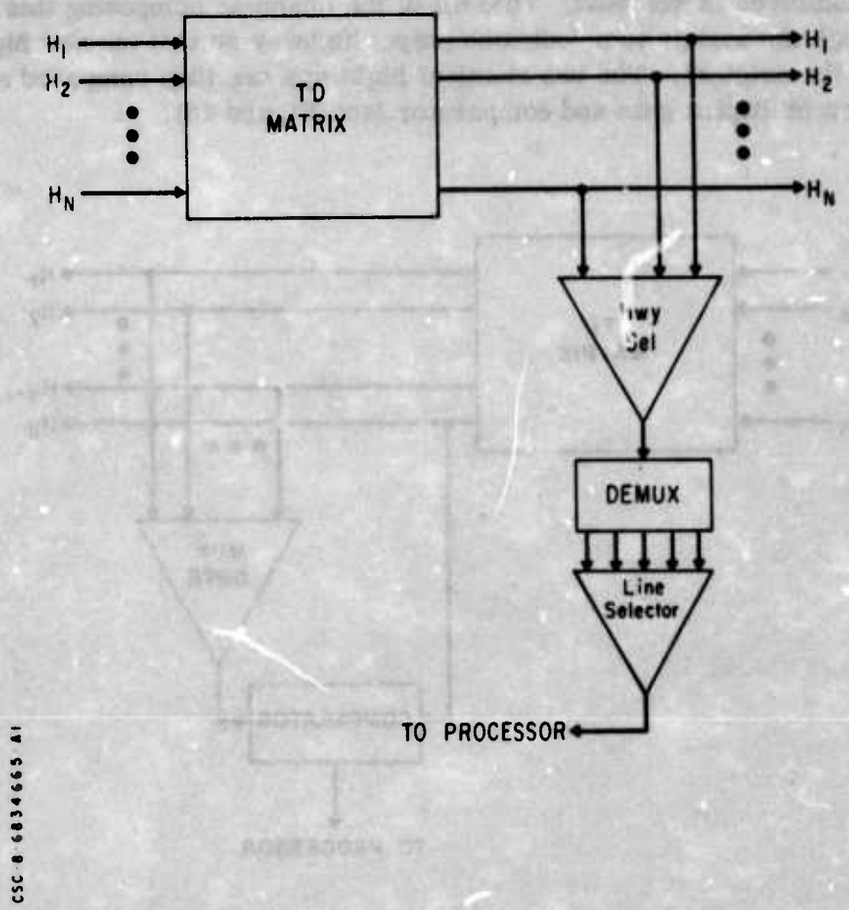



**Figure 47. Out-of-Service Matrix Testing - Candidate A**

More sophisticated tests may be implemented in which test patterns generated at the supervisory tone generator or in the processor could be switched through the matrix to various idle outputs under processor control. A degree of fault isolation could be achieved by implementing a series of elimination tests which would route test messages around or through suspected modules.

4.5.1.1.2 Duplicate Path Technique (Candidate B)

An alternate approach to Candidate A might be to consider dedicating a portion of the original matrix to perform part of the error detection function. First the output highway to be monitored is selected. Then all of the channels composing this highway are routed through the matrix to a dedicated output highway so that the new highway is a duplicate of the original. The two identical highways are then compared at the matrix output using a multiplex gate and comparator (see Figure 48).

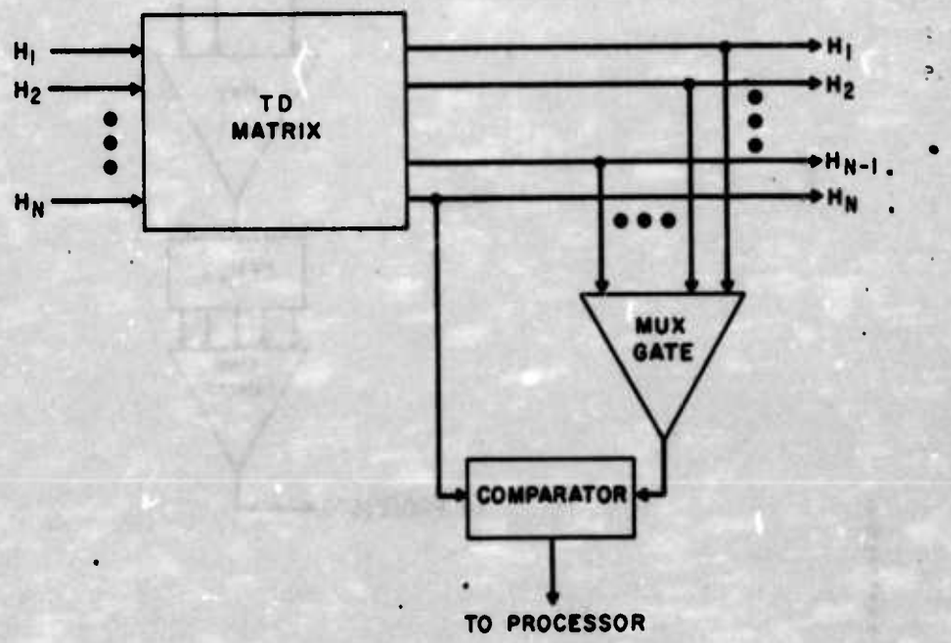



Figure 48. Duplicate Path Error Detection - Candidate B

It should be noted that Candidate B is an in-service technique as opposed to the out-of-service scheme described previously.

The obvious disadvantage of this approach is that the presence of duplicate messages increases the traffic loading and may cause matrix blocking during heavy traffic load periods. This problem may be avoided by constructing a larger matrix with one or

more additional highways to decrease the matrix blocking probability. The extra highway, or highways, could be used as spare capacity in the event that another internal path has failed. This would be in place of including a spare module to restore the matrix path as is required for Candidate A.

Another serious disadvantage to the Candidate B approach is that the action of duplicating an entire output highway could represent a large processing workload for the computer. Once a duplicate highway is set up by the controller, it may be monitored as long as necessary. However, in order to examine a new highway the duplication process must be repeated. In fact, this processing requirement is the limiting constraint on the channel scanning rate for this scheme. In order to ease the processor workload it may require on the order of 100 ms to monitor a highway. The determination of the monitoring interval requires an analysis of processor load in terms of line setup time and processor analysis required. Of course, this monitoring rate could be speeded up or slowed depending upon the traffic load.

Candidate B could be a viable in-service matrix error detection technique if:

1. It is permissible to scan at a moderate rate;

2. The particular matrix type used does not require much expansion to provide the specified blocking probability;

3. The processor workload due to other functions is not too great.

4.5.1.1.3 High Speed Fault Detection (Candidate C)

Two possible methods have thus far been discussed which may be used to monitor matrix errors. An important system consideration is the inherent fault detection delay associated with a particular monitoring technique. The TRI-TAC system design objective for fault detection time for a channel or subsystem failure is given to be a fraction of the average time interval between successive messages or calls using the facility. However, it appears feasible to drastically reduce this criteria so that subscribers are less likely to experience loss of synchronization due to a matrix failure. Therefore, this paragraph is oriented toward high speed error detection.

One possible high speed error detection technique is a direct comparison of the switch inputs to outputs. Such a method is illustrated in Figure 49. Selector gates are included to provide the capability of connecting any matrix input highway and any matrix output highway to a comparator. A time slot interchange (TSI) has been inserted into each highway path between the input selector gate and matrix input in order to achieve timing coincidence between input and output time slots. Errors are detected in this system by comparing, on a bit-by-bit basis, the matrix input with the corresponding output. Output highways $H_1$ to $N_n$ are scanned sequentially under the control of a counter.

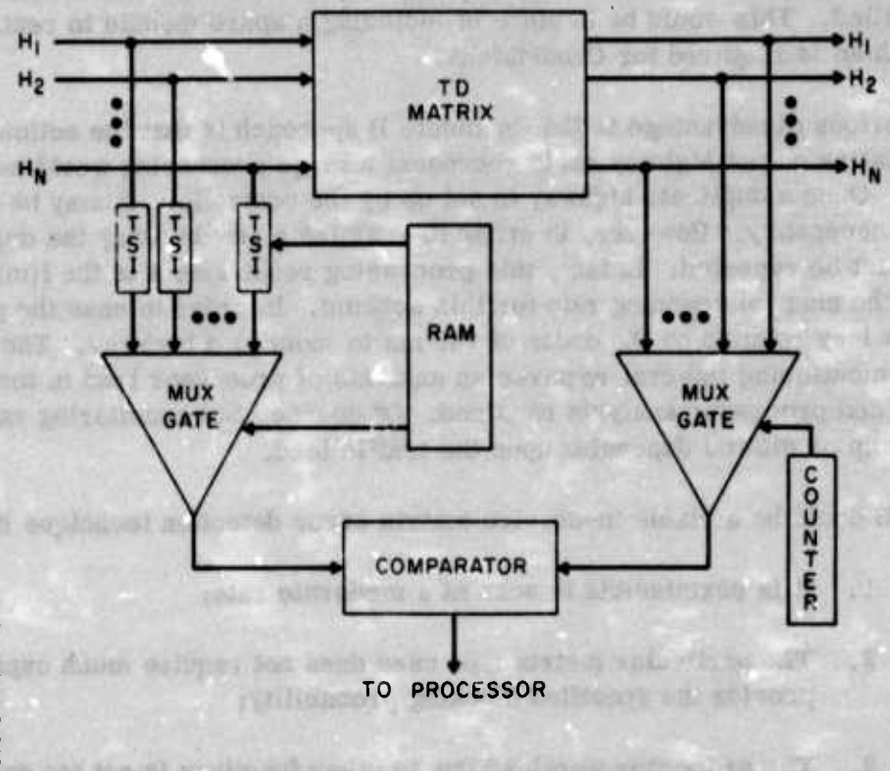



Figure 49. High Speed Error Detection - Candidate C

Although the fault detection equipment control information is contained in the matrix connection control RAMs, these control words would have to be reformatted before use in the error detection process. This control word formatting could be accomplished with either a hardware or software approach. Note that this scheme requires an additional memory capacity (RAMs) in the error detection equipment to store the reformatted control words. In addition, each time the processor alters the matrix connection control memory the error detection equipment RAMs must also be updated.

The high speed fault detection capability achieved with Candidate C is counter balanced by the significant amount of additional hardware required for implementation. An increase on the order of 50 percent above matrix requirements is estimated. Such a penalty may be excessive unless such high speed operation becomes a requirement.

4.5.1.2 Matrix Fault Isolation

There are essentially two broad approaches to matrix fault isolation. The first is primarily a hardware approach in which error detection devices are inserted at critical points internal to the matrix. The disadvantage of this technique is the increased size and cost of the matrix. The alternate approach is to use the information pertaining

to internal switch routing already stored in the processor memory to isolate problems based only upon the matrix output errors. Although minimal additional hardware is required, increased processing time and storage are among the penalties to be paid. The latter approach appears to be more in keeping with the program objectives and therefore will be explored in greater detail in this paragraph.

The fault isolation methods for Candidate A and Candidate B consist of routing messages through and around suspected modules. However, the fault isolation technique for Candidate C is quite different and is described below.

Based upon the fact that the route for each call through the matrix is stored in the processor memory, it is possible in many instances to isolate faults down to the chip level. Exceptions are components configured in series and faults within a control RAM. For the latter case fault isolation is possible only to the specific control word which may span on the order of a dozen RAMs. The exact quantity is a function of the number of matrix stages and number of input/output lines. The difficulties of fault isolation in a series connection are illustrated in the Candidate 5 switch (see paragraphs 2.1.2.1.4). Note that within a single basic module one cannot distinguish between a failure in a multiplex gate and a tertiary stage RAM (time slot interchange) by merely observing matrix inputs and outputs. However, since this study is concerned with the tactical environment, the isolation of faults to the chip level may not be warranted. It is more likely that fault isolation to a module will be sufficient.

The fault isolation algorithm to be used is based upon the computer's ability to associate each individual matrix path with a set of modules through which the signal must pass. Thus, when an error is detected, the processor determines which output contained the failure and uses look-up tables to determine the corresponding route and modules involved. Thus, after several errors the failed system component (or components) may be identified by determining which modules are common to all of the errors. It should be noted that for certain channel sequences it may sometimes be necessary to analyze many errors in order to identify the basic common fault.

4.5.1.3 Fault Tolerant Matrix Design

Fault tolerant design can be achieved via any of three techniques.

1. Status redundancy uses extra hardware to mask the failures. An example is triple modular redundancy (TMR) in which a module is triplicated and a majority vote circuit is used at the module output. The main advantages of static redundancy are instantaneous fault correction and simplicity of design and operation. Unfortunately, the particular logic structures of the candidate matrices considered for this study program do not lend themselves to static redundancy techniques without the requirement for large amounts of redundant hardware. Thus, such an approach is not cost effective for the ISMTC.

2. Fail-soft systems (graceful degradation) use a highly modular structure which allows the loss of one unit to be tolerated. Cost savings are provided with degraded performance since fault tolerance can be achieved without redundancy. However, degraded service in a tactical environment, especially during times of conflict, is undesirable. Furthermore, certain component failures within the matrix may not produce uniformly degraded performance to all users. Instead a complete outage to one node (or group of local loops) might result while the remaining nodes are unaffected. Certainly, this situation is unacceptable.

3. Dynamic redundancy (standby sharing, selective redundancy) provides spares for replacement when a faulty module is detected. The advantage of such a technique is that a fraction of the redundant hardware needed for method (1) is required. Although failures will cause periods of outage or degraded performance, these intervals may be minimized by using high speed fault detection and fault isolation techniques. Therefore, this approach appears to be the best suited to the ISMTC application and will be discussed in greater detail.

4.5.1.3.1 Automatic Cutover to Spare Modules

Once it is established that errors are originating from the matrix it is desirable to automatically cut over to a spare module (dynamic redundancy) as soon as possible. The procedures involved in such an operation and the factors impacting on cutover time are detailed in this paragraph.

Prior to any cutover the processor must identify the module to be replaced. Thus, the fault isolation process is the first factor to impact on cutover time.

Another factor affecting cutover time is the loading of the control RAMs located on the spare module. Each basic module stores the control words pertaining only to its own switching operation. Since it is not possible to predict which module will fail, the applicable control words must be supplied to the spare module after the decision for cut over is made. The minimum total time required for the computer to load the RAM would be the product of the machine cycle time and number of control words per basic module. Assuming a machine cycle time of one microsecond, the time to load 60 control words would be 60 microseconds. This is approximately double the frame time for a 60-channel highway.

A further consideration during the cutover procedure is the testing of the spare module before it is switched in. It is possible to virtually eliminate this source of delay prior to an actual cutover by including the spare output highways in the normal scanning sequence.

#### 4.5.1.3.2 Cutover Flow Chart

Figures 50 and 51 contain a flow chart describing the sequence of events associated with the automatic cutover to a spare module assuming the Candidate C fault detection technique. First a check is made to determine if a spare module is available. Next all highways are scanned sequentially including those for the spare module. Thus, the spare module is constantly being tested which eliminates any test time delays.

Once the fault has been isolated (Figure 51) the spare module's control RAM is loaded from the computer. As soon as the loading is completed the failed module is switched out of service and the spare is switched in. Scanning of all lines is resumed in an effort to isolate the fault in the failed module and to look for new system failures.

### 4.5.2 Impact of Transmission Monitoring on Matrix

Although the monitoring of transmission equipment external to the ISMTC modules is expected to impact significantly on processor memory requirements and workload, the effects of such activity on the matrix will very likely be minimal. The only matrix impact foreseen is a possibility that the in-station transmission monitoring equipment may be expensive enough to require the sharing of this equipment between transmission paths. This would be required only in situations where the transmission equipment is not colocated with the ISMTC.

#### 4.5.2.1 In-Station TC System Configuration

One possible nodal technical control equipment configuration is shown in Figure 52. All the various technical control transmission status and fault detection signals to be monitored are converted to a digital format by means of A/D converters. A selector gate for each transmission path enables the selected technical control signal to arrive at a line driver. The line driver transmits the digital signal to a switching device which may be either the actual switch matrix or a separate scanner. The signal is now routed through the matrix (or scanner) to the RF and baseband monitors via D/A converters. The monitors output the results of the analysis to the processor.

#### 4.5.2.2 Matrix vs Scanner

The use of monitoring equipment common to all the transmission paths implies that a switching device must be used to route the various signal sources to the common monitors on a time-sharing basis. The most obvious answer to the switch problem is to use the circuit switch matrix already integrated into the ISMTC. This approach is attractive from the viewpoint that minimal additional hardware is required. The primary disadvantage of this technique is that a number of matrix terminations must now be allocated exclusively for technical control purposes. In addition, the matrix is capable of accommodating only digital signals. Thus, analog signals must be A/D converted at the input and D/A converted at the output.

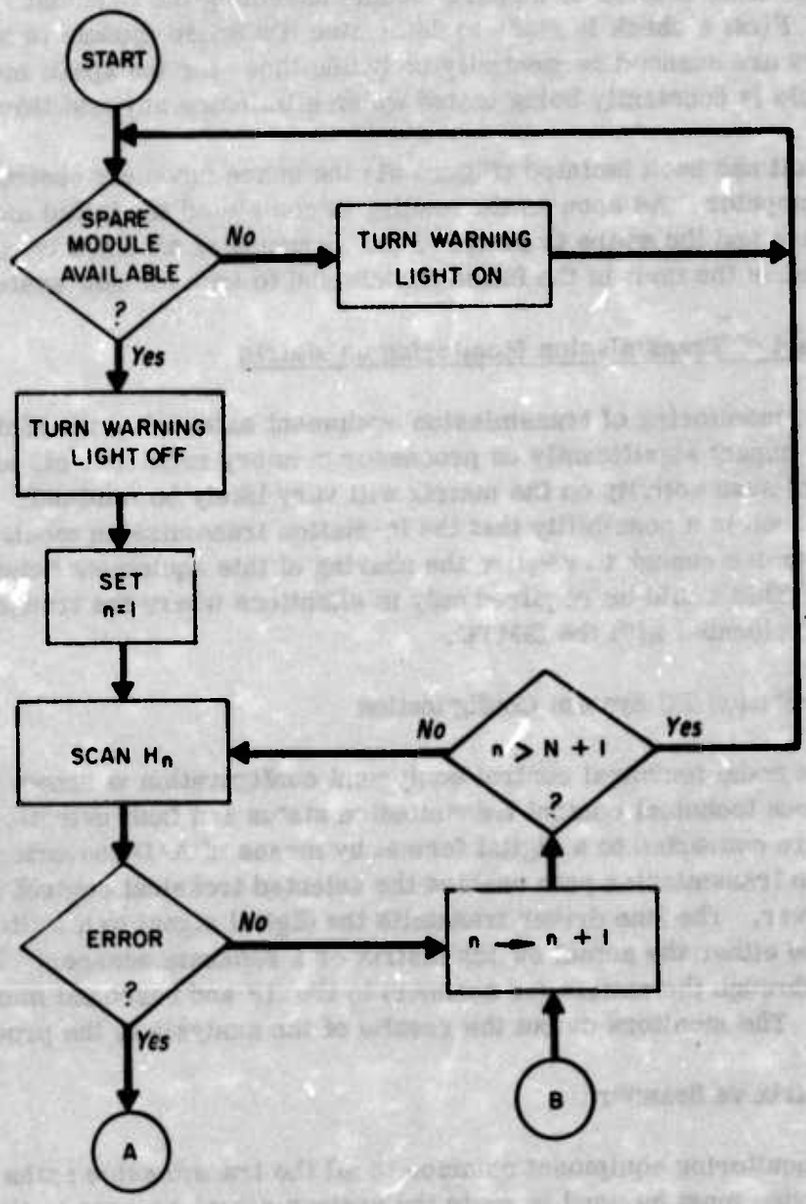



Figure 50. Automatic Module Cutover Procedure Flow Chart - Part I

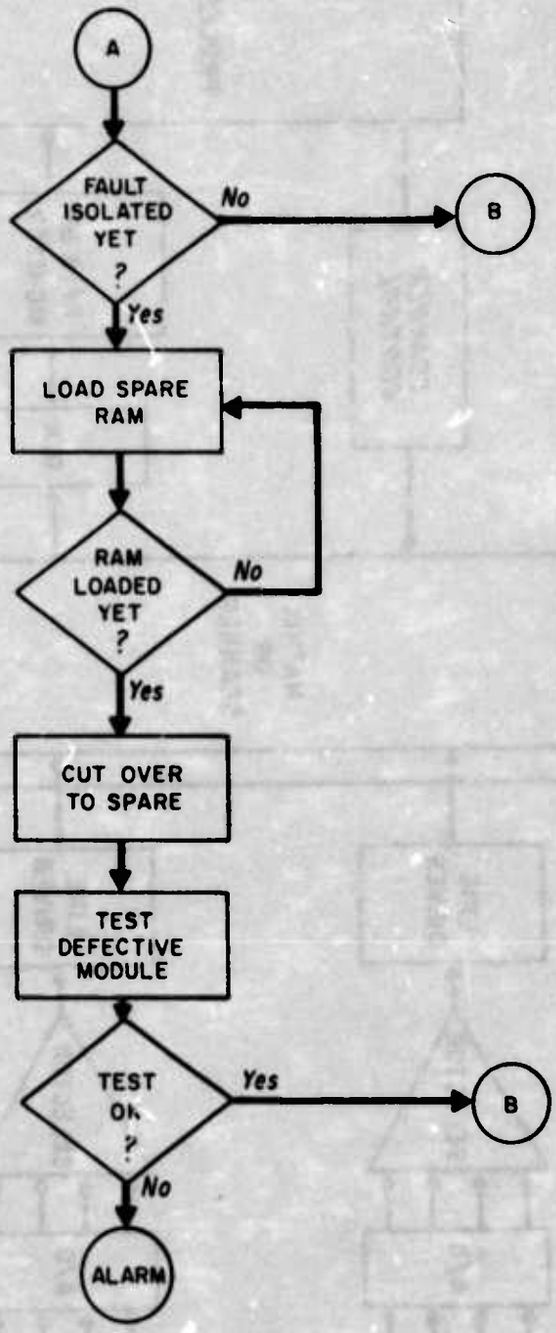



Figure 51. Automatic Module Cutover Procedure Flow Chart - Part II

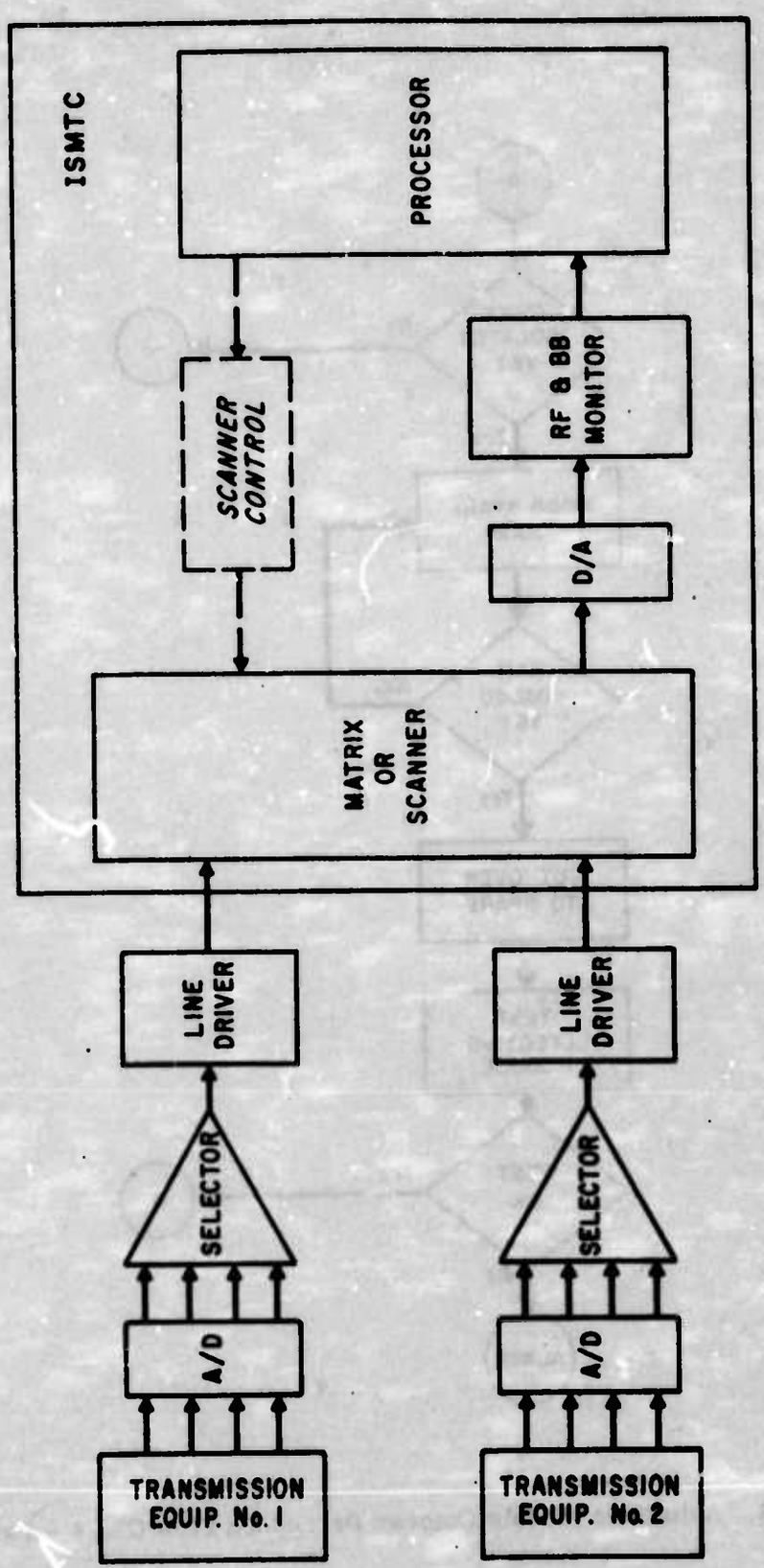



Figure 52. Common Analog Monitoring Equipment Configuration

The impact on the matrix for monitoring technical control analog signals which require bit rates less than 32 kb/s is minimal. This is due to the fact that only one line termination per nodal transmission path is required. However, if the monitoring of wideband signals is desirable, then more than one 32 kb/s matrix line per wideband signal will be required. For example, a signal which requires a two-megabit per second signal rate for three separate transmission paths would occupy approximately 180 terminations (three 60-channel highways). For such an application a separate scanner dedicated to the TC function and capable of handling analog waveforms may be the superior approach.

# 5.0 INTEGRATED SWITCH/MULTIPLEX/TECHNICAL CONTROL

## 5.1 INTRODUCTION

Sections 2.0, 3.0 and 4.0 have discussed the ISMTC from the viewpoints of switching, multiplexing, and technical control, respectively. In this section, system considerations are discussed which do not necessarily apply exclusively to one of these three disciplines but rather are more properly considered as part of an integrated system. Such an integrated system is described in the following section.

## 5.2 ISMTC SYSTEM DESCRIPTION

This section describes the general system design approach developed as a result of this study for the ISMTC. Several techniques utilized in the ICMS report relating to switching and multiplexing concepts have been adapted for use in this report. Only those concepts have been incorporated which are compatible with the expected "ground rules" for the 1980s and which appear to be the most cost-effective approach to satisfying those requirements.

A general block diagram of the ISMTC system is shown in Figure 53. The left-hand portion of the diagram contains equipment composing the switch. The right side of the figure mainly shows the technical control subsystem, transmission equipment, and the input/output subsystems. The figure will be described in greater detail in the paragraphs to follow.

### 5.2.1 Switch Description

#### 5.2.1.1 Switch Operation

The processor controls the operation of the overall equipment complement shown via a stored program. All processor input/output (I/O) control signals pass through the I/O interface.

The Hook Scanner sequentially examines (scans) each subscriber loop to determine which lines are on hook and which are off hook. When a change from on hook to off hook is detected, a dial tone signal from the supervisory Tone Generator (STG) is switched through the matrix to the caller's subset. A Digit Receiver is then connected to the loop to receive the dialing digits. This information is sent to the processor which determines the specific path through the matrix for the call. The Connection Control (CC) unit stores this information and causes the matrix to establish the connection. If the call is not a local one (requires a trunk connection), the Trunk Send Buffer (TSB) and Trunk Receive Buffer (TRB) are used for signaling to the next node via an out-of-band signaling channel. Each of the above equipments are now discussed more fully.

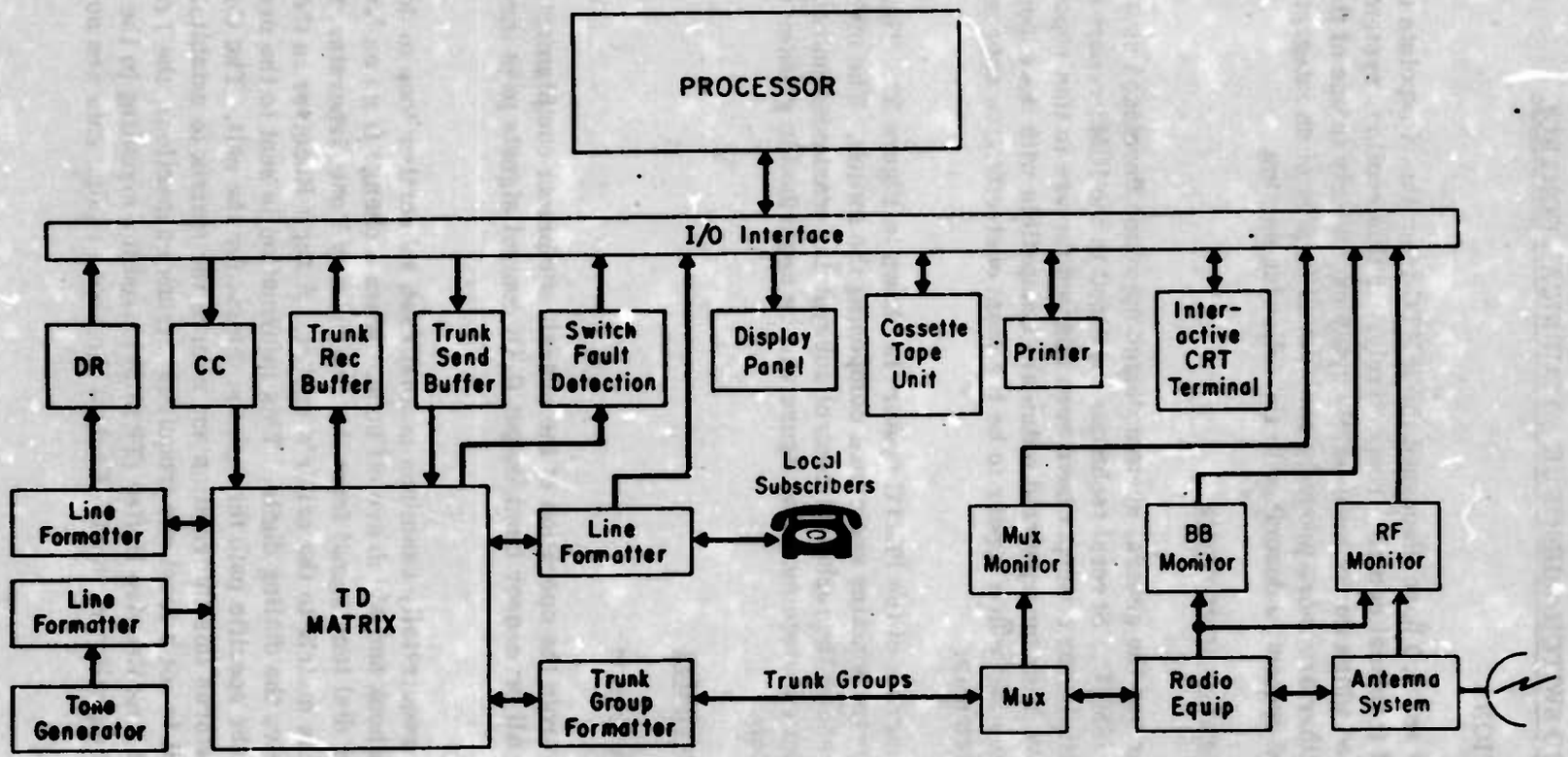



**Figure 53. ISMTC Nodal Configuration Block Diagram**

5.2.1.2 Matrix

A time division matrix capable of switching 32 kb/s channels is shown in Figure 53. The internal TD highways are composed of 60 channels. The matrix may be one of the four types described in paragraph 2.1.2.1. Multiplex equipment is integrated into the input/output portions of the matrix to form trunk subgroups (perhaps 15 or 20 channels). See paragraph 3.2.1 for further details.

5.2.1.3 Connection Control

The CC provides the control bits to the TD matrix for switching any channel input to any channel output. See paragraph 2.2.1.1.2 for further details.

5.2.1.4 Line Formatter and Hook Detector

The line formatter is the interface between a group of subscriber loops and the TD matrix. This unit performs the following functions:

1. Multiplexing/demultiplexing
2. Hook status detection
3. Bit alignment
4. Line termination

The bit alignment function is necessary to permit the multiplexing of the individual subscriber inputs onto a common TD highway entering the matrix (see Figure 54).

The function of the hook detector is to examine the subscriber loops and determine if the received signal is all ones (on hook) or a combination of ones and zeros (off hook). When the hook detector is interrogated by the processor, it transfers the hook status back to the processor. In order to decrease the chances of a status error due to noise bursts or an abnormal percentage of ones during conversation, the scanner should monitor on the order of 100 bits.

Another system constraint imposed is the assumption that each line must be sampled every 200 milliseconds. One hook scanner is capable of scanning sixty 32-kb/s lines every 188 msec. Although it is possible to share one hook scanner with sixty lines, the failure of the formatter would affect all sixty lines. A submultiple of 60 such as 15, 20, or 30 may be more suitable. For the purpose of this report, 20 lines will be assumed to be serviced by one hook scanner. This would permit lines to be scanned every 63 msec and also reduces the matrix interface data rates.

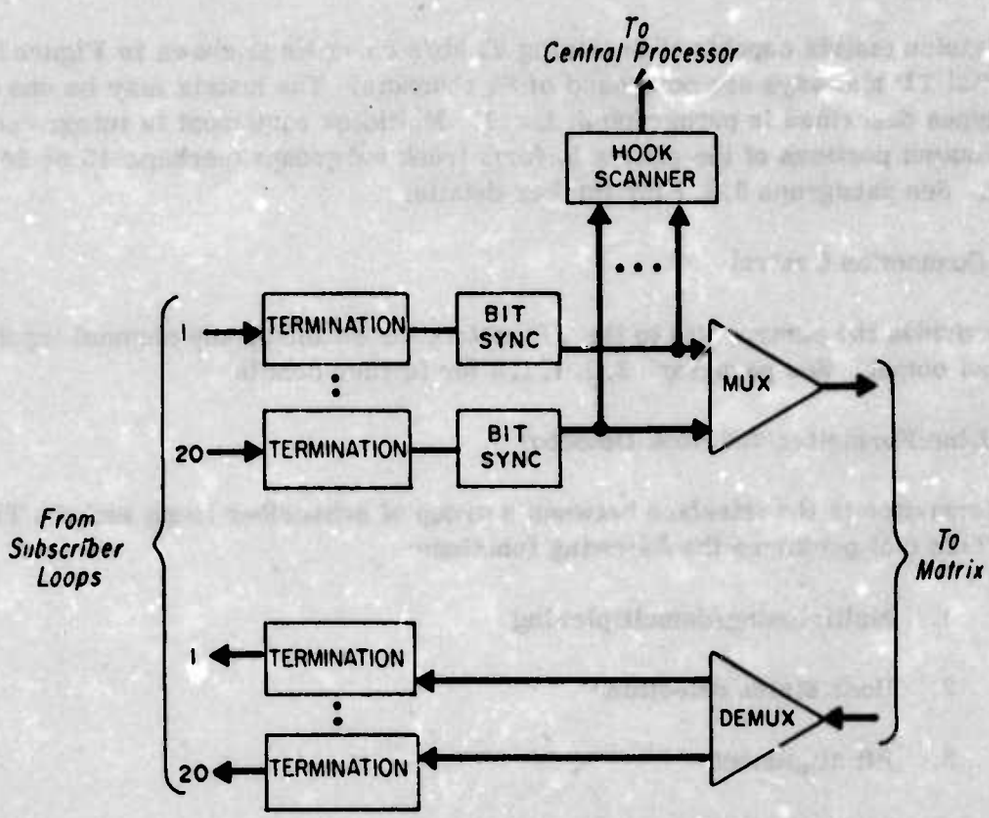



Figure 54. Line Formatter

5.2.1.5 Digit Receiver

The Digit Receiver (DR) detects dial digits transmitted from subscriber loops and forwards the information in binary coded decimal form to the processor one digit at a time. The DR has its own device address and is scanned by the processor at a rate such that no digits are lost. The switch will contain a number of these units to be shared among all of the subscriber loops. This is accomplished by giving each DR a matrix appearance via a line formatter and then using the matrix to switch individual subscribers into an available DR. An insufficient quantity of DRs results in servicing delays. The precise number of DRs required is determined by the allowable delay, service rate, and calling rate.

5.2.1.6 Trunk Group Formatter

The Trunk Group Formatter (TGF) functions are:

1. Input trunk termination
2. Bit and frame alignment
3. Elastic buffering
4. Multiplexing/demultiplexing
5. Extraction and insertion of signaling and supervision information.

5.2.1.7 Trunk Receive Buffer and Trunk Send Buffer

The TRB and TSB are the interfaces which transfer information from the trunk signaling and supervision channel to the processor and vice versa. Within each TDM trunk group, one time slot per frame is reserved for signaling and supervision information. This is called common channel (out-of-band) signaling. This technique is also capable of performing certain orderwire functions (see Section 5.3).

Substantial economy may be obtained by having several trunks share one TRB. This may be achieved by terminating the out-of-band trunk channel on the matrix via a trunk formatter. Thus, the matrix may connect any out-of-band channel to any TRB on a first-come first-served basis. The exact number of TRBs required is dependent on the allowable trunk call holding time and reliability considerations. For example, 60 channels could be serviced by a single TRB and still only occupy less than one percent of the available time. Thus, very little delay is involved due to the contention of 60 channels for a single TRB. Relatively few TRBs would be required even for a 2400-line system. In case of failure an additional TRB should be provided.

5.2.1.8 Supervisory Tone Generator

The STG generates digital waveforms which are switched to selected subscriber loops via the matrix. These digital signals are converted to distinguishable supervisory tones by the subset. The audible tones include ring forward, ring back, busy, dial tone, and an idle pattern. Many subscribers can be connected to the same supervisory tone because of the inherent ability of TD systems to make "one to many" connections.

### 5.2.2 Technical Control Subsystems

The technical control subsystems include:

1. RF and IF Monitoring Equipment
2. Baseband Monitoring Equipment
3. Multiplex Monitoring Equipment
4. Matrix Fault Detection Equipment
5. Orderwire

#### 5.2.2.1 Transmission Equipment Monitors

The RF and IF Monitors will measure vital analog quantities (see paragraph 4.1.1) related to RF, IF, modulator, demodulator, and antenna equipment operation and forward the result in digital form to the processor. Similarly, the baseband monitor will measure various baseband characteristics in order to detect system degradations before significant deterioration of performance occurs.

#### 5.2.2.2 Multiplex/Demultiplex

The multiplex/demultiplex equipment shown in Figure 53 is required only for TDM basebands greater than sixty channels. This is due to the fact that the trunk formatter contains multiplex equipment capable of handling sixty channels as well as certain submultiples of 60. Additional multiplex equipment as well as other signal processing circuits may also be required for user terminals employing rates other than specific multiples of 32 kb/s (see paragraph 3.3).

The TGF multiplex or the external multiplex may be tested by using the Multiplex Monitoring Equipment to monitor the framing pattern. This signal could be monitored at both the TGF and external multiplex outputs and thus isolate faults to either of these equipments. Errors detected by the Multiplex Monitor are transmitted to the processor via the I/O interface.

#### 5.2.2.3 Matrix Fault Detection Equipment

Several schemes for detecting faults within the matrix are discussed in Section 4.5. The first is an out-of-service scheme which requires no external hardware. The other approaches provide in-service testing by utilizing additional hardware to compare matrix inputs and outputs.

5.2.2.4 Orderwire

One 32-kb/s channel of each trunk group is submultiplexed into subchannels to provide certain signaling, supervision, and orderwire functions (see Section 5.3). Continuous reporting from baseband repeater stations may also be handled via these subchannels. However, IF repeaters cannot use such facilities unless special orderwire modulators and demodulators are employed. Alternate methods of providing orderwire facilities at IF or RF repeater stations are discussed in Section 4.2.

5.2.3 Input/Output Subsystems

The I/O subsystems provide the man/machine interface for efficient operation of the ISMTC. These items include:

1. Interactive CRT Display
2. Display Panel (Optional)
3. Low Speed Printer
4. Cassette Tape Unit

These units are described in the following paragraphs.

5.2.3.1 Interactive CRT Display

The interactive CRT display terminal will provide the operator with real-time control of the ISMTC complex. The terminal contains both a keyboard and CRT display. By this means the operator can request the display of specific information not otherwise available. Such a device is useful with respect to operator functions such as:

System Activation/Set-up

Deactivation/Tear-down

Reporting and Recordkeeping

System Reconfiguration

Updating Routing Tables

Updating Fixed and Mobile Directory Information

Dial Assistance

Testing

Coordination

Section 5 6 contains a description of these operator functions.

5.2.3.2 Display Panel

An auxiliary display facility may be desirable from an operational point of view. For example, a display and alarm panel which includes indicators for such ancillary support items as

Prime Power

Environmental System (A/C, heating, and ventilation)

Fire Detection

Security

would be more effective than a CRT display alone. Other switch or TC status items might also be included. Size and power requirements constrain the number of possible display items.

5.2.3.3 Low Speed Printer

Even though the ISMTC may contain real-time displays of current status, it will be necessary to provide hard-copy printouts. A teletypewriter (10-30 characters/sec) will probably be adequate.

5.2.3.4 Cassette Tape Unit

A cassette tape unit is capable of providing the following functions with minimum size and weight requirements.

Program Storage and Loading

Restart

System Recovery

Journaling of Current Configuration

Event Journaling for Performance Evaluation and Statistical Data Gathering

Program Changes (new software)

Ancillary Recordkeeping (TC Reports)

## 5.3 TECHNICAL CONTROL ORDERWIRE

### 5.3.1 Introduction and Definitions

The technical control functions of automatic fault detection, fault isolation, circuit restoral, and reporting and recordkeeping require internodal communication between the processors. In addition, status reporting from remote repeater stations to the applicable node is also required. Much of this traffic is carried by dedicated circuits called orderwires.

The orderwire functions mentioned above may be economically integrated into the ISMTC by utilizing the trunk signaling and supervision facilities inherent in the switch. However, the addition of these technical control orderwire functions may require additional send and receive buffers to serve the orderwire channels. The type, quantity, and control of these buffers is determined in part by the nature of arrival time statistics and the traffic load associated with each orderwire function. For example, reporting may be classified into three broad categories, as described next.

#### 5.3.1.1 Aperiodic Reporting

These reports are provided on an as-required basis. This type of reporting includes reports similar to the Near Real Time (NRT) Report defined as "A report of DCS status required as soon as possible after major or special interest outage, restoral, traffic, or hazardous conditions occur" (Reference 6). Transmissions such as updated routing and class-mark tables are also aperiodic reports.

In addition to the above reports, also included in this category are transmissions permitting automatic fault isolation. When a random fault occurs, the various ISMTC nodes report the detection of this failure to a higher echelon station for fault isolation analysis. Such reports are transmitted in real time and the arrival times are randomly distributed.

#### 5.3.1.2 Periodic Reporting

These reports are prepared by the processor and transmitted on a fixed schedule, as opposed to the random times of aperiodic reports. Included in this category are the following:

1. Periodic Report. A report containing status information on previously reported NRT items and other network and equipment status exceeding established thresholds.

2. End-of-Shift/Day Report. A report containing status information on previously reported NRT or periodic report items and all other reportable information which has not been previously reported in the NRT or periodic reports. These reports are required either near the end of a shift or at the end of a communication day, whichever is directed by the System Control Element and may be combined with a periodic report.

The aforementioned reports may be issued at 1- to 24-hour intervals or possibly even for periods as small as 15 minutes. The contents would be similar to the Maintenance, Status, and Supervisory Reports discussed in Section 4.4.

5.3.1.3 Continuous Reporting

This term is defined here to mean the transmission of processed or unprocessed data which reflects current system performance and status on a "minute-by-minute" basis. Such reporting is usually required at 1- to 10-minute intervals.

Continuous reporting between the local processor and system control will contain current switch status and traffic information.

5.3.2 Orderwire Description

5.3.2.1 Out-of-Band Signaling and Supervision

Although many present day analog military switching systems use in-band trunk signaling and supervision techniques, using a dedicated channel (i.e., common channel) in a digital trunk group for the purpose of signaling and supervision has significant advantages. The former techniques are generally based on using tone signaling and supervision within 4-kHz FDM derived channels. An all digital network using TDM, however, requires different considerations. Discrete analog tone signaling is not applicable and the use of digital signaling and supervision is necessary. In this case, the out-of-band approach requires signaling and supervision equipment for the common signaling channel only and, as a result, is the more cost-effective approach for interswitch signaling.

Furthermore, a significant difference exists between in-band and out-of-band signaling and supervision with respect to preemption. Since the in-band techniques use the same channel for both signaling and information, an idle channel must be available before signaling can take place. In order to make a channel available when all channels are busy, a routine call must be preempted. Call disruption takes place even though the priority call may still fail if the called user is busy on another call of equal priority. With out-of-band signaling, preeemption is not effected until it has been established that a call can be completed.

Out-of-band signaling and supervision (i.e., common channel signaling) is the favored approach for the ISMTC.

5.3.2.2 Submultiplexed Channels

One 32-kb/s channel in each 60-channel trunk group is dedicated to the orderwire function and this channel would provide a subchannel for interswitch signaling and supervision. The orderwire channel can be submultiplexed to provide four 8-kb/s subchannels containing the following information:

Framing

Error protection

Signaling and supervision

Routing information

Aperiodic reporting

Periodic reporting

Continuous reporting

Figure 55 illustrates an orderwire subchannel assignment scheme.

Subchannel 1 carries the framing and error protection coding. Subchannel 2 is dedicated to the transmission of remote status reporting. Subchannel 3 contains Signaling and Supervision (S&S) including the signaling required by the routing scheme. Subchannel 4 provides a communication channel for interchanges between the ISMTC node and the System Control (SC) and System Planning and Engineering (SP&E) Elements including the required continuous reports. Some aperiodic and periodic reporting is handled on a dial-up basis. Further details on the handling of the various functions are contained in paragraph 5.3.3.

5.3.2.3 Block Diagram

Figure 56 contains a block diagram of the ISMTC orderwire and S&S system. The trunk groups from other ISMTC nodes are shown entering at the right. One 32-kb/s channel in each trunk group is submultiplexed into four subchannels as shown in Figure 55. The framing (subchannel 1) information for each trunk group is extracted in the TGF.

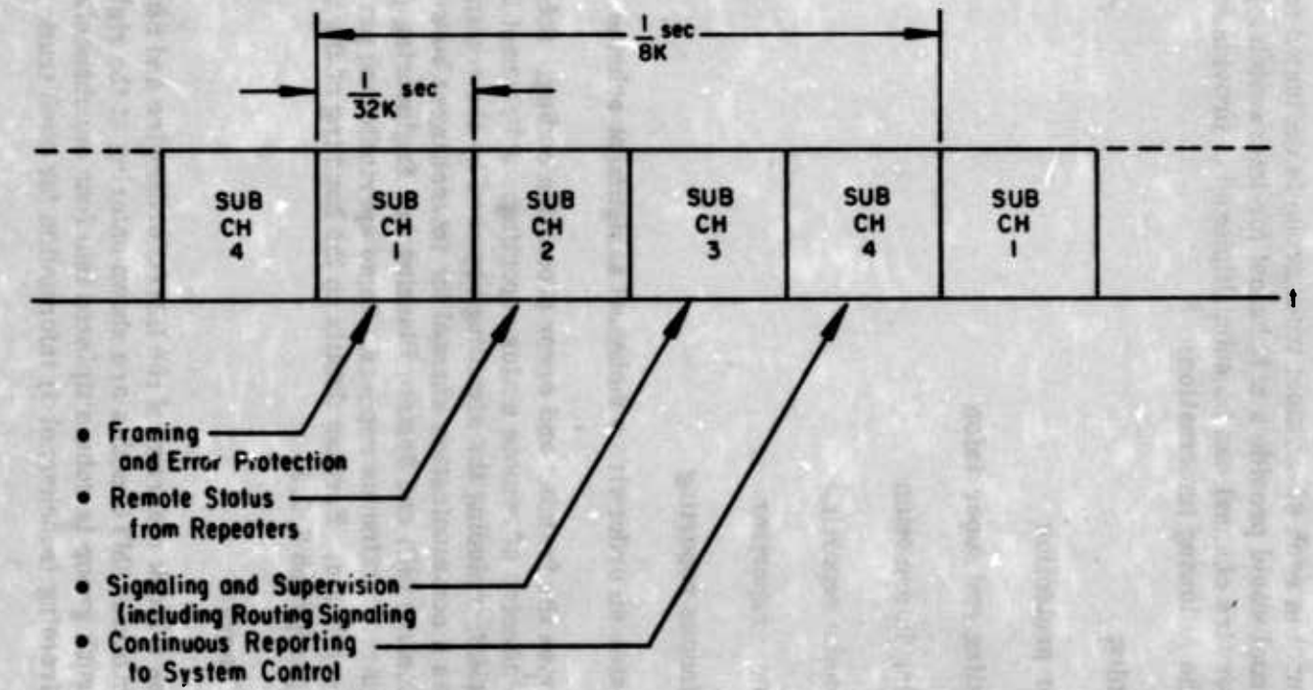



**Figure 55. Orderwire Subchannel Assignments**

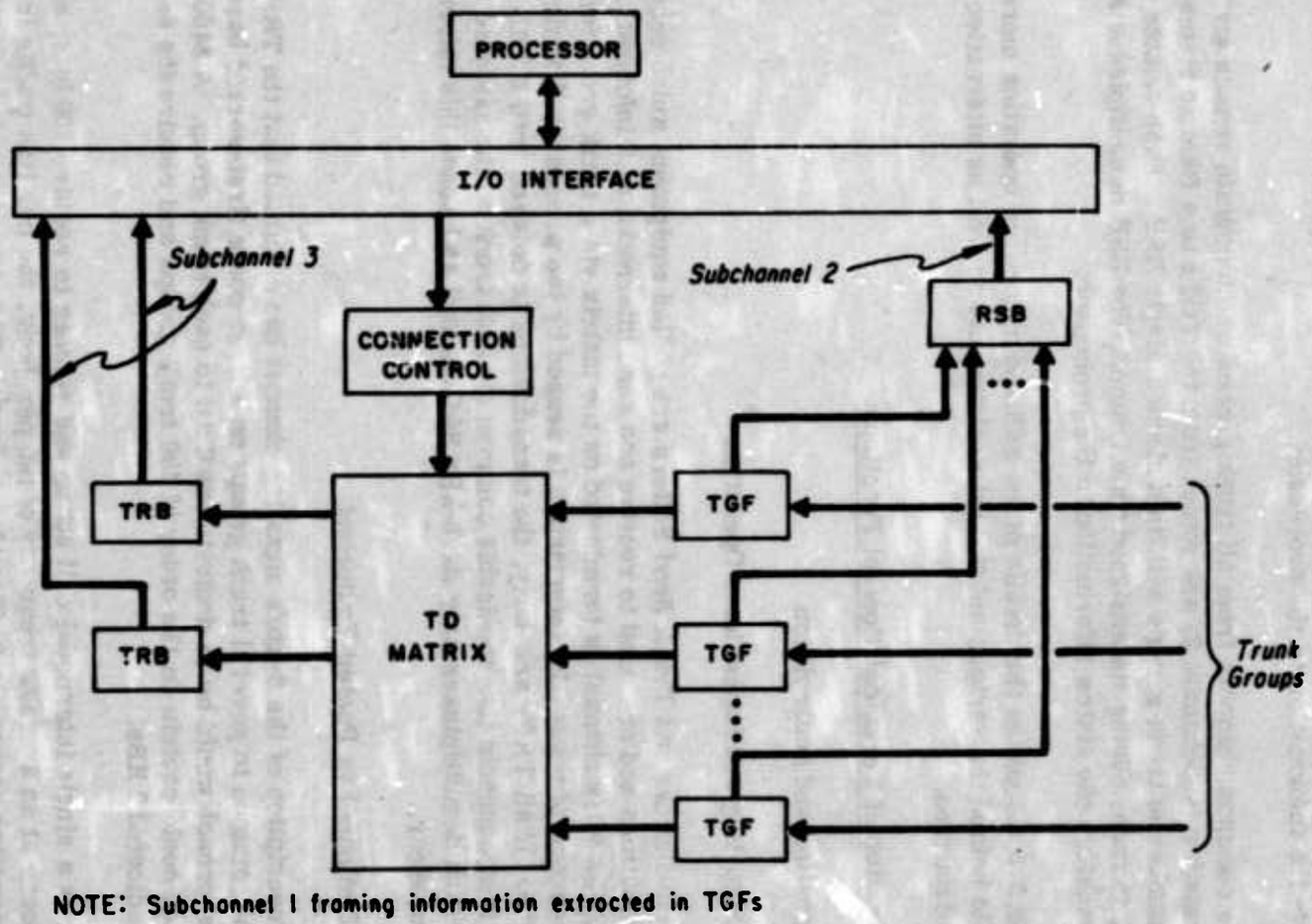



Figure 56. Orderwire Block Diagram

When the processor is informed by the TGF that subchannel 3 contains information, the matrix creates a path from the applicable TGF to an available TRB. The TRBs are pooled equipment and shared by all TGFs on a first-come first-served basis. All four subchannels (still multiplexed as a 32 kb/s channel) are routed via the matrix to the applicable TRB. The TRB then demultiplexes the channel to yield subchannel 3 and forwards the information to the processor.

The 32-kb/s common channels from all trunk groups which contain remote station status information (subchannel 2) are routed from the TGFs to a Remote Status Buffer (RSB). A number of trunk groups will time share a single RSB. Each remote station will report, in turn, during its assigned time frame. The RSB demultiplexes subchannel 2 and transfers the status information to the processor.

Paragraph 5.3.3 discusses the details of the S&S and orderwire operation more fully. The rationale behind the various subchannel assignments as well as alternative techniques are discussed.

5.3.3 Integration of Technical Control Functions

5.3.3.1 Signaling and Supervision

5.3.3.1.1 Signaling and Supervision Operation

Trunk Receive Buffers and Trunk Send Buffers are pooled equipment which occupy matrix terminations and are used to receive and send internodal S&S information. The incoming S&S 32-kb/s channel is terminated on the matrix via a trunk group formatter. When the presence of trunk S&S information is sensed by the processor it assigns an available TRB. If all TRBs are busy, the transmission is delayed until a TRB is free. The matrix then connects the applicable common channel trunk to the assigned TRB. The TRB in turn demultiplexes only the 8-kHz S&S channel and sends this information on to the processor.

5.3.3.1.2 Dedicated vs Pooled Equipment

The above description of the 8-kb/s signaling channel has assumed that the TRBs will be equipment common to several trunk groups on a first-come first-served basis. An alternative approach would be to dedicate one TRB to each trunk group. A 2400-line tandem switch could contain on the order of 100 trunk groups and require the same number of dedicated TRBs.

If one assumes a single internodal call set up and release to require 600 bits, and such calls occur at an average frequency of ten per hour, the per line traffic load on the 8-kb/s signaling channel is $2.08 \times 10^{-4}$ Erlangs. This is extremely light loading and therefore the contention of many lines for the same TRB would produce only occasional delays. For example, 60 lines would produce a traffic load of $1.25 \times 10^{-2}$

Erlangs and, therefore, one TRB could service 60 lines with a small delay. Several TRBs could accommodate all 2400 lines. The precise delay is a function of the number of program modules associated with each call and their corresponding execution times.

Trunk Receive Buffer failures are easily handled with pooled equipment. First it should be noted that existing calls are unaffected by TRB failures; only the ability to set up new calls is lost. Once a failure is detected, the processor merely reroutes all future trunk signaling information to other TRBs. Thus operation is carried on in a slightly degraded manner until replacement or repair is made.

It is clear from the above analysis that pooling of the TRBs for the signaling subchannel is the favored approach.

5.3.3.2 Continuous Reporting to System Control

Continuous reporting to the SC and SP&E Elements is handled on a 8 kb/s subchannel. In addition, this subchannel provides the means for the SC and SP&E Element to send reconfiguration information to the ISMTC nodes. The amount of traffic anticipated for this subchannel indicates that it would be lightly loaded.

5.3.3.3 Periodic and Aperiodic Reporting

Periodic reports occur at regularly spaced but infrequent time intervals for short periods. One possible transmission scheme would be to dedicate the periodic reporting function its own 8-kHz subchannel. However, this would be wasteful since the subchannel would not be in continuous use. A more economical approach would be to have the processor "dial up" system control when required. The same technique could be used to transmit aperiodic reports.

5.3.3.4 Remote Status Reporting

This paragraph considers the transmission of status information from repeater station to ISMTC nodes. The problem differs considerably from the functions already discussed in this section. First the transmission may not be processor controlled. Secondly, the arrival time statistics are not random if a periodic status reporting scheme is used. Such information is provided at frequent intervals and is allocated to subchannel 2.

An important consideration is how to economically interface the subchannels from the various trunk groups with the processor. Several alternatives include:

Continuous Reporting

Time Slot Reporting

Polled System

Reporting by Exception

In a continucus reporting system each remote station reports the status of its test points continuously and automatically over a dedicated facility. Reporting may be performed at a rapid rate since the transmission facilities are not time shared with other remote stations. Only one-way transmission is required, thus providing increased reliability. The disadvantage of such an approach is that a receive buffer is required for each trunk group from a remote station. Such buffers may be built into the TGFs; also processor activity is constantly required.

For time slot reporting a group of remote stations time share a single receive buffer. Each station is allotted a time slot in which to report. This is done sequentially. Of course, such a system requires occasional synchronization of all remote station clocks and two-way transmission is required. Reliability is not significantly compromised here even if the synchronization path should fail. The system timing stability would keep the system running satisfactorily until repairs are made. This reporting technique is economical for ISMTC stations accepting transmissions from a large number of remote repeaters, each providing low traffic levels of status and fault information. This scheme has the same disadvantages as the above method, however, in that considerable processor activity is required.

Polling refers to the method of operation where the ISMTC sends a request to each remote station sequentially to report its status. This type of operation requires a two-way transmission and, therefore, has the disadvantage of being disabled if transmission in either direction is lost. In addition, increased load on the processor is incurred by the requirement to control the polling process and, therefore, this technique may not be desirable for this application.

Reporting by exception is still another means of providing remote status information to the ISMTC processor. In this case, the processor would retain the monitored status condition last reported from the remote station until updated. This method has the least impact on required processor activity; however, it has the disadvantage that a system failure which disrupts the orderwire channel (e.g., communication link down or repeater station destroyed) prevents the receiving of status information. Another disadvantage of this scheme is that additional processing hardware is required at each remote site.

#### 5.3.3.5 Impact on Switch

The impact on the switch matrix due to the integration of orderwire facilities into the ISMTC is small. The major orderwire impact upon switch design will be on the processor.

The most significant problems are associated with the processing of continuous reports from remote repeater stations. In order to estimate the traffic load from these repeater sites it is assumed that 25 points will be monitored and the results for each monitored point are transmitted to the ISMTC node as an 8-bit character. This yields a total of 200 bits from each repeater site. Assuming a maximum of eight repeater stations per 2400-line node and a reporting period of one minute, a total data rate of about 30 b/s will result. The processing of this type of data requires a relatively small number of instructions and, therefore, it is anticipated that the work load on the processor imposed by remote monitoring will be small.

## 5.4 PROCESSOR REQUIREMENTS

### 5.4.1 Introduction

This section describes the processor requirements entailed in implementing the integrated switch/multiplex/technical control. Program description and sizing estimates are presented for a baseline system for several different switch sizes. No specific processor(s) has been recommended, but a section on desirable processor characteristics is included as well as a survey of typical minicomputers suitable for this application. In general, the conclusion reached from studying the various requirements indicates that current processor technology is capable of fully supporting the ISMTC. In fact, the risks involved in configuring a processor system from the operational characteristics viewpoint appear to be low. More risk appears in satisfying the stringent environmental and tactical specification.

The approach taken in analyzing the program requirements for the integrated system involved splitting the requirements into two functional groups. The first group contains those functions traditionally performed by a circuit switch/multiplexer, including internal switch monitoring, switch fault isolation, and switch recovery. These last functions are inherently closely related to the standard switching functions; hence they are considered together. The second functional group includes the category of technical control functions, which at present are performed apart from the switch. These include circuit monitoring, equipment monitoring, report generation, and so on.

Based on these function groups, two programs have been considered--a Switch Control Program and a Technical Control Program.

Those aspects of switch control entailing fault detection and isolation within the switch, automatic switch recovery, alternate routing, and the like are considered in the Switch

Control Program. This program delineation is made to highlight those additional processor requirements which result from integrating the technical control functions that traditionally have been performed independently of the switch and multiplex functions.

Technical control includes the detection and isolation of system faults and the necessary command and control required to optimize system availability and performance. More specifically, the technical control requirement includes monitoring of communication lines and the associated communication equipments and coordinating the various monitored data to assure maintenance of system quality. The concern here is primarily with the transmission equipment and only a limited part of the switch/multiplex subsystem, such as environmental (temperature, power levels, etc.) factors. As discussed in detail elsewhere, the overall TCCF concept is composed of four elements. The elements directly affected by integrating technical control and the switch/multiplexing functions are the Node Control and Equipment Support elements. System Planning and Engineering and System Control are performed at a specialized control point and interface with the node switches by means of data exchange on the orderwire channel.

Figure 57 shows the information flow required to support the integrated switch. The ISMTC complex is shown in the dotted box. There are three components shown including a control element, switching functions, and technical control functions. The interfacing between the components can be considered as that information flow required to coordinate and control node activities. The links to the System Control Element and other switching nodes are numbered 1 and 2, respectively. These links are common out-of-band channels. Besides carrying TC data, the S&S information required for circuit switching is normally sent on this channel as discussed in the previous section. It is also necessary to monitor remote repeaters. The monitored data are multiplexed onto an orderwire channel as shown by link 5.

The ISMTC has been shown as distinct elements in order to emphasize that, to perform properly, it is necessary that only certain information be exchanged between the functional elements. The switching control function need not be aware of much of what the TC function is doing and vice versa. The actual information transfer required is very small compared to the internal processing load. Thus, it is possible to consider performing TC processing in a separate processor. If a separate processor (or processors) were employed to perform the bulk of TC processing, and a satisfactory data interface is used to transfer the necessary control information, then the feasibility of integration would not depend on one processor being able to meet the memory and execution speed demands of both functions. A federated computer complex or multiprocessor may be considered to meet the desired objectives, although there may be disadvantages to such an approach. An additional processor to support technical control would impact on system complexity and the stringent limitations imposed by tactical deployment considerations.

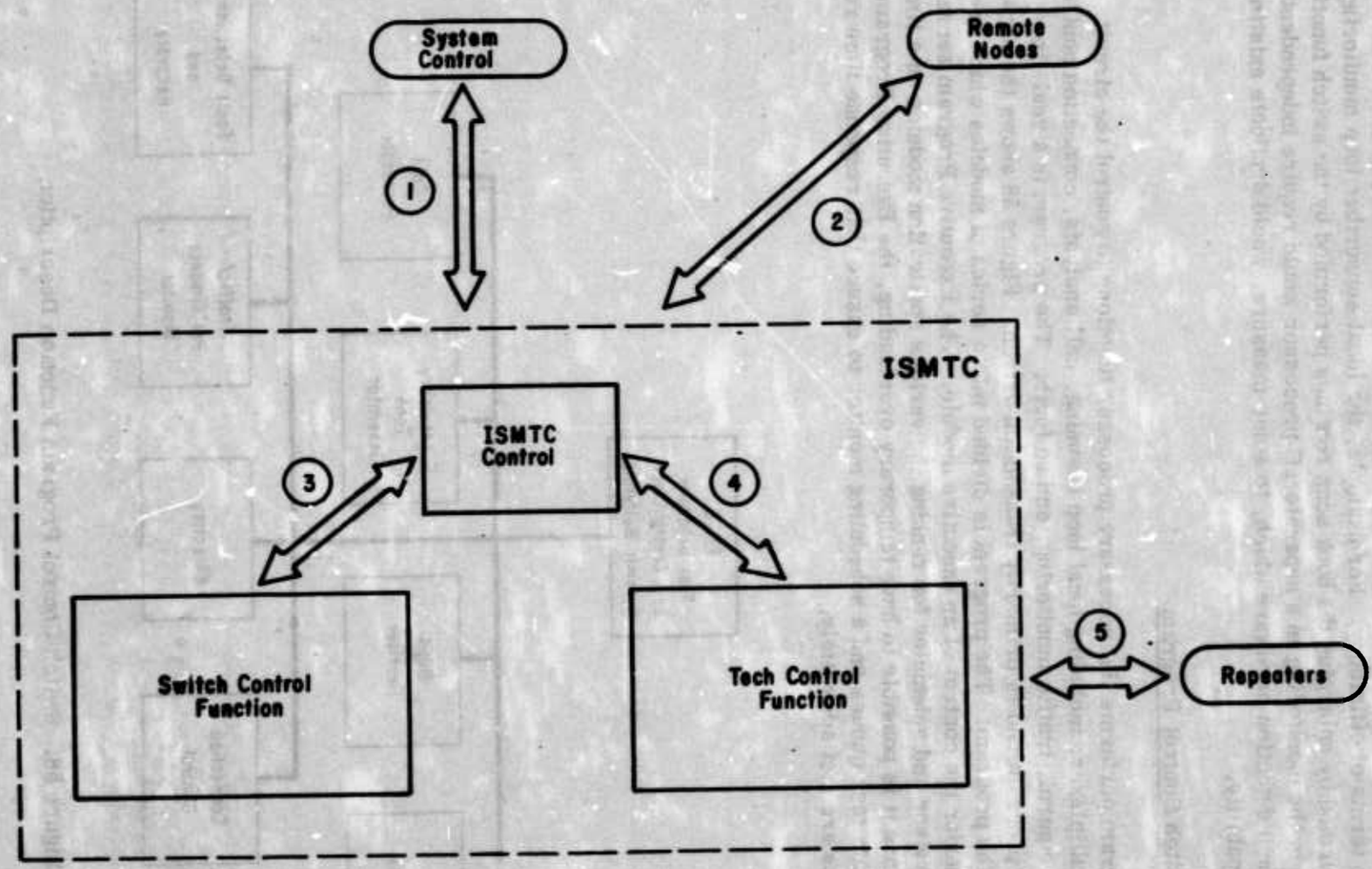



Figure 57. Control Information Flow

In addition, there does exist a certain portion of the TC function which is so closely interrelated with the switch function that separating the processing might incur some penalty in terms of efficiency. For example, the local subscriber loop monitoring is best performed by enlarging the hook scan routines performed by the switch function. To perform the monitoring in a separate TC processor would require independent line scanning and detection hardware which, to some measure, would duplicate existing switch capability.

### 5.4.2 Switch Control Program

This program performs the necessary processor functions to control the circuit switch/multiplexer, including local loop scanning, call analysis, connection control, directory control, traffic monitoring, and so forth. The program is a real-time dedicated program and is primarily transaction driven. Figure 58 shows the organization of the program. The program is divided into a series of modules which are executed under the control of an executive module. The Executive Program serves as a supervisor and scheduler for running the various application modules on a timely basis. Since it is possible to have temporary overloading, the Executive Program must contain task queues and a scheduling monitor to ensure that response time requirements are met adequately.

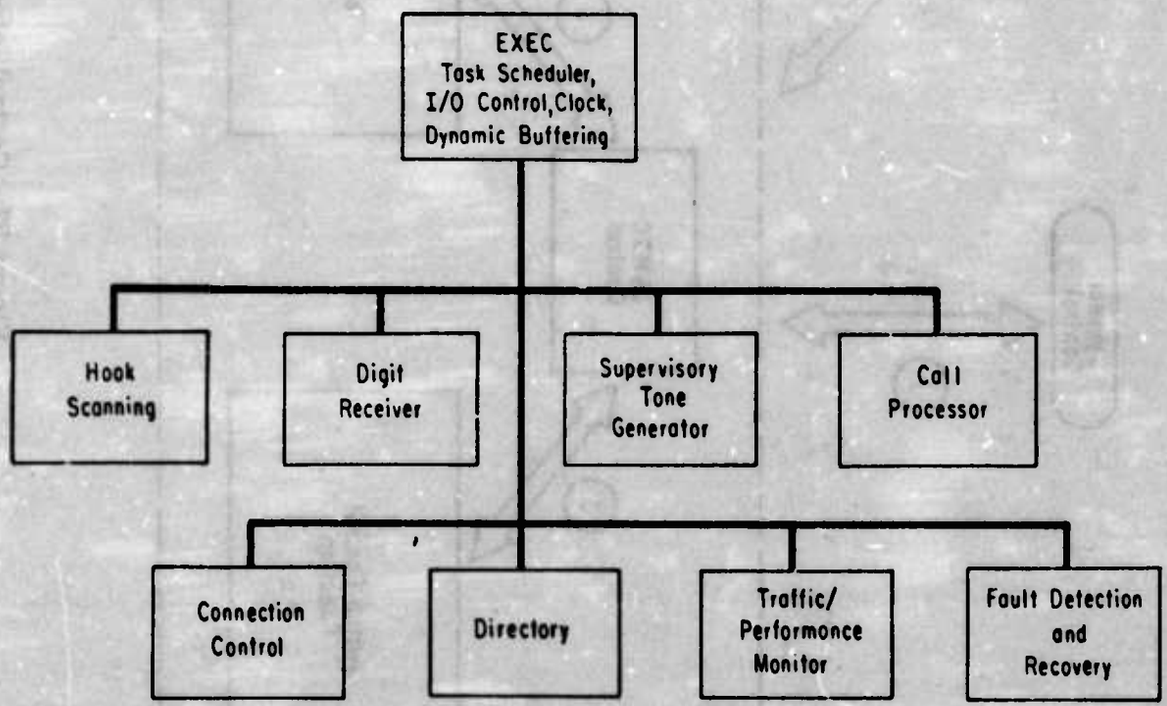



Figure 58. Switch Control Program Function Description

The Executive Program also contains an I/O control program to service I/O channels. Due to the extensive and diverse I/O which the processor is controlling, a multi-level interrupt priority system is advisable, including vectored interrupt addressing. The interrupt service routines are considered to be the foreground or immediate processing units, while the application modules operate in the background or deferred mode.

Essential to the Executive Program is a clock routine, which processes timeouts to schedule tasks on time and to detect malfunctions. For this purpose an interval timer on the order of 100 Hz is required.

Table 8 shows sizing and loading estimates for the Switch Control Program. The estimates are made for four switch sizes: 300, 600, 1200, and 2400 lines. The sizing is done in number of processor words, assuming a 16-bit word size. The loading estimates are based on a baseline worst case traffic loading. Traffic loads will be less than or equal to the following values 99.9 percent of the time.

| Switch Lines | Worst Case Load (Calls/Sec) |
|---|---|
| 300 | 6 |
| 600 | 9 |
| 1200 | 12 |
| 2400 | 19 |

The loading is in thousands of operations per second (K ops).

5.4.2.1 Digit Receiver Module

This module controls the receiving of the keyed digit information from the local subscriber after the subscriber has been connected. It has direct control of the DR units which are connected to the subscriber dialing in. The actual digits are buffered by the DR which interrupts the processor. The digits are inputted and checked for validity and assembled into complete numbers. When an entire number has been received, it is passed on to the Call Processor Module and the DR is released.

5.4.2.2 Supervisory Signal Generator Control Module

This module controls the operation of the Supervisory Signal Generator (SSG). As requested by other modules, the SSG module "connects" the required S&S signal to the desired subscriber lines. These signals include ring forward, ring back, busy, dial tone, and idle.

Table 8. Switch Control Program - Sizing Estimates

| Program Title | Switch Size (No. of Lines) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 300 | | 600 | | 1200 | | 2400 | |
| | A | B | A | B | A | B | A | B |
| Switch Executive | 3 | 20 | 3.0 | 24 | 3.5 | 28 | 4.0 | 40 |
| Hook Scanning | 1 | 10 | 1.5 | 15 | 2.0 | 20 | 2.5 | 30 |
| Digit Receiver | 1 | 5 | 1.0 | 7 | 1.5 | 10 | 2.0 | 14 |
| Supervisory Tone Generator | 1 | 5 | 1.0 | 7 | 1.5 | 10 | 2.0 | 14 |
| Call Processor | 6 | 35 | 8.0 | 50 | 10.0 | 65 | 12.0 | 100 |
| Connection Control | 2 | 10 | 2.0 | 15 | 3.0 | 20 | 3.0 | 30 |
| Directory | 10 | 55 | 12.0 | 60 | 16.0 | 100 | 24.0 | 160 |
| Traffic/Performance Monitor | 2 | 10 | 2.5 | 14 | 3.0 | 20 | 4.0 | 30 |
| Fault Detection/Recovery | 2 | 15 | 2.5 | 24 | 3.0 | 40 | 3.0 | 60 |
| Buffer Area | 4 | - | 6.0 | - | 8.0 | - | 12.0 | - |
| TOTAL | 32 | 165 | 39.5 | 216 | 51.5 | 313 | 68.5 | 478 |

Column A = Number of Instructions (in thousands)

Column B = Number of Operations/Second (in thousands)

Word Size = 16 bits

#### 5.4.2.3 Call Processor Module

This module controls the processing of both local and foreign (introduced from a remote exchange) calls. The type of call, including requests for special services, is determined. Call routing information is received from the other modules in order to complete the call. The routing algorithm (e.g., saturation, quick trace, deterministic, fixed, etc.) is called upon to establish a call route. The required information necessary to connect the call to a local subscriber or relay the call to another switch is transferred to the Connection Control Module.

#### 5.4.2.4 Connection Control Module

This module controls the switch connection configuration. One method used to implement this function is to maintain an internal table to reflect the current state of the switching matrix. As requests for connection and releases are received, the appropriate commands are outputted to the CC unit. When a connection request is made, a search is made through the internal table to determine if any available paths through the matrix exist. If so, the path is established. If the switch matrix is blocked, the Call Processor Module is flagged to check priority and determine whether another call should be preempted. This procedure is unnecessary if a nonblocking switching matrix is employed. A cost and size penalty is incurred, however, if a completely nonblocking design is used.

#### 5.4.2.5 Directory Module

This module maintains the local directory and can also maintain a remote user directory if required. When a call request is received, the local directory is searched to determine if the subscriber is local. If so, the Executive Program is signaled and the subscriber data are transferred to the CC Module. If establishing the call requires the use of interswitch trunking, the routing procedure is activated to determine a best route between the originating node and the terminating node. When the subscriber is found, the node information is sent to the Call Processor. This module also handles directory updates and specialized directory features.

#### 5.4.2.6 Traffic/Performance Monitor Module

This module monitors the switch operation to record pertinent traffic and performance statistics. This is essentially a technical control function but is better built into the Switch Control Program because the necessary data are readily available at the switch control point. The data to be monitored include call loading, holding times, distribution of types of calls, and amount of blocking. These statistics are updated at a regular interval, but at a low priority to the processor.

5.4.2.7 Fault Detection and Recovery Module

This module monitors internal switch performance. Switching paths through the matrix are continually tested. As faults are detected, diagnostic and error recovery routines are brought into action. If possible, spare modules will be switched in automatically or, at a minimum, maintenance personnel will be alerted.

## 5.4.3 Technical Control Program

This section describes the function performed by the technical control software. The program is similar to the Switch Control Program in that it is a real-time dedicated program. The executive structure is expected to be the same as for the switch program. Figure 59 shows the program organization. Following is a description of the modules and sizing estimates.

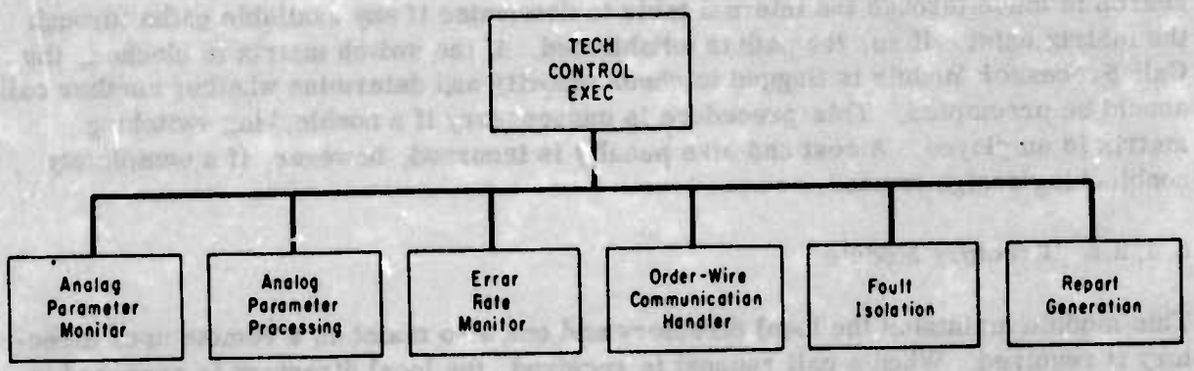



Figure 59. Technical Control Program Function Description

5.4.3.1 Analog Parameter Monitor Module

This module monitors analog parameters (e.g., RSL) to detect abnormal conditions. The points may either be scanned periodically or report in a fault interrupt mode. The former implies significantly more processing, while the latter implies additional outboard hardware, including threshold detectors and so forth. The program monitors each selected analog level to determine one of three states: satisfactory, marginal, or failure. This implies two thresholds per monitored point.

1. Scan Method

For the purposes of this analysis several assumptions must be made pertaining to the ISMTC nodal transmission configuration. Since it is unlikely for a node to possess more than about eight links, this number will be used as a worst case value. It is further assumed that these transmission paths are equally divided between dual and non-diversity links. The combination of these two assumptions should be sufficiently pessimistic to accommodate virtually all cases.

Non-diversity links require about 11 monitor points while a dual diversity configuration yields 15 such points. Thus, an average of 13 monitor points per link is assumed. This amounts to 104 points per 2400-line node. Approximately 200 instructions are required to scan each point and detect a threshold. This implies a scanning processing load of about 20,000 instructions per second.

2. Interrupt Method

Actual threshold crossing detection is performed by outboard hardware. The processor is interrupted only when status changes. The processing load, therefore, is a function of failure rate which should be much lower than the load imposed by the scanning technique. Average load would be nearly zero, while for short peak periods the maximum load would be approximately 1000 instructions per second.

5.4.3.2 Analog Parameter Processor Module

This module processes the output of the Analog Parameter Module. While the monitor program is required only to determine the current level of each of the monitored points, this processing module must maintain the overall status of the analog points. This requires that the monitor point level data be integrated into a status table. The status of each point would be broken down to the three measurement levels and, in addition, would contain an in-service/out-of-service indication and, perhaps, the time(s) of the recent changes.

The module would operate at fairly low priority. During normal trouble-free operation the processing load would be minimal but, as status changed (e.g., circuits failing), the load would increase significantly.

5.4.3.3 Error Rate Monitor Module

This module would measure the error rate performance of the orderwires and idle channels to monitor the inter-switch circuit quality. It is assumed that continual monitoring

of each of the orderwire channels is necessary. Periodic scanning of the idle channels is sufficient in order to detect gradual degradation. For program sizing estimates it has been assumed that each trunk group is measured constantly.

The primary objective is to find bit error rates on the 32 kb/s trunks. The bit error performance would be divided into several levels from near error free to unacceptable. In addition, limited P (m, n ) and burst error statistics might be taken.

The actual implementation has significant hardware/software tradeoff consideration. Due to the high total data rate of the channels to be monitored at any one time and the other tasks the processor must perform, a hardware approach is considered more viable. This could consist of outboard comparators and counters which would measure the number of errors occurring. The error counts are then gated to the processor. The module maintains the bit error rate over the different channels and checks for the error rate exceeding threshold.

5.4.3.4 Orderwire Communication Module

This module controls the orderwire communications in order to receive TC and signaling data from other switch nodes and from remote repeater sites. The information rate is expected to be low, indicating that this module would be lightly loaded.

5.4.3.5 Fault Isolation Module

This module processes the data from the other modules to determine, if possible, where faults are occurring and which equipment, system, or subsystem has failed. A failure matrix is maintained indicating most probable equipment affected for the particular data received. All data including analog parameters and error rates are used to isolate failures. In addition, this module must flag the Report Generation Module as failures are detected.

5.4.3.6 Report Generation Module

The Report Generator Module formats and sends the TC reports to the local operator's console and to the System Control Element over an orderwire. These reports include maintenance reports, status reports, and supervisory reports. The formats of these reports should be kept as concise as possible to minimize memory requirements. The reports are generated periodically and aperiodically, but at a low priority.

Table 9 shows sizing and loading estimates for the Technical Control Program. Program sizes are in processor words, assuming a 16-bit word size, while the processor load estimate is in thousands of operations per second. It should be noted that only TC programs are listed. Programs normally associated with the switching function including fault detection and isolation within the switch, automatic switch recovery, and

Table 9. Technical Control Program - Sizing Estimates

| Program Title | Switch Size (No. of Lines) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 300 | | 600 | | 1200 | | 2400 | |
| | A | B | A | B | A | B | A | B |
| Tech Control Executive | 2.0 | 20 | 2.0 | 24 | 2.5 | 28 | 3 | 40 |
| Analog Parameter Monitor | | | | | | | | |
| (1) Software | 1.5 | 9 | 2.0 | 11 | 2.5 | 16 | 4 | 26 |
| (2) Hardware | 1.0 | 4 | 1.2 | 6 | 1.4 | 10 | 2 | 20 |
| Analog Parameter Processing | 4.0 | 16 | 4.0 | 20 | 5.0 | 28 | 6 | 40 |
| Error Rate Monitor | 2.0 | 10 | 2.5 | 15 | 3.0 | 25 | 4 | 50 |
| Orderwire Communication Handler | 3.0 | 6 | 3.0 | 8 | 4.0 | 10 | 4 | 12 |
| Fault Isolation | 5.0 | 20 | 6.0 | 30 | 8.0 | 50 | 10 | 80 |
| Report Generation | 8.0 | 10 | 8.0 | 15 | 10.0 | 30 | 12 | 60 |
| Buffer Area | 2.0 | - | 3.0 | - | 6.0 | - | 12 | - |
| TOTAL | 27.0 | 86 | 29.7 | 118 | 39.9 | 181 | 53 | 302 |

Column A = Number of Instructions (in thousands)

Column B = Number of Operations/Second (in thousands)

Word Size = 16 bits

alternate routing are considered in Table 8. Note that two alternative programs are listed under the Analog Parameter Monitoring category, one a hardware and the other a software approach to monitoring. Only the program requirements pertaining to the hardware approach are included in the totals at the bottom of Table 8.

### 5.4.4 Processor Characteristics

This section describes the desirable characteristics of an ISMTC processor. In general, the existing technology can and does produce processors with these characteristics (see Table 10). To support the wide range of functions a general-purpose digital computer with a communication-oriented instruction set is needed. The processor should have extensive and rapid bit and byte manipulation capability but need not have high speed double precision floating point and other such number manipulation capability. A uniprocessor architecture appears adequate but the processor probably needs high speed scratch pad memory and a microprogramming capability.

#### 5.4.4.1 Machine Cycle Time

In order to obtain an upper limit on the switch processing requirements, Table 8 was prepared on the basis of a worst case analysis. The estimates are traffic dependent and the baseline traffic loads were chosen such that the results would be valid 99.9 percent of the time. If the switching functions were accommodated in a single processor, separate from the TC functions, a 2-microsecond machine cycle time would be adequate for a 2400-line switch.

Another approach to the estimation of required machine speed is the consideration of call processing times. The effect of processor overloads, due to high traffic, manifests itself as delays in call processing. Thus, it is these delays which are one of the criteria by which switch performance is ultimately judged. Therefore, in the following paragraphs the processor delays are calculated as a function of average processor utilization.

Relatively simple instructions are required for switch control processing and, therefore, the execution time for most instructions is governed by the maximum rate at which the program and/or data memories can be accessed (cycles). For example, if call intervals were to occur uniformly spaced in time, a 1-microsecond cycle time would permit a processing workload of one million operations per second. However, this assumption pertaining to the call arrival time distribution does not represent a realistic situation. In fact, it is well known that the number of call arrivals within a specified time interval displays random variations. More specifically, the probability distribution is exponential (Poisson). Thus, momentary fluctuations in the call arrival rate will overload a processor designed to accommodate only a slightly greater than average load. The result would be intolerable delays in call processing. Thus, for a given average processor load a machine cycle time must be chosen to provide adequate margin

against statistical processor load variations. This is a problem in queuing theory for which a simple model is postulated in the following paragraphs. The solution provides some guidance as to the permissible processor loadings and therefore the required cycle time.

5.4.4.1.1 Queuing Model

The Queuing Model is the single exponential channel illustrated in Figure 60. Incoming calls shown entering from the left are processed in the single processor represented by the box at the right side of the figure. The call arrival distribution is assumed to be exponential in time. The average call arrival rate is $\lambda$ calls per second. The service rate, $\mu$, is the average number of calls which are processed per second. The service completion distribution is also assumed to be exponential which is a good approximation to the actual situation. The queue is considered to be infinite in possible length; that is, no calls are lost.

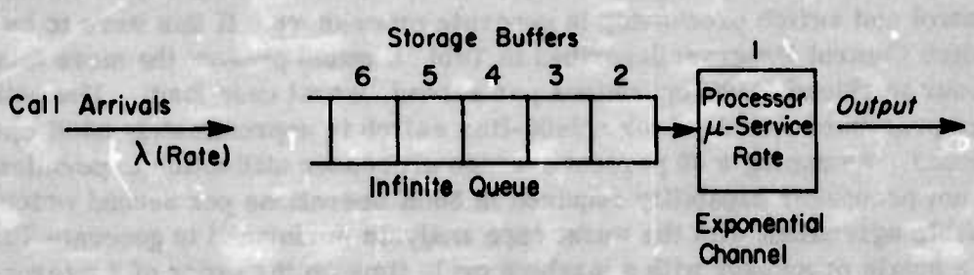



Figure 60. Queuing Model

5.4.4.1.2 Call Processing Delays

The average number of calls in queue $L_q$ is given by Morse (Reference 7) to be:

$$L_q = \frac{\rho^2}{1-\rho} \qquad (1)$$

where $\rho = \frac{\lambda}{\mu}$

Here the physical significance of $\rho$ is the average processor utilization. For example, when the average arrival rate equals the average call service rate, the processor is fully loaded and $\rho = 1$. Therefore, only the case for $\rho$ between zero and one is considered here.

The average processing service delay per call, D, is defined as the time spent in queue, $L_q/\lambda$, plus the actual time required to process the call, $1/\mu$. Therefore

$$D = \frac{L_q}{\lambda} + \frac{1}{\mu} \qquad (2)$$

Substituting equation (1) into (2) yields

$$D = \frac{1}{\mu}\left(\frac{1}{1-\rho}\right) \qquad (3)$$

The above equation expresses the average call delay as a function of average processor utilization and is plotted in Figure 61. Note that delay increases monotonically with increasing $\rho$. Of even greater significance is the extremely large rate of ascent for D when $\rho$ approaches one. Although actual service time values have not been used, it is apparent that D could become excessive due to variations about an average $\rho$ above about 60 percent. It should be emphasized that 60 percent was chosen somewhat arbitrarily and a more precise value would depend on the actual allowable call delay and the actual call processing times involved. However, this value is useful as a "rule of thumb."

As previously stated in paragraph 5.4.1, it is possible to consider performing technical control and switch processing in separate processors. If this were to be the case, the Switch Control Program described in Table 6 would present the more formidable processor workload (480K operations per second, worst case load). The estimated average processor workload for a 2400-line switch is approximately 330K operations per second. Assuming a 60 percent average processor utilization is permissible, the maximum processor capability required is 550K operations per second which is in reasonable agreement with the worst case analysis performed to generate Table 8. Thus, a single processor with a machine cycle time on the order of 2 microseconds should be adequate to handle the switching function.

5.4.4.2 Uniprocessor Characteristics

Tables 8 and 9 indicate that it is possible to perform both switching and TC functions in a uniprocessor. The following is a list and discussion of desirable uniprocessor characteristics.

- Processor Type - General Purpose Uniprocessor

  Currently available uniprocessors appear adequate to meet the processing loads. The processors listed in Table 10, however, are not militarized machines.

- Register Organization - 16 General Registers

  A set of general registers, which can be used as accumulators and index registers, is desirable.

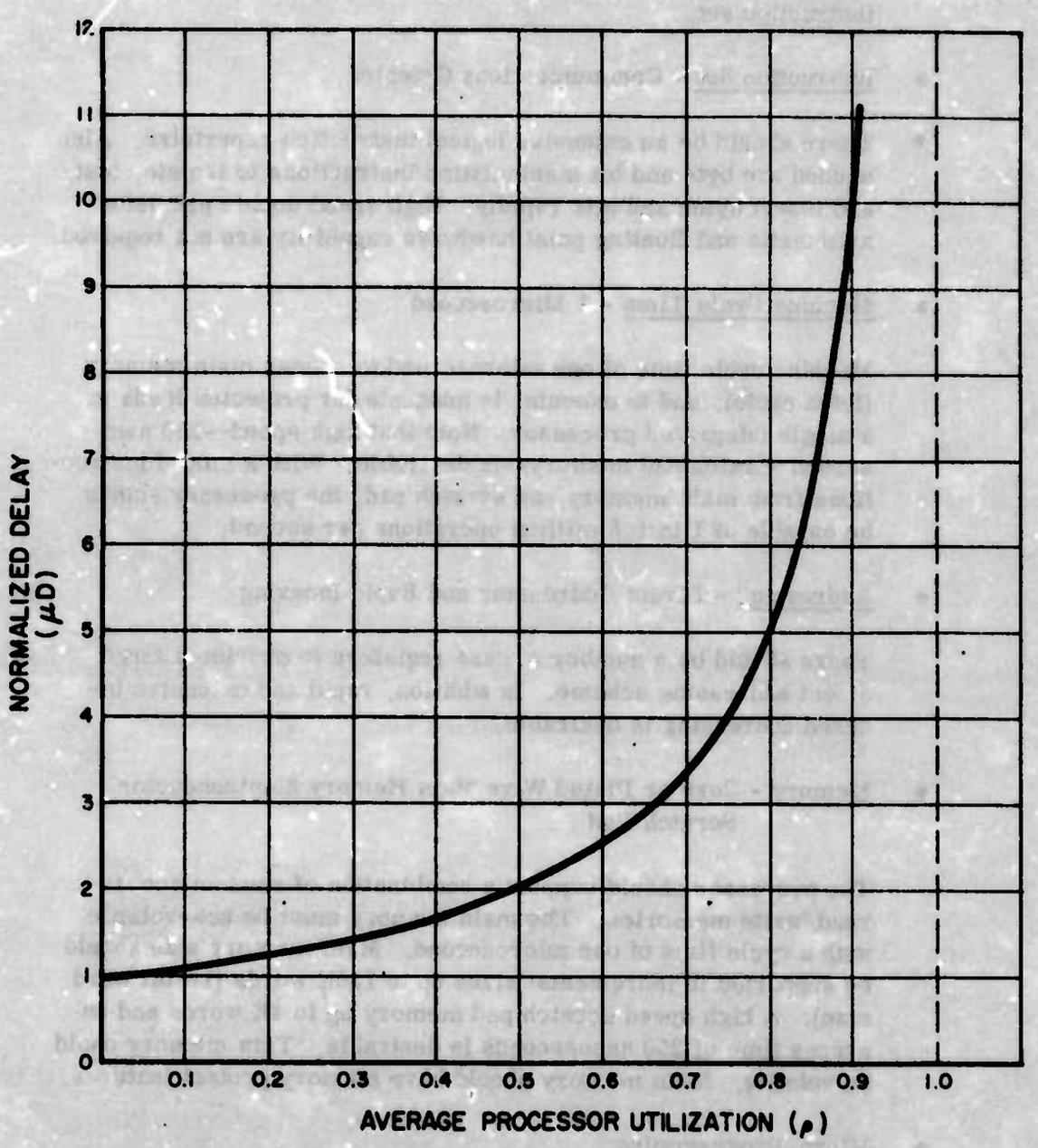



**Figure 61. Normalized Delay/Call Vs Average Processor Utilization**

- Word Size - 16 or 32 bits

  Either is satisfactory, assuming 16-bit character addressing (i.e., half-word for 32-bit word size). The 16-bit word may be superior due to more efficient use of bits in desirable instruction set.

- Instruction Set - Communications Oriented

- There should be an extensive logical instruction repertoire. Also needed are byte and bit manipulation instructions to isolate, test, and insert bytes and bits rapidly. High speed double precision arithmetic and floating point hardware capability are not required.

- Machine Cycle Time - 1 Microsecond

  Machine cycle time of one microsecond to access main memory (fetch cycle), and to execute, is adequate for projected loads in a single integrated processor. Note that high speed--250 nanosecond scratch pad memory--is desirable. With a mix of instructions from main memory and scratch pad, the processor should be capable of 1 to 1.5 million operations per second.

- Addressing - Direct Addressing and Rapid Indexing

  There should be a number of base registers to provide a large direct addressing scheme. In addition, rapid and extensive indexed addressing is desirable.

- Memory - Core or Plated Wire Main Memory Semiconductor Scratch Pad

  The processor should support a combination of random access read/write memories. The main memory must be non-volatile with a cycle time of one microsecond. Main memory size should be supported in incremental sizes up to 130K words (16-bit word size). A high speed scratch pad memory up to 4K words and an access time of 250 nanoseconds is desirable. This memory could be volatile. Main memory should have memory protect features.

- Micro-Programming

  To implement the desired byte, bit, immediate, etc., type instruction, some sort of micro-programming is advisable.

- Input/Output - Multi-Channel/Low Overhead

  The processor should support a wide range of I/O devices. There should be a multi-level interrupt capability with automatic vectoring to minimize processor load. Direct memory access I/O should be available as well as register driven I/O.

5.4.5 Minicomputer Survey

It appears that an ISMTC processor is feasible using present technology. Table 10 is a current survey of typical minicomputer characteristics and prices. The machines chosen represent a cross section of processors which are commercially available and which may be capable of supporting ISMTC control functions. It should be noted that these machines do not meet military environmental specifications. However, Tables 11 and 12 present the characteristics and specifications of the 1602 RUGGEDNOVA, a militarized version of the Data General NOVA 1200 machine which is qualified to MIL-E-5400 (Airborne Equipment) and MIL-E-16400 (Naval Equipment). Prices in Table 11 are shown for selected options required in a 32K word memory system. For other configurations consult the manufacturers' price list.

5.5 INTERFACE/PHASE-IN CONSIDERATIONS

It is possible that an ISMTC facility, along with related transportable transmission equipment, could be deployed to support various types of military communications systems other than tactical systems. For instance, an ISMTC facility could be called upon to:

1. Extend the DCS into a contingency area.

2. Replace a fixed DCS node which has been destroyed.

3. Augment existing DCS facilities until permanent upgrading can be accomplished.

All of the ISMTC deployments listed above will require inter-operation with the DCS. To permit the phasing in of an ISMTC into the DCS, a compatible interface between the two systems will be required. Interface as defined here pertains to the boundary between two systems that are functionally interconnected. The basic problems associated with the design of such a boundary are twofold--equipment and procedural. Consideration must also be given to interfaces which are internal and external to the system.

The following sections present a discussion on equipment and procedural interfaces, internal and external interfaces, followed by examples applicable to the interfacing of an ISMTC with the DCS.

## Table 10. Typical Minicomputer Characteristics

| Characteristics | MANUFACTURER AND MODEL NO. | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Computer Automation Alpha 16 | Digital Comp. Controls D-112 | Digital Comp. Controls D-112H | Digital Comp. Controls D-112H/SC | Digital Comp. Controls D-116 | Data General Nova 800 | Data General Nova 1200 | Data General Supernova/ Supernova SC | Digital Equipment Corp. PDP-8E | Digital Equipment Corp. PDP-11/20 | General Automation SPC-16 | Texas Instruments 960A | Honeywell DDP-516 | Varian 620/L | Varian 620/f |
| Word length (bits) | 16 | 12 | 12 | 12 | 16 | 16 | 16 | 16 | 12 | 16 | 16 | 16+1 | 16 | 16 | 16 |
| No. of Index Reg's. | 1 | 8/Field | 8/Field | 8/Field | 2 | 2 | 2 | 2 | 15 in Core | 6 | 6 | 16 | 1 | 2 | 2 |
| No. of GP-Reg's. | 2 | 1 | 2 | 2 | 4 | 4 | 4 | 4 | 1+ Extension | 6 | 16 | 16 | 1+ Extension | 2 | 2 |
| Interrupts (Auto) | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| I/O Channels | 64 | 64 | 64 | 64 | 128 | 64 | 64 | 128 HDX, async | 64 | >200 HDX, async at 100 baud | 250 async | 8K I/O lines via CRU* | 128 | 64 | 64 |
| A/D Interface | Yes | Yes | Yes | Yes | Yes (up to 256 chnls) | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Cycle Time (μsec) | 1.6 | 1.2 | 0.9 | 0.9/0.2 | 1.2 | 0.8 | 1.2 | 0.8/0.3 | 1.2 | 0.95 | 0.96 | 0.75 MOS 0.96 CORE | 0.96 | 1.8 | 0.75 |
| Memory Size (min/ max words) | 2K/32K | 4K/32K | 4K/32K | 4K/32K | 2K/32K | 1K/32K | 1K/32K | 1K/32K | 256/32K | 1K/28K | 4K/32K | 4K/64K | 4K/32K | 4K/32K | 4K/32K |
| Peripherals | | | | | | | | | | | | | | | |
| Disc/Drum | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Mag. Tape | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Printer | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Cards | Yes | No | No | No | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Paper Tape | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Visual Display | Yes | Yes | Yes | Yes | Yes | | | | Yes | Yes | | Yes | | Yes | Yes |
| Plotter | No | No | No | No | Yes | Yes | Yes | Yes | Yes | Yes | | | | Yes | Yes |
| Software | | | | | | | | | | | | | | | |
| Data Comm. | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| O/S | Yes | Yes | Yes | Yes | Yes(DOS) | Yes(DOS) | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| BASIC | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | | | | |
| FORTRAN | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| ALGOL | | Yes | Yes | Yes | | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| FOCAL | | Yes | Yes | Yes | | | | | Yes | | | | | | |
| Price (Basic System) | $5.5K with 4K/TTY | $4K | $5.4K | $6K | $5.1K | $7K | $5.5K | $11.9K(SC) | $6.5K | $10.8K | $9.2K | $2.9K | $23K | $5.4K | $10.5K |

*CRU - Communications Register Units - Provides capability to read, write or test I/O lines with a single instruction.

Table 11. ROLM Corporation - 1602 RUGGEDNOVA
Physical Characteristics and Prices

| Model No. | Description | Size (In.) | Weight (lbs) | Temp. Range (C°) | Price ($K) |
|---|---|---|---|---|---|
| 1602 | Central Processor and Chassis | 7.62 x 10.12 x 12.56 | 34.0 | 0° to +65°<br>-25° to +75°<br>-55° to +95° | 12.5<br>16.0<br>20.0 |
| 1635 | Control Panel | 7.75 x 10.25 x 3.9 | 9.0 | -55° to +55° | 2.25 |
| 2142 | Memory Chassis-24K | 7.62 x 10.12 x 7.9 | 8.4 | - | 2.0 |
| 2015 | Core Memory-8K | - | 5.2 | 0° to +65°<br>-25° to +75°<br>-55° to +95° | 6.0<br>7.5<br>9.0 |

Table 12. Environmental Specifications

| | |
|---|---|
| Case Temperature | Standard (0° to +65°C)<br>Wide (-25° to +75°C)<br>Extreme (-55° to +95°C) |
| Vibration | 10 g, 5 Hz to 2000 Hz, with vibration isolators (MIL-E-5400, curve IV)<br>2 g, 5 Hz to 2000 Hz, hard mounted (MIL-E-5400, curve 11) |
| Shock | 15 g, 11 msec (MIL-E-5400)<br>400 lb hammer, with isolators (MIL-S-901) |
| Humidity | 95% relative |
| RFI | MIL-STD-461 |
| Altitude | 80,000 ft |

### 5.5.1 Equipment Interface Considerations

The function of the interface from an equipment point of view is to enable the two systems to interoperate smoothly with each other once it has been determined that traffic must cross the interface. The specification for such an interface must state the type, quantity, and function of the interconnection, as well as the type and form of the signals that are to be interchanged. In some cases, it is possible for the equipment to provide a simple electrical connection. However, in many cases the equipment required consists of a sophisticated array of matching (level, impedance, etc.) and conversion (A/D, data rate, code and format, signaling and supervision, etc.) devices. If the types of traffic are varied on a periodic basis, the equipment interface structure must be varied by a control system, either manual or automatic, with its attendant array of sensing and activating devices.

### 5.5.2 Procedural Interface Considerations

Solutions to a number of operational problems quite distinct from that of equipment configurations will be required to achieve mutual system interoperability. Typical problems may be grouped under the general areas of system control, system test and lineup, allocation of frequencies, allocation and execution of precedence levels, preemption, etc. There is a relationship between equipment and procedural interface considerations. The extent of this relationship is primarily a function of the degree of automation desired, e.g., manual vs automated call setup between users of the different systems, manual vs automated transfer of system control information, etc.

### 5.5.3 Internal/External Interfaces

With respect to tactical military communications systems there are two basic types of interfaces which must be considered, internal interfaces and external interfaces. Internal interfaces relate to the interconnections between the various types of user and subscriber access loops and the tactical switch. External interfaces are those associated with the interconnection of other systems which are not part of the tactical network supported by ISMTC facilities.

#### 5.5.3.1 Internal Interface Considerations

Basically, ISMTC internal or intrasystem interface design must be concerned with the types of user access loops associated with:

1. Users so located with respect to the ISMTC that they can be tied to it through a wire circuit.

2. Isolated users who are essentially stationary with respect to the ISMTC but located beyond normal wire communication range.

3. Colonies of users who are in close proximity to each other but remote from the ISMTC.

4. Mobile subscribers.

5.5.3.2 External Interface Considerations

During the post-1980 time frame it is highly probable that networks supported with ISMTCs will have to interface with a great variety of military and civil communication systems of allied countries and NATO, as well as national communication systems. These systems may be grouped into the following general categories:

- Strategic communication systems (DCS)
- National and foreign civil communication systems
- Air defense/support/traffic control systems
- Allied/NATO tactical communication systems
- Weapons systems
- Non-military government systems
- Information processing systems, e.g., fire direction, combat service support, tactical operations, etc.

It should be recognized that within each of the above groups the equipments and systems anticipated to be operating in the field in the post-1980 ISMTC time frame may exhibit some of the following characteristics:

1. Independently designed and not mutually compatible.
2. Assembled into special purpose systems handling a limited number of users and types of traffic, e.g., analog voice only, data only, etc.
3. Employing various standards.
4. Employing widely differing operational doctrines.
5. Composed of devices based on outdated technology.

It probably will not be possible to specify general interface criteria which will assure a compatible interface with all possible networks requiring interconnect. However, it must be recognized that the ISMTC system design should not be carried out independently or without regard to the characteristics of the external systems; that is, consideration must be given to the technical characteristics and operational doctrine of all equipments composing the systems with which ISMTCs will have to interface. Depending upon the anticipated amount and type of traffic an external system may carry, the ISMTC design may have to be modified to provide the most cost-effective system design.

5.5.4 DCS Interface

The major objective to consider when two different systems must be interconnected is the provision of an optimum interface which can reduce the impact on overall system design of the two systems to be interfaced. The two systems considered in the following discussion on interfacing are the DCS and a tactical communications system in which ISMTCs are deployed.

There are two basic techniques for providing an interface capability between two systems. They are:

- Through compatible system design.
- Through the introduction of applique units, i.e., "black boxes".

When possible, compatible system design is the preferred method to achieve an optimum interface. Unfortunately, this approach is not universally applicable since many system designs must be considered fixed and not subject to change to achieve mutual compatibility. Furthermore, the conflicting requirements among the various systems generally rule out a unilateral effort to achieve total compatibility. This fact, however, does not rule out the possibility that evolutionary trends in various systems may open up the possibility of a compatible approach in the future.

The possibility exists that, during the 1980 time frame, the DCS will be an all-digital system. If this possibility becomes a reality, and if the ISMTC is designed to be compatible with the all-digital DCS, the interface between the two systems would not pose any problems. However, the worst case situation must be considered, i.e., the two basic systems will not be designed to be completely compatible. Therefore, the interface must be provided through the introduction of applique units. Applique units as used in this discussion refer to manual, semi-automatic, or automatic interface facilities to compensate for various system and user end instrument incompatibilities. In general, applique units would be required only at gateway interfaces.

The concept of a gateway interface provides that a limited number of nodes from each system are involved in the interconnection. Since all intersystem traffic must cross

this interconnection, equipment complexity would tend to be high although operational procedures would be simplified. The major advantage of using a gateway interface is that it minimizes the impact of interoperability requirements on individual system design and procedures by concentrating the problem to a few areas.

As noted earlier, the interface of concern in this discussion is the interface between the DCS (strategic network) and a tactical system composed of one or more ISMTCs. Within the DCS there are three major common-user elements, AUTOVON, AUTODIN, and AUTOSEVOCOM. In the discussion that follows, emphasis will be placed on describing how the AUTOVON and AUTODIN interface with the ISMTC could be provided. Similar techniques could be used for AUTOSEVOCOM, and other external systems such as those listed in paragraph 5.5.3.2.

5.5.4.1 AUTOVON Interface

Figure 62 illustrates a simplified block diagram of the possible interface between an AUTOVON switch and an ISMTC. The basic system characteristics pertinent to this case are listed in Table 13. With reference to Figure 62, the purpose of the Interface Module (IM) is to make the AUTOVON channel content appear to be the same as a user connected to the ISMTC. The interface system would operate as follows:

1. Certain AUTOVON subscriber numbers would be reserved as a means of entry into the ISMTC and in turn certain ISMTC user numbers would be reserved as a means of entry into AUTOVON.

2. When desiring to go out of the tactical system and into AUTOVON, the ISMTC user would dial (key) one of the reserved ISMTC numbers indicating to the switch a request for a line into AUTOVON. (This signaling does not provide the AUTOVON subscriber address.)

3. The ISMTC automatically switches the tactical user to one of a number of Interface Modules (IM) designed for connection to AUTOVON interswitch trunks. On the AUTOVON side, each IM looks like a 4-wire subscriber.

4. The IM effectively goes "off hook" and waits for a dial tone from the AUTOVON switch, then sends a distinctly recognizable signal back to the ISMTC user.

5. When the tactical user hears this signal, he dials (keys) the desired AUTOVON number. If he does not know the desired AUTOVON number, he requests the dial assistance operator.

6. The IM translates each digit into the proper signaling tones for AUTOVON and the connection proceeds normally.

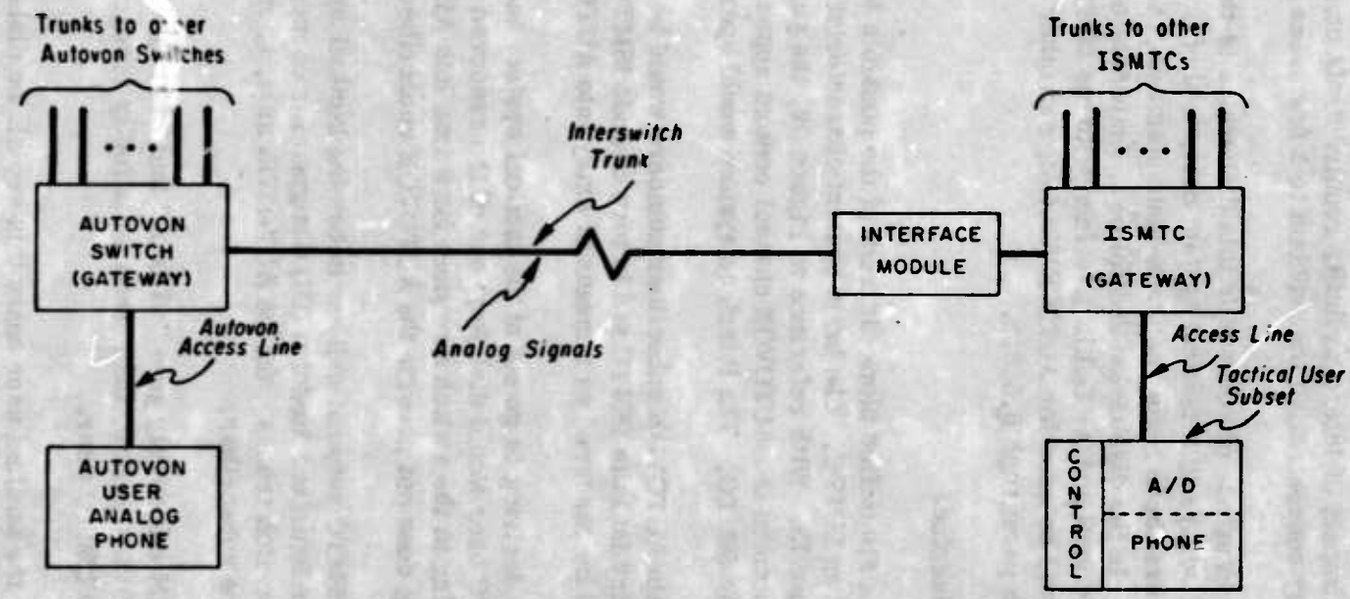



Figure 62. AUTOVON/ISMTC Interface

Table 13. AUTOVON/ISMTC Interface System Characteristics

| | AUTOVON | ISMTC |
|---|---|---|
| Basic Channel | 4 kHz analog or data (quasi-analog) up to 9.6 kb/s | 32 kb/s digital |
| End Instrument | 4-wire or 2-wire phone | Delta modulated phone (CVSD) |
| Control Signaling | | |
| Local Loop | DTMF (in-band) | Digital (in-band) |
| Trunk | 2/6MF (in-band) | Digital (out-of-band), i.e., separate signaling and supervision channels |
| Supervision & Signaling | E&M | Time division at 32 kb/s |
| Baseband Composition | FDM | TDM |

7. The IM performs the A/D and D/A conversion for all signals crossing the interface. (The same basic A/D-D/A converter used in the tactical user subset could be used to provide this function.)

A minor disadvantage of the method just presented is that the user must know the numbers of the called party in the other system. This is not too restrictive, since in many cases he will be calling a familiar number or responding to some instruction from someone who knows the number. If such is not the case, he must take a two-step approach and contact the dial assistance operator.

The major advantages are summarized below:

1. Complete independence of numbering plans.

2. Simple IM equipment without memory. (The basic requirements are to provide only a digit-by-digit translation, recognition of signaling tones, and A/D-D/A conversion.)

3. Possibility of pooling identical IMs.

4. Easily understood discipline (similar to getting an "outside line" through present day PBXs).

5.5.4.2 AUTODIN Interface

Figure 63 illustrates a simplified block diagram of a possible interface between an AUTODIN user and a user associated with an ISMTC. In this illustration it is assumed that the interswitch trunk to the gateway ISMTC is a dedicated circuit provided by the AUTOVON system. If the interswitch trunk is a dedicated circuit, the Interface Module (IM) would then be nothing more than a data modem converting quasi-analog signals into digital signals.

It should be noted that the most significant feature of store-and-forward traffic (AUTODIN type traffic) affecting the interfacing of AUTODIN and tactical systems is that the end instruments do not have to be compatible. The only requirement is that each end instrument be compatible with the capabilities of its associated store-and-forward module.

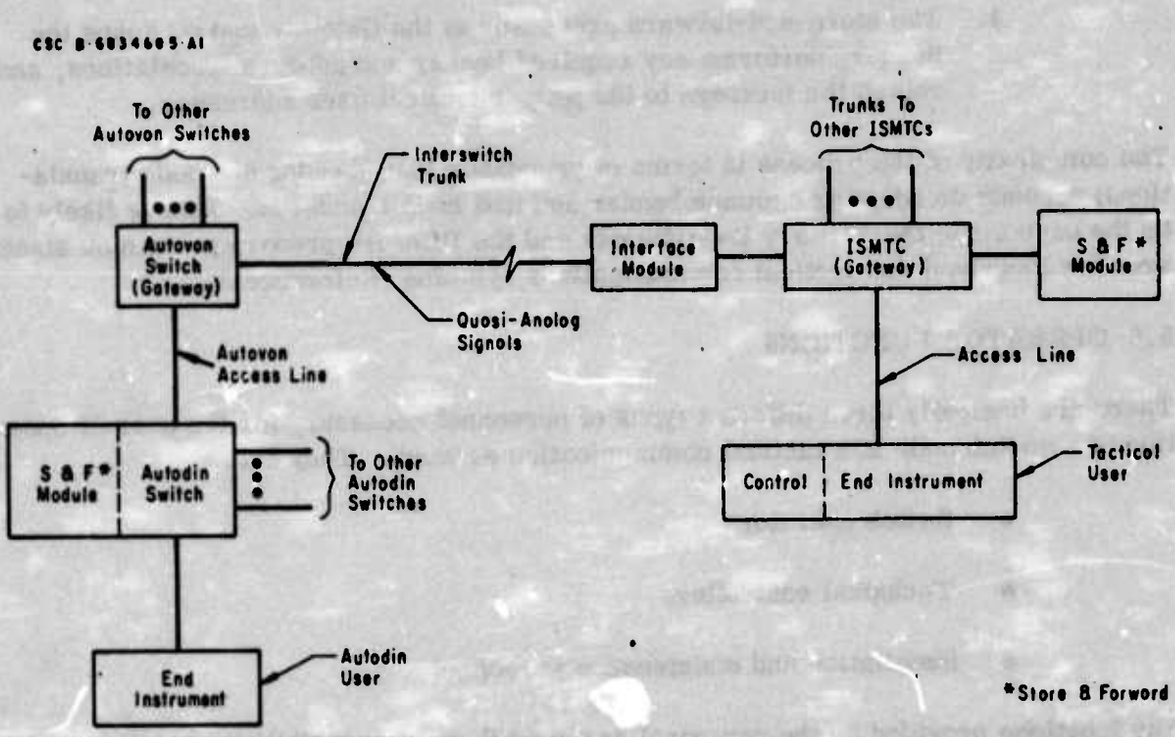



Figure 63. AUTODIN/ISMTC Interface

With reference to Figure 63, digital traffic between an AUTODIN user and a tactical user would be accomplished as follows:

1. Assume the message originates at an AUTODIN subscriber's end instrument. The header part of the message must contain the tactical system user address in a form compatible with the tactical system (if not, format translation will be required in the processor serving the ISMTC store-and-forward module).

2. The message is read into the associated AUTODIN store-and-forward switch with all the multiple addresses inserted if applicable. Precedence and security are dealt with in an AUTODIN standard manner.

3. The AUTODIN store-and-forward switch examines its precedence queue log and at the earliest time compatible with the priority and traffic volume the message is transmitted on the proper AUTODIN trunk (likely derived through AUTOVON) to the Gateway ISMTC node.

4. The store-and-forward processor at the Gateway ISMTC scans the header, performs any required header and address translations, and routes the message to the proper tactical user addressee.

The complexity of the process in terms of processor load (header and code translations) depends on adopting common header and text code standards. This is likely to be the case since the Military Departments and the DCA are preparing common standards for long-haul and tactical communications systems (Reference 5).

## 5.6 OPERATOR FUNCTIONS

There are basically three different types of personnel necessary for the overall operation of a switch node in a tactical communication network. They are:

- Switch operators
- Technical controllers
- Installation and maintenance personnel

The functions provided by the personnel assigned these responsibilities are briefly described here. At present, most required actions are provided on a manual basis in tactical military communication networks. However, many of the required functions are readily adaptable to automation. Table 14 lists operation functions required in both manual non-integrated facilities and in an ISMTC applicable to the tactical networks of the 1980s and indicates which functions can be aided by automation. A discussion of each function is provided below.

### 5.6.1 Dial Assistance

Since users of tactical communication systems tend to be more mobile than users of strategic networks, up-to-date information on user addresses is more critical. The use of dial assistance operators provides a manual means of achieving network flexibility and responsiveness in order to accommodate rapidly changing user locations (i.e., addresses). Automation achievable in an ISMTC node can alleviate some of the work load on dial assistance operators by incorporating deducible numbering plans and processor stored location information. Implementation of such schemes entails assignment of user numbers as a function of miliary unit assignment as opposed to fixed line termination. These schemes, however, place increased load on the switch processor since dynamic table lookups are required each time a call setup is accomplished. Routines are also required in the processor to permit the user to change his switch line termination when he homes on a new node. Although direct user/processor interaction can accomplish directory updating on an automatic basis and a deducible numbering plan can alleviate the dial assistance operator work load, it is anticipated that the 1980s ISMTC will require the assignment of dial assistance

Table 14. Major Operation Functions at a Switching Node

| Required Function | Provided Manually By | | | With ISMTC | |
|---|---|---|---|---|---|
| | Switch Operators | Tech Controllers | Installation and Maintenance | Manual | Automated |
| Dial Assistance | x | | | x | x |
| Updating Routing Tables | x | | | | x |
| Updating Fixed & Mobile Directory Information | x | | | | x |
| Trunk Barring | x | | | | x |
| Line and Load Control | x | | | | x |
| Activation/Set-Up | x | x | x | x | |
| Deactivation/Tear-Down | x | x | x | x | |
| Patching/Rearrangement | | x | | x | |
| Testing | | x | x | x | x |
| Monitoring | | x | | | x |
| Conditioning | | x | x | x | |
| Fault Detection | | x | | | x |
| Fault Isolation | | x | | x | x |
| Coordination | | x | | x | x |
| Restoral | | x | x | x | x |
| Reporting | | x | | | x |
| Recordkeeping | | x | | x | x |

operators to assure the required flexibility and responsiveness under stress condition. Table 14, therefore, shows the need for manual dial assistance operators in both the non-ISMTC and ISMTC facilities with automation assisting the dial assistance operator as discussed above.

5.6.2 Updating Routing Tables

In a tactical environment the traffic load on the trunks of the communications network is subject to unanticipated changes due to any of the following situations:

- Redeployment of forces
- Outages due to equipment failure
- Outages due to action by the enemy

When one or more of the above situations occurs, the network must be reconfigured as rapidly as possible through reassignment of primary and alternate routes associated with the affected nodes. Therefore, personnel responsible for the operation of the switching system must be made aware of and maintain updated routing tables.

A system where the switching function and the TC functions associated with traffic and circuit monitoring are disassociated requires technical controller actions to "patch in" new trunks and provide trunk group rearrangements to accommodate new internode throughputs. These technical controller actions performed independently from the actions of the switching centers necessitate coordination between the technical control and switching position if the switch is to maintain an efficient trunk selection routine. An integrated facility has the significant advantage of accomplishing the technical control required operator function of circuit rearrangement and the switch-related function of revising routing tables, automatically, through a common processor system supporting both switching and technical control operations.

5.6.3 Updating Fixed and Mobile Directory Information

This function is required to support the dial assistance function as described above. Automation of directory updating can be achieved in a non-integrated switching center by providing a means of sending user location information to affected switching centers on an orderwire or common signaling channel. A number of techniques are available to update location information concerning rapidly moving users (i.e., aircraft) and involve system tradeoffs between node complexity and user equipment complexity in terms of receiver, transmitter, and signal processing equipment costs. Random Access Discrete Address (RADA) is an example of one technique applicable to tactical users. It is recommended that updating fixed and mobile directory information be handled on an automated basis in the ISMTC of the 1980s by a software table updating in the common switching/multiplexing technical control processing system.

### 5.6.4 Trunk Barring

Trunk barring is a means of network control whereby some users are barred access to interswitch trunks while permitted to make calls to others homed on the same node. Generally, networks become trunk starved during high traffic conditions while maintaining adequate capability to satisfy intraswitch traffic. The ability to handle local traffic is a function of the blocking probability of the switch matrix while interswitch calls are limited, in most networks, to the transmission capacity between nodes. In manually-controlled networks, trunk barring can be instituted during high-traffic or system-degraded conditions by limiting interswitch calls to priority users. In the ISMTC network it is contemplated that traffic as well as quality monitoring information will be integrated within the node's processor system. As a result, thresholds can be set within the traffic monitoring routines which will activate the trunk barring routine within the switch common control processor. Although preemption on a priority basis does assure trunk access to callers having sufficient priority, trunk barring is recommended in combat theater networks since extreme congestion is often experienced during crisis conditions. This condition can be somewhat alleviated by means of automated trunk barring procedures.

### 5.6.5 Line Load Control

Line load control is similar to trunk barring in that network congestion is alleviated by denying certain users access to the network. Line load control is more severe than trunk barring since users are not permitted access to their local switches even for local calls. Commercial switching systems perform line load control by not connecting a dial input receive register in response to an off-hook request. Military networks are more complex since call denial must be accomplished on a priority basis. As discussed in the paragraph on trunk barring, line load control is accomplished in the ISMTC network by integrating switch processor functions with technical control traffic monitoring and quality monitoring functions. An advantage of integrating the technical control and switching functions in a common processing system is the ability to distinguish between the necessity for trunk barring and line load control on an automated basis; that is, the technical control trunk monitoring function and the switch's inherent common knowledge of matrix congestion permit an automated decision to be made between enacting line load control and trunk barring.

### 5.6.6 Activation/Set-up

The ability to rapidly activate or set up the switched network is an important consideration in the tactical environment. The equipment is held in a staging area prior to deployment and must be transported and installed in support of tactical operations. Setup consists of installing and cutting over subscriber loops and interswitch trunks and establishing the appropriate switching and technical control tables. The primary actions required in both the integrated and non-integrated system are manual with the heaviest burden going to the installation function. Initially a great deal of interaction

is required between the switching, technical control, and installation and maintenance function until each node is properly configured for optimum system performance. It is recommended that node setup tables be preprogrammed on magnetic tape (e.g., cassette tapes) for various deployment scenarios and that a high level command language be established to permit processor access by switch and technical control operators. Use of powerful command language macro-instructions will alleviate operator setup difficulty.

### 5.6.7 Deactivation/Teardown

Similar to the activation/setup operation, the deactivation/teardown operation requires manual action on the part of switch, technical control, and installation and maintenance personnel. Each subscriber loop and interswitch trunk must be removed from service and coordinating information passed on to the System Control Node in order to permit network reconfiguration actions. In this case, network redeployment actions are the responsibility of the Planning and Engineering and System Control echelons.

### 5.6.8 Patching/Rearrangement

Patching and circuit rearrangement are presently technical control manual actions. Some thought has been given to automatic patching at technical control positions (e.g., ATEC), but most networks handle this function by means of jack fields which permit manual circuit replacement and circuit conditioning by insertion of attenuators, amplifiers, repeat coils, and equalizers. The integrated system, however, envisions a switched network serving almost all users and the small number of validated dedicated lines (less than 20 percent of the users) being terminated on the switching matrix for rearrangement purposes. By this means, the present clearly separable functions of technical control circuit rearrangement by means of manual patching and the switching operation of alternate route selection are merged. This operation is performed automatically in the integrated system since the technical control monitoring function is used to update switch routing tables and thereby alter trunk route selections. This procedure can be used with either fixed or adaptive routing doctrines in the switch. In any case, the restoral/rearrangement operation is handled as an automatic operation in the processor system software rather than as a manual action by technical control operators. Some patch panels will be required at the ISMTC node, however, to provide manual backup under emergency conditions.

### 5.6.9 Testing

Testing is a technical control operation and is generally performed to determine if a circuit is within tolerances for operation before being installed or activated. Testing is also performed for the isolation of faults when a circuit or switch fails to function properly. The electrical separation of the circuit and switch enables the testing to be accomplished in both direction, i.e., the circuit and the switch can be tested separately. Testing is an essential part of the fault isolation, repair, and restoral process

and is distinguished here from the automated fault and quality monitoring which is envisioned in the integrated system. Testing presently is accomplished manually by technical controllers who are responsible for initiating tests, diagnosing faults, and coordinating testing activity with remote stations. Processor assisted automation of the testing operation is incorporated in the ATEC system being implemented for existing strategic networks and, similarly, processor-assisted testing is envisioned for the integrated tactical system although the type of testing would differ appreciably from the analog ATEC type tests. Manual operations are required, however, in either an integrated or non-integrated network. For example, specialized test equipment will occasionally be necessary to enable fault isolation and coordination with remote sites.

### 5.6.10 Monitoring

Monitoring is the technical control process of measuring the quality of a circuit without disturbing the transmission path. The process of monitoring circuits is usually performed in order to detect degradation of the circuit before complete failure. The ISMTC system envisions automating this function by use of a node processor system. As discussed elsewhere, certain monitoring functions can be built directly into the switch processor and associated hardware inherent to the switching function. For example, the hook scanner circuit could be used to monitor error rate on the subscriber loop by monitoring the known idle pattern and relaying gross error statistics to the switch processor. Similarly, the idle pattern on the interswitch trunks can be monitored by the switch processor. In any case, it is recommended that monitoring be handled on an automated basis in the integrated system since there is a natural overlap between certain switching operations (e.g., trunk testing for connection, hook scanning, idle detection, etc.) and technical control monitoring functions.

### 5.6.11 Conditioning

Conditioning consists of altering the electrical characteristics of a transmission channel to make it suitable to the user and to permit compatible interfacing within the transmission system. In normal practice conditioning is accomplished when the channel is initially established. However, since circuits are subject to change with time, adjustments in conditioning are required to restore circuit quality when degradation is detected. Conditioning, therefore, is directly tied to the technical control functions of circuit monitoring and testing. In existing networks conditioning represents a significant portion of the technical controller's responsibility and is handled manually by means of equipment patching between voice frequency (VF), circuit level, DC, and cable patch bays. Many of the technical control conditioning concepts are applicable to analog FDM-derived voice circuits and, therefore, are not applicalbe to TD-derived digital circuits. Some simplification results from handling digital circuits on a wideband time interleaved basis rather than using 4-kHz voice circuits.

### 5.6.12 Fault Detection

Fault detection is the process by which a faulty circuit or malfunctioning equipment is discovered by the technical controller or maintenance personnel. In the past, the most common method of fault detection in the tactical environment, with manual facility control, was reports from subscribers and switchboard operators. With the advent of electronic automatic switching systems it is possible to enhance this function through automation, i.e., automated fault detection. It is possible in the integrated system to automate the process of fault detection both on an equipment and circuit basis. The process is directly related to the technical control functions of testing and monitoring and, as discussed previously, the intention is to make use of the processor system at the node to automate this technical control function.

### 5.6.13 Fault Isolation

The basic process of fault isolation consists of breaking down a circuit into its component elements and testing each to determine which element is faulty. Short cuts to this process are usually developed as characteristics and failure patterns are established. The proper selection of monitor points and the means to telemeter the fault reports to the ISMTC processor permit the automation of the fault isolation process. In-station fault isolation is accomplished by means of the diagnostic routines built into the processor software. The depth to which out-of-station fault isolation occurs is a function of loading on the orderwire channel and the processor work load. The tradeoff between processor and channel load and maintenance requirements indicates it is not practical to attempt fault isolation to each replaceable card at a remote station and, therefore, maintenance personnel will be required to perform fault isolation at this level.

### 5.6.14 Coordination

Coordination is the process by which the technical controller directs the actions necessary to test, activate, or restore a circuit involving participation by far-end and/or intermediate sites. The critical item in coordination is reliable communications external to the circuit being tested, activated, or restored. Orderwires are generally used for this purpose. Coordination is basically a manual operation requiring participation by personnel at each affected site. Some automation of the operation is possible in the integrated system by means of interaction between the switching and the technical control functions. For example, loop arounds can be accomplished by providing appropriate circuitry in modems, multiplexers, and switches. Coordination with the switch processor permits seizure of idle return paths between nodes and, therefore, permits testing on a non-interfering basis.

### 5.6.15 Restoral

Restoral as used here is the replacement of service which is denied through faulty circuits or equipment. Generally, restoral consists of replacement of faulty components or repair of faulty circuits as compared to the substitution of one communication channel with another as is done in circuit patching or rearrangement. Restoral requires coordinated action between technical control and maintenance personnel and, therefore, some degree of manual action. In the integrated system, automation is brought to the process by means of the software-controlled fault detection and fault isolation routines discussed above.

### 5.6.16 Reporting

Reporting consists of the dissemination of information concerning circuit and traffic status, faults, implementation plans, circuit routing tables, etc. Reporting procedures for the various operational elements of the network will vary depending upon their functions in the system. The reporting function as done manually in existing networks is a time-consuming operation for the technical controller. As discussed previously in Section 4.4, the intention is that the integrated system will decrease the technical controller burden by instituting an automated reporting procedure which provides the System Control and System Planning and Engineering elements with the data required to assure satisfactory communication support to the overall tactical operation. The reporting is provided on the orderwire; the basic form of the reports is discussed in Section 4.4.

### 5.6.17 Recordkeeping

The recordkeeping function consists of the collection and maintenance of records related to the current status of all monitored circuits and equipment, test data from testing programs, circuit technical data concerning the routing equipment used, and operational characteristics of all circuits, circuit rerouting assignments, and other similar operational data. At present, recordkeeping is basically a manual technical control operation using documentation such as Circuit Record Layout Cards. As indicated in the paragraph above on the reporting function, recordkeeping is a tedious and time-consuming process amenable to automation. In the integrated approach it is recommended that a data base be kept in mass storage by the System Control and the System Engineering and Planning Elements. Some updating of records will be required on a manual basis by means of entry terminals at the ISMTC nodes such as notification of circuit and equipment return to service. Such entries are made by means of the conversational command language.

## 5.7 RED/BLACK CONSIDERATIONS

The ultimate objective for both tactical and strategic (DCS) communications networks for the post-1980 time frame is a fully secure all-digital system capable of handling voice, data, message, and graphic (fax, video, etc.) traffic. To meet this objective, specially designed communications security (COMSEC) equipment will be required for both loop and trunk (bulk) encryption/decryption. The COMSEC equipment designed for use during the post-1980 time frame will have to interface with the Integrated Switch/Multiplex/Technical Control facility. Therefore, consideration must be given to satisfying the Red/Black Engineering Installation Criteria at the interface between the switch module and COMSEC module.

When discussing Red/Black considerations the terms "Red Area" and "Black Area" are generally used. These terms can be defined as follows:

- "Red Area" - That area of a secure communications complex in which classified information appears in the clear.

- "Black Area" - That area of a secure communications complex in which classified information appears in protected form, i.e., the classified information has been encrypted.

Detailed information related to Red/Black engineering installation criteria and guidelines can be obtained from the following documents:

1. AFNAG-5A (Amendment 2) (C); Red/Black Engineering and Installation Criteria (U)/31 March 1969.

2. MIL-HDBK-232(C); Military Standardization Handbook, Red/Black Engineering Installation Guidelines/14 Nov 1972.

The major consideration with respect to Red/Black interface for the integrated switch is that of hardware; that is, hardware such as isolation devices will be required on all lines crossing the Red/Black interface. The Red/Black isolation device must provide isolation of signal lines and their associated timing leads when they enter the Red area from the Black area. Basically, the isolation device must provide high attenuation to any Red signal which could appear on the Black side of the interface. In addition to isolation devices, consideration must be given to the avoidance of secure information and crypto key stream being simultaneously transmitted through inadvertent electromagnetic radiation or other types of emanation, i.e., consideration must be given to TEMPEST requirements.

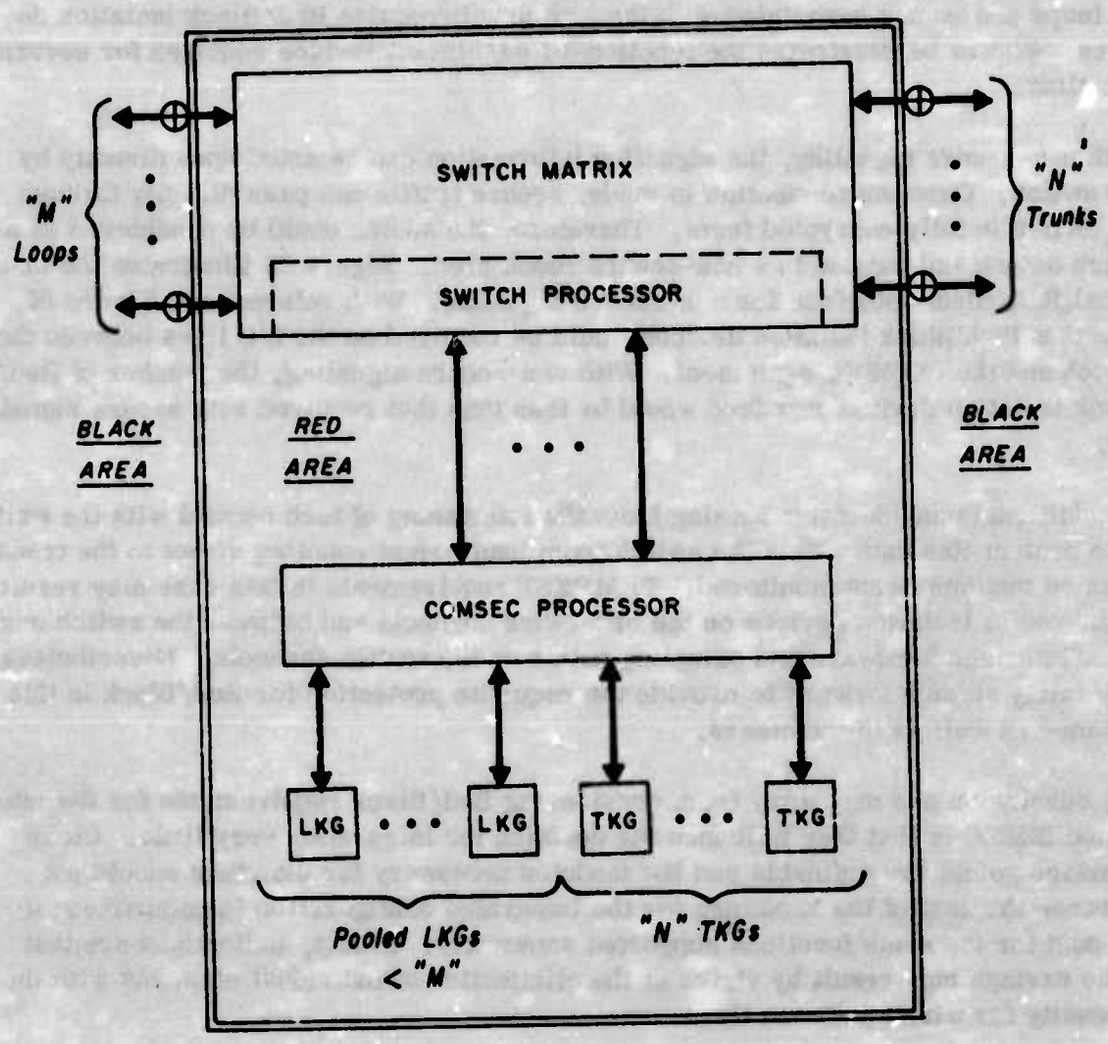
The number and location of the Red/Black isolation devices will be dependent upon the COMSEC doctrine related to loop and trunk signaling, i.e., secure vs non-secure signaling. With secure signaling the encrypted signaling information must be decrypted

by the COMSEC equipment before the switch can act to establish the proper connection. Since the signaling information is in the clear within the switch, the switch must be considered as a Red switch and be located in a secure Red area. Therefore, all loops and trunks associated with the switch will require Red/Black isolation devices. Figure 64 illustrates the functional Red/Black interface required for secure signaling.

With non-secure signaling, the signaling information can be acted upon directly by the switch. Once the connection is made, secure traffic can pass directly through the switch in fully encrypted form. Therefore, the switch could be considered as a Black switch and located in a non-secure Black area. Figure 65 illustrates the functional Red/Black interface for non-secure signaling. With reference to Figure 65, note that Red/Black isolation devices would be required on the I/O lines between the switch and the COMSEC equipment. With non-secure signaling, the number of Red/Black isolation devices required would be less than that required with secure signaling.

An additional consideration arising from the interfacing of tech control with the switch is to protect Red data within the switch from inadvertent coupling direct to the transmission medium being monitored. TEMPEST requirements in this case may result in the use of isolation devices on the orderwire channels and between the switch computer interface hardware and sampling points on the traffic channels. Nevertheless, it is fairly straightforward to provide the requisite protection for Red/Black in this instance as well as in the others.

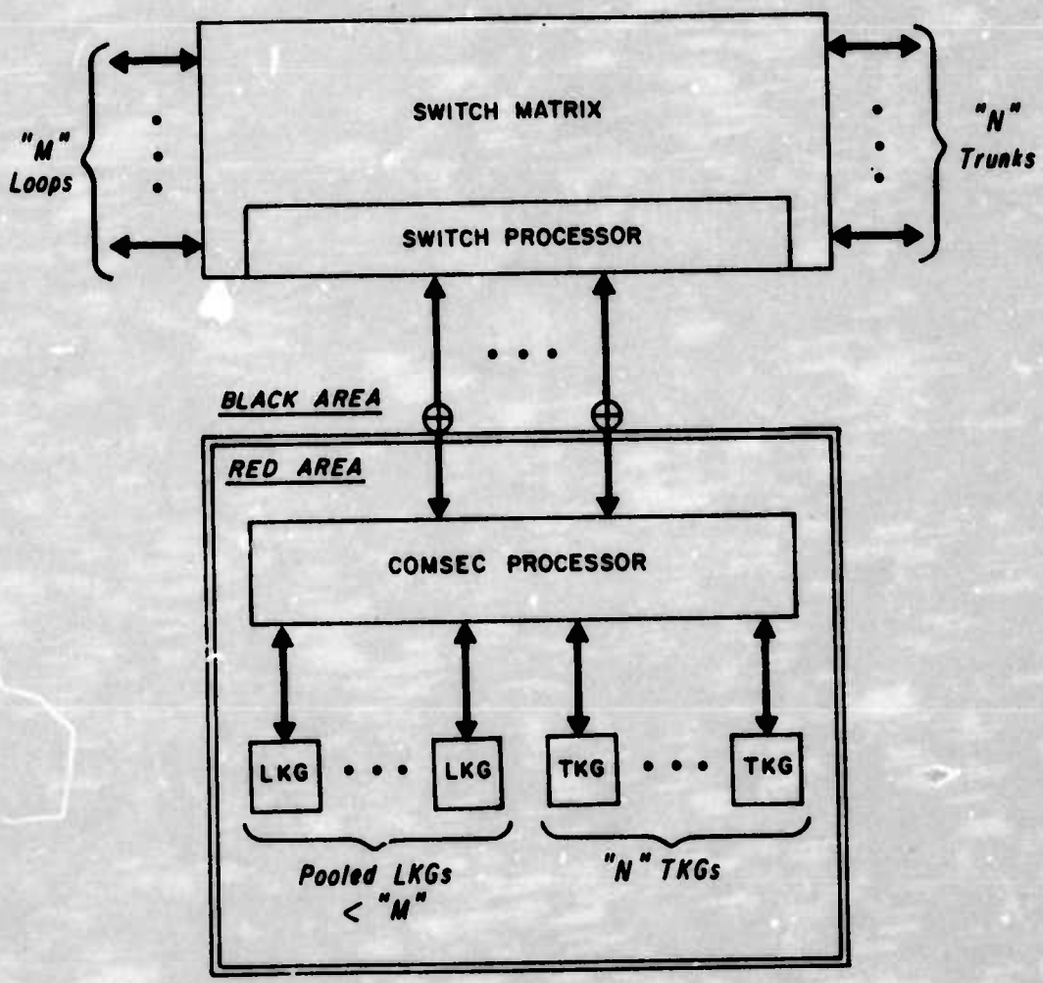
The conclusion one may draw from considering Red/Black requirements for the integrated ISMTC is that they influence the decision for integration very little. Clear interface points are definable and the modules necessary for interface should not increase the cost of the hardware for the integrated configuration in comparison to the cost for the same functions supported separately. In fact, indications are that some savings may result by virtue of the elimination of individual elements with the necessity for wiring between them.




LEGEND

LKG – Loop Key Generator
TKG – Trunk Key Generator
⊕ – Isolation Device

Figure 64. Red/Black Interface - Secure Signaling




LEGEND

LKG - Loop Key Generator
TKG - Trunk Key Generator
⊕ - Isolation Device

Figure 65. Red/Black Interface - Non Secure Signaling

## 6.0 PHYSICAL CONSIDERATIONS

Aside from installation time and effort considerations, the question of equipment transportability ultimately resolves itself to the sizes, weights, and number of the various equipment "packages" (e.g., integrated switch/multiplex/tech control, power supplies, display panel, printer, CRT terminal, etc.) making up a given overall configuration. These characteristics directly dictate the enclosure and transport vehicle requirements. The transportability requirements, therefore, are important in determining the usefulness of an equipment configuration in contingency applications.

To consider the equipment packages in the proper perspective, it is necessary, therefore, to consider the various types of enclosures that might be used as well as the means for transporting the enclosures. Equipment enclosures and associated land transport vehicles are classified in the following categories:

1. Shelters - Box-like enclosures for equipment, usually rectangular and made out of metal, that have no wheels or motive power of any kind.

2. Box trucks - Trucks that have enclosed cargo carriers integral with the truck bodies.

3. Flat-bed trucks - Trucks with flat, open cargo carriers (amenable to carrying shelters).

4. Trailers - Cargo-carrying wheeled vehicles that have no motive power (must be towed) but which support their own weight. These vehicles may be towed by ordinary trucks.

5. Semi-trailers - Again, cargo-carrying vehicles that have no motive power and must be towed but which do not support their entire weight when towed. These vehicles are coupled to tractors which partially support the trailer weight and supply the motive power, forming a semi-integrated vehicle.

Shelters could theoretically come in any size but, since they must be lifted on and off flat-bed trucks or other vehicles for ground transport, they are practically limited to relatively modest dimensions. They are convenient for use when overall equipment configurations are fairly compact.

Box trucks, with equipment enclosures integral to the motor-drive units, are usually not desirable for the ISMTC application since it may not be practical to require the air transport of the equipment enclosures.

## 6.1 OPTIMUM ENCLOSURE SIZE CONSIDERATIONS

Insofar as the optimum enclosure size for a given configuration is concerned, several factors must be considered.

Among these are:

1. The feasibility of moving the equipment to the desired location;
2. The number of units required;
3. The complexity of inter-unit wiring if a large number of units are used;
4. The amount of operating space required and its relation to particular pieces of equipment;
5. The stability of the equipment, particularly during transportation over rough ground;
6. Heating and cooling requirements both for personnel and equipment;
7. The desirability of grouping a number of small units for ready access from one to another; and,
8. The manpower required for operation.

Cramped operating conditions are not conducive to good equipment performance. The amount of operating space required will depend upon the type of equipment. Operation of patch bays, meters, tuning and adjustments, etc., must be considered along with space requirements dictated by maintenance needs. In addition, some specifications require that 20 percent surplus equipment space be allowed when equipment is first designed so there will be room for minor modifications at a later date.

The center of gravity of the transportable enclosure must be kept sufficiently low so that the mobile unit is not likely to overturn in traversing sloping ground. SCL-1280D "Design of Electronic Equipment for System Installation in Shelters and Vans" contains requirements in this regard. There is also a requirement of not over five percent unbalance in the loading of the roadside and curbside sides of the shelter as well as additional limitations on fore and aft balance. Air-conditioning and cooling equipment could occupy a significant amount of room and, along with the heating equipment, must hold interior conditions reasonably uniform under extreme variations in environmental weather conditions. The sensitivity of the advanced integrated circuitry contemplated for the ISMTC should be considered with regard to the environmental conditions expected in the shelter.

The manpower required for operation will depend upon the number of shelters that are used and the way the equipment is distributed. Tech control operations or equipment operation may require full-time operators. These requirements could be reduced if suitable alarms are installed and reserve manpower is available to follow up on the alarms.

Finally, the optimum shelter or enclosure size is heavily dependent on the particular sizes and shapes of the equipment to be packaged. The utmost in equipment transportability feasible must be maintained while the functional usefulness of the configuration must not be unduly sacrificed. Nor would it be practical to utilize a great variety in shelter/van sizes for a single configuration. The transportability is determined by the largest enclosure size used, since all of the packages have to get to the same destination in the end.

## 6.2 SHELTERS

There are a large variety of shelters currently in military nomenclature inventory which encompass both "standard" and "non-standard" models. A representative sampling of military shelter models suitable for this type of application and their characteristics is given in Table 15.

Table 15. Typical Standard Shelters

| Nomenclature | Length (inches) | Width (inches) | Height (inches) | Weight* (pounds) | Nominally Designed for Vehicle Carrying Capacity (tons) |
|---|---|---|---|---|---|
| S-308 | 72.0 | 70.5 | 66.5 | 475 | 3/4 |
| S-318 | 72.5 | 71.5 | 69.5 | 475 | 3/4 |
| S-250 | 96.0 | 84.0 | 60.0 | 825 | 1-1/4 |
| S-141 | 143.0 | 80.5 | 81.0 | 1200 | 2-1/2 |
| S-280 | 147.0 | 87.0 | 83.0 | 1200 | 2-1/2 |
| S-252 | 168.0 | 96.0 | 78.0 | 1500 | 5 |

*Approximate

In Table 15, the dimensions of the shelters are listed along with the nominal designed weight-carrying capacities of the corresponding vehicle. In most cases the dimensions of the shelters are sufficient to contain somewhat more than the design weights. It will therefore generally be the vehicle weight hauling limitation which will determine how much equipment can be carried in a shelter. For example, the S-280 shelter, nominally designed for a 2-1/2 ton vehicle, could easily carry about 4-1/2 tons of equipment (giving a gross weight of 5 tons) without overcrowding. Such factors as whether or not personnel are to be stationed in the shelter, ease of maintenance, and equipment accessibility would indicate the desirability of using a larger shelter. Although larger shelters introduce a slight additional weight overhead, it is important that sufficient space be allowed for proper equipment weight distribution. Weight unbalance between the two sides of the shelter must be avoided while a low center of gravity must be maintained to avoid the danger of overturning during land transport.

## 6.3 ISMTC PHYSICAL REQUIREMENTS

Preliminary estimates of ISMTC physical requirements indicate that it may be possible to house the complex in as few as one or two shelters. Accurate size and weight estimates for the RF, BB and multiplex monitoring equipment are not possible without some sort of a preliminary equipment design effort. However, the processor, switch, CRT terminal, cassette tape unit, and low-speed printer should weigh about 400 lbs and require approximately 3,000 watts of power. This weight figure seems compatible with the typical standard shelters described in Table 15. Note that the overall weight and power requirement is obtained by adding the contributions from the RF, BB, and multiplex monitors, multiplex external to switch, display panel, DC supplies, A/C, heating, ventilation, etc.

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