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AFAL ltr, 6 Nov 1978

AFML-TR-75-160

IMPROVED CVD TECHNIQUES FOR DEPOSITING PASSIVATION LAYERS ON ICs

RCA LABORATORIES
PRINCETON, NEW JERSEY 08540

OCTOBER 1975

TECHNICAL REPORT AFML-TR-75-160
FINAL REPORT FOR THE PERIOD APRIL 1974 – JUNE 1975

AIR FORCE MATERIALS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio 45433

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This technical report has been reviewed and is approved for publication.

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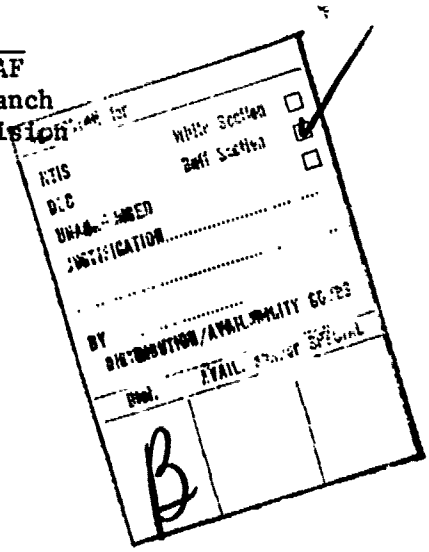

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: AFML-TR-75-160
2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle): IMPROVED CVD TECHNIQUES FOR DEPOSITING PASSIVATION LAYERS OF ICs,

5. TYPE OF REPORT & PERIOD COVERED: Final Report 22/4/74 - 30/6/75

6. PERFORMING ORG. REPORT NUMBER: PRRL-75-CR-38

7. AUTHOR(s): Werner Kern, A. Wayne Fisher, Robert B. Comizzoli, George L. Schnable

8. CONTRACT OR GRANT NUMBER(s): F33615-74-C-5146 NEW

9. PERFORMING ORGANIZATION NAME AND ADDRESS: RCA Laboratories, Princeton, New Jersey 08540

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: Project No. 7371, Task No. 74-1

11. CONTROLLING OFFICE NAME AND ADDRESS: Air Force Materials Laboratory, Wright-Patterson Air Force Base, Ohio 45433

12. REPORT DATE: October 1975

13. NUMBER OF PAGES: 256 p.

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Final rept. 22 Apr 74-30 Jun 75,

15. SECURITY CLASS. (of this report): Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Distribution limited to U. S. Government agencies only; (Test and Evaluation of military hardware); (October 1975). Other requests for this document must be referred to Air Force Materials Laboratory (LTE), Wright-Patterson AFB, Ohio 45433.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

16 AF-7371

17 737174

18. SUPPLEMENTARY NOTES

DDC RECEIVED MAR 19 1976 C

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Passivation glass
Integrated circuits
Chemical vapor deposition (CVD)
Phosphosilicate glass (PSG)
Aluminum corrosion
Glass densification
Process control methods
Film stress
Failure mechanisms

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the results of studies to increase the understanding of the requirements for successful glass passivation, by chemical vapor deposition (CVD), of metallized silicon planar integrated circuits (ICs) to improve both performance and reliability. The effects of various conditions for low-temperature (350° to 450°C) CVD of phosphosilicate glass (PSG) layers by oxidation of silane plus phosphine were correlated with the physical and chemical properties of deposited films. It is

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299 000

concluded that the important conditions to control are substrate temperature of deposition, oxygen-to-hydride ratio, hydride input, silane-to-phosphine ratio, and nitrogen input.

The composition and quality of passivation layers of commercially available ICs were determined to establish baseline CVD conditions. Detailed background information based on extensive literature surveys is provided on the state-of-the-art of passivation of ICs in the industry, on failure mechanisms in glass-passivated ICs, and on characteristics of equipment for deposition of passivation layers.

The fundamental properties of CVD PSG films were determined and correlated with mechanisms that can cause electrical degradation or catastrophic failure of ICs with inadequate CVD passivation; specifically, failure mechanisms of glass-passivated devices were induced on test devices using CVD films deposited by baseline conditions. Process conditions were established for achieving low stress films, and a new technique was devised for achieving further reduction in intrinsic tensile stress of CVD films. The effects of temperature and humidity on the bulk and surface electrical conductivity of SiO_2 and PSG films were determined and their implications to IC glass passivation were explored in detail. Devices with similar test patterns, fabricated by improved CVD conditions, were shown to have superior electrical stability, better ability to withstand thermal stresses, and lower catastrophic failure rates than baseline devices prepared by unsuitable CVD conditions, The comparison included structural and electrical tests, and stability of parameters during accelerated stress tests. A number of test patterns were used, each selected because of high sensitivity to the failure mechanism being investigated. Studies of corrosion of glass-passivated aluminum metallization under accelerated stress conditions of bias, temperature, and humidity demonstrated that devices were especially susceptible to failure due to cathodic aluminum corrosion when, simultaneously, cracks existed in the passivation layer and the phosphorus content of the PSG film was too high (8 wt % phosphorus).

Excessively low phosphorus content in CVD films was correlated with excessive intrinsic tensile stress leading to crack formation. CVD SiO_2 films containing no phosphorus were shown to be electrically inferior to PSG films containing a small percentage of phosphorus (e.g., 4 wt % phosphorus). Specific recommendations have been made for processing conditions for passivation of aluminum-metallized ICs with a PSG layer which is free of cracks and pinholes. Practical techniques for low-temperature densification of CVD PSG films were developed, and their compatibility with electrical properties of bipolar and MOS ICs was demonstrated.

Analytical process and materials control methods were examined, and refinements were made to seven of them, including etch rate, stress, x-ray fluorescence, and sheet resistance techniques. New methods were devised for analysis of overcoats on single IC chips.

A number of specific recommendations have been made on programs for future study. Data and conclusions derived from program studies have been disseminated in technical presentations and published papers.

The results of this program have significantly increased understanding of material and processing requirements for glass passivation of ICs; application of the findings to production of ICs will result in less lot-to-lot variation and significant improvement in device reliability.

PREFACE

This Final Report describes work performed from 22/4/74 to 30/6/75 in the Process and Applied Materials Research Laboratory of RCA Laboratories, Princeton, NJ, under Contract No. F33615-74-C-5146, Project No. 7371, Task No. 74-1. P. Rappaport is the Laboratory Director, G. L. Schnable is the Project Supervisor and Group Head, and Werner Kern is the Project Scientist. Additional members of the research team are Robert B. Commizzoli, A. Wayne Fisher, Kenneth W. Hang, Robert D. Vibronek, Ruth E. Allen, and Edward C. Tracy. The manuscript of this report was submitted by the authors on July 30, 1975.

Major areas of technical project assignments are as follows: R. B. Comizzoli - electronic research and electrical measurements; A. W. Fisher - stress and corrosion measurements; K. W. Hang - consulting on glass science; W. Kern - chemical vapor deposition and analytical studies; G. L. Schnable - stress and corrosion theory; R. E. Allen, E. C. Tracy, and R. D. Vibronek - technical assistance.

The contract has been administered under the technical direction of Major R. Bellem (AFML/LTE), Air Force Materials Laboratory, Wright-Patterson Air Force Base, Ohio. Dr. D. Hutchens was government project monitor during most of the contract period. This program was partially funded by the Rome Air Development Center, Reliability Branch.

It is a pleasure to acknowledge the help of a number of individuals who have contributed to this work by the performance of several analytical techniques: A. Decker - gas mass spectrometry; B. L. Goydish, L. R. Schneid, and J. Sabo - wet chemical analysis; R. J. Paff - X-ray fluorescence analysis; H. H. Whitaker - atomic spectroscopy; G. R. Auth - surface profilometry; B. J. Seabury - scanning electron microscopy; and E. M. Botnick - solids mass spectrometry. We acknowledge the able assistance of R. D. Vibronek - CVD and etch rate measurements; R. E. Allen - electrical measurements; and E. C. Tracy - examination of structural defects. We also wish to thank G. H. Hughes for providing us with the SHBD ramp generator, and M. Polinsky for supplying corrosion test patterns and photomasks.

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SUMMARY

This report describes in detail the results of a program of materials studies to increase the understanding of the requirements for successful glass passivation by chemical vapor deposition (CVD) of metallized silicon planar integrated circuits (ICs) to improve both IC performance and reliability. The effects of various conditions for low-temperature (350° to 450°C) chemical vapor deposition of phosphosilicate glass (PSG) layers by oxidation of silane plus phosphine correlated with the physical and chemical properties of deposited PSG films. It was concluded that the important conditions to control are substrate temperature of deposition, oxygen-to-hydride ratio, hydride input, silane-to-phosphine ratio, and nitrogen input.

The composition and quality of passivation layers on several type of commercially available ICs was determined, and baseline CVD conditions were established to produce a range of glass compositions which bracketed those found in commercial ICs manufactured in the last several years.

Detailed background information is provided on the state-of-the-art of passivation of ICs in the industry, on failure mechanisms in glass-passivated ICs, and on characteristics of equipment for deposition of passivation layers.

The fundamental properties of CVD PSG films were determined, and were correlated with mechanisms that can cause electrical degradation or catastrophic failure of ICs with inadequate CVD passivation. Excessive tensile stress in deposited glasses was correlated with crack formation over aluminum metallization. Process conditions were established for achieving low stress films, and a new technique was demonstrated for achieving further reduction in intrinsic tensile stress of CVD films.

The effects of temperature and humidity on the bulk and surface electrical conductivity of SiO_2 and PSG films were determined. The surface conductivity of CVD films in moist ambients was shown to be orders of magnitude greater than the sheet conductivity through the bulk of the CVD films. Thus, in moist ambients, leakage currents between adjacent metal lines in CVD passivated devices with cracks in the glass are very much higher than in devices of similar geometry, but without cracks.

Specific failure mechanisms of glass-passivated devices were demonstrated on test devices using CVD films deposited by baseline conditions. Test devices were also fabricated using improved CVD processing conditions; these were compared with similar test devices prepared using baseline CVD passivation conditions. Devices with similar test patterns, fabricated by improved CVD conditions, were shown to have superior electrical stability, better ability to withstand thermal stresses, and lower catastrophic failure rates than baseline devices prepared under unsuitable CVD conditions. The comparison included structural and electrical tests, and stability of parameters during accelerated stress tests. A number of test patterns were used that had been selected because of high sensitivity to the failure mechanism being investigated.

Studies of corrosion of glass-passivated aluminum metallization were made under accelerated stress conditions of bias, temperature, and humidity. It was shown that devices were especially susceptible to failure due to cathodic aluminum corrosion when, simultaneously, cracks existed in the passivation layer and the phosphorus content of the PSG film was too high (8% phosphorus by weight).

Excessively low phosphorus content in CVD films (less than 1% phosphorus by weight) was correlated with excessive intrinsic tensile stress which led to crack formation. CVD SiO_2 films containing no phosphorus were shown to be electrically inferior to PSG films containing a small percentage of phosphorus (for example, 4% phosphorus by weight).

Specific recommendations have been made for processing conditions for passivation of aluminum-metallized ICs with a PSG layer that is free of cracks and pinholes.

Practical techniques for low-temperature densification of CVD PSG films were developed, and the compatibility of such techniques with bipolar and MOS integrated circuit electrical properties was demonstrated.

Analytical process and materials control methods were examined, and refinements were made in a number of procedures, including etch rate, stress, x-ray fluorescence, and sheet resistance techniques. New methods were devised for analysis of overcoats on single IC chips.

A number of specific recommendations have been made on programs for future study. Included are programs to implement in production the findings of this

program, to improve the passivation of gold-metallized ICs, and to provide low-temperature passivation layers that are effective moisture and alkali ion barriers.

Data and conclusions derived from program studies have been disseminated in two invited technical presentations and two published papers; several additional papers are being prepared for submission for publication.

We believe that the results of this program have significantly increased understanding of material and processing requirements for glass passivation of ICs, and that application of the findings of this program to production of ICs will result in less lot-to-lot variation and significant improvement in the reliability of devices. For the benefit of the busy reader we have listed below the major accomplishments under this contract.

MAJOR ACCOMPLISHMENTS

1. Established effects of ten *critical CVD conditions* on PSG properties.
2. Determined the effect of temperature and humidity on *bulk and surface conductivity* of PSG films.
3. Elucidated *cathodic corrosion mechanism* of glassed aluminum conductor lines.
4. Demonstrated interrelationship of *intrinsic stress and cracking* of CVD films.
5. Achieved *fundamental understanding* of both materials and processing aspects of CVD glass passivation for ICs.
6. Invented new technique for *lowering intrinsic stress* in CVD films.
7. Innovated practical *low-temperature catalytic densification* process for PSG overcoats.
8. Examined and compared analytical *process and materials control methods.*
9. Refined several control methods based on: *etch rate; stress; x-ray fluorescence; sheet resistance.*
10. Devised new *micromethods* for analysis of overcoats on single IC pellets.
11. Analyzed and compared overcoats on *commercial IC products.*
12. Defined and classified dielectric-related *failure modes* of ICs.
13. Categorized *commercial CVD equipment* on basis of operating principles.
14. Surveyed in depth current *passivation technology* for all silicon devices.
15. *Disseminated results* in 2 symposium presentations, 2 published papers, 2 submitted papers, and several technical reports to be published.
16. Recommended *optimized processing conditions* to achieve successful IC overcoat passivation.

I. INTRODUCTION

A. BACKGROUND AND DEFINITIONS

The terms "glassing" and "glass passivation" are commonly used to denote the process in which a glass-like, amorphous, inorganic dielectric layer is formed over the surface of a completed microcircuit wafer for the purpose of ambient protection. The sequence for glass passivation consists of deposition of the dielectric layer over the entire surface of the device wafer with completed metallization patterns, followed by photolithographic delineation to remove glass from the central region of bonding pads and from scribe line areas. Typical deposited films are 0.5 to 2 μm thick.

The majority of modern integrated circuits (ICs) are metallized with aluminum. A compatible glass passivation process must therefore be performed under conditions where the maximum processing temperature is below the Al-Si eutectic temperature (577°C) to avoid alloying or metallization melting problems. Similar considerations hold for metallization systems involving gold. Chemical vapor deposition (CVD) of dielectric films at low temperature (300 to 500°C) is ideally suited to fulfill these requirements. Reactive sputtering, rf sputtering, and plasma deposition techniques can also be used for depositing dielectric layers, but their use is generally limited to certain applications, and to devices that are not degraded by these treatments.

Superficially considered, glass passivation may appear to be a simple process. In principle it is, but there are several critical steps that must be recognized to ensure successful implementation and effective use with the present-day sensitive and highly complex silicon devices. Glassing of microcircuit wafers was originally used to provide a mechanical protection against scratches of the soft aluminum interconnect lines. Vitreous silicon dioxide (SiO_2) prepared by CVD was first applied as the passivating glass, and is still being used by a number of IC manufacturers. However, to provide effective protection, a SiO_2 film thickness incompatible with the aluminum metallization is required, and cracking of the oxide film will result, with consequent problems of device reliability. Device manufacturers who have recognized these shortcomings have substituted more compatible lower-stress films of binary silicate glasses, especially phosphosilicate glass (PSG) films, for the

more highly stressed SiO_2 layers. However, before work on this contract was started, various problems associated with this promising approach remained and adversely affected the reliability, performance, and production yield of ICs. It was clear that a systematic investigation was needed to examine these problems and find suitable solutions.

B. OBJECTIVES OF RESEARCH PROJECT

The overall objective of the program was to gain an increased understanding of the material and processing requirements for successfully glass-passivating silicon planar metallized integrated circuits to improve both reliability and performance.

Specific research and development tasks have included the following: (1) Refining of processing conditions for glassing of aluminum-metallized IC wafers with PSG and SiO_2 layers, singly and in combination, that are free of microcracks and pinholes, to serve as mechanical scratch protection and passivation coating. The process technology was to be based mainly on production-type chemical vapor deposition conditions. A minimum of ten deposition parameters was to be investigated systematically for optimization. (2) Establishing a fundamental understanding of the material aspects of glass passivation of ICs including glass type, composition and densification effects, and dielectric layer combinations and thicknesses to provide defect-free and low-stress glass coatings. (3) Developing a fundamental understanding of dielectric- or glassing-related failure modes of glass-passivated ICs by studying passivated test wafers structurally, chemically, and electrically to identify failure mechanisms which have been attributed to inadequate CVD passivation. (4) Devising practical process and materials control tests to ensure glass properties within a realistic optimum range.

C. ORGANIZATION OF REPORT

Because of the volume of the work performed in the contract study reported here, an effort has been expended to make the various sections of the report self-explanatory. The reader who is interested only in particular information should find this helpful. Most of the material presented in the

various sections is interrelated. However, the separate treatment of the subject matter in self-contained sections according to specific disciplines should make the report easier to read and utilize.

The main sections consist of (1) a discussion of passivation materials and their functions, and processes to prepare them; (2) experimental results of CVD parameters, and parameter effects on deposition rate and film composition; (3) film stress as a function of CVD conditions and post-deposition treatments; (4) film densification studies at low temperature; (5) electrical measurements of bulk, surface, and interface dielectric properties, and a study of passivation layer-related IC failure mechanisms; (6) structural and electrical measurements of induced aluminum corrosion; and (7) presentation of experimental results on development work for analytical process control methods. Additional material has been provided in the appendices.

In some cases, for the sake of completeness or to provide desirable background information, this report contains results generated during RCA-supported research programs of thin-film dielectrics, CVD deposition systems, analytical method development, silicon device failure mechanisms, and extensive literature surveys related to these topics.

References to the primary literature are given as footnotes in *abbreviated* form to aid the microform reader and as a list, with titles of papers, beginning on page 161. References in the appendices, again, are given as footnotes where appropriate and are listed at the end of each appendix, if extensive. Appendices A and E, having been previously published, are included herein as reprints so that the references appear *only* at the end of the text.

II. TYPES, FUNCTIONS, AND PREPARATION OF PASSIVATION COATINGS

A. TYPES OF PASSIVATION COATINGS

Passivation coatings are widely used to improve the performance and reliability of silicon devices of various types, ranging from discrete mesa-type diodes and transistors to complex planar integrated circuits, and including both hermetic and plastic-encapsulated devices.

Passivation coatings may be classified as primary if they are directly in contact with the single-crystal silicon from which the device is fabricated, and as secondary if they are separated from the device by an underlying dielectric layer. The primary passivation layer provides good dielectric properties, low surface recombination velocity, controlled immobile charge density, and device stability at elevated temperatures under bias or operating conditions. The secondary passivation layer provides additional stability in various ambients and serves as getter, impurity barrier, or mechanical shield.

The comprehensive survey paper presented in Appendix A reviews the entire field of silicon device passivation and serves as a source of general background material in the present work [1]. It surveys primary and secondary passivation materials and the techniques used to obtain them, including thermal oxidation, high-temperature diffusion, low-temperature deposition of SiO_2 and binary silicates, deposition of alkali barrier-type layers, and deposition of glass frit followed by fusion. The effect of passivation layers on silicon device reliability is discussed, and the interrelationship between the technique used for final encapsulation, the passivation layers used, and device reliability is indicated. Emphasis is given to those processes and materials that are widely used to fabricate semiconductor devices in production facilities, rather than to processes used only to fabricate exploratory developmental devices.

The main portion of this technical report is concerned specifically with the application of chemical vapor deposition (CVD) for producing passivating

1. G. L. Schnable, W. Kern, and R. B. Comizzoli, J. Electrochem. Soc. 122, 1092 (1975); see Appendix A.

and protective layers suitable for overcoating aluminum-metallized silicon semiconductor devices in finished wafer form. Discussions are confined to the two materials of major importance in overcoat passivation, i.e., SiO_2 and PSG (phosphosilicate glass) deposited by thermally activated oxidation of the hydrides. These materials can be deposited in high quality at the low temperature prerequisite with aluminum-metallized silicon devices. Their functional requirements are summarized in Table 1.

Table 1. Functional Requirements of IC Passivation Overcoat Layers

No.	Functional Requirement
1	Mechanical and chemical protection for metallization interconnects
2	Diffusion barrier or gettering agent for ionic contaminants and other external impurities
3	Good adherence to metallization and primary passivating layers
4	Low stress from all causes
5	Good chemical and physical stability
6	Low defect density
7	Inertness toward metallization and other structural device components
8	High dielectric strength and electrical resistance
9	Low dissipation factor
10	Low mobile or trapped charge density
11	Isolation of electrical charge effects external to semiconductor
12	Sufficiently matching thermal expansion with device component materials
13	Reduce or maintain semiconductor surface state density
14	Moderately high dielectric constant to contain junction fringing field
15	Ease of preparation and subsequent processing
16	Ease of formability into patterns by photolithography and etching
17	Compatibility with plastic encapsulating materials

B. USES AND BENEFITS OF GLASS PASSIVATION OVERCOATS

Primarily, passivating overcoats provide protection against scratching of the vulnerable interconnect metallization during chip handling, ensure immunity to effects of loose conductive particles in hermetic packages, improve device stability in various ambients, lower susceptibility to metal corrosion and electromigration, and reduce effects of ion motion on the device surface. PSG has, in addition, alkali gettering capability which is of great importance in passivation and stabilization of devices, and exhibits less stress (tensile) than layers of CVD SiO_2. The effectiveness of PSG for gettering alkali ions is particularly advantageous for MOS ICs because of their increased surface sensitivity as compared with that of digital bipolar ICs.

Alkali gettering capability is also of great importance for devices enclosed in ceramic packages that are sealed by fusion of glass frits. These frits usually contain large amounts of sodium which is emitted during fusion into the ambient of the package enclosure. Encapsulating plastic formulations are also a source of ions and other impurities that must be prevented from penetrating into the sensitive device regions. A summary of benefits and advantages achieved by IC glass passivation by CVD overcoat layers for the vast majority of IC types is presented in Table 2. It is clear from these considerations that passivating overcoat layers constitute an important step in manufacturing ICs of high reliability and improved performance.

C. CHEMICAL VAPOR DEPOSITION

Chemical vapor deposition is a process by which gases or vapors are chemically reacted, leading to formation of a solid-phase reaction product on a substrate surface. Activation of the chemical reaction is most commonly effected by heating of the substrate. CVD is employed extensively in semiconductor device technology, for example, in the epitaxial deposition of single-crystal semiconductors, silicon nitride impurity-barrier films, oxide and nitride dielectric films, doped oxide layers as diffusion sources, silicate glasses for passivation, and, in some instances, metal films as conductor elements.

Table 2. Benefits of IC Glass Passivation by CVD Overcoat Layers

No.	Benefit
1	Gettering or immobilizing of harmful alkali ions (PSG)
2	Decreasing instabilities due to surface ionic drifts or horizontal surface-ion migration
3	Protection against metal corrosion
4	Suppression of electromigration susceptibility
5	Suppression of defect formation in aluminum metallization
6	Reducing penetration of moisture, gases, and chemical species from the outside, including components from the plastic encapsulating material forming the package
7	Quenching of fast states to lower leakage currents
8	Improved protection against high-energy electromagnetic radiation
9	Mechanical scratch protection during wafer and dice processing
10	Prevention of shorts from loose conducting particles in hermetic packages
11	Added reliability safety-margin for hermetic ICs developing leaks
12	Compatibility with many types of thin-film resistors used on ICs
13	Other benefits including general increase in device reliability and yield due to decreased failure rate and susceptibility to electrical instabilities

Theoretical and practical aspects of chemical vapor deposition processes have been treated extensively in several recent reviews [2-11].

The advantages and disadvantages of the CVD technique for device glassing are listed in Table 3. A survey of CVD reactor systems for depositing passivation coatings is presented in Appendix B.

D. BASIC CVD HYDRIDE REACTIONS

The basic process for depositing SiO_2 films from silane and oxygen at low temperatures (250° to 550°C) was reported in 1967 [12]. The exact details of this thermally activated, surface-catalyzed, heterogeneous branching-chain reaction are complex, but the overall reaction can be expressed as

$$SiH_4(g) + 2O_2(g) \rightarrow SiO_2(s) + 2H_2O(g) \quad (1)$$

but under some circumstances it may proceed as

$$SiH_4(g) + O_2(g) \rightarrow SiO_2(s) + 2H_2(g) \quad (2)$$

2. C. F. Powell, J. H. Oxley, and J. M. Blocher, Jr., Eds., *Vapor Deposition* (John Wiley & Sons, New York, 1966).
3. W. M. Feist, S. R. Steele, and D. W. Ready, in *Physics of Thin Films*, Vol. 5, G. Hass and R. E. Thun, Eds., (Academic Press, New York and London, 1969), pp. 237-314.
4. D. S. Campbell in *Handbook of Thin Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw-Hill Book Company, New York, 1970), pp. 5-1 to 5-25.
5. J. A. Amick and W. Kern, in *Chemical Vapor Deposition*, J. M. Blocher, Jr., and J. C. Withers, Eds. Second Intn'l Conf., The Electrochem. Soc., New York (1970), pp. 551-570.
6. T. L. Chu, J. Vac. Sci. and Technol. 6, 25 (1970).
7. RCA Review, Special Issue on Chemical Vapor Deposition of Electronic Materials, RCA Review 31, No. 4 (1970).
8. E. L. MacKenna, Proc. 1971 Semicond./IC Proc. and Prod. Conf., pp. 71-83, Ind. and Sci. Conf. Mtg., Chicago, Ill. (1971).
9. *Chemical Vapor Deposition* (International Conferences): J. M. Blocher, Jr., and J. C. Withers, Eds. - Second Intn'l Conf., The Electrochem. Soc., Inc., New York (1970); F. A. Glaski, Ed. - Third Intn'l Conf., The American Nuclear Soc., Hinsdale, Ill. (1972); G. F. Wakefield and J. M. Blocher, Jr., Eds. - Fourth Intn'l Conf., The Electrochem. Soc., Inc., Princeton, N.J. (1973).
10. T. L. Chu and R. K. Schmeltzer, J. Vac. Sci. Technol. 10, 1 (1973).
11. J. J. Tietjen, in *Ann. Rev. of Materials Science*, Vol. 3 (1973), R. A. Huggins, R. H. Bube, and W. Roberts, Eds., (publ. by Annual Reviews), pp. 317-326.
12. N. Goldsmith and W. Kern, RCA Review 28, 153 (1967).

Table 3. Advantages and Disadvantages of CVD Techniques for Preparing Passivation Overcoat Layers

No.	Advantages
1	Low deposition temperature
2	High chemical purity of deposited layers
3	Wide choice of compositions
4	Ease of preparing a variety of layered structures
5	Desirable physical and chemical film properties
6	Ease of thickness control
7	Good uniformity of film thickness and composition
8	Good adherence to oxides and aluminum
9	High-resolution patterns can be readily formed in layers by photolithography
10	Economical and practicable on a production scale
11	Process can be automated
	Disadvantages
1	Particulate impurities from the reaction must be minimized
2	Toxicity of reactants requires safety measures
3	Accurate control of gas flows needed

The reaction favored depends strongly on deposition temperature and silane concentration [12-16], and probably also on the oxygen-to-hydride ratio and variations in reactor geometry.

13. H. J. Emeleus and K. Stewart, J. Chem. Soc. (London), Part I: 1182 (1935).
14. T. L. Chu, J. R. Szedon, and G. A. Gruber, Trans. Met. Soc. AIME 242, 532 (1968).
15. K. Strater, RCA Review 29, 618 (1968).
16. B. J. Baliga and S. K. Ghandhi, J. Appl. Phys. 44, 990 (1973).

Phosphorus can be incorporated into the oxide layers as an oxide of phosphorus by the reaction of phosphine with oxygen:

$$2PH_3(g) + 4O_2(g) \rightarrow P_2O_5(s) + 3H_2O(g) \qquad (3)$$

forming phosphosilicates [16-26]. Specific effects of CVD parameters on the reaction chemistry are discussed in Section III.

E. COMPATIBILITY OF DEPOSITION TEMPERATURE WITH METALLIZATION

The theoretical maximum temperature which can be used in processing devices metallized with aluminum is limited by the melting point of the eutectic formed between silicon and aluminum 577°C). In practice, however, the maximum temperature during glass deposition is held below 500°C because solid-state reactions between aluminum and silicon begin to exert degrading effects in many sensitive devices at approximately 500°C. Some reaction of aluminum with SiO_2 or PSG can be detected in certain devices at temperatures as low as 400°C, forming a thin intermediate layer of aluminosilicate, but normally this presents no serious problems if proper etching techniques are used in delineation of the glass layer to expose the bonding pads and scribe lines.

Problems associated with corrosion, edge effects, stress, and expansion mismatches between aluminum and the passivation overcoats have been discussed in Ref. 1. An up-to-date bibliography of many other related aspects of aluminum and other metallization for silicon devices became available recently [27].

17. W. Kern and R. C. Heim, Electrochem. Soc. Ext. Abstr. 5, 234 (Spring 1968).
18. A. W. Fisher, et al., RCA Review 29, 533 (1968).
19. A. W. Fisher and J. A. Amick, RCA Review 29, 549 (1968).
20. K. Strater and A. Mayer, in *Semiconductor Silicon*, R. R. Haberecht and E. L. Kern, Eds., (The Electrochem. Soc., New York, 1969), pp. 469-480.
21. T. Tokuyama, T. Miyazaki, and M. Horiuchi, in *Thin Film Dielectrics*, F. Vratny, Ed., (The Electrochem. Soc., New York, 1969), pp. 297-326.
22. W. Kern and R. C. Heim, J. Electrochem. Soc. 117, 562 (1970).
23. W. Kern and R. C. Heim, J. Electrochem. Soc. 117, 568 (1970).
24. W. Kern and A. W. Fisher, RCA Review 31, 715 (1970).
25. M. M. Schlacter, et al., IEEE Trans. Electron Devices ED-17, 1077 (1970).
26. G. L. Schnable, IEEE '71 Intn'l Conv. Digest, pp. 586-587 (1971).
27. J. L. Vossen, A. W. Stephens, and G. L. Schnable, *Bibliography on Metallization Materials and Techniques for Silicon Devices*, Monograph #2, Thin Film Division, American Vacuum Society (1974).

F. LAYER COMBINATIONS

Combinations of PSG and SiO_2 layers can offer distinct advantages over any one single layer. Structures consisting of SiO_2 over PSG, or of SiO_2/PSG/SiO_2, can be readily prepared by CVD techniques, often in one continuous operation, simply by regulating the hydride input in the gas stream [22]. A thin (1000-Å) CVD SiO_2 top layer over the phosphosilicate main layer of 0.6- to 1.5-μm thickness is desirable for improved photoresist adherence and consequently improved pattern etching definition, unless organo-silane adhesion-promoting agents are used.

G. DENSIFICATION TREATMENTS

Heat treatments of CVD layers under conditions compatible with the temperature limitation of the metallized devices can improve the quality of the passivation overcoat [28]. Techniques to achieve this with PSG and SiO_2 overcoats, and their evaluation by etch rate analytical techniques [29], are presented separately in a subsequent section.

H. GLASSING-RELATED FAILURE MECHANISMS

Failure mechanisms that are related to the dielectric or to glass overcoating of metallized ICs can be caused by homogeneous or localized structural or compositional defects in the dielectric, by chemical interactions of dielectric with metallization, or by ionic or electronic charge motion in the dielectric.

Many of these defects arise from improper processing or from inherent mutual incompatibility of the films with the metallization. It is important that they be detected and identified so that steps can be taken to eliminate them. A discussion of each of these failure modes is presented in Appendix C.

28. W. Kern, J. Electrochem. Soc. 116, 251C (Abstract) (1969).
29. W. Kern, RCA Review 29, 557 (1968).

III. EFFECTS OF CVD PARAMETERS ON FILM GROWTH AND PROPERTIES

A. SUMMARY OF CRITICAL FACTORS

The exact conditions used in the CVD process for SiO_2 and PSG films can critically affect important film properties. Primary CVD parameters that affect deposited film properties, and must therefore be carefully optimized and controlled, include the following, listed in their approximate order of importance:

(1) Substrate temperature of deposition
(2) Oxygen-to-hydride ratio
(3) Hydride flow rate
(4) Silane-to-phosphine ratio
(5) Nitrogen flow rate
(6) Geometry of reaction chamber and gas inlet/outlet configurations
(7) Wall temperature of reaction chamber or gas disperser
(8) Cleanliness of CVD system and purity of gases
(9) Nature and cleanliness of substrate surface
(10) Surface topography of substrate

B. EFFECTS OF CVD CONDITIONS

The effects of these factors on the film deposition rate, the film uniformity, and the film composition (in the case of PSG) are discussed in this section in some detail, and are illustrated with experimental results obtained during this investigation. Experimental studies of the effects of important CVD parameters on stress, density, electrical conductance, dielectric properties, and other film properties will be discussed in subsequent sections. These film properties will be examined before and after various kinds of treatments and tests following the film deposition.

C. EXPERIMENTAL DATA, RESULTS, AND DISCUSSION

1. Gases, Equipment, and Methods

Semiconductor-grade 3.3 vol % SiH_4 and electronic-grade 1.0 vol % PH_3, both in ultra-high-purity N_2, were used in this work. Several premixed hydride compositions in nitrogen were also used in which the ratios of SiH_4:PH_3 were 6, 12, 23, and 60:1, respectively. The oxidant was O_2 of 99.9% purity, and the diluent was N_2 of 99.998% purity, both filtered through submicron filters.

The single-rotation vertical CVD reactor described in Appendix D was used with the glass deposition chamber, unless otherwise noted. The hydrides and N_2 were introduced through the center inlet at the top of the chamber after having passed through a terminal submicron large-area filter. The O_2 was added to this gas stream before it entered the deposition chamber. Surface temperatures were measured with bimetallic- and thermocouple-type surface thermometers. Other details on deposition technology were similar to those reported in previous papers [22-24].

A variety of substrate materials was used for film deposition, but most of the work reported in this section was carried out with polished and chemically cleaned (100)-oriented single-crystal silicon slices of 5-cm diameter and 0.3-mm thickness.

Film thicknesses were measured by interferometric and profilometric techniques. The PSG composition was routinely analyzed by etch rate measurements after densification of the films, and by x-ray fluorescence methods, which were both calibrated by wet chemical analysis. These methods, and the calibration graphs used, are described in Section VIII under analytical process control methods.

2. Effects of Temperature and Oxygen-to-Hydride Ratio

The effects of substrate temperature of deposition and O_2:hydride ratio are closely interrelated and are therefore best considered in the same context for both SiO_2 and PSG films. The effects on the deposition rate of SiO_2 and PSG are similar, and the composition of PSG is strongly dependent on both of these parameters.

We have previously shown [12] that SiH_4 diluted with N_2 begins to form SiO_2 films at a temperature of about 240°C if the O_2:SiH_4 ratio is in the range of 3:1. The rate of film growth at constant SiH_4 input increases rapidly as the substrate temperature is increased to 310°C. Further temperature increase to 450°C results in a very gradual increase in deposition rate. To attain a linear increase in the maximum deposition rate with temperature, the O_2:SiH_4 ratio must be increased as the temperature is increased. For example, at 475°C, an O_2:SiH_4 ratio of at least 14:1 is required to achieve this. Larger ratios of up to 33:1 have no effect, but ratios beyond this limit inhibit the reaction, leading to decreased rates of film growth. Thus, a plateau region exists at this temperature that is insensitive to the O_2:SiH_4 ratio. Temperatures lower than 475°C require a progressively smaller O_2:SiH_4 ratio to attain the plateau of maximum SiO_2 deposition rate. At the same time the extent of the plateau region narrows as the temperature is decreased. These observations have since been confirmed by several other workers [15,16,30] and were found to hold qualitatively even though different reactor geometries were used. The unusual reduction in SiO_2 deposition rate at high O_2:SiH_4 ratios has been explained by retardation theory where O_2 acts as the retardant by being adsorbed on the substrate [16].

The corresponding observations for PSG formation by co-oxidation of SiH_4 + PH_3 with O_2 are essentially analogous to those discussed for SiO_2 [16,20,31]. Figure 1 shows plots of typical data we obtained studying the effect of O_2:hydride ratio on the deposition rate of PSG at 300°, 350°, and 450°C. The SiH_4:PH_3 ratio was fixed at an intermediate value of 20:1, and the total gas flow rate was held constant at 11 liters per minute. The rate of PSG film deposition clearly depends on both the O_2:hydride ratio and the substrate temperature during deposition. The maximum deposition rate obtainable at a given temperature is a function of the O_2:hydride ratio. As the temperature is increased, the maximum deposition rate increases, but requires progressively larger O_2:hydride ratios to be attained. The semi-log plot in Fig. 1 indicates,

30. M. L. Hammond and G. M. Bowers, Trans. Met. Soc. AIME 242, 546 (1968).
31. M. Shibata and K. Sugawara, J. Electrochem. Soc. 122, 155 (1975).

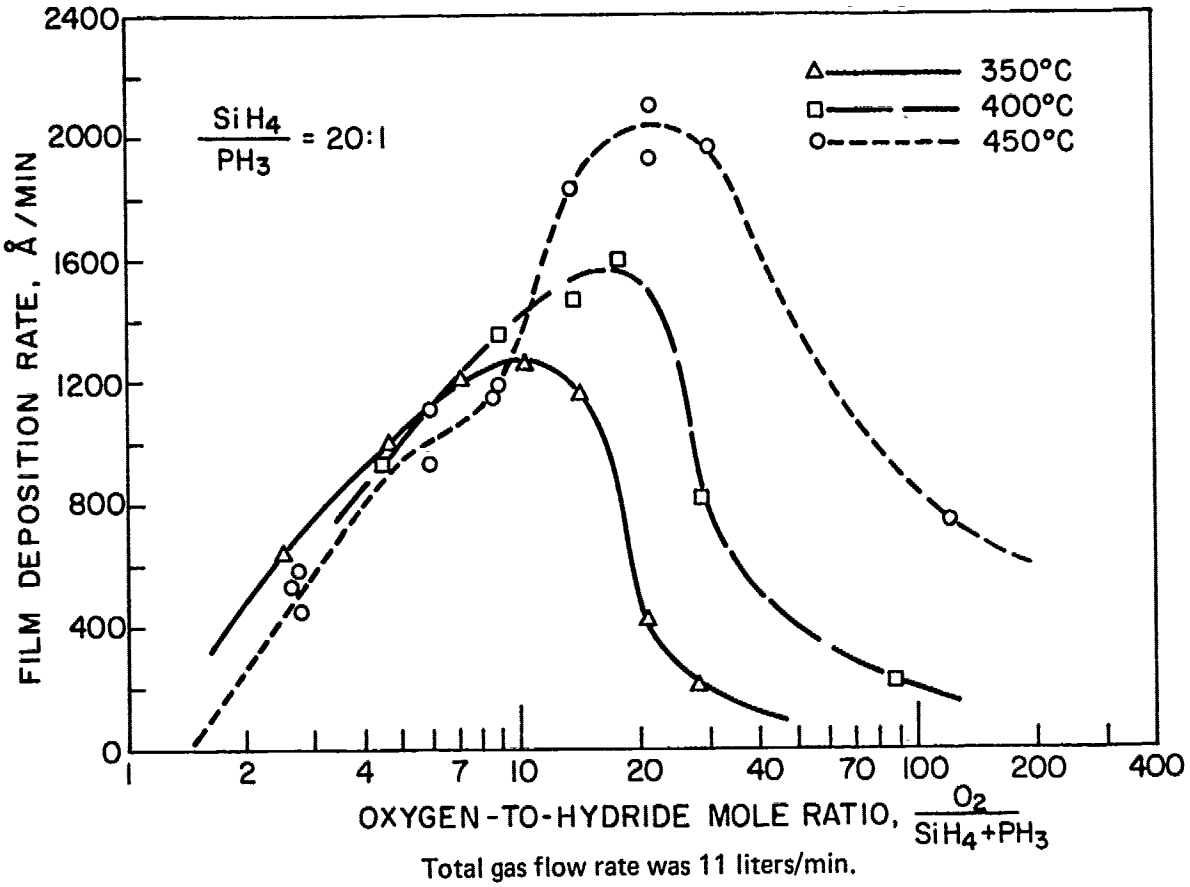


Figure 1. PSG film deposition rate vs oxygen/hydride ratio for three deposition temperatures.

furthermore, that the ratio range of the maximum region widens with increasing temperature.

Figure 2 depicts the effects of O_2:hydride ratio and temperature on the composition of PSG films, for the same samples and CVD conditions from which the deposition rate results in Fig. 1 were obtained. The phosphorus concentrations in the glass films generally increase with both increasing O_2:hydride ratio and with decreasing temperature. The phosphorus content of the PSG films deposited at 450°C is less critically dependent on the ratio than in the films deposited at lower temperature, making the higher temperature considerably more desirable from a practical point of view, especially since the level-concentration range occurs within the O_2:hydride ratio range of 17 to 30, which also coincides with the range of maximum film deposition rate.

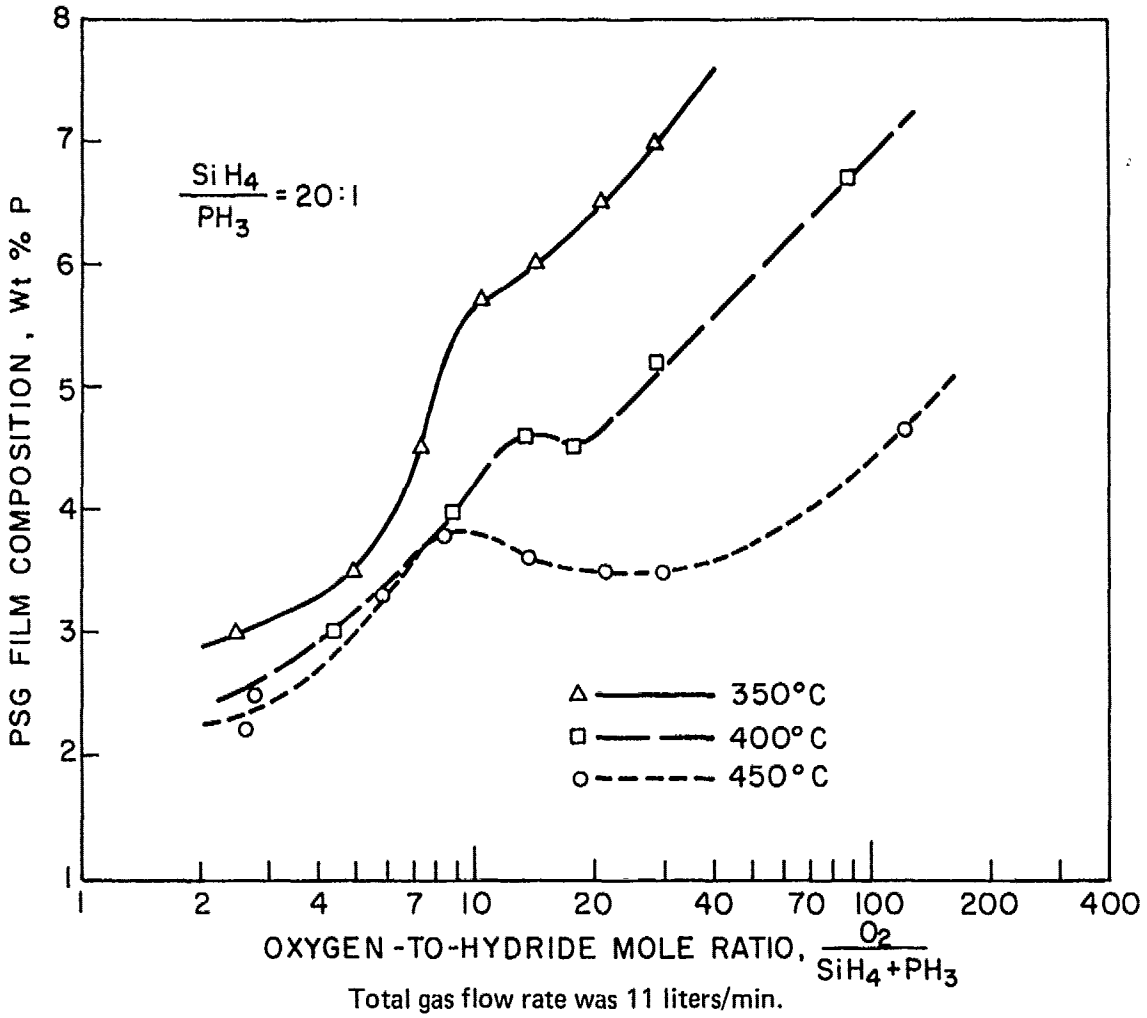


Figure 2. PSG film composition vs silane/hydride ratio for three deposition temperatures.

The effects of substrate deposition temperature for fixed O_2:hydride ratios are illustrated more directly in Figs. 3 and 4; they were both derived from Figs. 1 and 2.

Figure 3 shows the PSG film deposition rate at 350, 400, and 450°C as a function of selected O_2:hydride ratios (4, 6, 10, 24, and 30:1) and also for the ratios corresponding to the maximum deposition rate for each of the three temperatures. The curves exhibit negative slopes for the low ratios and change to positive slopes for the higher ratio. The curves indicate that the deposition rates at all three temperatures are similar for any one ratio in the lower range of 4:1 to 10:1 (not drawn for clarity) but differ increasingly

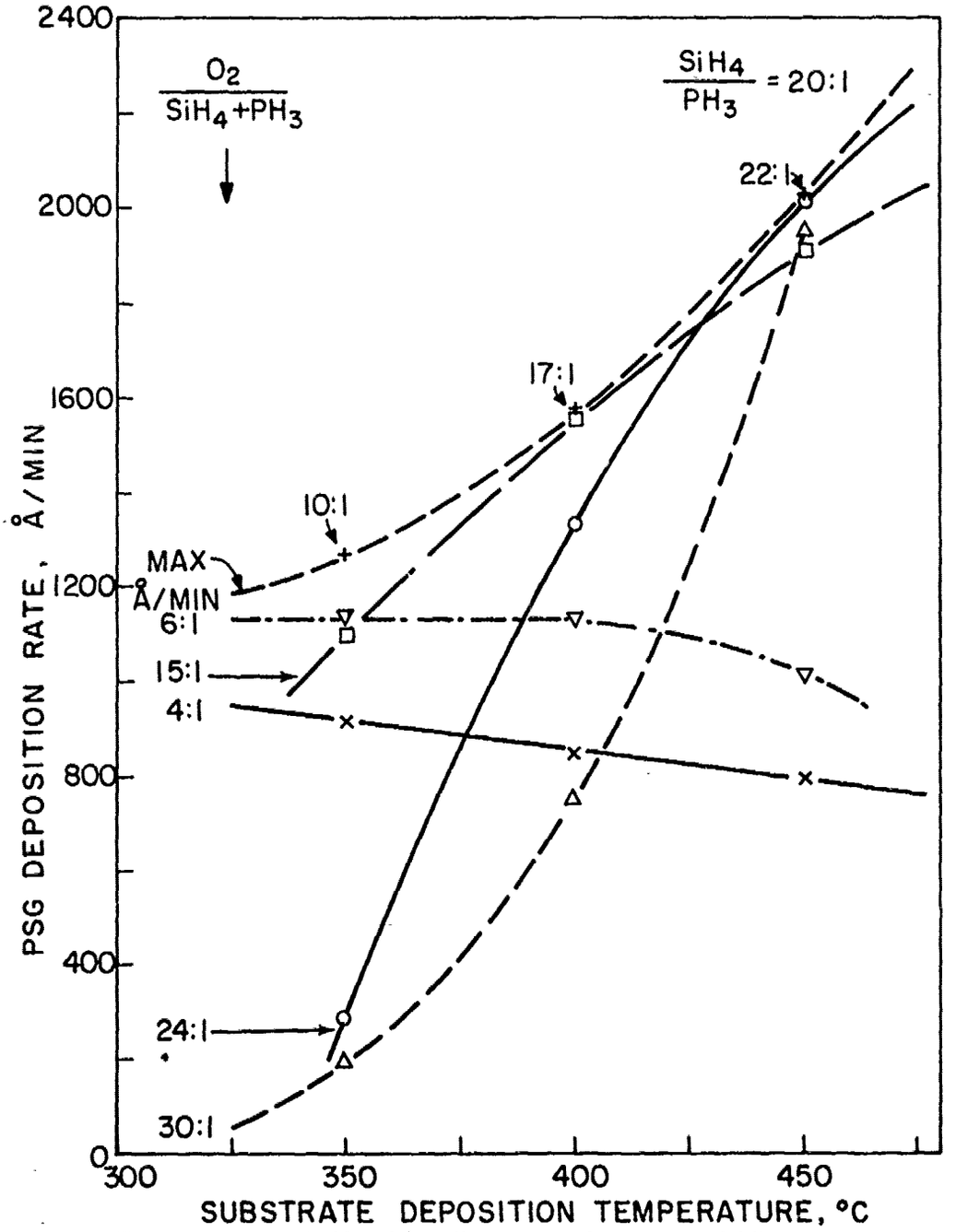
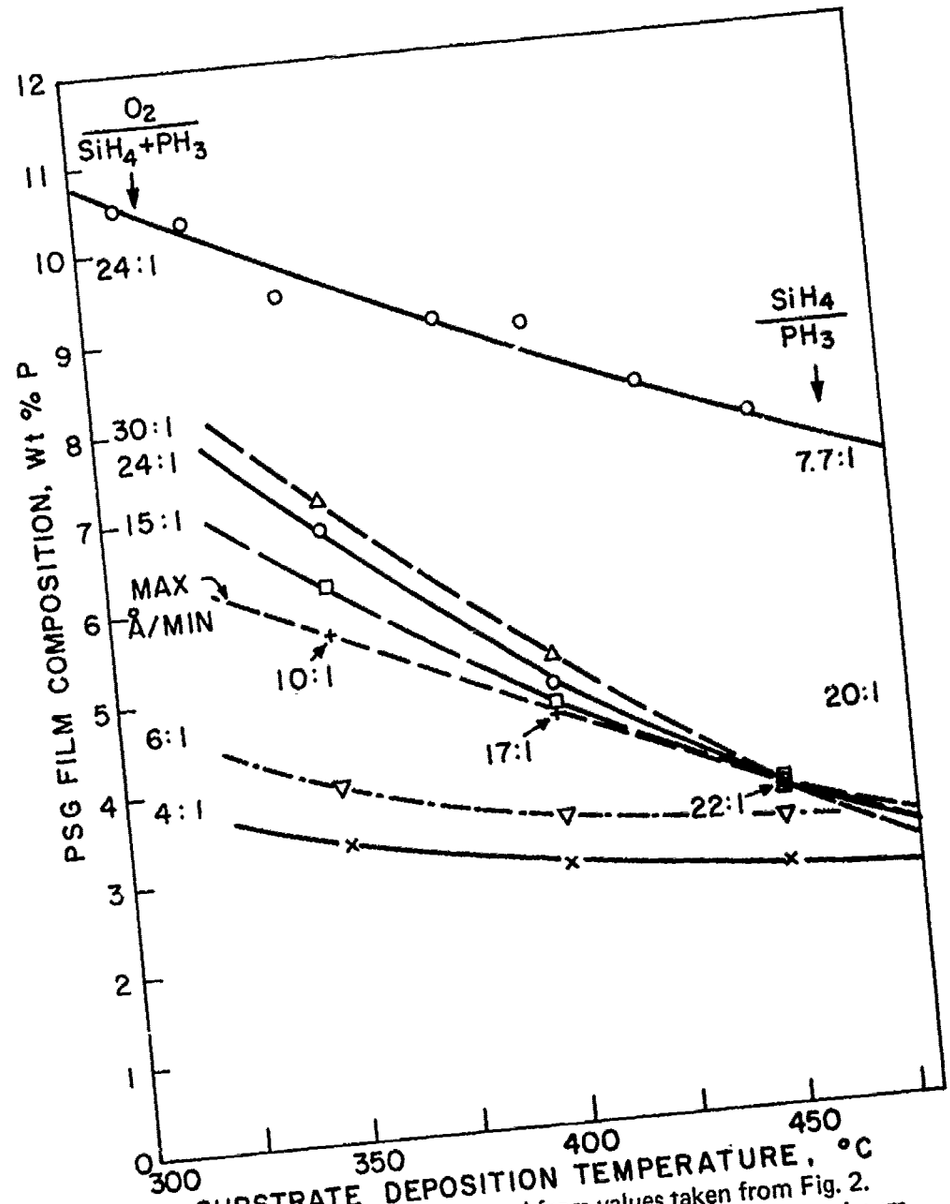


Figure 3. PSG film deposition rate vs deposition temperature for selected oxygen/hydride ratios.



Family of lower curves was plotted from values taken from Fig. 2. Curve marked "Max Å/min" corresponds to ratios yielding maximum deposition rates. Top curve shows temperature effect on composition for a silane/phosphine ratio of 7.7:1 at constant oxygen/hydride ratio of 24:1.

Figure 4. PSG film composition vs deposition temperature for selected oxygen/hydride ratios.

as the ratio is increased. Again, the least dependence is noted at 450°C, where all high ratios (15, 24, and 30:1) are close to the ratio of 22:1 corresponding to the maximum deposition rate.

Figure 4 shows the PSG phosphorus concentration as a function of the same O_2:hydride ratio values selected for Fig. 3, again for all three temperatures. Also included in this figure is a plot showing the temperature effect for a lower SiH_4/PH_3 gas ratio (7.7:1) over an extended temperature interval (310 to 450°C); the O_2:hydride ratio was held constant at 24:1. The difference in slopes of this curve and the 24:1 curve for the higher SiH_4/PH_3 ratio (20:1) indicates some dependence of the temperature effect on the hydride ratio. The family of curves for the 20:1 SiH_4/PH_3 ratio series shows that the effect of temperature on PSG composition becomes progressively less as the O_2:hydride ratio is decreased, similar to the effect on deposition rate. Again, the curves for the higher ratios converge at 450°C, demonstrating minimum dependence. The curve corresponding to the O_2:hydride ratios of maximum deposition rate is a straight line.

An immediate practical consequence of the temperature effect is the need for isothermal surface conditions of the substrate wafer. Good thermal contact of the wafer with the heated substrate plate is essential to effect good heat transfer and to avoid thermal variations in the wafer surface. Poor contact may arise if the wafers are warped (possibly due to improper annealing after diffusion), if wafers overlap on positioning, or if excessive quantities of CVD glass are allowed to accumulate on the substrate plate without the heat input being raised to compensate for heat loss.

3. Effects of Hydride Flow Rate

The quantity of SiH_4 or of $SiH_4 + PH_3$ introduced in the reaction chamber per unit time at a constant substrate temperature and O_2:hydride ratio determines the rate of film deposition, which follows a linear function up to some saturation level limited by the size and geometry of the reaction chamber. In other words, the film thickness increases proportionally with the hydride input and the time period of deposition, independent of the film thickness up to many micrometers, at which point decreased thermal conductance may become noticeable. Hydride input quantities for the reactor system we used to obtain the data in Figs. 1 and 2, for example, were 670 cm^3/min of 3.3%

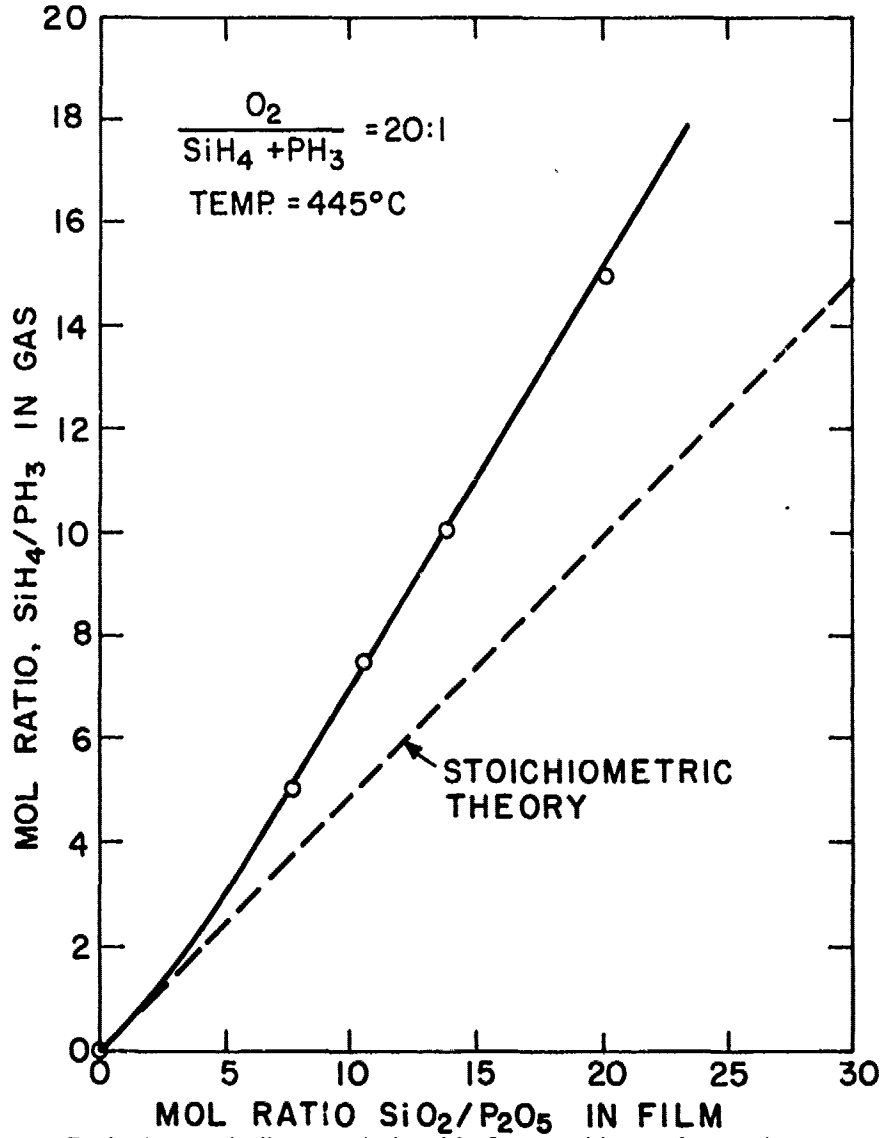
SiH_4 and 110 cm^3/min of 1.0% PH_3. The PSG film composition is affected only slightly by very large variations in the film deposition rate, so that this effect can be disregarded in practical applications.

4. Effects of Silane-to-Phosphine Ratio

The SiH_4:PH_3 ratio under otherwise constant CVD conditions determines the composition of the resulting PSG. The relationship of the mole ratio of SiH_4:PH_3 in the gas and of SiO_2:P_2O_5 in the resulting glass is nearly linear, as shown in Fig. 5 for a deposition temperature of 445°C. A plot of the same data in terms of mol % PH_3 in SiH_4 + PH_3 vs mol % P_2O_5 in SiO_2 - P_2O_5 in the resulting PSG is presented in Fig. 6. It shows a linear relationship up to about 10 mol % P_2O_5, followed by a less than linear increase in P_2O_5 beyond this point. Recent data reported in the literature [31] agree within approximately 10% with our curve shown in Fig. 6. Lower temperatures of deposition at constant SiH_4:PH_3 ratio increase the mol % P_2O_5 in the PSG if the O_2:hydride ratio is adjusted for the plateau region of maximum deposition rate for each temperature, in agreement with the data shown in Fig. 4 and with literature data [31].

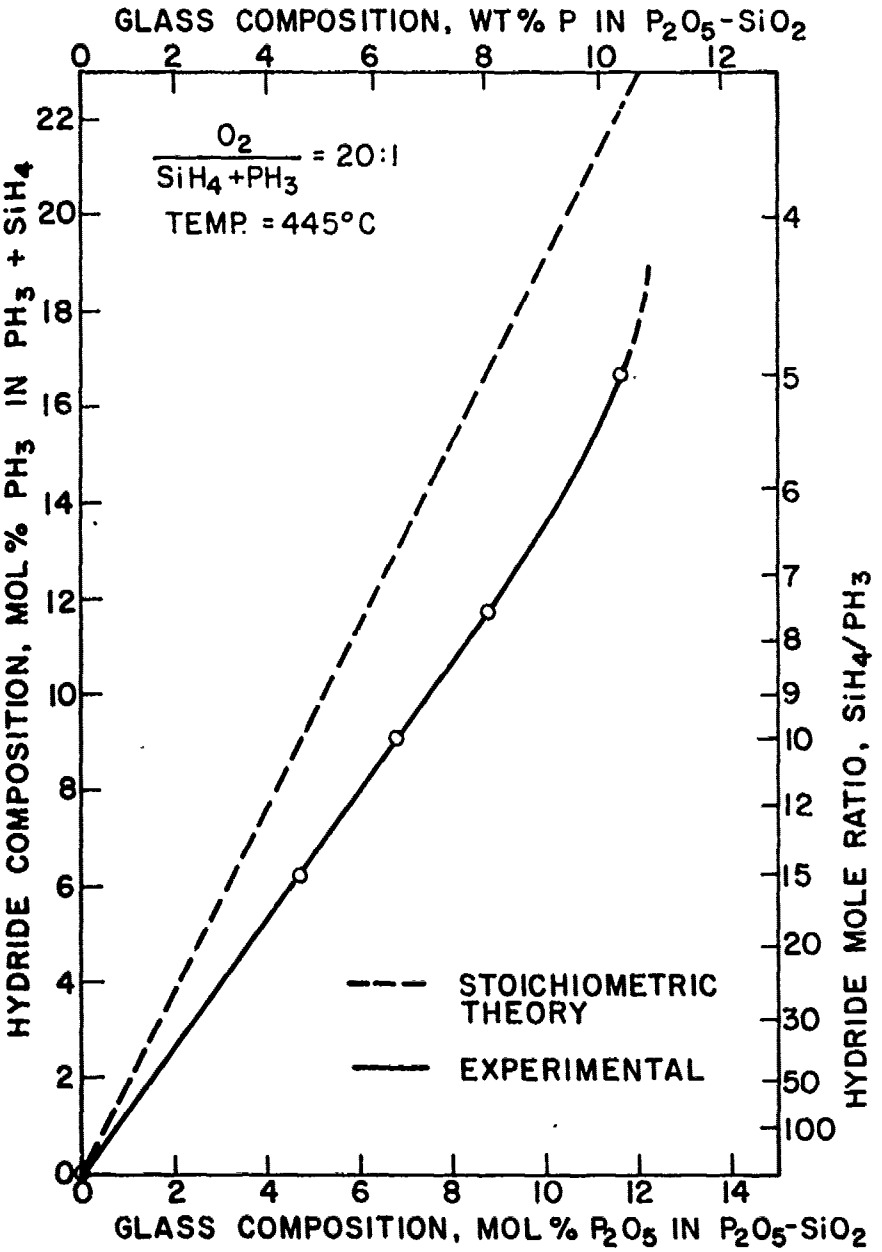
The relationship depicted in Figs. 5 and 6 indicates that the PSG resulting from the oxidation under the conditions stated contains more phosphorus than would be expected from stoichiometry, since two moles of PH_3 form one mole of P_2O_5. Figure 6 indicates that up to about 10 mol % P_2O_5 the coversion efficiency of PH_3 to P_2O_5 at 445°C is 1.4 times greater than that of SiH_4 to SiO_2. At lower temperatures it is still greater. Stated differently, the conversion efficiency of SiH_4 to SiO_2 during co-oxidation of SiH_4 + PH_3 is lower than that of PH_3 alone. Apart from kinetic [16] and thermodynamic [32] differences in the oxidation of the two hydrides, the previously mentioned retardation of SiH_4 oxidation by oxygen is almost certainly responsible for at least part of the observed effect. Hence, higher than expected phosphorus concentrations in the PSG result. In addition, PH_3 appears to have a retarding effect on SiH_4 oxidation, since our work as well as literature data [33] indicate that the film deposition rate is being depressed by the addition of PH_3. We have

32. A. Mayer, K. Strater, and D. A. Puotinen, *Manufacturing Techniques for Controlled Deposition and Application of Doped Oxides*, Tech. Rept. AFML-70-TR-191 (September 1970).
33. M. Shibata, T. Yoshimi and K. Sugawara, J. Electrochem. Soc. 122, 157 (1975).



Dashed curve indicates relationship for stoichiometric reaction. Total gas flow rate was 8 liters/min. Film deposition rate was 4000 Å/min. Film analysis based on wet chemical method.

Figure 5. Mole ratio SiO_2/P_2O_5 in PSG film vs mole ratio SiH_4/PH_3 of the hydride gas mixture.



Samples and CVD conditions are the same as those defined in Fig. 5. Also shown are PSG composition in terms of wt % P and hydride composition in terms of mole ratio.

Figure 6. Composition of PSG films vs composition of hydride gas mixture.

obtained similar results of retardation with diborane in the co-oxidation of $SiH_4 + B_2H_6$ to deposit borosilicates*.

Incorrect SiH_4:PH_3 ratios can lead to several problems in the glass. A PSG with low phosphorus content may result in inadequate gettering of externally introduced contaminants such as sodium ions; it may also cause cracking of the glass because of excessive stress. Too high a concentration of phosphorus, on the other hand, may result in current leakage across the surface or in a hygroscopic glass which may cause metal corrosion problems.

In adjusting the SiH_4:PH_3 ratio for otherwise fixed conditions, it is convenient to use a plot of etch rate values of the films as a direct function of the SiH_4:PH_3 ratio, as shown in Section VIII.

5. Effects of Nitrogen Flow Rate

The function of the diluent nitrogen is threefold: (1) to dilute the reactive gases to a sufficiently low concentration to prevent spontaneous combustion when combined with the oxygen, and in some systems, to afford premixing; (2) to force the reactive gas mixture over the heated substrate surface; and (3) to create gas flow conditions in the reaction chamber that result in good film uniformity across a maximum area of the substrate plate. Too low a nitrogen flow rate can severely depress the deposition rate of both SiO_2 and PSG films and lead to gross nonuniformities in film thickness across the wafers. Excessive nitrogen flow decreases the residence time for the gases at the substrate surface and causes the plate temperature to drop due to cooling, thus leading to nonuniform deposits which, in the case of PSG, contain more phosphorus than obtained under normal conditions (because of the decreased temperature as indicated in Figs. 3 and 4). A suitable flowrate for the reaction chamber described in Appendix A is in the range of 7 to 11 liters of total N_2 (including hydride diluent N_2) per minute, the correct quantity being determined by the attainment of good film thickness uniformity under the specific CVD conditions used.

Silane, despite its reactivity at high concentrations with oxygen, can be conveniently premixed for production applications with oxygen and nitrogen at

*W. Kern and A. W. Fisher, unpublished work.

sufficiently high dilutions in both oxygen and nitrogen (i.e., 0.5% SiH_4, 2.5% O_2, 97% N_2 by volume) forming a mixture that is inert until heated above 200°C [15,32].

6. Effects of Reactor Geometry

The shape and dimensions of the reaction chamber and the gas inlet/outlet configuration are very critical with respect to thickness uniformity of the film deposits. We have constructed and tested many reaction chambers and found that small differences can cause gross effects, particularly in single-rotation reactors, where a lesser degree of averaging is attainable than in planetary units. The type of bell jar shown in Appendix D has given particularly good results despite its deceptive simplicity.

7. Effects of Reaction Chamber Wall Temperature

The reactor wall, if hot, acts as a substrate for both glassy and powdery gas phase reaction products. Cooling the reactor parts that are not intended for heating the substrate results in a decrease of these undesirable coatings and also supresses homogeneous gas phase nucleation which is the cause of the powdery deposits, while at the same time promoting desirable heterogeneous reactions leading to glassy films. As a consequence, cleaner film deposits form and the deposition rate increases for the same reactant input. This means, in effect, that the yield of glassy product can increase considerably, since the input of expensive reactants can be reduced to attain the same deposition rate obtained with a hot-wall reactor. The composition, in the case of PSG films, can be slightly affected by this change, requiring some readjustment of the SiH_4:PH_3 ratio.

8. Effects of Cleanliness of CVD System and Purity of Gases

The surface-catalyzed free-radical reaction mechanism underlying CVD of oxide and glass films is quite sensitive to contaminants on the substrate surface and in the gas phase. Particles on the substrate wafer (such as powder from scribing) or in the gas stream (such as colloidal oxides) can cause microbubbles, pinholes, and other localized structural defects in the glass layer. Extreme cleanliness is therefore imperative.

As already noted, particulate contamination arises very often during CVD because of homogeneous gas phase nucleation reactions. Increasing the nitrogen diluent flowrate to a practical maximum suppresses this reaction, especially if combined with cooling of the reactor wall.

Silicon dioxide films deposited from semiconductor-grade silane (SiH_4) and oxygen are known to contain some sodium that may deleteriously affect MOS devices [25]. PSG passivation of proper composition is capable of gettering this contaminant to the extent that instability problems are eliminated. Nevertheless, it is safest to employ only high-purity gases in the CVD of passivating films and to ensure removal of particulate impurities by the use of large-area high-capacity submicron filters in the gas lines.

The presence of water vapor in the nitrogen carrier gas does not markedly affect the deposition rate, the film uniformity, or the chemical composition. In fact, the intentional introduction of water vapor during CVD can be utilized to decrease film stress, as will be shown in Section IV.

9. Effects of Substrate Surface

The type of material, the cleanliness, and the topographic structure - all affect the quality of the CVD films with respect to film growth and the presence or absence of structural defects. The quality of adhesion of the CVD glass to a substrate is dependent upon the cleanliness of the surface, the deposition conditions, and the nature of the substrate material. Peeling and blistering can be avoided by observing clean processing conditions, such as complete removal of photoresist residues and chemical adsorbates before glassing (by suitable wet cleaning techniques or plasma ashing treatments).

Surface cleanliness and surface-cleaning techniques for ensuring a good surface quality prior to vapor-deposition processing are therefore absolutely essential. These have been discussed in the previously mentioned papers [1,12]. The relation of film coverage and topography of the substrate surface is a specialized topic we have also reviewed recently [34].

34. W. Kern, J. L. Vossen, and G. L. Schnable, 11th Ann. Proc. Reliability Physics, 214 (1973).

10. Applicability of Results to Other CVD Reactor Systems

A considerable variety of CVD reactor systems for preparing SiO_2 and PSG passivating overcoats is now available. In Appendix B, we have categorized and described the design, operation, and capability of CVD equipment, which varies from relatively simple to sophisticated automated reactors. We have conducted a limited number of experiments with several of these types of reactor systems, including several commercially available continuous processing units*, to examine whether the experimental results presented in this section are applicable to other systems as well. We found that they not only agree in principle, but that they frequently relate on a semi-quantitative basis, despite the remarkable differences in geometry and system operation. Nevertheless, the performance of each reactor must be carefully examined and adjusted to attain conditions for producing films of specified properties.

D. CONCLUSIONS

Even though the principle of operation may differ greatly for various types of systems, the basic CVD parameters underlying oxide and glass film formation by gas phase oxidation of the hydrides at temperatures below 500°C are, in principle and often semiquantitatively, applicable to all systems. The critical factors determining PSG composition and film quality are substrate temperature of deposition, oxygen-to-hydride ratio, and silane-to-phosphine ratio. These factors must be controlled and optimized for a given CVD system by analysis of the film product obtained. The CVD process should be directed in a fashion conducive to heterogeneous gas-phase nucleation to produce clear, glassy films free of defects. Homogeneous gas-phase reactions produce particulate contaminants and must be suppressed by application of the techniques discussed. Even though the exact reaction mechanism of film formation is quite complex and is influenced by many variables, the optimized preparation of high-quality SiO_2 and PSG films for IC overcoat passivation is a CVD process well suitable for large-scale production.

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*Typical units and their manufacturers are listed below:
Rotox-60, Unicorp. Incorporated, 625 North Pastoria Dr., Sunnyvale, CA94086.
AMS-2000 Continuous Silox Reactor, Applied Materials Technology, Inc., 2999 San Ysidro Way, Santa Clara, CA95051.
PWS Model 2000 Vapor Deposition System, Pacific Western Systems, Inc., 855 Maude Avenue, Mountain View, CA94040; described in "Vapor Deposition Unit is Modular," Electronics, 138 (September 5, 1974).

The formation of low-stress CVD SiO_2 and PSG films by introducing water vapor during CVD has been noted and is discussed in detail in Section VI.

The feasibility of post-deposition catalytically accelerated densification of PSG films at 450°C using water vapor as catalyst will be demonstrated experimentally in Section V. Substantial degrees of densification can be achieved, and consequent improvements in the film qualities can be expected.

Part of the information presented in this section and in the appendix describing CVD equipment (Appendix B) has been summarized in a paper presented at NAECON '75 [35]; a copy of the paper is included herein as Appendix E.

The essential effects of CVD key parameters for preparing PSG films are presented schematically in the summary, Table 26 (Section IX.D., page 148).

35. W. Kern, Proc. IEEE 1975 National Aerospace and Electronics Conf.; NAECON '75 Record, pp. 93-100.

IV. STRESS IN CVD FILMS

A. INTRODUCTION

Intrinsic stress in passivation films is a major factor in determining whether cracks occur in glass over metallization on ICs. Since cracks in the passivation glass can result in substantially lower IC reliability, a detailed study was made of the effect of CVD deposition conditions on room-temperature stress of CVD films of SiO_2 and PSG on silicon wafer substrates. Variables studied included the effect of deposition rate, deposition temperature, addition of water vapor, hydride/oxygen ratio, and, in the case of PSG films, phosphorus content. Post-deposition storage and densification effects were also investigated.

B. SURVEY OF STRESS MEASUREMENT METHODS

A variety of techniques for measuring stress in thin films are described in the literature [36] (see Appendix A). X-ray and electron-diffraction analyses have been used to measure changes in lattice spacing and hence stress in films. However, more commonly, stress is calculated by measuring the deformation of a substrate, usually in the form of a beam, or a circular disc. In the beam bending method, stress is calculated by determining the radius of curvature of the beam. Several methods for measuring the radius of curvature of a cantilevered beam have been reported.

For a circular disc, the stress is calculated by measuring the displacement of the center of the circular disc in relationship to its edges. This can be accomplished by counting interference fringes between the disc and an optical flat, laser interferometry, holography, changes in location of the focal point, profiling the substrate with a light section microscope, or profiling the substrate by scanning with an optical microscope and measuring the change in focus from center to edge.

C. MEASUREMENT METHODS USED

For the work described in this report, the stress was determined by depositing films onto circular silicon wafers. Measurements of disc deflection

36. D. S. Campbell, in *Handbook of Thin Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw -Hill Book Co., New York, 1970), pp. 12-3 to 12-50.

were done at room temperature. Three methods were chosen for these measurements. The first method was to use an optical flat and calculate deflection by counting interference fringes [37]. The second method was to determine the focal point by reflecting a collimated light off the surface of the wafer [38]. The third method was to focus an optical microscope on one edge and then move the sample transversely from one edge to the other through the center of the wafer, and measure the change in focus at various points. Measurements were made in both x- and y-direction at 5-mm intervals. The micrometer on the focusing dial was zeroed at the edge of the wafer. Upward and downward movement of the microscope stage was recorded as positive and negative, respectively.

From this information, a plot of the wafer profile was then made, from which deflection was determined. Initially, all three methods were used to measure flatness of the substrate before CVD of the films. However, only profiling was used in the latter part of the work since it gave the best results. Corrections in the final profile were made if deviations from flatness occurred in the starting substrate. Typical plots of change of focus vs distance across wafers are shown in Fig. 7.

Stress in the CVD films was then calculated from the equation derived by Glang [39]

$$\sigma = \left(\frac{\delta}{r^2}\right)\left(\frac{E_s}{3(1-\nu)}\right)\left(\frac{t_s^2}{t_f}\right), \tag{4}$$

where

σ = Stress (dynes/cm^2),
δ = Deflection of disc (cm),
ν = Poisson's ratio for substrate,
E = Young's modulus of substrate,
t_f = Film thickness (cm),
t_s = Substrate thickness (cm), and
r = Radius of disc (cm).

37. R. W Hoffman, in *Physics of Thin Films*, Vol. 3, G. Hass and R. E. Thun, Eds., (Academic Press, New York and London, 1966), p. 211.
38. R. Lathlaen and D. A. Diehl, J. Electrochem. Soc. 116, 920 (1969).
39. R. Glang, R. Holmwood, and R. Rosenfeld, Rev. Sci. Instr. 36, 7 (1965).

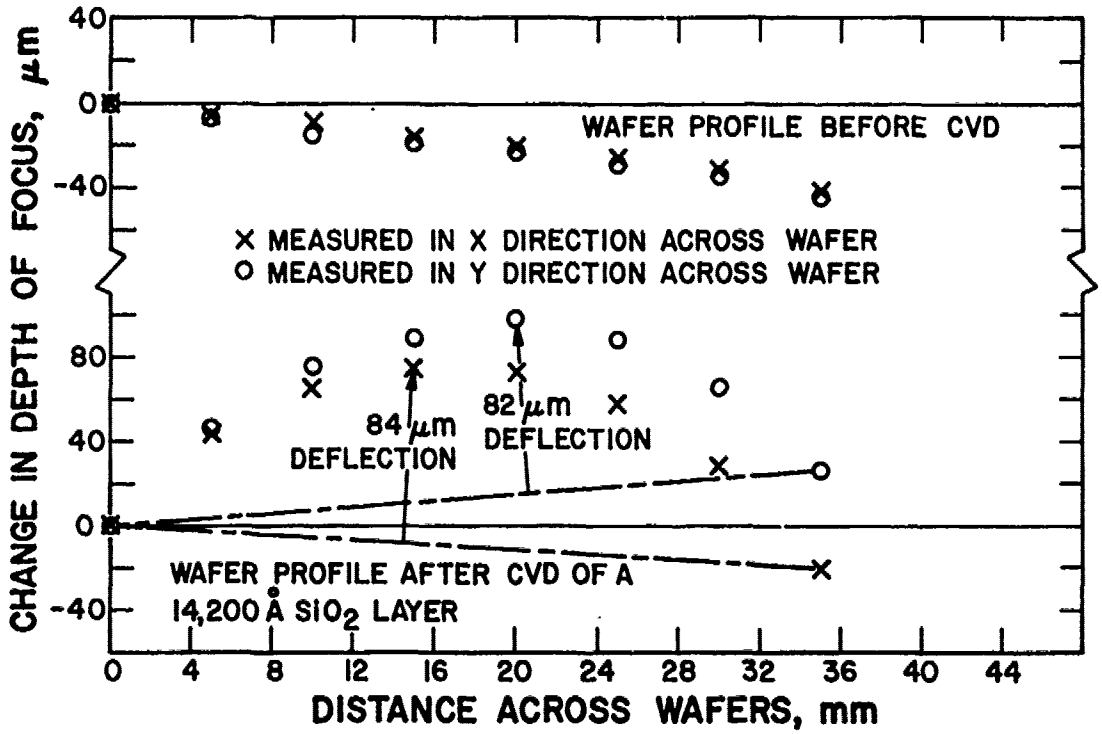


Figure 7. Wafer profiles before and after CVD of a 1.4-μm-thick SiO_2 layer.

D. PUBLISHED INFORMATION ON STRESS IN CVD FILMS

The literature contains some information on stress in CVD SiO_2 and PSG films. Comparisons are sometimes difficult to make because of the substantial differences in deposition systems. Generally, published data are based on room-temperature measurements. SiO_2 films nave been reported to be in tension as deposited [40]. Because silicon has a higher coefficient of thermal expansion than silicon dioxide, the residual stress in CVD SiO_2 films on silicon at room temperature is somewhat lower than the intrinsic stress of films as deposited, but the films are still in considerable tension [38-43].

PSG films are in lower tensile stress (at room temperature) than SiO_2 films deposited at the same conditions [25,47]. In general, however, residual stress at room temperature remains tensile [25,43].

40. H. Sunami, Y. Itoh, and K. Sato, "Low Stress CVD Glass Films in Multilevel Interconnection," Proc. 2nd Conf. Solid State Dev., Tokyo, 1970; Suppl. to J. Japan. Soc. Appl. Phys. 40, 67 (1971).
41. M. L. Barry, in *Chemical Vapor Deposition*, J. M. Blocher, Jr., and J. C. Withers, Eds. - Second Intn'l Conf., The Electrochem. Soc., New York (1970), pp. 595-617.
42. H. Sunami, Y. Itoh, and K. Sato, J. Appl. Phys. 41, 5115 (1970).
43. P. B. Ghate and L. H. Hall, J. Electrochem. Soc. 119, 491 (1972).

Some information is available on the effect of deposition rate [38,42] and silane/oxygen ratio [38] on CVD SiO_2 stress, and of phosphorus concentration on stress in CVD PSG [25,42]. Stress reduction in CVD films exposed to room air has been reported [42].

Deposited SiO_2 or PSG films, when heated above the deposition temperature, are put in additional tension, particularly in regions over the edges of delineated Al metal films. Accordingly, there is some correlation between the intrinsic tensile stress in deposited films and the temperature increment above deposition temperature which can be attained before cracks begin to form [25, 40].

In general, the lower the intrinsic stress in films, the thicker the CVD layer can be before severe cracking begins to occur [22,23,25].

E. EXPERIMENTAL RESULTS AND DISCUSSION

1. Evaluation of Substrates Used for Stress Measurements

Initially, 65-μm-thick, flat, circular (111)-silicon substrate wafers were used to measure film stress. During the chemical vapor deposition process, the substrates deformed because of the thermal gradients across the substrate, as well as from the strain that is being introduced from the depositing layer. The magnitude of the deformation of the thin silicon wafers used for stress measurements is, of course, much greater than that which occurs on normal integrated circuit wafers. Deformation of the substrate during CVD can cause errors in the stress measurements, and it is thus important that the substrates remain relatively flat during the CVD process. To maintain the flatness of the thin silicon wafer substrates during CVD, a fixture was designed to hold the substrates down by vacuum. The fixture consists of an aluminum block 5.7 mm in diameter and 18 mm in height, with a 6.3-mm stainless steel tube leading to a cavity in the center of the block; 0.3-mm holes were drilled through the top of the block to the cavity, in a circular area 35 mm in diameter. A vacuum line was connected to the fixture, and wafers placed over the holes in the top surface were held firmly in place.

While the vacuum holddown fixture worked satisfactorily, it could not be used with certain types of CVD systems. Moreover, the 65-μm wafers proved to be too fragile for easy handling in a large number of tests. Accordingly,

tests were carried out to determine what wafer thickness could be used that would not be excessively fragile and still give good results. It was found that wafers about 140-μm thick and 39 mm in diameter were sturdy enough so that excessive breakage did not occur. Because of the increased thickness, it was also found that it was unnecessary to use the vacuum fixture to hold the wafers during deposition. Tests revealed that stress measured on samples held fast during deposition was not appreciably different from that of wafers not held at all, and that uniform CVD film thicknesses resulted. For this reason the wafers were not held down during CVD. Profiles for two wafers with and without holddown are shown in Fig. 8.

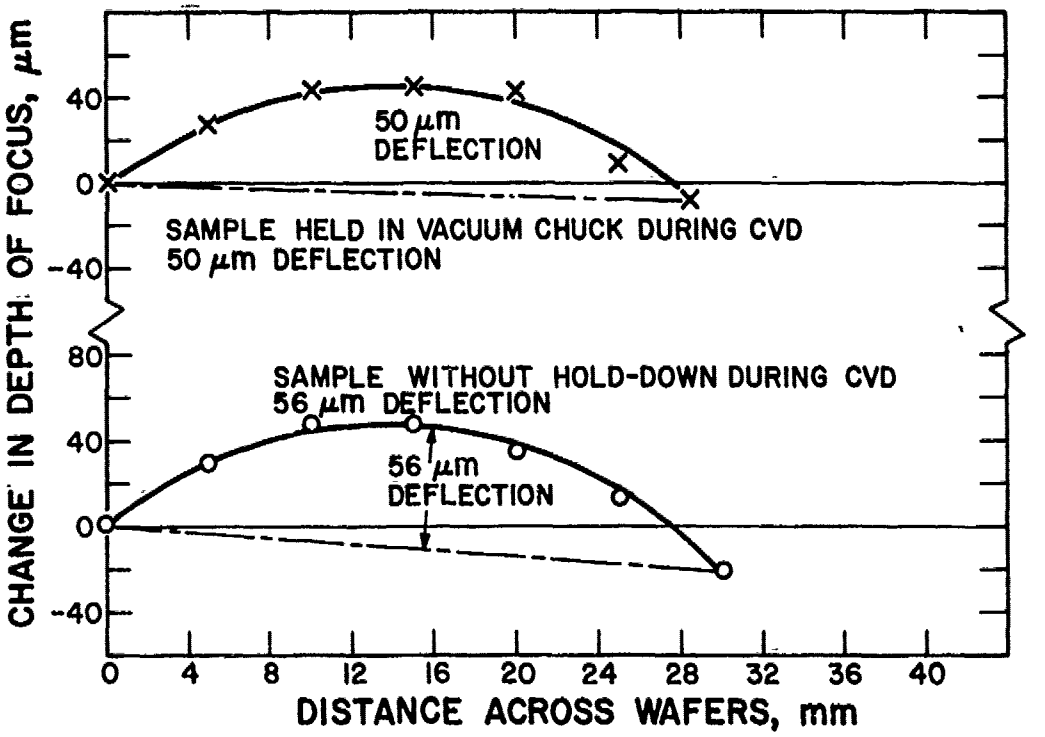


Figure 8. Profiles of two silicon substrates following CVD of a 1 μm thick layer of SiO_2.

Young's modulus and Poisson's ratios were measured for the silicon substrates used for film deposition. This was accomplished by thermally oxidizing the wafers in steam at 1100°C, removing the oxide from one side in aqueous HF, and measuring the deflection. Since the stress value of thermally grown SiO_2 has been published [44], this value was substituted into the stress equation,

43. R. Jaccodine and W. Schlegel, J. Appl. Phys. 37, 2429 (1966).

and $E/(1 - \nu)$ was calculated. The calculated value of 1.9×10^{12} dyne/cm^2 for (111)-oriented silicon is close to Glang's value of 2.3×10^{12} dyne/cm^2 [39].

However, for (100)-oriented silicon, the value of $E/(1 - \nu)$ was found to be 1.3×10^{12} dynes/cm^2. This difference between (111) and (100) silicon was also confirmed by stress measurements which showed that wafers of equal thickness with equal CVD oxide thicknesses deflected by different amounts, with larger deflection occurring on (100)-oriented silicon wafers.

In the process of making stress measurements in CVD layers, unexplained variations in measured stress were observed. Experiments revealed that some substrate wafers deflected more easily than others, thus resulting in a larger stress value than actually are present in the CVD layer. Variations in the depth of microcracks caused by lapping and polishing of the silicon substrate are probably the main cause for the difference between wafers. In an effort to eliminate these variations, an apparatus was set up to measure wafer deflection. Deflection was measured by placing the silicon substrates onto an O-ring support, and then applying a partial vacuum to the holder, thus causing the wafer to bow. A partial vacuum of 200 mm of H_2O was used since this deflected the substrates about the same amount as a CVD SiO_2 film of 1 μm in thickness. Each wafer used for stress measurements was checked, and only wafers that showed equal amounts of deflection for both sides for a given pressure were used for stress measurements.

For all stress data presented in this report, (111)-oriented silicon substrate wafers were used, and Glang's value for $E/(1 - \nu)$ was used in making the calculations.

2. Effect of Storage on Stress

Stress in CVD SiO_2 films has been shown to decrease with time, the amount of decrease being dependent upon the storage ambient. Wafers having a CVD SiO_2 layer are essentially totally relieved of their stress in about four hours if stored in 100% relative humidity at room temperature, whereas wafers prepared under the same deposition conditions showed little change in stress when stored in a dry box for 70 hours (Fig. 9). However, subsequent experiments showed that even in a dry box some stress with CVD oxide layers is relieved. Wafers with oxide layers whose stress had been relieved by storing in 100% relative

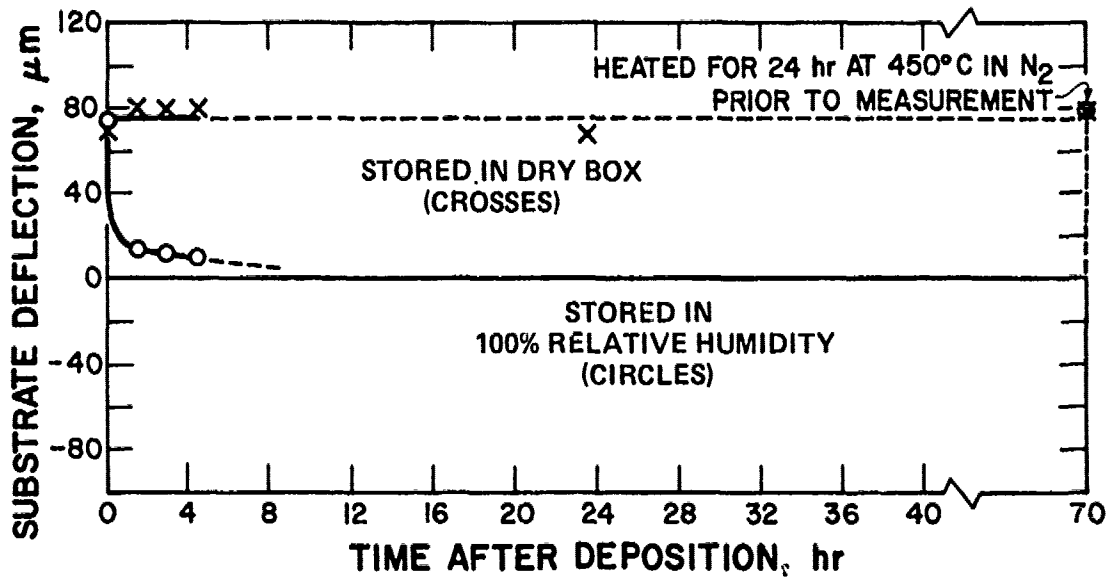


Figure 9. Plot of wafer deflection as a function of storage ambient and time.

humidity went back into tensile stress when the sample was returned to the dry box condition. These results indicate that for undensified, unencapsulated SiO_2 layers the stress will vary depending on ambient conditions.

3. Effect of Deposition Rate on Stress

Results have shown that SiO_2 films deposited at a very high rate (10,000 Å/min) are in tensile stress of about 3.1×10^9 dynes/cm^2 as compared with 2.7×10^9 dynes/cm^2 for films deposited at 1000 Å/min.

Stress as a function of film deposition rate for PSG layers containing 3.5 wt % phosphorus has been measured in the range of 1250 Å/min to 5000 Å/min, with the O_2 to hydride ratio held constant at 11.4 to 1. Stress was about 2.3×10^9 dynes/cm^2 for all the samples prepared in this range. Table 4 lists various characteristics of the PSG layers.

4. Effect of Deposition Temperature on Stress

Stress as a function of deposition temperature has been measured in the range of 340° to 450°C. The average stress for five samples of CVD SiO_2 films on silicon prepared at 340°C was 3.1×10^9 dynes/cm^2. Film average stress for five samples prepared at 400°C was 3.1×10^9 dynes/cm^2. Samples prepared at

Table 4. Properties of CVD Layers Prepared at Different Deposition Rates

Deposition Temperature (°C)	Deposition Rate (Å/min)	Stress (dynes/cm^2)	Etch Rate of Undensified Film* in P-Etch (Å/sec)	Etch Rate Ratio $\left(\frac{\text{Undensified Film}}{\text{Densified Film}}\right)$	Etch Rate of Densified Film in P-Etch (Å/sec)	Wt % P, Densified Film
400	1250	2.3×10^9	40.8	2.7	14.9	3.5
400	2500	2.3×10^9	38.9	2.4	16.2	3.7
400	5000	2.4×10^9	38.0	2.5	15.3	3.6

*After storage at 23°C in desiccator for 91 days.

450°C averaged 2.7×10^9 dynes/cm^2. Experimental conditions and evaluation data for these and similar tests are presented in Table 5.

An attempt was made to correlate stress with etch rate of CVD films. While some of the etch rate studies were inconclusive, there was a tendency for the etch rate to increase as deposition temperature was decreased, in correlation with the fact that as the deposition temperature is lowered, the intrinsic stress increases.

5. Stress as a Function of O_2 to SiH_4 Ratio for SiO_2 Films

Stress as a function of O_2 to SiH_4 ratio was measured for SiO_2 deposited at 450°C. Contrary to other published data [38] little difference was observed in the stress of the deposited film when the O_2 to SiH_4 ratio was varied between 3 and 36 to 1, as shown in Table 6.

6. Stress as a Function of Glass Composition

Experiments have shown that as the phosphorus content in a CVD SiO_2 layer increases from 0 wt % tc 8.5 wt % the room temperature stress goes down. Stress for pure SiO_2 films averages 2.7×10^9 dynes/cm^2 as shown in Subsection 4. As one increases the phosphorus content to 3.7 wt %, the stress averages 2.3×10^9 dynes/cm^2 (Subsection 3).

At 8.5 wt % phosphorus, tensile stress in the film at the 450°C deposition temperature was calculated to be 2.4×10^9 dynes/cm^2, but no stress could be measured in the CVD layer at room temperature; however, upon densification at 1000°C the layer went into compressive stress of 1.3×10^9 dynes/cm^2. Results thus show that room-temperature stress in CVD films can be reduced to nearly

Table 5. Relationship of Stress in CVD SiO_2 Films and Deposition Temperature

Sample No.	Deposition Temperature (°C)	Time (min)	Oxide Thickness (Å)	Deposition Rate (Å/min)	Etch Rate (Å/min)	Stress (dynes/cm^2 x 10^9)	Flow Rate, (cm^3/min)		
							N_2	O_2	SiH_4(10%)
V-98-1	450	10	11,140	1,110	-	2.8	6000	687	233
V-97-2	450	10	10,730	1,070	-	2.7	6000	687	233
V-97-3	450	10	12,700	1,270	16.6	2.6	6000	687	233
V-97-4	450	10	12,570	1,260	16.3	2.8	6000	687	233
V-97-1	400	10	12,620	1,260	17.0	3.6	6000	687	325
V-97-2	400	10	17,600	1,760	16.6	2.9	6000	687	325
V-97-3	400	10	13,800	1,380	-	3.3	6000	687	325
V-97-4	400	10	14,100	1,410	17.5	3.0	6000	687	325
V-97-5	400	10	12,380	1,240	-	3.3	6000	687	325
V-97-6	340	10	10,970	1,100	-	2.7	6000	687	375
V-97-7	340	10	11,200	1,120	17.8	3.1	6000	687	375
V-97-8	340	10	14,000	1,400	-	3.2	6000	687	375
V-97-9	340	10	11,570	1,160	17.2	3.2	6000	687	375
V-97-10	340	10	9,540	950	18.9	3.4	6000	687	375

Table 6. Relationship of Stress in CVD SiO_2 Layers and O_2 to SiH_4 Ratio

Sample No.	Temperature (°C)	O_2: SiH_4 Ratio	Oxide Thickness (Å)	Deposition Rate (Å/min)	Stress (dynes/cm^2)	N_2 Flow Rate (ℓ/min)	O_2 Flow Rate (cm^3/min)	SiH_4 10% Flow Rate (cm^3/min)
V-97-11	450	36:1	12,600	1,260	2.9×10^9	6	687	190
V-97-12	450	14:1	14,200	1,420	2.8×10^9	6	263	190
V-97-13	450	3:1	11,900	1,190	3.2×10^9	6	60	190

zero by increasing the phosphorus content, but too much phosphorus leads to corrosion (see Section VIII).

Layers of SiO_2 and 2, 3, and 4 wt % phosphorus PSG were deposited on IC device wafers and examined for cracks. CVD processing was under the usual conditions at 450°C, and the layer thicknesses ranged from 1.1 to 1.2 μm. Both linear bipolar ICs (CA3747) with large aluminum-metallized capacitor areas and CMOS ICs (CD4017A) were chosen for these tests. The overcoat layers were delineated by photolithography and chemical etching to open the aluminum bond pad areas and the grid lines. Microscopic examination showed that the highly stressed SiO_2 layer had cracked along the edges and in the interior of the large aluminum-metallized areas. Additional cracks formed along the entire edge of the circuit over the dense oxide. The glass layers containing 2, 3, or 4 wt % phosphorus exhibited no cracks, thus demonstrating that the incorporation of a relatively small amount of phosphorus in the glass can have a very large effect on preventing glass cracking. Another important finding concerns step coverage. We found by special etching techniques, that 2 to 4 wt % phosphorus PSG affords a substantially better conformal edge coverage over aluminum than does SiO_2. Again, the difference between 0 and 2 wt % phosphorus is remarkable, and is definitely due to the overcoat material since the conditions of CVD were kept exactly analogous, and the effect occurred on both types of ICs, even though the aluminum thickness and edge contour are not exactly the same.

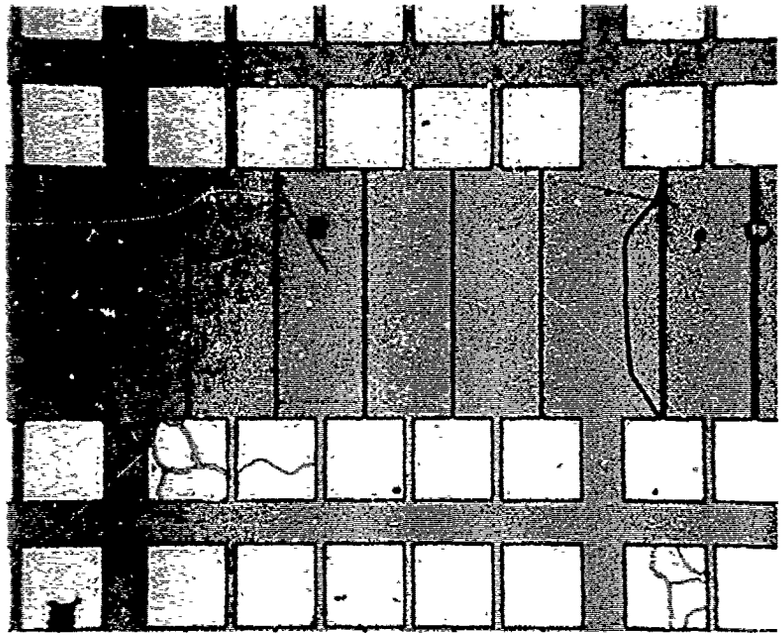
7. Effect of Intentionally Introduced Water Vapor During CVD of SiO_2 and PSG Films on Stress

It has been demonstrated that substantial degrees of densification of CVD films can be achieved by prolonged heat treatments at 450°C in ambients

containing water vapor. To attempt to lower the tensile stress directly in the as-deposited layers, H_2O vapor was intentionally added into the CVD reaction chamber at a deposition temperature of 450°C.

Since H_2O is one of the reaction products when SiH_4 is oxidized, it was necessary to substantially increase the H_2O content to observe an effect. This was easily accomplished simply by passing the main N_2 carrier gas through a fritted bubbler to saturate the N_2 with H_2O vapor at room temperature. Assuming a 50 percent oxidation of the SiH_4 in the reaction chamber, the H_2O vapor content was increased 9.2 times. O_2 could also be passed through a bubbler to further increase the H_2O vapor content.

Tensile stress in the CVD SiO_2 films deposited onto silicon wafers by this technique was reduced from 2.7×10^9 dynes/cm^2 to 2.4×10^9 dynes/cm^2. To further confirm that tensile stress was lowered by deposition in wet N_2, two CVD SiO_2 layers, one prepared with wet N_2, the other with dry N_2 were deposited over a 1-μm-thick aluminum test pattern. These test patterns were used since CVD oxide layers over aluminum are very susceptible to cracking. Subsequent to CVD deposition the samples were etched in hot (55°C) aluminum etch for 10 min to reveal cracks in the SiO_2 films (cracks or pinholes in the overlying glass will allow the etch to reach the metal, thus etching it away). The sample having an oxide prepared with wet N_2 had no cracks, while cracks were observed on the sample prepared with dry N_2. Both samples were then reheated at 450°C for 1.5 hours in nitrogen, cooled and re-etched for an additional 10 minutes in the hot aluminum etch. Microscopic examination showed a few cracks on the sample prepared with wet nitrogen, while the sample prepared with dry nitrogen was severely cracked (Fig. 10). A scanning electron micrograph of the sample prepared with dry nitrogen, taken at 2000 x magnification at an incidence angle of 30°, is shown in Fig. 11. The aluminum film etched away between 6 to 8 μm from the crack in the SiO_2 layer. Studies employing selective etching techniques and SEM have shown that these stress-induced microcracks in SiO_2 layers deposited under "dry" CVD conditions over aluminum patterns do not extend beyond the aluminum area, but run across the aluminum patterns and along most of the SiO_2 layer top corner covering the edge of the aluminum pattern. The cracks are not nucleated by pinholes or other defects in the SiO_2 or aluminum films.



(a) Deposition of SiO_2 layer performed in wet N_2.

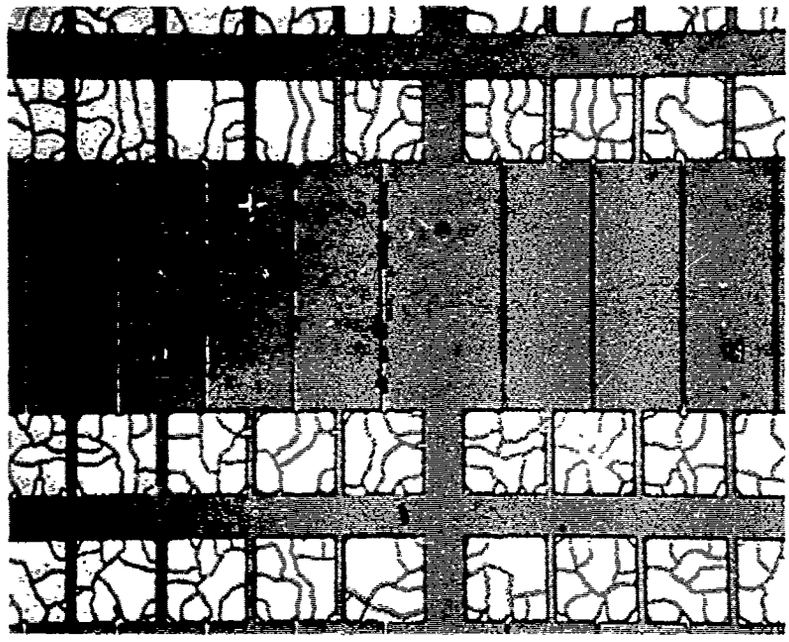


Figure 10. Cracks revealed in a 1-μm-thick CVD SiO_2 layer deposited over an Al pattern, followed by 450°C heat treatment and Al etching.

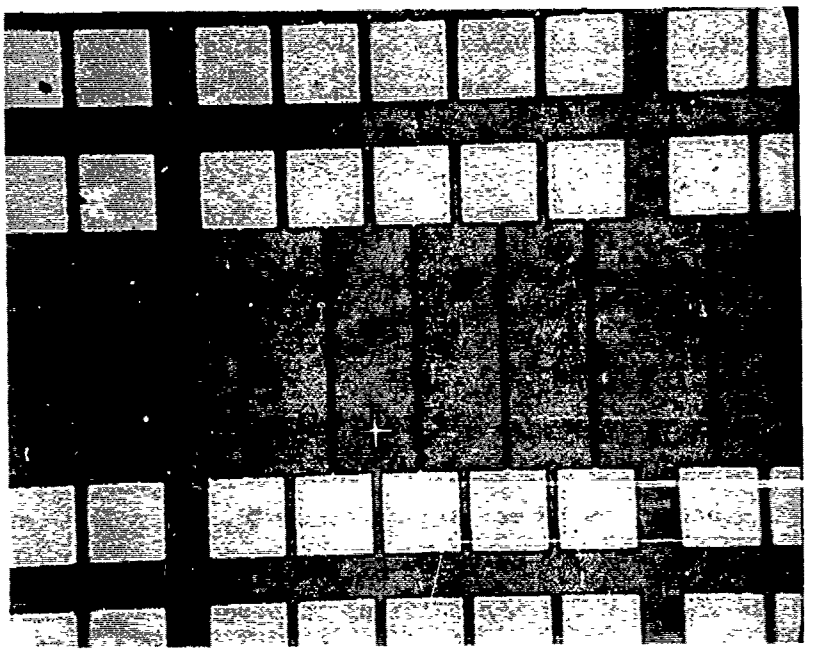
Sample was etched in hot aluminum etch, resulting in removal of aluminum from the area adjacent to the cracks.

Figure 11. Scanning electron micrograph of cracks in CVD SiO_2 over aluminum, 2000X, 30° incidence.

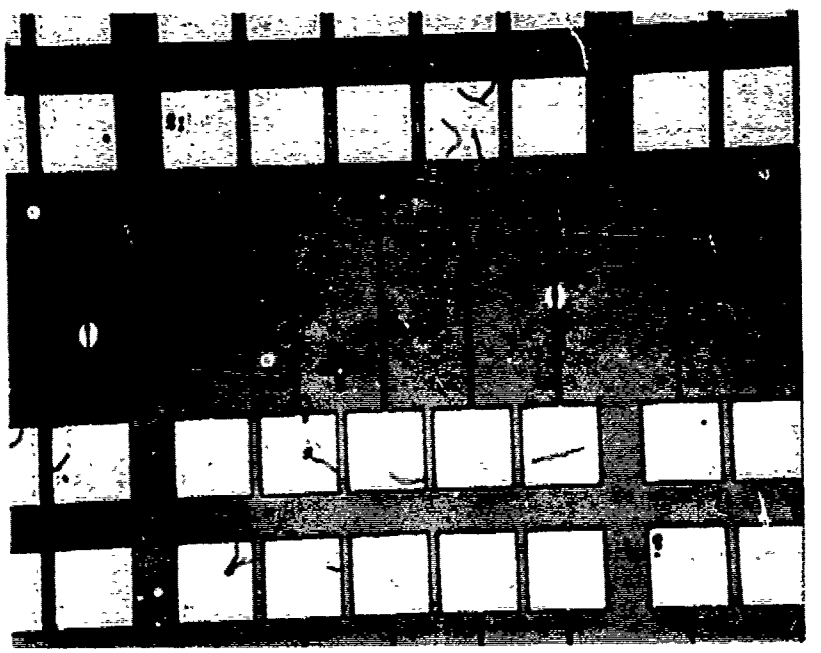
This same test was repeated using a 1-μm-thick PSG layer over 1-μm-thick aluminum patterns. Because PSG glass layers are under less tensile stress as-deposited, no cracks were observed on either the wet or dry nitrogen samples. However, by heating the samples to 525°C for 10 minutes and by giving the samples a hot aluminum etch, some cracks did appear in the PSG layer deposited with dry nitrogen, while none were observed on the sample prepared with wet nitrogen (Fig. 12). The results reveal that under the same deposition conditions, CVD SiO_2 films or PSG films deposited with wet nitrogen carrier gas have lower intrinsic tensile stress than films deposited with dry nitrogen.

The use of such CVD films in the manufacture of semiconductor devices should result in higher yields and greater reliability, expecially where the CVD oxide layers are used as an insulator or passivating glass, since glass cracking is a major cause of device failures and degradation.

Infrared absorption spectroscopy of SiO_2 and PSG films deposited in the presence of water vapor have shown no larger quantities of included water in



(a) Deposition of PSG layer performed in wet N_2.



(b) Deposition of PSG layer performed in dry N_2.

Figure 12. Cracks revealed in a 1-μm-thick CVD PSG layer deposited over an aluminum pattern, followed by 525°C heat treatment and aluminum etching.

the film structure than is normally observed under dry conditions. Compositional analysis of the PSG films has shown that the phosphorus content is not markedly affected by these deposition conditions.

8. Stress Measurements of CVD SiO_2 Films for Various CVD Reactors

A comparison of stress in CVD SiO2 films deposited in four different CVD systems, including several commercially available systems, was made. The CVD reactors used in the comparison tests had deposition temperatures in the range of 400° to 450°C and deposition rates ranging from 1000 Å/min to 10,000 Å/min. The highest stress observed, 3.1×10^9 dynes/cm^2, was on samples prepared on the AMS-2000 model. The lowest stress observed, 2.7×10^9 dynes/cm^2, was on samples prepared on the RCA-designed rotary reactor. A description of the stress results and deposition conditions is given in Table 7.

Table 7. Stress in CVD SiO_2 Films Deposited in Various Types of Reactors

CVD System	Deposition Temperature (°C)	Deposition Rate (Å/min)	Stress (dynes/cm^2) x 10^9
AMS-2000 Continuous Silox Reactor†	410	1,060	3.1
PWS Model 2000 Vapor Deposition System*†	450	10,000	3.0
Rotox-60 Reactor†	400	1,000	2.9
RCA Single-Rotation Reactor**	450	1,000	2.7

*Single-head nozzle array (4 cm width)
**Appendix D
†For addresses of manufacturers see Appendix B.

9. Effects of Densification on Stress

Stress has been measured on a 2-μm-thick CVD SiO_2 film before and after thermal densification. Prior to densification the film was in tensile stress. The stress was calculated to be 4×10^9 dynes/cm^2. After densification of the

film at 1000°C in air for 30 minutes, the stress became compressive and was calculated to be 3.3×10^9 dynes/cm^2. Figure 13 shows the profiles of the wafer before and after densification. The inverted profile indicates that the stress has changed from tension to compression.

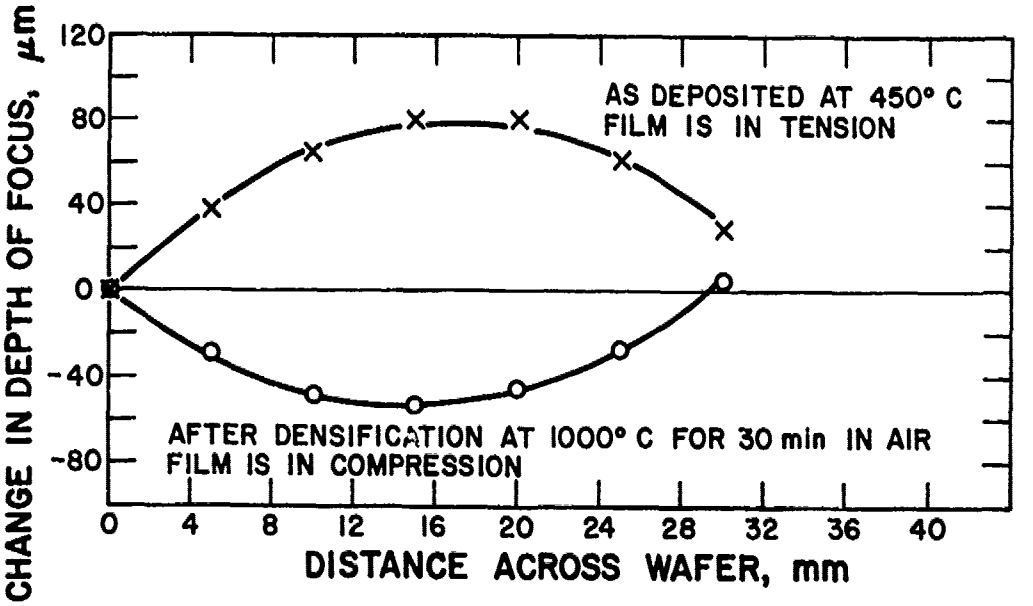


Figure 13. Profiles before and after densification of a silicon wafer with a 2-μm-thick CVD SiO_2 layer.

CVD PSG layers with very little stress at room temperature have been deposited. The layers were 9400-Å thick and contained approximately 8.5 wt % phosphorus. After deposition on both 190-μm and 63-μm-thick silicon substrates, no appreciable deformation of the substrate could be observed at room temperature, thus indicating no room-temperature stress. Upon densification of the glass layer at 1000°C for 15 minutes in O_2, the layer was in compressive stress of 1.3×10^9 dynes/cm^2.

The effects of densification were also examined with glass-overcoated ICs in terms of microcrack formation. The samples described in Subsection 6 were used. Details of the densification process are discussed in Section V. Heat treatments at 450°C in steam and in moist H_2-N_2 gas mixture for periods of up to 10 hours were applied. Glassed CMOS device wafers with overcoats of 1.1-μm thickness having $\geq$ 2 wt % phosphorus showed no signs of crack formation after the 10-hour heat treatment in steam. The linear bipolar ICs with 2 and 3 wt %

phosphorus PSG did show some small cracks over the aluminum of the unusually large capacitors, indicating that excessive stresses can form in these extreme cases of large aluminum areas. Moist forming gas (10% H_2 + 90% N_2) was less favorable than steam in preventing crack formation during the extended 450°C heat treatment.

10. Stress as a Function of Film Thickness

Stress as a function of film thickness was measured for CVD SiO_2 layers deposited at 450°C. A sequential deposition was carried out, and stress measured at intervals of 3200, 6400, 9600, 12,800, and 16,000 Å.

A plot of stress vs film thickness is shown in Fig. 14. Stress remains relatively constant up to 16,000 Å. As one increases the thickness beyond 16,000 Å, cracks form and meaningful values of stress cannot be calculated.

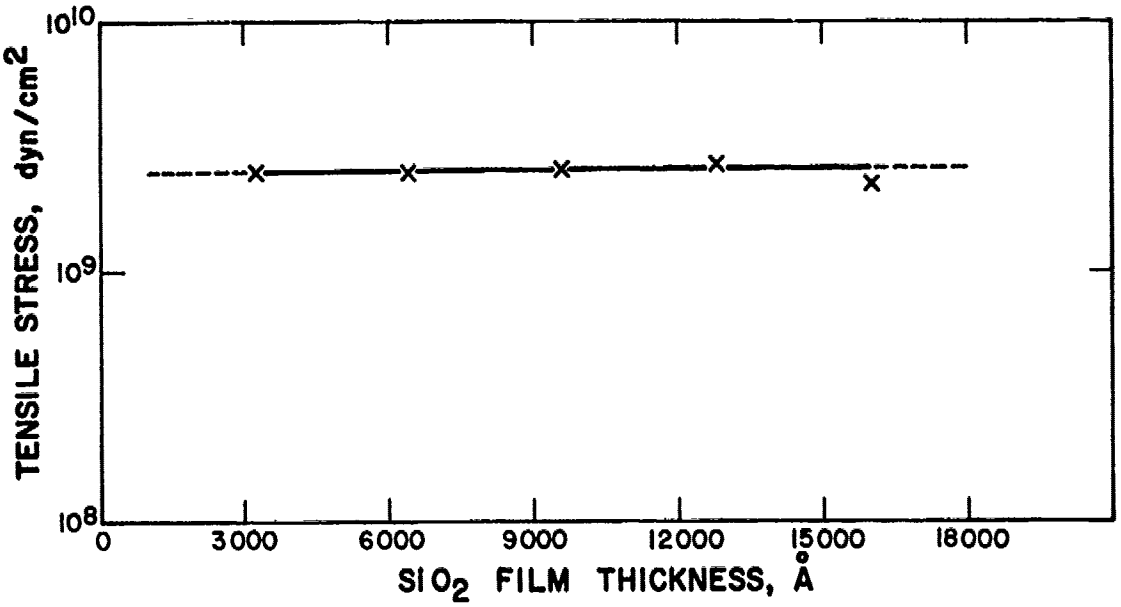


Figure 14. Stress as a function of CVD SiO_2 film thickness. Deposition rate - 1300 Å/min.

Tests with various types of integrated circuits showed that crackfree overcoat layers of PSG can be deposited to thicknesses of at least 1.2 μm, if the phosphorus content is 2 wt %. Thicker layers require higher phosphorus concentrations to avoid formation of defects due to stress. A layer of 4 wt % phosphorus

at a thickness of 2.0 μm (plus a top layer of 0.1-μm SiO_2) still cracked, indicating that the layer thickness is excessive for this phosphorus concentration.

11. Stress Measurements at Elevated Temperature

The total stress measured at room temperature is a combination of the intrinsic stress in the film as deposited by CVD at elevated temperatures and the stress arising as a result of mismatches in the thermal coefficients of expansion of the CVD film and the silicon substrate. Typically, SiO_2 of PSG films are in tension as deposited, for example, at 450°C. As the sample is cooled to 25°C, the coefficient of expansion of SiO_2, being lower than that of silicon, results in some reduction in the net tension in the CVD film.

An experiment was conducted whereby stress at the deposition temperature of 450°C for a 1-μm-thick layer SiO_2 film on silicon substrate was measured. The focal point method was used for this experiment. The focal point was measured at both 450°C and room temperature. A room-temperature calculation of stress was also made by the profiling method, as a comparison. Stress at 450°C was calculated to be 4.7×10^9 dynes/cm^2, while at room temperature the stress was 2.9×10^9 dynes/cm^2. Room-temperature stress measured by the profiling method was 2.7×10^9 dynes/cm^2. Thus, stress in this particular CVD SiO_2 film is approximately 60% greater at the deposition temperature of 450°C than at room temperature.

F. CONCLUSIONS

A number of generalizations can be made concerning the effect of deposition conditions on stress in CVD films. In particular, lower stress is attained with lower deposition rates, with higher deposition temperatures, and with higher phosphorus content. In some cases, lower oxygen/silane ratios result in lower stress levels. Relatively small changes in the magnitude of the residual stress at room temperature can correspond to relatively large differences in the incidence of cracks over large metal areas or along the edges of delineated metal films.

Since cracking at the edge of metal films depends on many factors, including the angle of the edge of the delineated metal areas, the size of the

metal area, the thickness of the metal film, and the nature of heat treatments after metallization, an appropriate technique for production control purposes is to perform selective aluminum etch tests after appropriate heat treatments of the wafer. If essentially no additional microcracks form as a result of a heat treatment step (50°C or more above the maximum processing temperature of the particular device type under study), it can be concluded that intrinsic stresses during CVD were not excessively high.

V. POST-DEPOSITION DENSIFICATION STUDIES

A. INTRODUCTION

The physical properties of oxide and silicate glass layers deposited at low temperature can generally be improved by a suitable densification treatment. In the absence of aluminum metallization, this process can be readily carried out by exposing the coated wafers to a temperature of typically 800°C for a few minutes [23]. However, for devices where such layers are deposited as an overcoat over aluminum metallization (as in the typical and important cases of most ICs and multilayer interconnect devices), it is impossible to heat the devices above the Al-Si eutectic temperature of 577°C without causing excessive and damaging alloying of the aluminum. A practical densification temperature of 450°C has been found safe, but requires thousands of hours to attain a satisfactory degree of densification, unless the densification process is catalytically accelerated by suitable means. In this section we report experimental results of studies directed toward the development of a practical process to achieve this. Chemical etch rate measurement was the primary technique used to monitor the progress of film densification.

Films of CVD SiO_2 are known to be densifiable at low temperatures [45,46]. As far as silicate glasses are concerned, we previously reported that for vapor-deposited borosilicate glass films, low-temperature catalytic densification involving use of water vapor in the furnace ambient makes it possible to improve the film properties to the point where they approach those of the bulk glasses [28], but no data were available for PSG films. We have now found that, under similar conditions, a substantial degree of densification can be attained with CVD films of PSG in a reasonable period of time (on the order of several hours) at temperatures as low as 450°C without damage to the aluminum metallization, the devices, or the structural or chemical properties of the glass itself.

The results of exploratory studies using atomic hydrogen or ultraviolet radiation will be briefly presented, although these agents have proven less

45. W. A. Pliskin, in *Semiconductor Silicon 1973*, H. R. Huff and R. R. Burgess, Eds., (The Electrochem. Soc., Princeton, NJ, 1973), pp. 506-529.
46. B. Swaroop, in *Thin Film Dielectrics*, F. Vratny, Ed., (The Electrochem. Soc., New York, 1969), pp. 407-431.

effective than thermal treatments in the presence of water vapor. There were reasons to expect that the energy available by these environments might be sufficient to effect some degree of structural bond rearrangements, resulting in molecular compaction and associated improvements in film quality that might be of practical interest. For example, atomic hydrogen is known from solid-state studies [47,48] to be a highly reactive species that could well be capable of inducing beneficial changes in the glass. Structural changes and volume compaction were measured on SiO_2 layers bombarded with ions and electrons [49]. Furthermore, it has been recently reported that substantial degrees of stress relief in silicon oxide (SiO) films deposited by reactive sputtering can be attained by ultraviolet irradiation [50]. Measurements in the present work were confined to isothermal etch rate determination to detect changes in film density. Infrared absorption spectra were taken in several instances to monitor structural changes. Some degree of stress release and densification occurs under storage at room temperature, as will be shown. High-temperature (800°C) densification is important for analytical consideration and will be noted in that connection in Section VIII.

B. EXPERIMENTAL TECHNIQUES

1. Film Deposition

Uniform PSG films of several compositions were deposited in the single-rotation reactor and by the CVD techniques described in Section III. Polished and chemically cleaned wafers of single-crystal silicon were used as substrates. For infrared absorption measurements, float-zone-refined, oxygen-free high-resistivity (100 ohm-cm) silicon slices of 0.65-mm thickness were used; these wafers were polished on both sides and had an infrared transmission in the 670 to 4000 cm^{-1} wavenumber range of 60%. Aluminum metallized device wafers with linear bipolar ICs (CA3747) and CMOS ICs (CD4017A) were included in the deposition runs. Each run consisted of an assortment of, typically, seven

47. B. E. Deal, E. L. MacKenna, and P. L. Castro, J. Electrochem. Soc. 116, 997 (1969).
48. W. Kellner and A. Goetzberger, IEEE Trans. Electron Devices ED-22, No. 8, 531 (1975).
49. E. P. EerNisse and C. B. Norris, J. Appl. Phys. 45, 5196 (1974).
50. I. J. Hodgkinson and A. R. Walker, Thin Solid Films 17, 185 (1973).

wafers of 5-cm diameter to produce in sufficient number samples of exactly identical films for different tests.

Films for thermal densification studies were deposited at a deposition temperature of 450°C. The rate of film deposition was 2000 Å/min, and the oxygen-to-hydride ratio was kept constant at 20:1. Film thicknesses of 1.0 to 1.2 μm were deposited. Films of SiO_2 used for comparison tests were deposited under the same conditions.

Films for the UV radiation and atomic hydrogen experiments consisted, in addition to those above, of thinner layers (2000 to 3000 Å) deposited at 350°C to increase the sensitivity of the tests. Films deposited at this lower temperature have a lower density; small effects of densification treatments should therefore be more readily measurable. Thinner films should be more sensitive in integrated etch tests if surface densification effects would occur.

2. Thermal Densification Treatments

All thermal densification experiments were carried out at 450° ± 3°C in resistance-heated quartz tube furnaces with quartz substrate holders. The dimensions of the quartz tubes were 5.1 cm I.D. x 100 cm length, with constricted end caps to prevent backflow of air. The ambient gas flow and water vapor conditions used are listed in Table 8. The moist gases were prepared by passing the carrier gas through a fritted glass filter type gas wash bottle maintained at 25° to 26°C. Steam was generated in an all-quartz boiling flask with ground connector joints and introduced undiluted into the furnace tube.

In the first series of tests, 3.8 wt % phosphorus PSG films were heated in moist forming gas (10 vol % H_2 + 90 vol % N_2) and in steam for periods ranging from 90 seconds to 100 hours.

In the second series of tests, films of SiO_2, 2.1 wt % phosphorus PSG, and 3.0 wt % phosphorus PSG were heated in all four ambients listed in Table 8 for periods of 0.1 to 10 hours.

3. Densification Treatments Under UV Irradiation

The radiation source used in these studies consisted of a standard mercury arc lamp with the outer glass envelope removed (GE H3T7, arc length 6.8 cm, tube diameter 2.2 cm). The lamp was operated at 1750 W, which is

Table 8. Ambient Conditions During Thermal Densification at 450°C

Nominal Ambient	Carrier Gas Purity (%)	Gas Flow Rate (cm^3/min)	Water* Evaporation Rate (cm^3 liquid/min)
Dry N_2**	99.9995	650	0
Moist N_2	99.9995	650	<0.002***
Moist(10% H_2-90% N_2)	>99.996	700	<0.002***
Steam*	---	0	5.8

* Water used was deionized and distilled.
** High-purity grade; water content 1 ppm.
*** Water source at 25 to 26°C.

above its rated value, and was positioned in front of a concave reflecting mirror. The emitted radiation was in the wavelength range of 180 to 1400 mμ, and was collimated by two pairs of plano-convex quartz lenses of 10.2-cm diameter with effective focal length of 7.6 cm, and of 7.6-cm diameter with effective focal length of 10.2 cm. These lens pairs were positioned at 15 cm and 28 cm, respectively, from the source. The projected circular radiation area was 11.4 cm in diameter with an intensity distribution of ±5%. No optical filters were used. The incident radiation was normal to the sample surface. One half of each coated wafer was shielded from UV during the irradiation with a half-wafer of silicon placed on top of the sample wafer.

In the first series of tests, irradiation was conducted for a period of 65 hours at a substrate temperature of 47°C in room air. The radiation source-to-sample distance was 35 cm. In the second series of experiments, UV irradiation was conducted at a substrate temperature of 450°C in air for an irradiation period of 20 hours. Radiation source-to-sample distance in these tests was 47 cm.

4. Densification Treatments in Atomic Hydrogen

Partly shielded film samples identical to those described in the UV tests were exposed to atomic hydrogen plasma generated by an rf glow discharge under the following conditions: The reactant gas mixture consisted of 30 vol % H_2 plus 70 vol % Ar at a pressure of 100 mm. The target area diameter was 7.5 cm.

The substrate temperature was held at approximately 300°C. Two rf potentials and exposure time periods were used. The first experiment was conducted at an rf potential of 350 V for a period of 3.25 hours, the second experiment was run at 150 V for 6.5 hours.

5. Changes in Film Properties during Room Temperature Storage

All PSG films were stored in desiccators over a drying agent (activated silica gel or Drierite) at room temperature. Films of SiO_2 were stored under the same dry conditions, and also in room air of high relative humidity. Film analyses were carried out at intervals, typically, from 15 minutes after completion of film deposition to several thousand hours of storage.

C. FILM ANALYSIS

The composition of the PSG films was determined by the etch rate analytical method described in Section VIII. The relative degree of densification effectiveness was determined by chemical etch rate measurements initially and after various periods of treatment. The isothermal etch rate of CVD oxide or glass film of constant composition is a very sensitive measure of film density, the etch rate decreasing as the density increases. Analysis was carried out by partly masking each heat-treated sample with wax, followed by measurement of the etch time [29] in P-etch [2 vol HNO_3 (70%) + 3 vol HF (49%) + 60 vol H_2O dist.] at 25.0° ± 0.2°C. The wax was then stripped and the film thickness measured by interferometric techniques using the film wedge formed along the masked area. Selected samples were checked by profilometric techniques using a Talysurf. The etch rate was calculated in Å/sec.

Infrared absorption spectra were obtained with a Perkin-Elmer double-beam spectrophotometer using the uncoated half of the identically heat-treated wafer in the reference beam. Evaluation of IR frequency shifts and absorbance ratios of representative absorption bands was carried out by techniques previously reported [23,28,45].

Measurement of film stress and electrical measurements of the IC samples were done as explained in Sections IV and VI, respectively.

D. EXPERIMENTAL RESULTS AND DISCUSSION

1. Thermal Densification at 450°C

The etch rate results for the first series of densifications in moist forming gas and steam for heat treatment periods of 90 seconds to 100 hours are presented graphically in Fig. 15. The resulting semilog plots demonstrate that densification of PSG films in steam for 1 hour decreases the etch rate to 58 percent of what it was initially, and to 38 percent in 25 hours. The etch rate decreases uniformly with the logarithm of time up to about 10 hours, and then decreases more slowly. In wet forming gas, the corresponding values to which the etch rate decreased are 75 percent and 60 percent, respectively. For comparison, high-temperature densification at 800°C (15 min, N_2) decreases the etch rate to about 31 percent of the as-deposited value (longer heat periods at 800°C have no significant additional effect).

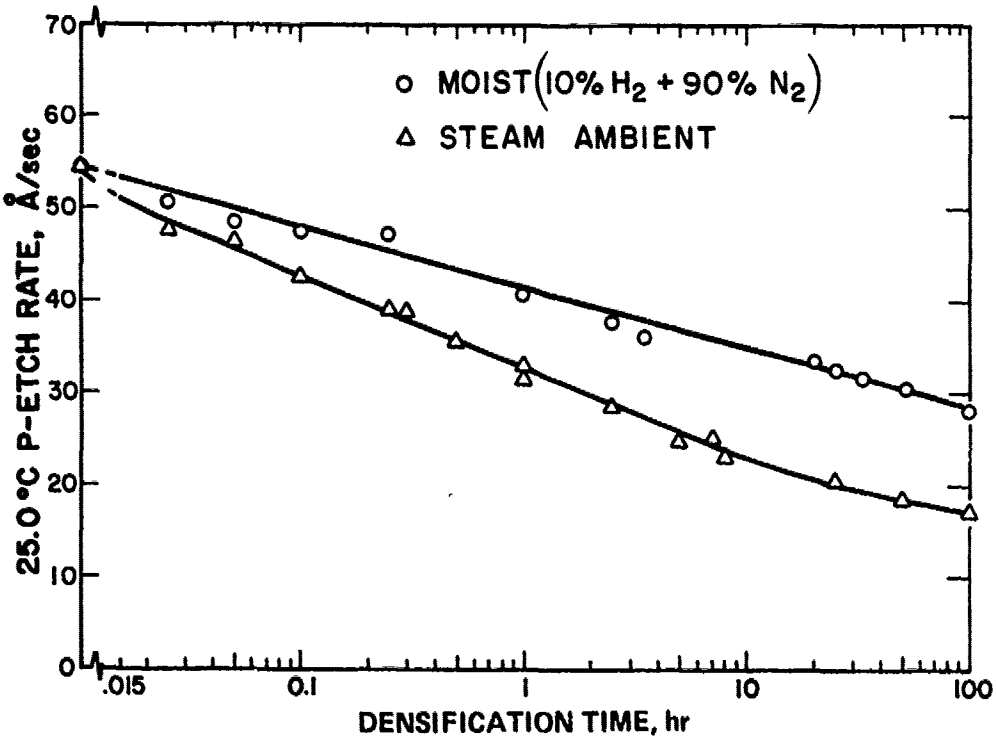


Figure 15. Etch rate of a 3.8 wt % phosphorus PSG film vs densification time and ambient at 450°C.

Infrared absorption spectra of samples from the same series, taken after 11 time intervals over a heating period of 100 hours, showed only small changes from that of the initial film. Changes in both frequency and net absorbance were measured at the positions of maximum absorption of hydrogen-bonded SiOH at about 3650 cm^{-1}, absorbed H_2O in the range of 3400 to 3300 cm^{-1}, P=O at 1335 to 1330 cm^{-1}, Si-O at 1080 to 1060 cm^{-1} and its secondary at 830 to 800 cm^{-1}. The important results are the demonstration that (1) moist H_2-N_2 or steam at 450°C do not introduce additional water into the films (in fact, some drying appears to occur), and (2) the absorbance intensity of the P=O band remains constant, indicating that no loss occurs during heating. Frequency shifts of absorption maxima were too small (within the error of analysis) to resolve quantitatively; however, the most pronounced changes appear to have occurred in the first 3 minutes of humid heat treatment at 450°C. The frequency of the secondary Si-O band shifted from an initial wave number of 830 cm^{-1} to 810 cm^{-1} for moist forming gas, and to 805 cm^{-1} for steam, and then remained essentially constant to 100 hours.

The second series of thermal densification experiments was carried out under all four conditions listed in Table 8 using films of SiO_2, 2.1 wt % phosphorus PSG, and 3.0 wt % phosphorus PSG. All three types of films were heat-treated simultaneously for direct comparison. Etch rate measurements were done after treatment periods of 0.1 to 10 hours, periods of time that are of practical interest in device processing. The results obtained are presented in Figs. 16 to 19. The initial etch rate (time zero) is the etch rate just before the start of each densification experiment; it varies slightly for each type of treatment because the samples had to be stored for various lengths of time until use. The etch rate of all samples decreases linearly with the logarithm of heating time for all four ambient conditions. The rate of decrease depends on both the ambient conditions and film type. Moist nitrogen and moist forming gas effect a considerably greater rate of decrease than dry nitrogen. Steam ambient, in turn, effects a still greater rate of decrease than the moist gases, but for the PSG films only; the rate for SiO_2 is nearly the same within the period of 0.1 to 10 hours, but the drop from the initial etch rate within the first 6 minutes is greater.

Actual and normalized etch rates for the 10 hours of heat treatment are summarized in Table 9 to facilitate numerical comparison between the various

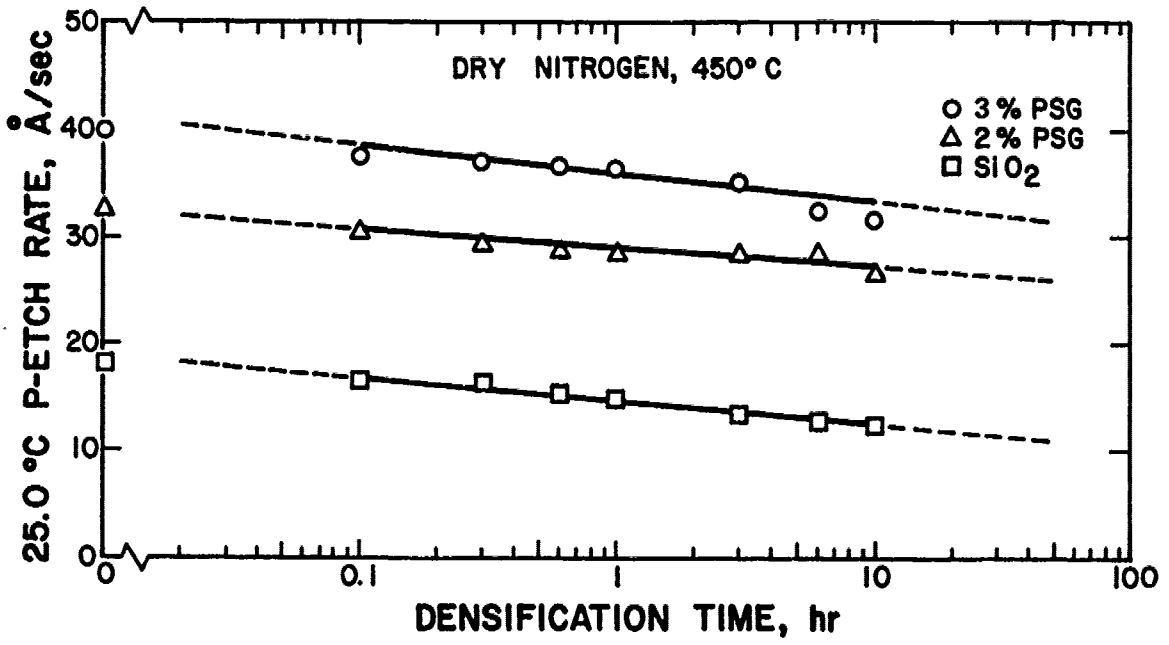


Figure 16. Etch rate of SiO_2 and PSG films vs densification time at 450°C in dry nitrogen.

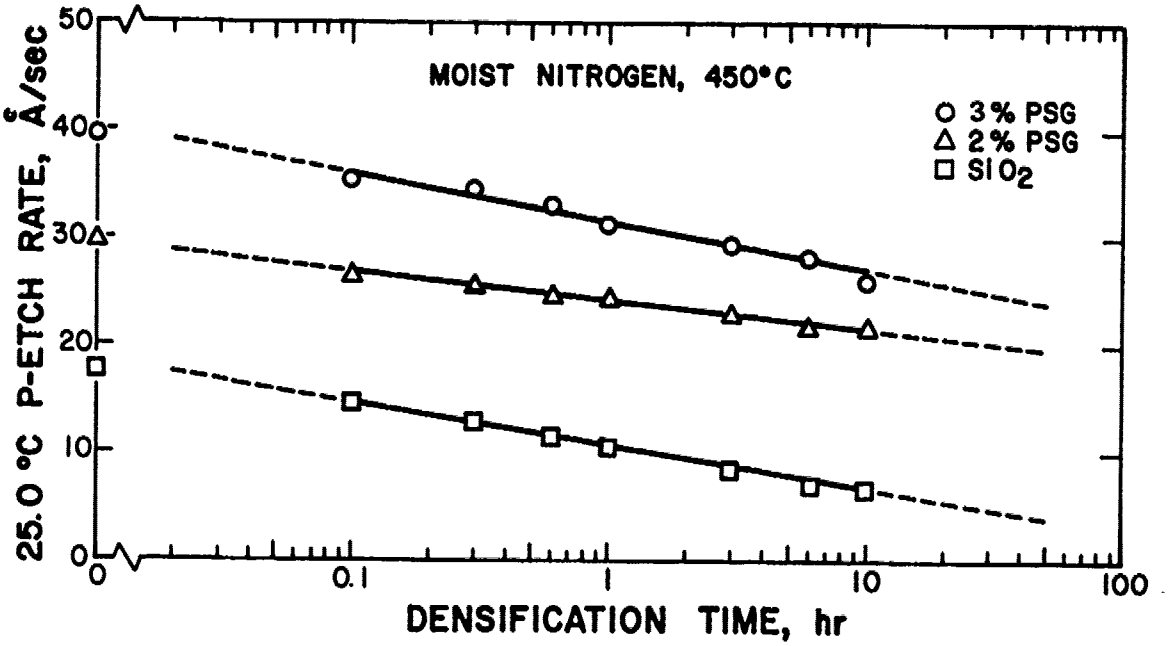


Figure 17. Etch rate of SiO_2 and PSG films vs densification time at 450°C in moist nitrogen.

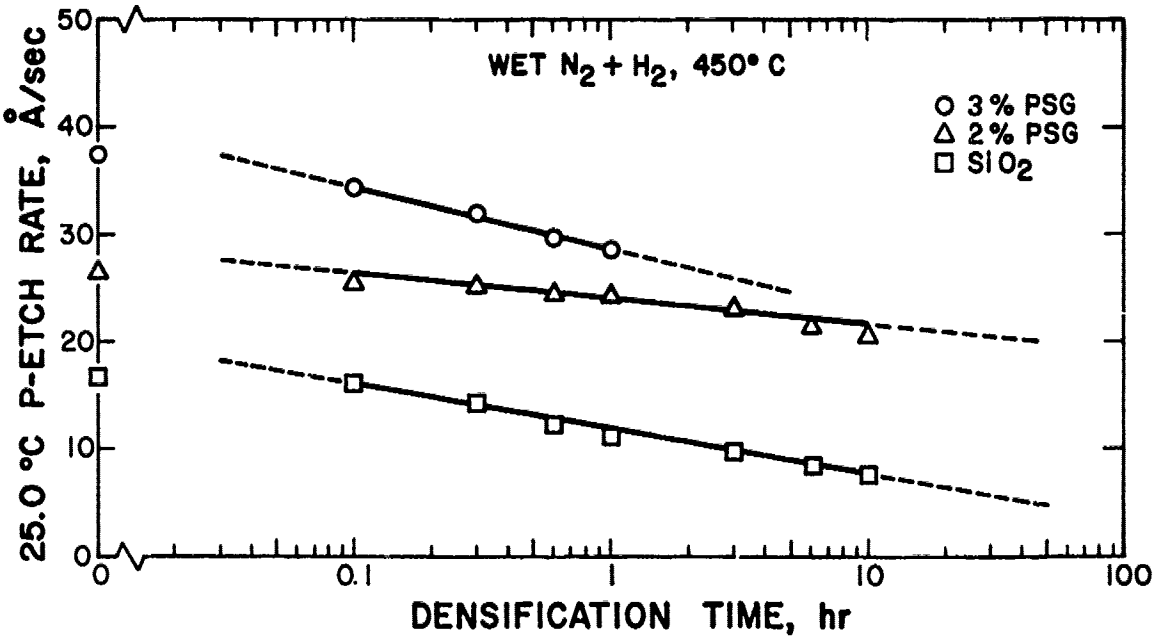


Figure 18. Etch rate of SiO_2 and PSG films vs densification time at 450°C in moist forming gas.

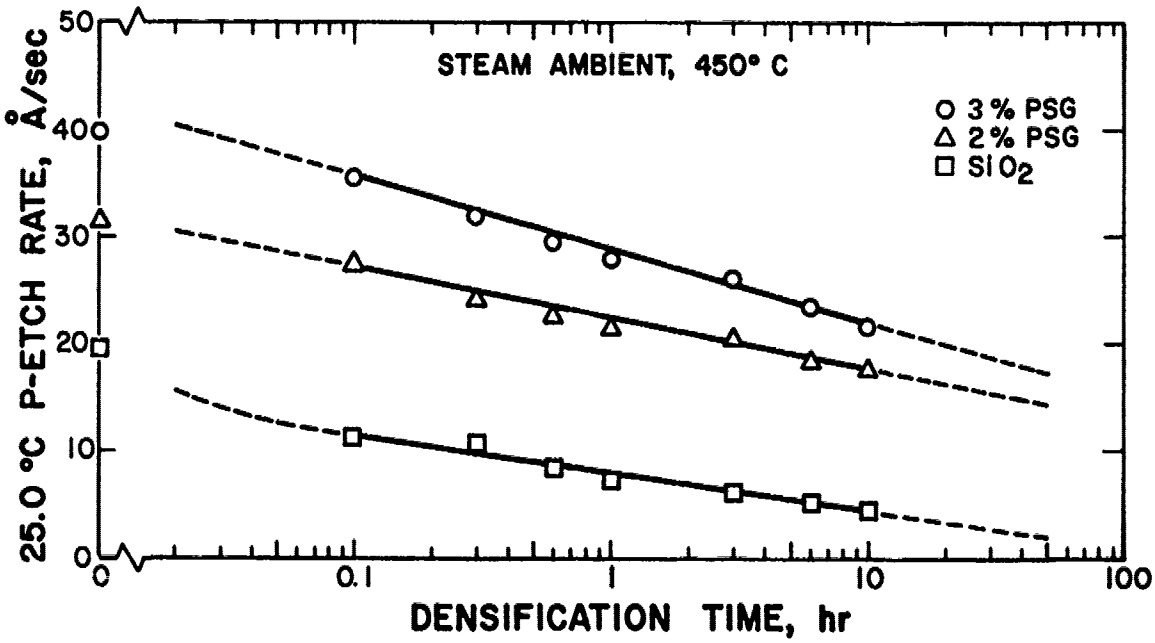


Figure 19. Etch rate of SiO_2 and PSG films vs densification time at 450°C in steam ambient.

Table 9. Summary of Results on Low-Temperature Thermal Densification

Parameter	Film Thickness (mμ)	Film Composition: Nominal, wt % P	Film Composition: Exact, wt % P	Unit	Ambient at 450°C: Dry N_2	Moist N_2	Moist N_2+H_2	Steam
Etch Rate[1] After 10 hours of Densification Treatment (P-Etch, 25.0°C)	1.10	0	0	Å/sec	12.6	6.7	7.6	4.4
				Norm[2]	1.00	0.54	0.60	0.35
				% Decr[3]	26	55	53	62
	1.15	2	2.1	Å/sec	27.3	21.3	21.8	17.7
				Norm	1.00	0.78	0.80	0.65
				% Decr.	8.4	20	19	35
	1.20	3	3.0	Å/sec	33.3	27.2	23.0	22.1
				Norm	1.00	0.82	0.70	0.66
				% Decr.	14	25	33	38
	1.00	4	3.8	Å/sec	(50.7)	(41.5)	35.0	23.0
				Norm.	(1.00)	(0.82)	(0.70)	0.45
				% Decr.	11	20	27	46

1. Note that etch rate is an inversely proportional measurement of densification (i.e., etch rate decreases as density increases).

2. All normalized etch rates are normalized to dry N_2 values.

3. Refers to decrease in etch rate from the densification period of 0.1 to 10 hours.

(). Parenthetical etch rate, normalization, and % decrease values are mathematically derived in proportion to 3% PSG etch rates.

treatments for all films. Also listed are actual and normalized values for the rate of densification in terms of etch rate decrease per hour of densification treatment.

The effects of these treatments on film stress and structural integrity have been described in Section IV. Electrical measurements (channel leakage, interelectrode and junction currents; breakdown and MOS threshold voltages; CV-BT) indicate that the electrical performance of both linear bipolar and CMOS ICs glassed with PSG overcoats is not deleteriously affected to a significant degree by the steam or moist gas heating treatment at 450°C, even in periods of up to 10 hours. Details of these measurements are described in Section VI.

2. Studies Involving UV Irradiation

The results obtained in the attempted glass densification at elevated temperature using high-intensity UV radiation as an accelerator were negative. Corrections had to be made for the temperature increase in the shielded sample area, which caused an increase in the rate on densification. Evaluation of the etch rate data showed that UV irradiation caused no measurable difference in densification. Infrared absorption spectra and metallurgical microscopy also showed no measurable changes in structure or composition of the films. Electrical analysis of the overcoat passivated ICs showed only small changes, similar to those observed during thermal desification at 450°C.

3. Densification in Atomic Hydrogen Plasma

Results obtained using atomic hydrogen plasma generated by an rf glow discharge as a densifying agent proved partly successful. Etch rate measurements showed a consistent 20% decrease in the case of the exposed portion of the sensitive 2900-Å-thick SiO_2 films, and a smaller decrease in the thicker SiO_2 films, indicating that a moderate degree of densification can be achieved by this method.

It should be noted that all samples, including quartz and glass monitor plates, became coated during these treatments with a thin, semiconductive, brownish film that was insoluble in concentrates HCl, HNO_3, NH_4OH, and hot aqueous H_2O_2-NH_4OH but was soluble in aqua regia. Auger electron spectroscopic analysis showed that the film consisted of a tungsten compound (28 at % W,

30 at % C, 17 at % O, 7 at % N, ∿18 at % miscellaneous) and has apparently originated from the tungsten heater filaments. The film was removed prior to the etch rate analyses.

4. Film Changes During Storage

We have known for a long time that the chemical etch rate of CVD dielectric films immediately after deposition is different from that measured some time later. Observations reported in the literature have indicated similar changes in etch rate, depending on storage conditions. These changes are apparently due to ambient-sensitive hydration-dehydration reactions accompanied by densification effects and partial stress release. The degree of change must be taken into account in compositional analysis based on etch rate, unless the samples are first densified (800°C) to eliminate these effects, but this is often not readily possible (i.e., analysis of mounted IC pellets). The work reported here is the first attempt to systematically examine the etch rate changes as a function of time under controlled storage conditions.

Results derived from isothermal etch rate measurements of typical films of CVD SiO_2 and PSG are summarized in Table 10. These results were obtained from data collected over a period of 15 minutes after film deposition to 2500 hours of storage of the films at room temperature in dry air. The plots of the etch rate vs log time were straight lines whose slope represents the rate of densification. The values for the measured etch rate, the normalized etch rate, and the rate of densification stated in Table 10 were read from the curves of best fit through the data coordinates. They show that the rate of densification at room temperature is linear with the logarithm of time (as at higher temperature), that the rate of densification is about 6 times greater for SiO_2 than for 4 wt % phosphorus PSG, and that the absolute density increase (in terms of etch rate decrease) is also greater for SiO_2 than PSG (i.e., 15% vs 8% in 25 hours; 29% vs 18% in 2500 hours).

Analogous analysis of PSG film compositions of phosphorus concentrations intermediate to those given in Table 10 (2 and 3 wt % phosphorus) have shown behavior similar to that of the 4 wt % phosphorus PSG listed. We also found that films deposited under different CVD conditions behave differently during storage at room temperature. For example, PSG films of similar phosphorus content, but deposited at greatly different oxygen-to-hydride ratios, exhibited different rates of densification. Some of these effects can be associated with

Table 10. Summary of Results on Long-Term Room-Temperature Densification

Parameter	Film Thickness (μm)	Film Composition (wt % P)	Unit	Storage Time in Dry Ambient (hr)				
				0.25	2.5	25	250	2500
Etch Rate[1] in P-etch at 25.0°C	0.97	4.1	Å/sec	60.0	55.6	51.3	47.0	42.7
			Norm.[2]	1.00	0.93	0.85	0.78	0.71
			% Decr.[3]	0	7.0	15	22	29
	1.00	0	Å/sec	19.2	18.4	17.6	16.7	15.8
			Norm.	1.0	0.96	0.92	0.87	0.82
			% Decr.	0	4.0	8.0	13	18

1 Etch rate is an inversely proportional measurement of densification, decreasing as density increases. Values are taken from semilog plots of best fit.

2 Etch rates are normalized to 0.25-hour values.

3 % Decrease shows exponential decrease of etch rate with time starting with 0.25-hour value.

the different rates of film deposition resulting from different O_2-to-(SiH_4 + PH_3) ratios, as explained in Section III. Different deposition rates give films of varying density, which in turn exhibit different etch rates.

To study these parameters more closely, the less complicated SiO_2 films were used. The effect of storage in humid laboratory air (∿50 to 60% R.H.) on the etch rate has been measured as a function of substrate temperature of deposition and rate of film growth at fixed O_2-to-SiH_4 ratio (18:1). These data are presented in Table 11; both measured and normalized etch rates are shown. The results show that the film deposition rate at 450°C has a pronounced effect on the etch rate, the etch rate increasing with deposition rate. The initial etch rate increases from a low of 21.3 Å/sec for a film deposited at 400 Å/min to 23.3 Å/sec for an intermediate deposition rate of 2000 Å/min, and to 25.2 Å/sec for a film grown at the high rate of 7000 Å/min. All three etch rates decrease exponentially with time at about the same rate, as seen from Fig. 20.

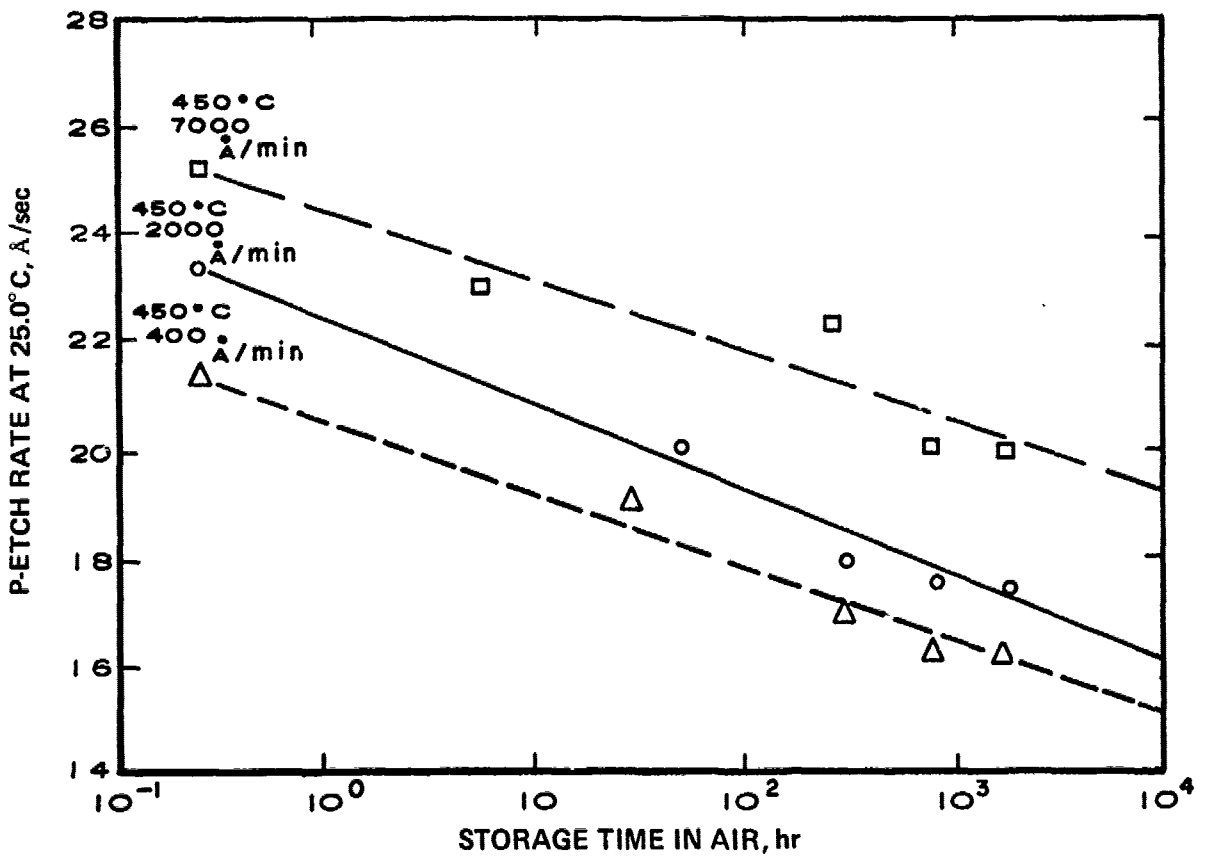


Figure 20. Etch rate as a function of air storage time of SiO_2 films deposited at 450°C at low, medium, and high rates.

Table 11. Etch Rate of SiO_2 Films as a Function of Deposition Temperature, Deposition Rate, and Storage Time

Depos. Run, #	Depos. Temp. (°C)	Depos. Rate (Å/min)	Measurement A			Measurement B			Measurement C			Measurement D			Measurement E		
			Time (hr)	Etch Rate (Å/sec)	(%)*	Time (hr)	Etch Rate (Å/sec)	(%)*	Time (hr)	Etch Rate (Å/sec)	(%)*	Time (hr)	Etch Rate (Å/sec	(%)*	Time (hr)	Etch Rate (Å/sec)	(%)*
91-1	300	1500	0.25	22.2	100	-	-	-	243	18.5	83.3	746	18.4	82.9	1776	17.7	79.7
91-2	375	2000	0.25	20.5	100	72	18.0	87.8	337	17.6	85.9	839	16.8	82.0	1867	16.2	79.0
91-3	450	2000	0.25	23.3	100	50	20.0	85.8	314	17.9	76.8	816	17.5	75.1	1844	17.4	74.6
91-4	450	400	0.25	21.3	100	29	19.0	89.2	292	16.9	79.3	794	16.3	76.5	1822	16.2	76.0
91-5	450	7000	0.25	25.2	100	5.5	23.0	91.3	262	22.3	88.5	772	20.1	79.8	1775	20.0	79.4

Fixed CVD Parameters

Reactor: Single-rotation hotplate reactor (see Appendix D).
Total gas flow: 11,050 cm^3/min
O_2/SiH_4 Ratio: 18:1

Film Storage and Analysis

In containers open to laboratory air of ∿50 to 60% R.H. at 23°C. Etchant was P-etch at 25.0°C.

Graphical Presentation of Data

See Fig. 20

*% of etch rate at t = 0.25 hr.

SiO_2 films deposited at the intermediate rate but at lower temperatures (300°, 375°C) had lower initial etch rates than the 450°C film (contrary to what was expected), but the decrease with time was distinctly slower. It also should be pointed out that the etch rates, both initially and after storage, shown in Table 11 are somewhat higher than those observed for films prepared in subsequent work under similar conditions. This effect may be due to small differences in CVD conditions that are not fully understood. Nevertheless, the results obtained demonstrate the general behavior and the magnitude and the time-exponential function of the etch rate decrease with time under room-temperature conditions.

E. CONCLUSIONS

(1) CVD PSG and SiO_2 films can be densified to a substantial extent by heating for several hours at 450°C in gaseous ambients containing water vapor as catalyst, as evidenced by isothermal etch rate measurements.

(2) The treatments do not introduce water vapor into the films; in fact, less water tends to be present after densification treatments (even in steam at 450°C) than was initially present after CVD, as confirmed by infrared spectroscopic measurements.

(3) No microcracks or other observable defects are introduced in these treatments in typical PSG (but not SiO_2) films of up to at least 1.2-μm thickness, deposited on silicon or over aluminum-metallized linear bipolar or CMOS ICs, as shown by microscopic examination and selective aluminum etching.

(4) No significant changes in properties resulted in PSG-overcoat passivated linear bipolar or CMOS ICs during these treatments for periods up to at least 10 hours at 450°C (including steam).

(5) No densification effects were detectable in SiO_2 and PSG films on exposure to high-intensity ultraviolet radiation in room air at elevated temperature.

(6) Exposure to atomic hydrogen plasma at elevated temperature in low-pressure H_2-Ar led to a moderate degree of densification in the more sensitive SiO_2 films.

(7) Room-temperature storage of SiO_2 and PSG films in dry or humid air leads to an etch rate decrease due to densification, and to stress release

effects. Measurements taken at intervals of 15 minutes after CVD to over a thousand hours of storage have demonstrated that the etch rate decreases linearly with the logarithm of time, analogous to the effects observed at higher temperatures. In all cases, the rate and absolute level of decrease depend on the phosphorus content of the films, the CVD conditions, and the densification conditions.

(8) High-temperature treatments (800°C, N_2) of PSG and SiO_2 films decrease their etch rates rapidly (within 15 minutes) to a level lower than obtainable at 450°C in steam for many hours. The etch rate beyond this period of heat treatment remains essentially constant. The degree of densification attained by this heat treatment diminishes as the phosphorus concentration increases. The largest degree of densification results at 0 wt % phosphorus (pure SiO_2), namely, about 4-fold in terms of etch rate. The two curves converge at about 15 wt % phosphorus (17 mol % P_2O_5), indicating no additional densification on heating films of this and higher phosphorus content. The high phosphorus content apparently yields a high-density film as-deposited at 450°C. Application of high-temperature densification is of great practical importance in analytical work, and is discussed further in Section VIII.D.1.

VI. ELECTRICAL PROPERTIES OF CVD SiO_2 AND PSG LAYERS

A. INTRODUCTION

SiO_2 and phosphosilicate glass (PSG) are important materials in silicon device passivation [1]. Thin layers of PSG (hundreds of angstroms) have been described as useful for sodium-gettering under gate metal of MOS devices [51-53]. Thin layers must be used to avoid instabilities due to PSG polarization [52,54-56]. For over-metal passivation of ICs, thicker layers (about 10^4 Å) can be used (since polarization of the PSG is unimportant in this geometry). Generally, over-metal layers are deposited by chemical vapor deposition (CVD) [22-24,35]. The phosphorus addition lowers intrinsic stress over aluminum metal and provides sodium gettering capability [25], which is particularly useful in plastic packaged devices. In addition, the passivating glass over metal provides important scratch protection during the device production process [57] and serves as insulating protection against loose conducting particles in hermetic packages [58].

The bulk and surface electrical properties of CVD passivation over metal are important in understanding sodium-gettering [53,59], device leakage as

51. D. R. Kerr, J. S. Logan, P. J. Burkhardt, and W. A. Pliskin, IBM J. Res. Develop. 8, 376 (1964).
52. P. Balk and J. M. Eldridge, Proc. IEEE 57, 1558 (1969).
53. J. M. Eldridge and D. R. Kerr, J. Electrochem. Soc. 118, 986 (1971).
54. E. H. Snow and B. E. Deal, J. Electrochem. Soc. 113, 263 (1966).
55. J. M. Eldridge, R. B. Laibowitz, and P. Balk, J. Appl. Phys. 40, 1922 (1969).
56. L. Kasprzak and A. Hornung, IBM J. Res. Develop. 19. 127 (1975).
57. L. K. Karstadt, W. G. Burger, C. M. Sieh, and W. A. Cosgrove, Solid State Tech. 16, No. 8, 41 (1973).
58. W. McQuitty and C. R. Lively, Electronic Pkg. and Prod. 11, No. 11, 112 (Nov. 1971).
59. T. W. Hickmott, Phys. Rev. Letters 32, 65 (1974).

affected by lateral charge spreading [60-65], metal corrosion [66-69], and moisture effects [68-69].

In this Section, measurements of bulk conductivity as a function of water uptake and temperature, and surface conductivity as a function of relative humidity (RH) are reported for CVD SiO_2 and CVD PSG. The data are used in estimating electrical and moisture effects typical for ICs. In the last Subsection (VI.G.), we report and discuss other electrical properties. All electrical test conditions refer to dc bias.

B. SAMPLE PREPARATION FOR CONDUCTIVITY EXPERIMENTS

The glass layers were deposited on degenerate n-type (0.01 ohm-cm) silicon wafers at 450°C at a growth rate of about 1000 Å/min to a total thickness of 1 μm, using a reactor described by Kern [35,70]. Phosphorus concentrations are 0, 4.8, and 8.5 wt % phosphorus in the glass. No post-deposition heat treatments were applied.

Aluminum was evaporated to a thickness of 8700 Å on the surface of the CVD layers and delineated by photolithography into an interdigitated electrode pattern (shown in Fig. 38, Section VII). By proper electrical connection, this pattern allows measurement of bulk conductivity through the glass between one aluminum surface electrode and the silicon wafer, with the other surface electrode acting as a partial guard band, or it allows measurements of surface conduction between the two surface electrodes. The interdigitated pattern has an electrode spacing of 1.3×10^{-3} cm, an effective electrode width of 0.23 cm, and an electrode area (used for bulk measurements) of 10^{-3} cm^2.

60. W. Shockley, W. W. Hooper, H. J. Queisser, and W. Schroen, Surface Science 2, 277 (1964).
61. E. S. Schlegel, G. L. Schnable, R. F. Schwarz, and J. P. Spratt, IEEE Trans. Electron Dev. ED-15, 973 (1968).
62. E. S. Schlegel and G. L. Schnable, IEEE Trans. Electron Dev. ED-16, 386 (1969).
63. E. S. Schlegel, R. S. Keen, and G. L. Schnable, 8th Ann. Proc. Reliability Physics, 9 (1971).
64. R. Castagne, P. Hesto, and A. Vapaille, Thin Solid Films 17, 253 (1973).
65. G. A. Brown, K. Lovelace, and C. Hutchins, 11th Ann. Proc. Reliability Physics, 203 (1973).
66. R. S. Alwitt, J. Electrochem. Soc. 121, 1322 (1974).
67. S. C. Kolesar, 12th Ann. Proc. Reliability Physics, 155 (1974).
68. H. Koelmans, 12th Ann. Proc. Reliability Physics, 168 (1974).
69. W. M. Paulson and R. W. Kirk, 12th Ann. Proc. Reliability Physics, 172 (1974)
70. W. Kern, RCA Review 29, 525 (1968).

The wafers were subdivided into pellets containing four interdigitated patterns each, and some pellets were mounted on TO-5 headers without hermetic cover for bulk measurements. This provided convenient handling and circuit connection and allowed exposure to steam. On each header-mounted pellet, three surface electrode pairs were connected to leads by means of bonded wires, and one connection was provided to the silicon substrate. Other pellets were not mounted on headers but were tested "as is" in a probe station for both bulk and surface measurements. Conductive silver-epoxy pastes were used as back electrodes in all cases.

C. MEASUREMENT AND TEST PROCEDURE

1. Bulk Electrical Conductivity

In all electrical measurements, a Keithley 602 or 610B electrometer was used, and a strip chart recorder continuously monitored the current.

Preliminary measurements of bulk and surface current as a function of voltage, temperature, ambient (air or N_2 with varying relative humidity), and autoclave exposure time (in steam at 15 psig, 121°C) established the following:

(1) In dry N_2 ambient, measurements of current flow between one surface electrode and the silicon substrate could be made without surface current contributions, thus permitting measurement of bulk properties of the glass.

(2) In most cases the time rate of change of current decreased 10 to 100x one minute after voltage application compared with initial values, and after one minute, the current level was approximately linear with voltage, in the voltage range from 50 to 200 V. Little dependence on polarity was observed.

(3) Leakage current of the TO-5 header itself was negligible.

Based on these preliminary results, a test procedure was established and carried out as follows:

(1) The current between one surface contact and the substrate was measured in dry N_2 flow at 100 V. The current level one minute after voltage application was selected for evaluation.

(2) Measurements were done at three temperatures: 20°, 60°, and 95°C. Initially, all chips used were measured at the three temperatures. After autoclave stress treatment, each chip was measured at only

one of the three temperatures for all succeeding measurements. In the data to be presented, each data point at 0 hour autoclave time represents an average of 24 measurements, while each data point after autoclave exposure represents an average of eight measurements.

(3) The samples were placed in the steam phase of the autoclave with a cover arrangement to minimize condensate dripping. Exposure was usually five hours at a time, with current measurements made at the end of each stress period. After removal from the autoclave the samples were dried for five minutes in dry N_2 flow at room temperature to remove surface water, and the measurements were done immediately thereafter. The current was measured in a small oven whose temperature was continuously monitored; variation was less than $\pm 2°C$.

2. Surface Electrical Conductivity

For these measurements the pellets were placed in a probe station to which mixtures of dry and wet N_2 were admitted to achieve controlled, variable relative humidity. All these measurements were done at 23° $\pm 2°C$, and no autoclave stress was used. Two probes were used to contact the interdigitated patterns on the pellet, and the four patterns on each pellet were measured at 100 V. The substrate was grounded. Again, the 1-min current level was chosen for analysis.

D. EXPERIMENTAL RESULTS

1. Bulk Conductivity

The time dependence of the current after voltage application depends on the presence of phosphorus. For SiO_2 the current increases slowly to a steady-state value, while with the 4.8 and 8.5 wt % phosphorus samples the current decreases after voltage application. This behavior is shown in Fig. 21. As mentioned previously, currents at 1 minute are chosen for evaluation in all succeeding analyses. For all samples, evidence of a polarization process exists. If the sample is short-circuited after voltage application, a reverse current is measured for several minutes.

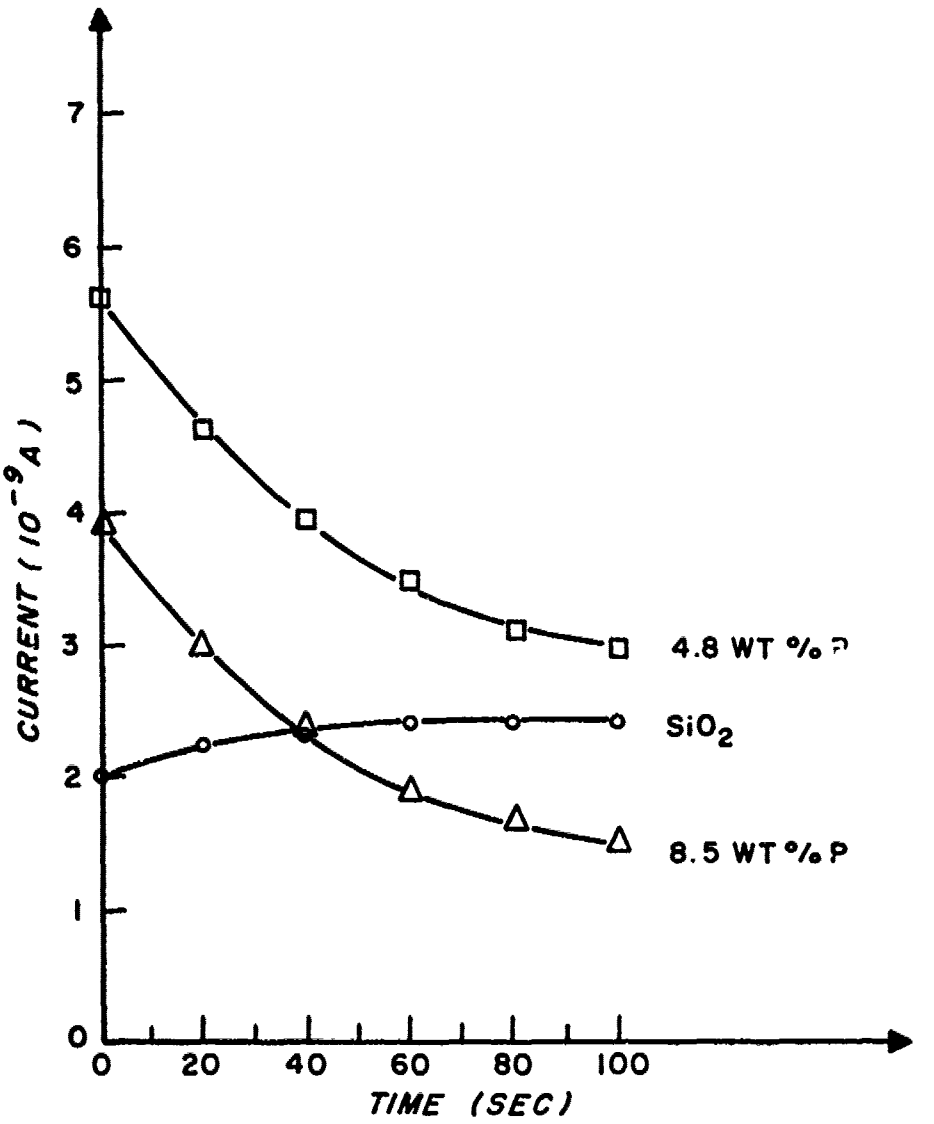


Figure 21. Time dependence of current in PSG and SiO_2 samples.

At 95°C the current in the SiO_2 sample decays upon reaching a maximum value after the initial slow increase. The decay lasts more than one hour, and at the end of one hour it has decayed to 25% of its peak. For the PSG at all temperatures the decay also continues for at least one hour, and the current decreases about an order of magnitude from the 1-min level. Current levels at one minute were used for analysis for convenience.

As expected, the bulk current increases with cumulative steam exposure. The 0 wt % and 4.8 wt % phosphorus samples show an initial bulk conductivity

increase which saturates at about 10 hours of moisture exposure. The 8.5 wt % samples show a smaller initial conductivity increase followed by a second increase at about 20 hours. After 20 hours the conductivity of the 8.5 wt % samples is generally higher than that of the 0 wt % and 4.8 wt % samples. This general dependence was found at all three measurement temperatures. A typical case is shown in Fig. 22.

The dependence of the current level on the phosphorus concentration varies with autoclave time. Before autoclave stress, the current of the phosphorus-containing glass is lower than that of the phosphorus-free glass (SiO_2). This is shown in Fig. 23 for three temperatures. After 10 hours of steam exposure, the current is greatest for the 4.8 wt % sample and lowest for the 8.5 wt % sample, as shown in Fig. 24. After 25 hours, Fig. 25 shows that the current level increases with increasing phosphorus content.

The temperature dependence of the current is different for the SiO_2 as compared with the phosphorus-containing glass. As shown in Figs. 26 to 28, the current-temperature dependence of the SiO_2 is well characterized by a single activation energy of 0.6 eV, and this energy is independent of autoclave exposure. The current level increases with autoclave exposure, but the activation energy is unchanged. The phosphorus-containing glass before autoclave stress has an activation energy of 0.8 eV, independent of phosphorus concentration, as shown in Fig. 26. After steam exposure, the activation energy tends to decrease for these samples, as shown in Figs. 27 and 28, and in some cases a thermally activated process is not indicated.

For the 8.5 wt % phosphorus samples after long autoclave exposure, it was found that a decrease in measured conductivity occurred for the elevated temperature measurement due to the several-minute delay between placing the sample in the oven and performing the current measurement. This was at most a decrease of 40% and has little effect on the activation energy determinations.

2. Surface Conductivity

The current at 23°C is constant and very low below about 30% RH and begins to increase above that value. Below 30% RH the current reflects bulk contributions. The SiO_2 above 30% RH has a greater surface current than the PSG samples as shown in Fig. 29, at least up to about 70% RH.

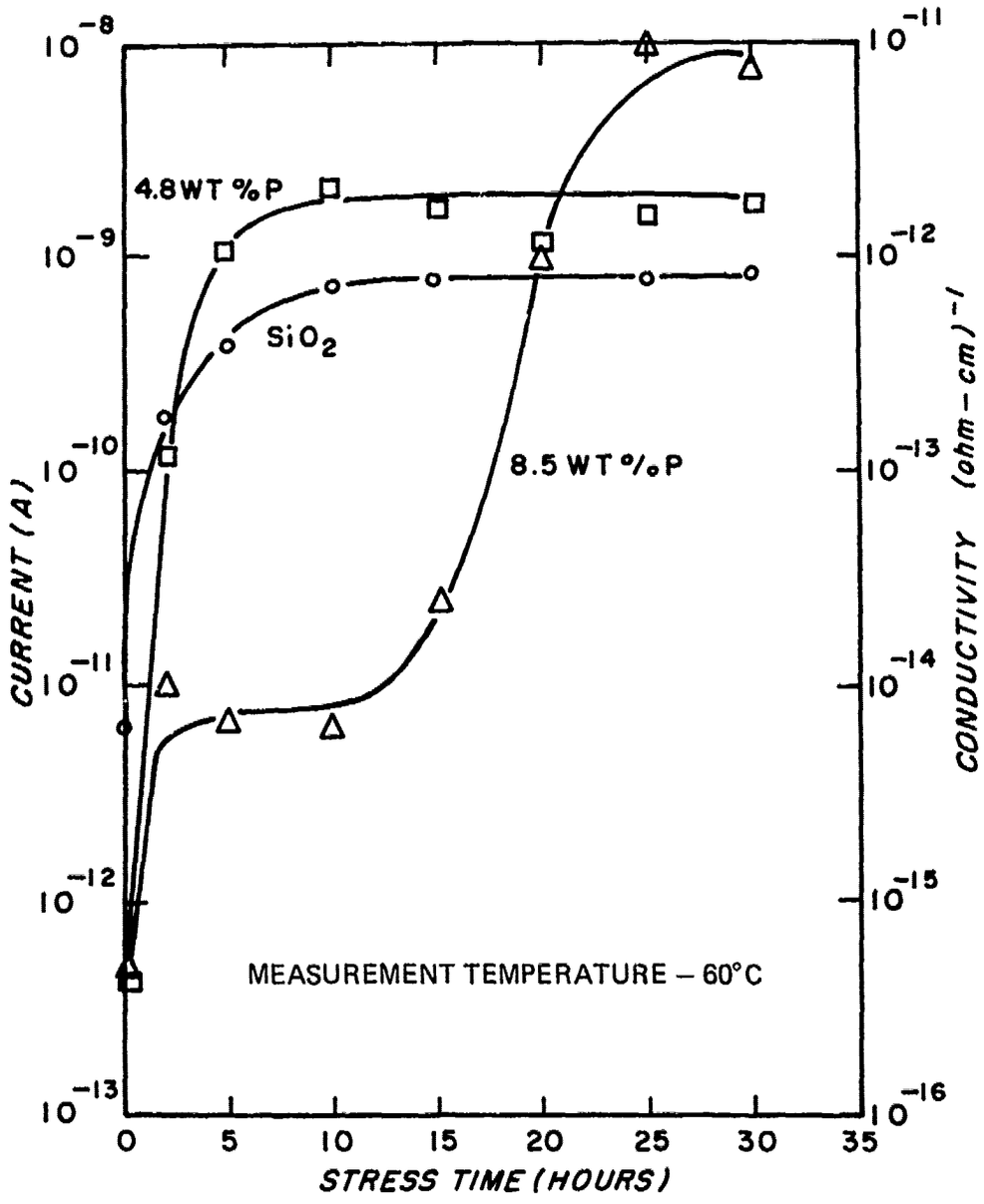


Figure 22. Typical effect of cumulative steam exposure on current and conductivity of PSG and SiO_2 samples.

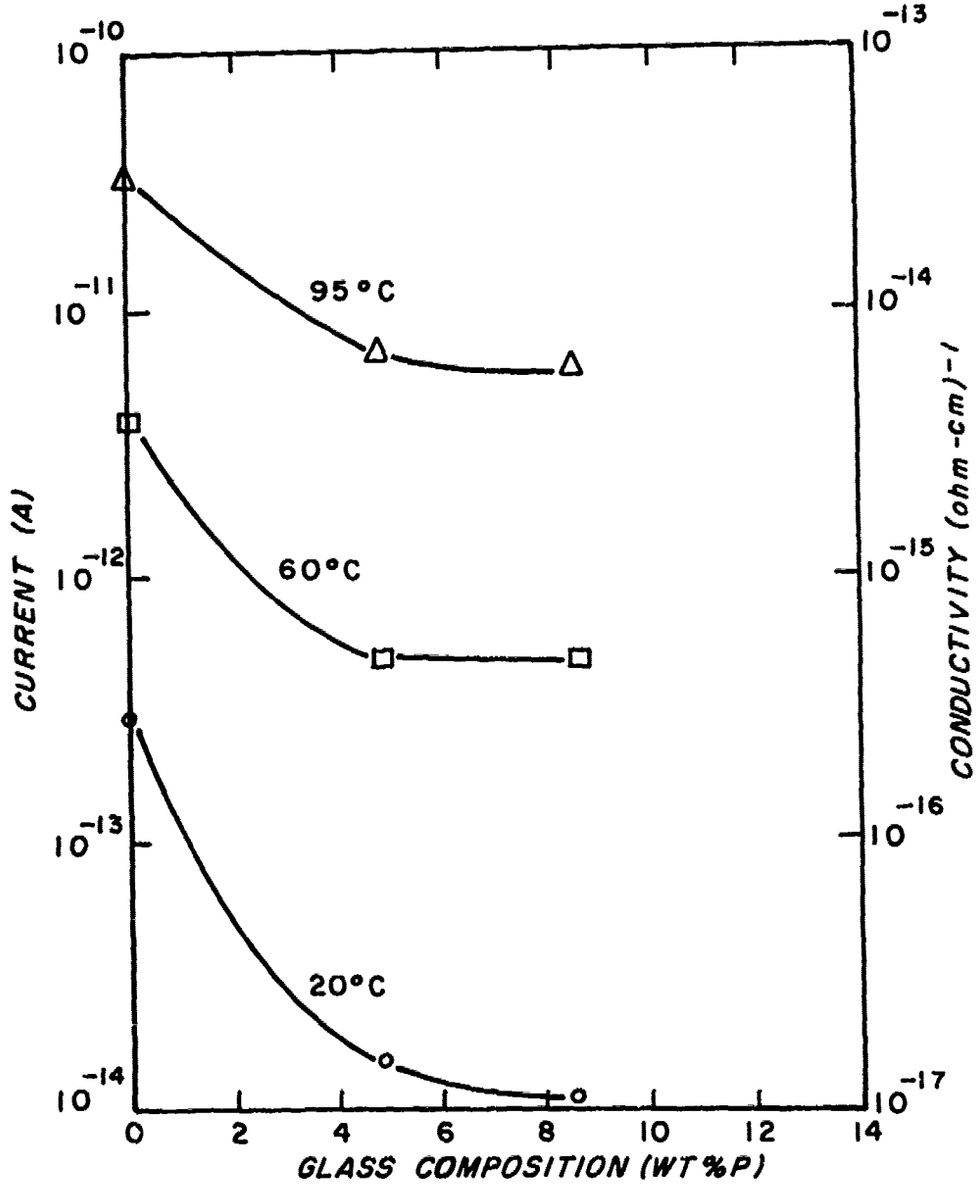


Figure 23. Typical effect of phosphorus concentration on current and conductivity at three different temperatures.

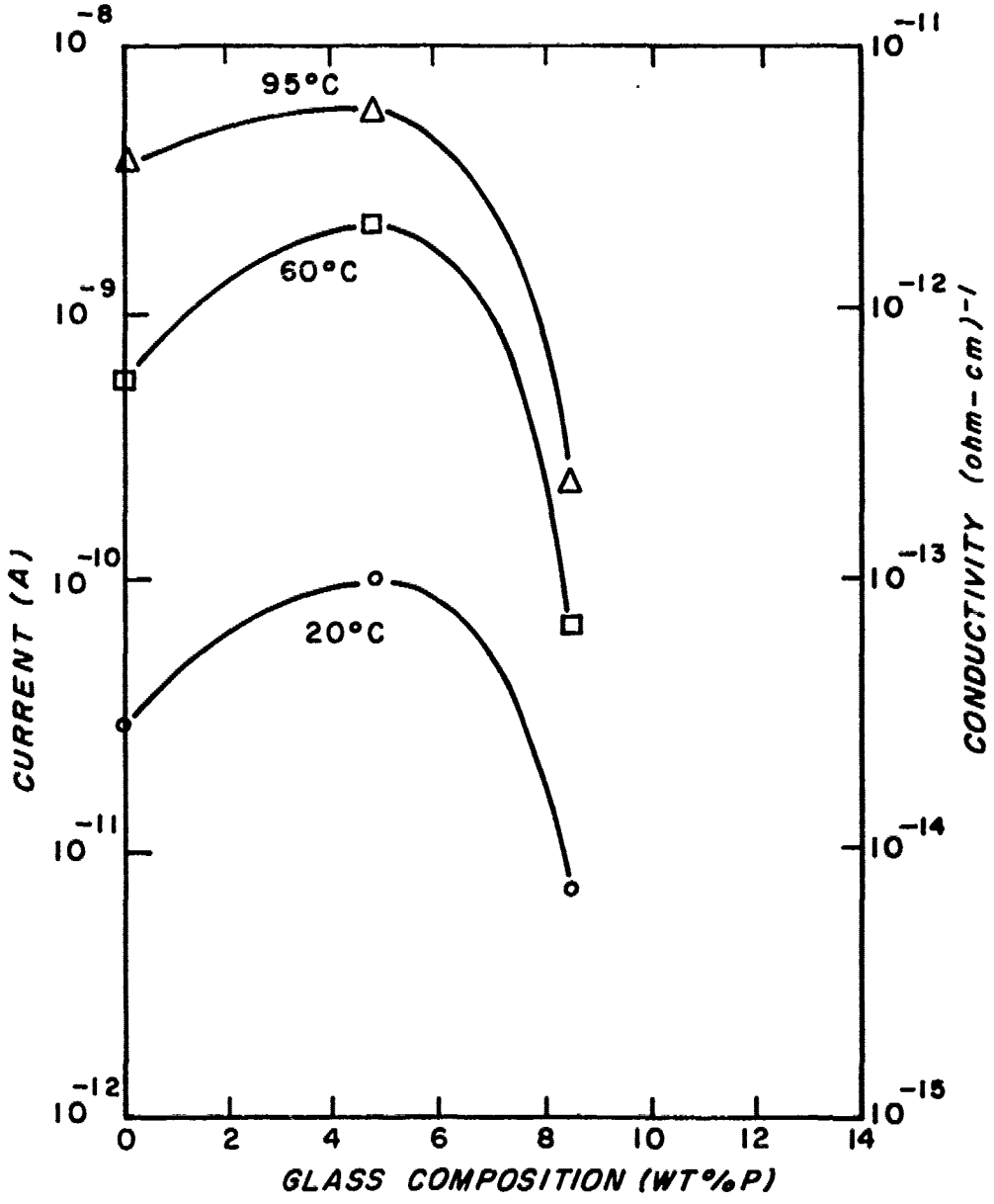


Figure 24. Effect of phosphorus concentration on current and conductivity at three different temperatures *after* 10-hr exposure to steam.

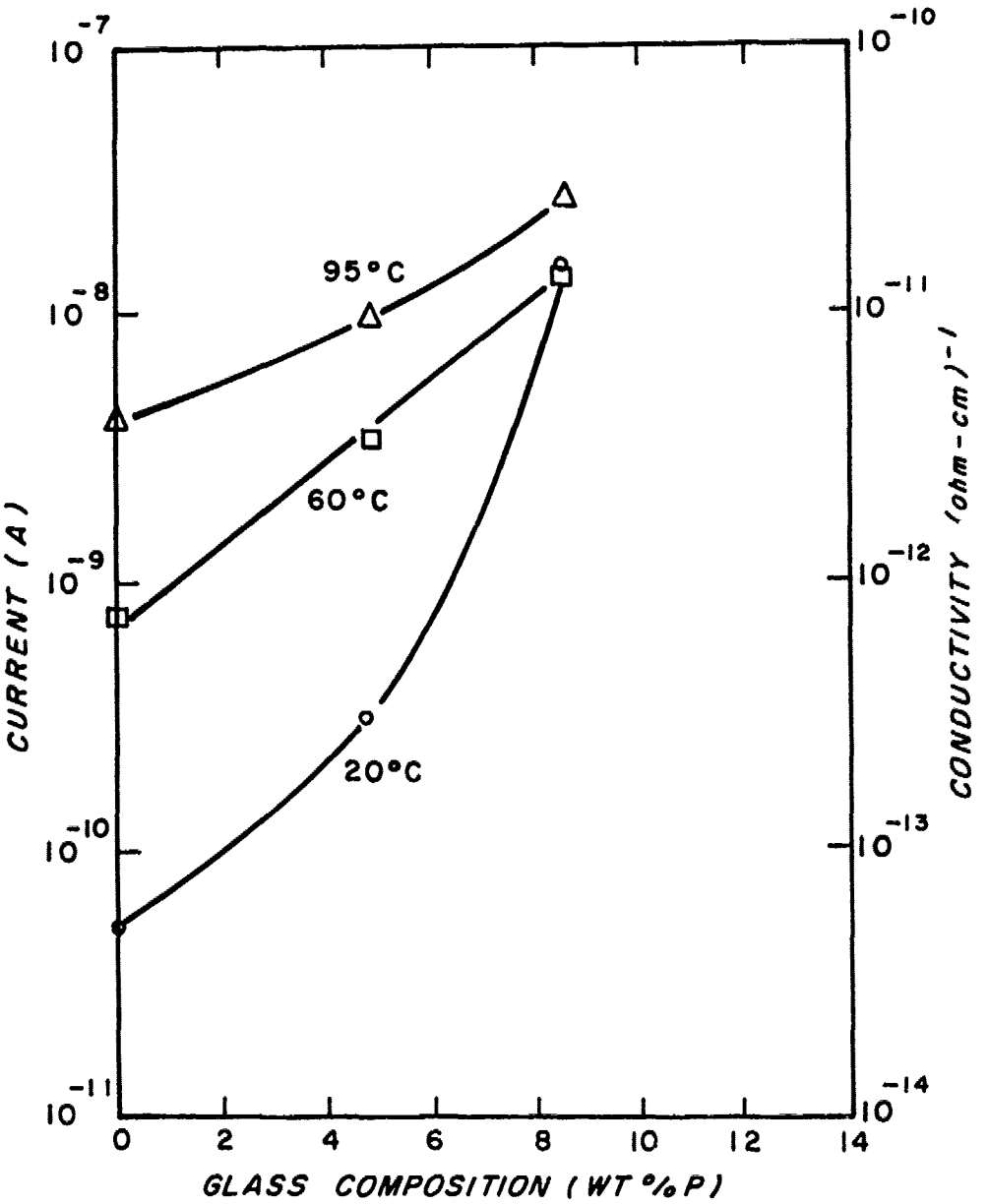


Figure 25. Effect of phosphorus concentration on current and conductivity at three different temperatures *after* 25-hr exposure to steam.

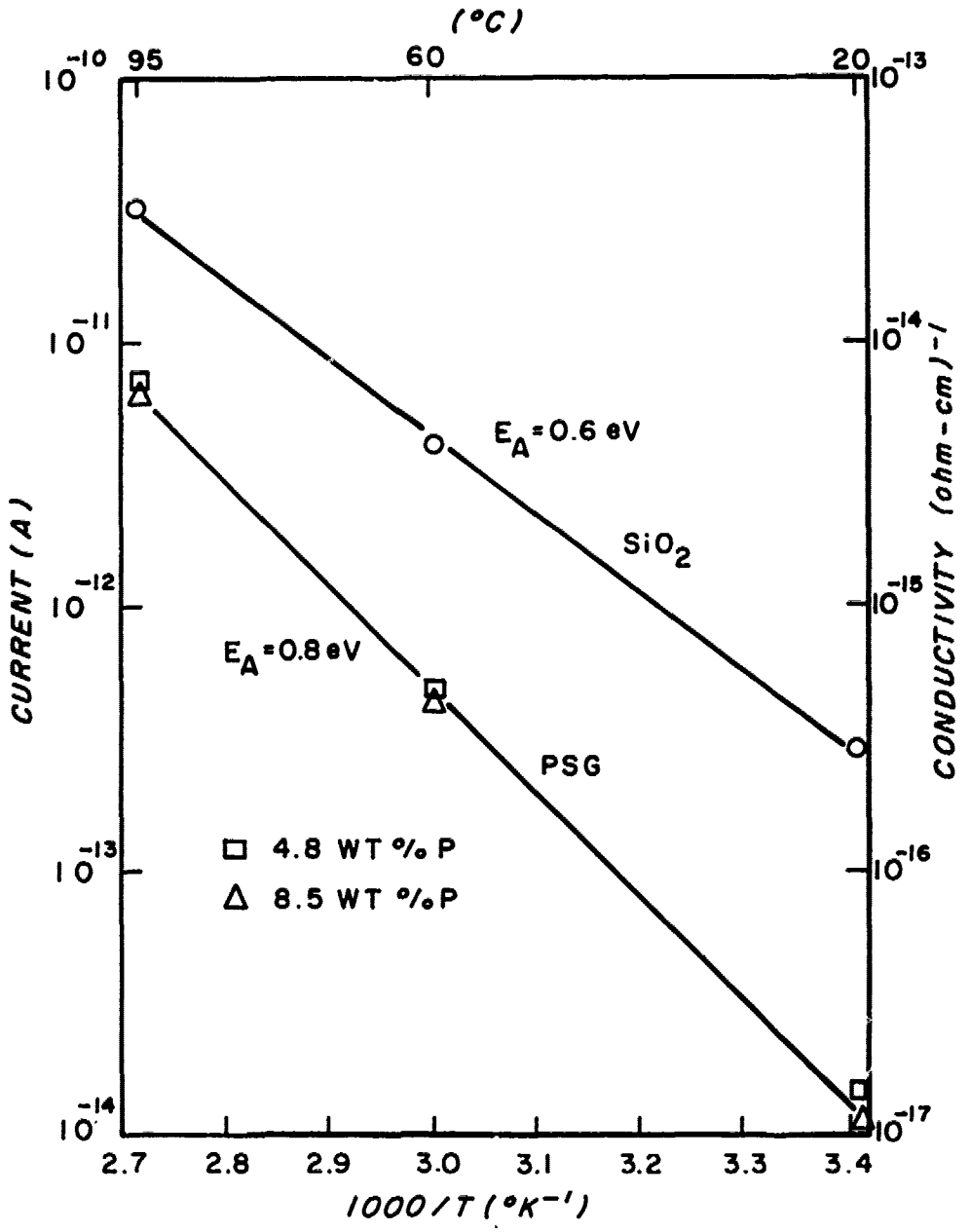


Figure 26. Temperature dependence of current and conductivity as a function of temperature for SiO_2 and PSG samples.

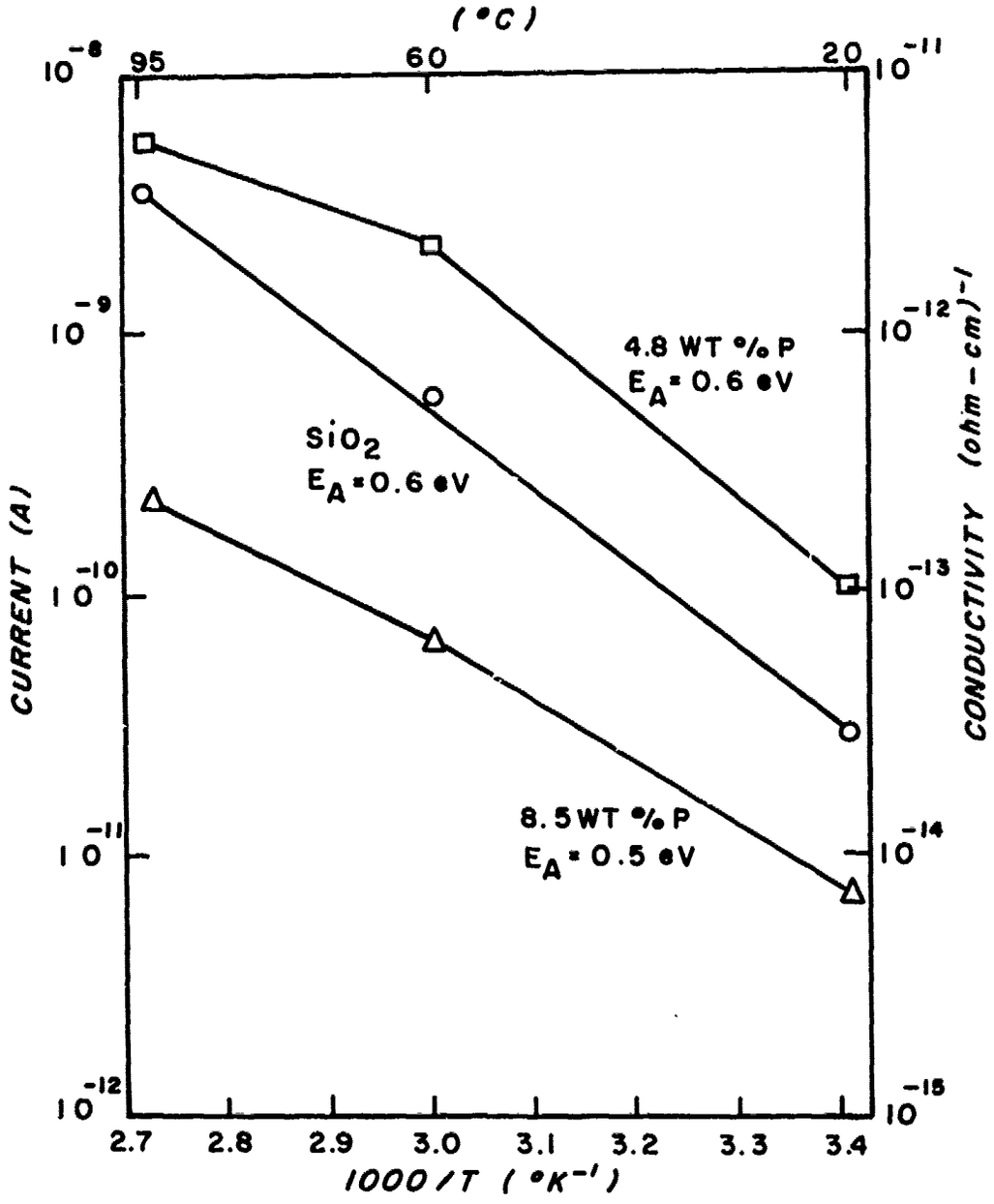


Figure 27. Temperature dependence of current and conductivity as a function of temperature for SiO_2 and PSG samples after 10-hr exposure to steam.

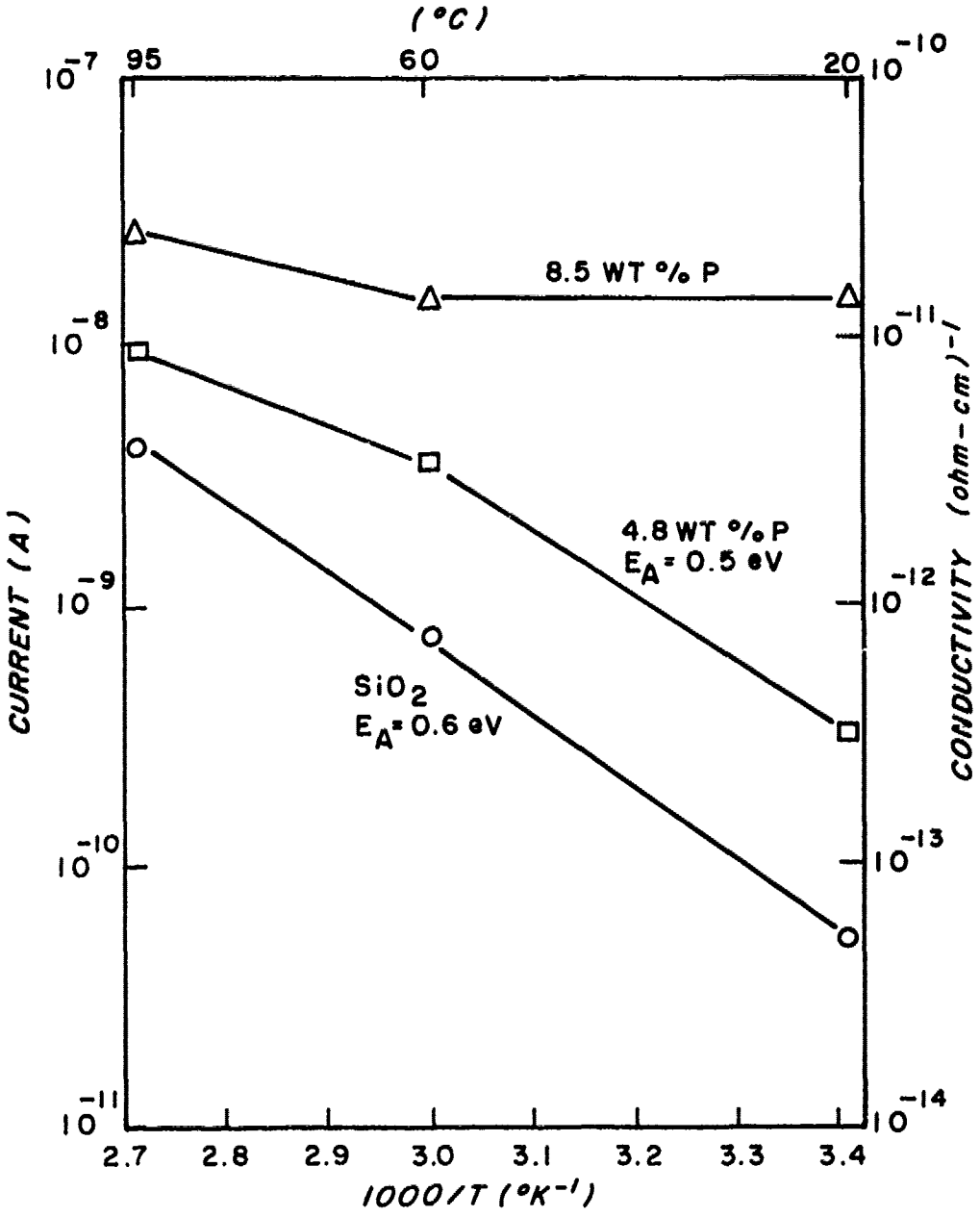


Figure 28. Temperature dependence of current and conductivity as a function of temperature for SiO_2 and PSG samples after a 25-hr exposure to steam.

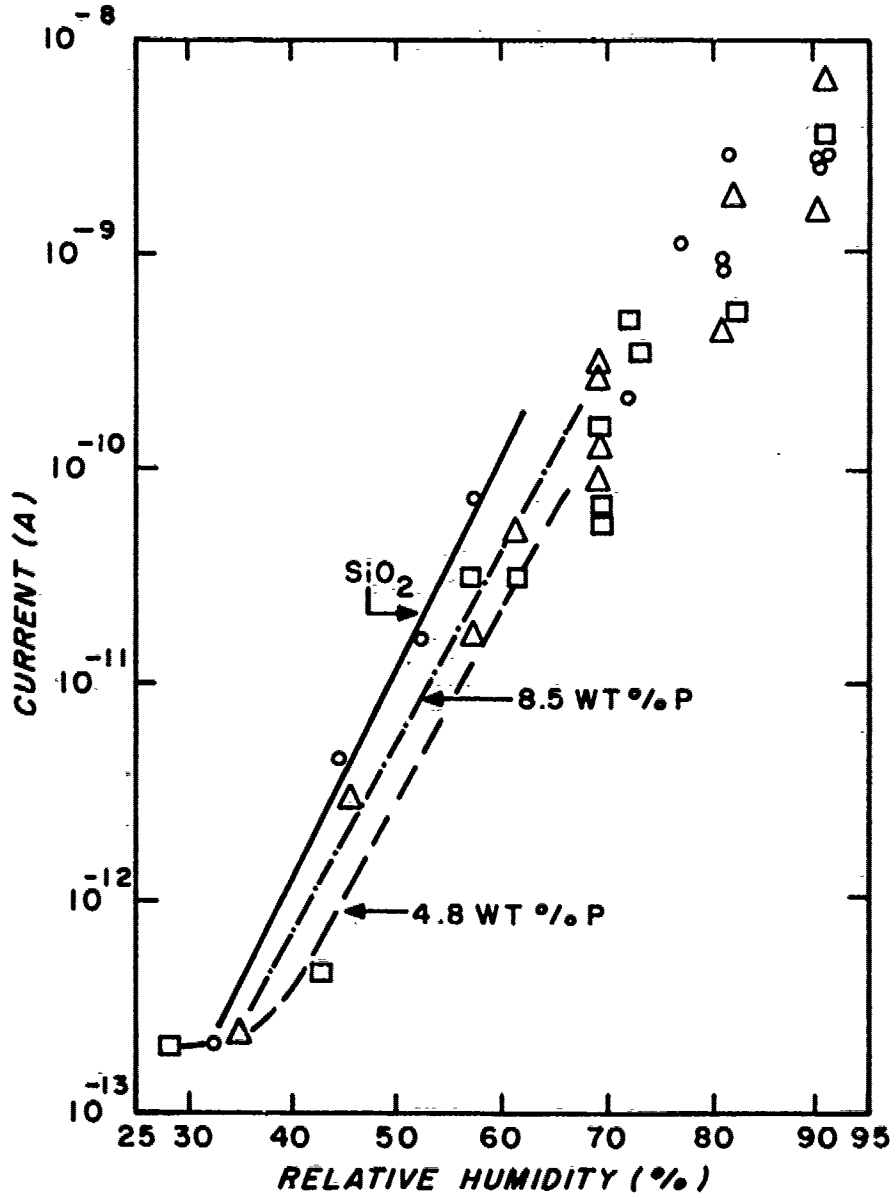


Figure 29. Current as a function of relative humidity for SiO_2 and PSG samples.

3. Effect of Cracks in PSG

In a separate experiment the effect of cracks in PSG over metal was determined. An aluminum line pair pattern on thermal SiO_2 with an electrode gap of 1.0×10^{-3} cm and a line length of 7.5×10^{-2} cm was overcoated with about 1.0×10^{-4} cm of 5 wt % phosphorus PSG. In humid nitrogen (RH 60%) the current at 100 V between line pairs was determined to be about 5×10^{-13} A. Probes

were then used to crack the glass over each of the metal line pairs, and the current level increased to about 5×10^{-10} A. Upon introducing a dry nitrogen ambient, the current decreased to about 10^{-14} A.

E. DISCUSSION OF CONDUCTIVITY EXPERIMENTS

1. Conductivity and Activation Energies

The difference in time dependence of the bulk current between the SiO_2 and PSG samples and the fact that before autoclave stress the SiO_2 conductivity is higher than that of the PSG suggest that sodium ion motion in the SiO_2 accounts for all or a large part of the observed current. CVD SiO_2 films frequently have high sodium content [62]. Sources of sodium in the films discussed here are not known, but are probably numerous since sodium-free aluminum was not used and clean MOS fabrication procedures were not followed.

The long-term steady-state value of current in the SiO_2 samples (greater than that of the PSG) suggests a large reservoir of sodium at the aluminum contact interface or at the silicon interface. This large reservoir contributes a constant release rate of charge which results in a constant current. At 95°C the release rate is high enough that an effective decrease in the reservoir is observed, leading to a gradually decreasing current. For the PSG samples, sodium motion is blocked so that the currents, before autoclave moisture is introduced, are lower.

The activation energy of the bulk conductivity for the SiO_2 layer does not change with moisture content. The value of 0.6 eV may be compared with that of 0.5 eV for thermal SiO_2 contaminated with 1.0×10^{13} Na/cm^2 [53], and with 0.6 eV (thermal oxide) previously reported [71]. It should be pointed out that activation energies of sodium motion in SiO_2 and PSG depend both on sodium concentration and phosphorus concentration [53]. The 0.8-eV activation energy for PSG before autoclave exposure is also in the range reported previously for sodium drift in PSG [52,53].

For thermal SiO_2 at 200°C, resistivity values of 2×10^{15} and 5×10^{16} ohm-cm have been reported for phosphorus-doped and undoped layers, respectively [54]. Extrapolation of data in Fig. 26 to 200°C yields about 5×10^{11}

71. M. Kuhn and D. J. Silversmith, J. Electrochem. Soc. 118, 966 (1971).

ohm-cm for both phosphorus-doped and undoped CVD SiO_2. CVD PSG films are less dense and have higher etch rates than densified PSG films of similar composition [23], and, thus, greater conductivities might be expected in low-temperature CVD films.

As pointed out previously, the SiO_2 is more conducting than the PSG before autoclave exposure. With sufficient autoclave exposure the PSG layers are more conducting than the SiO_2. Note that the SiO_2 and 4.8 wt % phosphorus PSG currents increase to a saturation value in about 10 hours of steam exposure, while the 8.5 wt % phosphorus PSG layer increases in two steps to a saturation value at about 25 hours. These times are functions not only of the glass properties but also of the sample and electrode geometry. In the test samples used in this study, water must penetrate the glass surface and diffuse laterally under the metal to result in current increase. For PSG used as over-metal passivation on an IC it is expected that moisture penetration into the PSG would be faster under the same conditions we describe.

The much greater increase of conductivity after autoclave exposure of the PSG as compared with that of the SiO_2 is not unreasonable in view of possible phase segregation of the PSG into small pockets of a phosphorus-rich phase in a SiO_2 matrix [72]. The presence of two phases furnishes interface paths for water penetration and enhanced electrical conduction. At high autoclave steam temperatures (200°C) it has been reported [73] that the P_2O_5 is actually leached out of the PSG, leaving behind a network structure [73]. The authors state that this does not occur at 120°C [73]. Phosphorus leaching into saturated water vapor at 120°C has been reported [74] for PSG films of high phosphorus content (about 10 mol % P_2O_5 for films deposited at 450°C). This leaching out is easily detected by microscopic examination [73]. None of the samples considered here showed this effect. In addition, IR absorption measurements showed no decrease in phosphorus content after autoclave exposure at 121°C.*

72. P. F. Schmidt, W. vanGelder, and J. Drobek, J. Electrochem. Soc. 115, 79 (1968).
73. J. Sato, Y. Ban, and K. Maeda, 9th Ann. Proc. Reliability Physics, 96 (1971).
74. N. Nagasima, H. Suzuki, K. Tanaka, and S. Nishida, J. Electrochem. Soc. 121, 434 (1974).

*See Section VIII. D.6.

2. Surface Current

The behavior of the surface current in Fig. 29 is consistent with the presence of sodium on the surface and with previous results [63]. At low RH (below about 70 percent) the phosphorus blocks sodium ion motion in contrast to the SiO_2 samples. The large scatter from sample to sample above ∿80% RH may reflect the presence of more than a monolayer of water and widely varying sodium contamination of the surface from sample to sample.

3. Leakage Effects in ICs

In this section, a worst-case estimate of leakage current for a typical IC in plastic will be made, based on the highest bulk and surface conductivities described previously. These values are those after 25 hours of autoclave treatment with current measured at 95°C. For the typical IC we assume the following geometry: electrode gap of 2×10^{-3} cm, length of 0.1 cm, and metal line width of 10^{-3} cm. A metallization overcoat of 5×10^{-5} cm of 8.5 wt % PSG is also assumed. Figure 30 shows the possible current paths in a schematic IC cross section. Path c is an interface path between the thermal oxide and the PSG interface. This current contribution is neglected. Path A represents the bulk conduction through the PSG between buried metal lines. Paths B and b represent the bulk and surface components of the surface path not involving openings in the PSG. Path b alone represents current flow between conductors which have discontinuities in the PSG above them. Leakage current flowing between open bond pad areas to other bond pads or to metallization lines is assumed small compared with that flowing between closely spaced metal interconnects since lateral bond pad spacing is usually large compared with interconnect lateral spacing. We ignore current at the thermal SiO_2-PSG interface and in the thermal SiO_2 and calculate the parallel contributions of the bulk flow component through the PSG between metal lines (path A), and of the surface component (path B-b), which has a series bulk term (path B) for current flow from the line to the surface, and from the surface back through the PSG to the other line. At 95°C, after 25 hours of autoclave exposure, the bulk resistivity is about 5×10^{10} ohm-cm (Fig. 28). The surface resistance in humid ambient is about 2×10^{12} ohms/sq., obtained by using the value measured at room temperature and extrapolating to 95°C using Koelmans' activation energy of 0.35

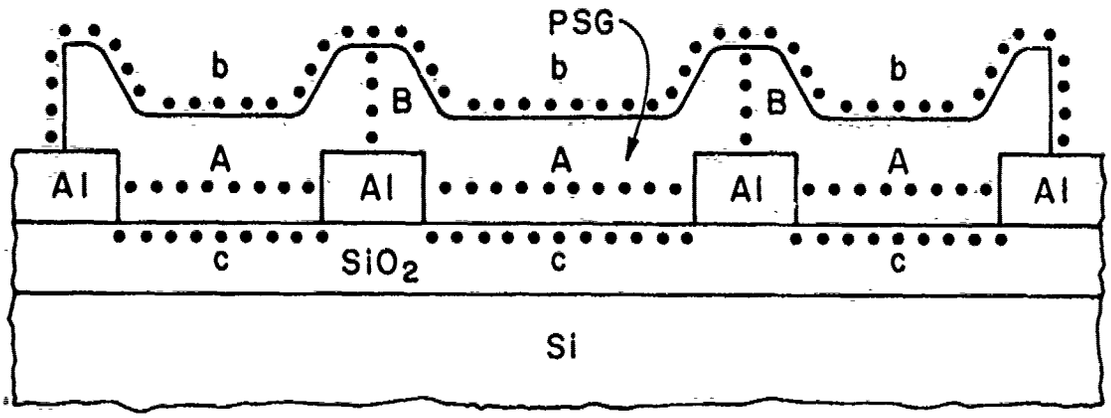


Figure 30. Current paths in a schematic IC cross section.

eV [68]. (We assume that the plastic, at least for a short time, traps water at the PSG surface and that the chip is thus effectively in a humid environment, since we are interested in worst-case estimates.) Using these values and the assumed geometry, we calculate a bulk resistance between lines of 2×10^{13} ohms, and a surface path resistance of 1×10^{11} ohms. This latter term consists of the actual surface component of 4×10^{10} ohms and the two bulk components in series with this of 2.5×10^{10} ohms each. Thus, in this worst case, the surface path contributes essentially all the current, and at 15 V the contributed leakage current is 1.5×10^{-10} A. This is negligible for almost all applications and is about 4 to 5 orders of magnitude below specified leakage currents for most IC applications.

In a separate experiment, a typical IC metallization pattern over thermal SiO_2 (no contact to silicon) overcoated with 5×10^{-5} cm of 8.5 wt % phosphorus PSG and packaged in plastic showed a leakage current of 3×10^{-11} A at 95°C after 24 hours autoclave. The electrode length in this structure was 0.06 cm; for comparison then, the current should be approximately doubled, yielding 6×10^{-11} A, in reasonable agreement with the previously calculated value of 1.5×10^{-10} A.

Even though bulk and surface leakage currents are negligibly small, they can have indirect effects related to surface charge inversion [60-63,65]. Using a specially fabricated MOS IC, an inversion-induced leakage after autoclave stress was observed. The increased leakage occurred between the positively biased n-type regions of the IC and the negatively biased p-type regions.

Upon voltage applications at 60°C, the leakage was constant at 10^{-9} A. After about 30 sec the leakage increased with a time constant of several minutes to 5×10^{-9} A. The increase was limited to this easily tolerable level by proper channel stoppering. In a poorly designed IC (no channel stoppers) the effect could be disastrous, however.

4. Aluminum Corrosion Effects

In this Subsection estimates of the time for complete corrosion of an aluminum line will be made. The possibility of cathodic aluminum corrosion in the presence of PSG of sufficiently high phosphorus content and water has been reported [69]. Several hypothetical test situations are possible, and current between aluminum lines of the geometry described in the previous section will be calculated. From the estimated currents, times for complete corrosion of the negative aluminum line will be determined, assuming a Faraday efficiency of one and uniform current distribution.

The mass of aluminum available for corrosion is 2.7×10^{-8} g for the assumed geometry and for aluminum thickness of 10^{-4} cm, and the charge needed for complete corrosion is 3×10^{-4} C. This value will be used to estimate corrosion time.

Autoclave stress followed by voltage application in dry ambient at elevated temperature is not expected to result in aluminum corrosion. In this situation the bulk resistance of 2×10^{13} ohms at 95°C for the typical electrode pattern limits the current to 5×10^{-13} A at 10 V (path A). The surface conduction in dry ambient is negligible. In time, the current will decay, and 5×10^{-14} A is a reasonable value for long-term estimates. This results in a corrosion time of 190 years.

Exposure of a device to humid ambient at room temperature without previous autoclave exposure is also not expected to result in aluminum corrosion, *except at bonding pads, pinholes, or cracks as found previously* [69].* Paulson and Kirk found that corrosion occurred in areas where the PSG was not continuous over the aluminum, such as at a bonding pad [69]. This indicates that the bulk path resistance (path B) through the PSG to the surface is not grossly affected by long-term high humidity exposure. Thus, we ignore the bulk path

*See Section VII.

resistance (path A) in this case, and note that the surface path resistance is limited by the metal-to-surface resistance through the PSG (path B). This is about 5×10^{13} ohms in this situation. The current is then 2×10^{-13} A, and the corrosion time is 45 years.

The presence of discontinuities at bonding pads, pinholes, or cracks in the PSG layer over the aluminum acts to shunt out the high bulk resistance of the PSG in surface path conduction (path b). For the conditions of the previous paragraph the surface path resistance is reduced to 4×10^{11} ohms for a surface current of 2.5×10^{-11} A at room temperature. The corrosion time is then 115 days. At 95°C the corrosion time would be reduced to about 10 days, using Koelmans' [68] or Paulson and Kirk's [69] temperature acceleration factors. With specially prepared samples containing deliberate cracks and pinholes in the PSG, we have found noticeable cathodic aluminum corrosion after three days in humid ambient for PSG with greater than 8 wt % phosphorus.* The effects of current concentration would decrease further the corrosion times at cracks and pinholes compared with the estimate made here. Since cracks and pinholes can occur over closely spaced metal lines it is expected that these open areas are much more serious corrosion sites than the open bond pad areas, which are much more widely spaced. Even if some corrosion of bond pad metal occurs, it should not affect device performance since on three sides of the pad there is no connection to the circuit, and on the fourth side design consideration can minimize the effects of corrosion.

The three-orders-of-magnitude increase in current between line pairs under PSG in humid ambient resulting from cracking of the PSG establishes directly that surface path conduction is greatly enhanced when openings in the PSG over metal can act to short out the bulk resistance of the surface path conduction (path B of Fig. 30). The decrease in current upon introducing dry nitrogen ambient confirms that the increased current after cracking the PSG is actually a moisture-induced surface current.

The occurrence of corrosion at cracks and pinholes is consistent with the observation that cathodic corrosion is much more probable than anodic corrosion [69].* If anodic corrosion begins at a pinhole or crack over metal, then the anodizing process will result in an electrically insulating product, which

*See Section VII.

will cut off or decrease current flow, in the absence of chloride [68]. The anodic current then is furnished at some other crack or pinhole, or by a bonding pad area. No such self-limiting process occurs at the cathode.

F. SUMMARY

The bulk and surface conduction of CVD SiO_2 and PSG have been measured as functions of temperature and phosphorus concentration. Effects of autoclave stress were determined. The measured electrical properties of these typical passivation layers were related to IC leakage and were shown to have no direct contribution to leakage currents, apart from the possiblity of surface inversion effects. Estimates of times for cathodic aluminum corrosion were made, and, based on the results, it was shown that the high bulk resistivity of the PSG limits the current sufficiently so that corrosion occurs only at discontinuities in the PSG coverage of the aluminum.

G. OTHER ELECTRICAL PROPERTIES

In this Subsection other electrical test results are given as functions of layer composition and structure, deposition rate, oxygen/hydride ratio, and various densification treatment. The techniques used for CVD of the dielectric layers were described in Section III. The electrical tests used include the following:

(1) Junction and MOS transistor channel leakage currents
(2) Breakdown voltage of oxides and of junctions
(3) Interelectrode currents
(4) MOS threshold voltage
(5) Capacitance-voltage curves of MOS capacitors vs bias-heat treatment

The test results pertaining to each layer or deposition parameter will be discussed as a group. All measurements were made at room temperature.

1. Rate of Deposition

Since it is expected that high deposition rate leads to more localized defects due to nonuniformities in deposition, it was decided to use dielectric breakdown voltage measurements to study the effect of this parameter.

In the literature, self-limiting breakdown (or so-called self-healing breakdown, SHBD) has been described as being used principally to assess the integrity of relatively thin layers, typically about 1000-Å thick, whereas PSG layers intended for IC protection are generally in the thickness range of 5,000 to 15,000 Å. Since the energy stored in the SHBD electrode at a given breakdown field is proportional to film thickness, smaller dots (∿250 μm diameter) have been used in our work than those generally used for the thinner layers (typically 750 μm). This is at once a disadvantage in PSG evaluation since many more such electrode dots have to be measured to arrive at a statistically significant wafer evaluation. In addition, defects associated with the electrode perimeter become much more important, and a large fraction of the breakdown events observed occurs at the perimeter. It is not felt that the perimeter breakdown events are related to film quality, as such.

A large fraction of elctrode dots, other than those exhibiting perimeter breakdown, suffers from propagating breakdowns and other effects which destroy large areas of the electrode. These effects are related to moisture. After several weeks of storage in room air, bubbles will form at the metal electrode/PSG interface upon voltage application. This can be eliminated by heating (at 300°C, for example), but propagating breakdowns still occur. The number of these can be decreased to some extent by using dry nitrogen ambient in the SHBD experiment.

The propagating breakdowns are caused by the relatively high prebreakdown conduction of the PSG and SiO_2 CVD films as compared with thermal oxides. This was found by a variation of the experimental technique. In conventional SHBD tests, a ramp voltage is applied to the electrode dot. In our variation, a constant-current source is used to capacitively charge the electrode to the breakdown field. It was found that near the breakdown voltage the conductivity of the film is sufficiently high that relatively large currents (about 1 μA) are needed to reach the critical voltage. These currents are high enough to cause propagating breakdown.

Because of the combination of the above adverse factors, it was decided to use the voltage of the first breakdown event for each dot as a measure of film quality.

Aluminum dots of 0.025 cm diameter and 1000-Å thick were evaporated on CVD SiO_2 deposited at 450°C on n-type silicon wafers at low and high deposition

rates. The voltage of the first breakdown for each capacitor dot upon application of a ramp voltage was used to characterize layer quality. Table 12 summarizes the results after heating in air at 200°C for 2 hours and for 16 hours to drive off adsorbed and absorbed water. Standard deviations are indicated for both breakdown voltage and breakdown field values.

Table 12. Initial Breakdown Data for CVD SiO_2

Deposition Rate (Å/min)	SiO_2 Thickness (Å)	Breakdown Voltage (V)	Breakdown Field (V/μm)
	After 2-hour bake (20 dots tested)		
400	3900	279 ± 113	715 ± 290
7000	5200	297 ± 178	571 ± 342
	After 16-hour bake (90 dots tested)		
400	3900	316 ± 63	810 ± 162
7000	5200	349 ± 135	671 ± 260

Measurements of electrical breakdown were also done on PSG films deposited at 450°C on silicon after 16-hour bake at 200°C. The results for 54 capacitor dot readings on a wafer are given in Table 13.

Table 13. Initial Breakdown Data for CVD PSG

Deposition Rate (Å/min)	PSG Composition (wt % P)	Film Thickness (Å)	Breakdown Voltage (V)	Breakdown Field (V/μm)
400	1.6	3950	293 ± 66	742 ± 167
5000	5.0	4300	377 ± 74	877 ± 172

In addition to comparing the average breakdown values, it is also useful to plot a frequency distribution of the breakdown field for the capacitor dots tested on a wafer. Figures 31 and 32 show the data plotted in this fashion for CVD SiO_2 and PSG, respectively, after 16 hours baking in each case. Note that in Fig. 31 the slow deposition data show a shift and tightening to higher fields, while the fast deposition data tend to a bimodal distribution. The

bimodal distribution has often been used to characterize dielectric strength. The lower grouping reflects defects while the grouping at the higher level reflects an approach to the intrinsic breakdown strength.

The following conclusions may be drawn:

(1) Heating to remove water improves both dielectric breakdown strength and dot-to-dot uniformity (as represented by the decrease in the standard deviations).

(2) Low deposition rates yield films exhibiting both increased breakdown strength and greater uniformity.

(3) Phosphorus content can have a greater effect on breakdown voltage than deposition rate. Higher phosphorus content increases the dielectric breakdown field maximum, even though less beneficial very high deposition rates were used.

(4) The improvements associated with slow deposition rate and higher phosphorus content tend to shift the distribution of breakdown field from a fairly broad or bimodal distribution to a distribution more characteristic of high intrinisic breakdown voltage. Thus, these improvements tend to eliminate defects leading to low voltage breakdown.

2. Oxygen-to-Hydride Ratio

Measurements of leakage currents on bipolar IC CA3747 and on CMOS IC CD4017A were made for devices passivated with PSG layers deposited at 450°C with two different oxygen:hydride ratios. No differences were seen with the linear devices, but decreased gate leakage at 0 gate voltage and 10-V drain-to-source on the CMOS devices was found for the lower ratio. The CMOS leakage average of ten devices is summarized in Table 14.

Table 14. CMOS Leakage Current vs. Oxygen:Hydride Ratio

O_2:Hydride Ratio	wt % P	PSG Thickness (Å)	I_L (A)
21.4:1	5.8	10,000	8.0×10^{-7}
21.4:1	5.8	20,000	4.1×10^{-8}
6.0:1	4.5	20,000	1.4×10^{-9}

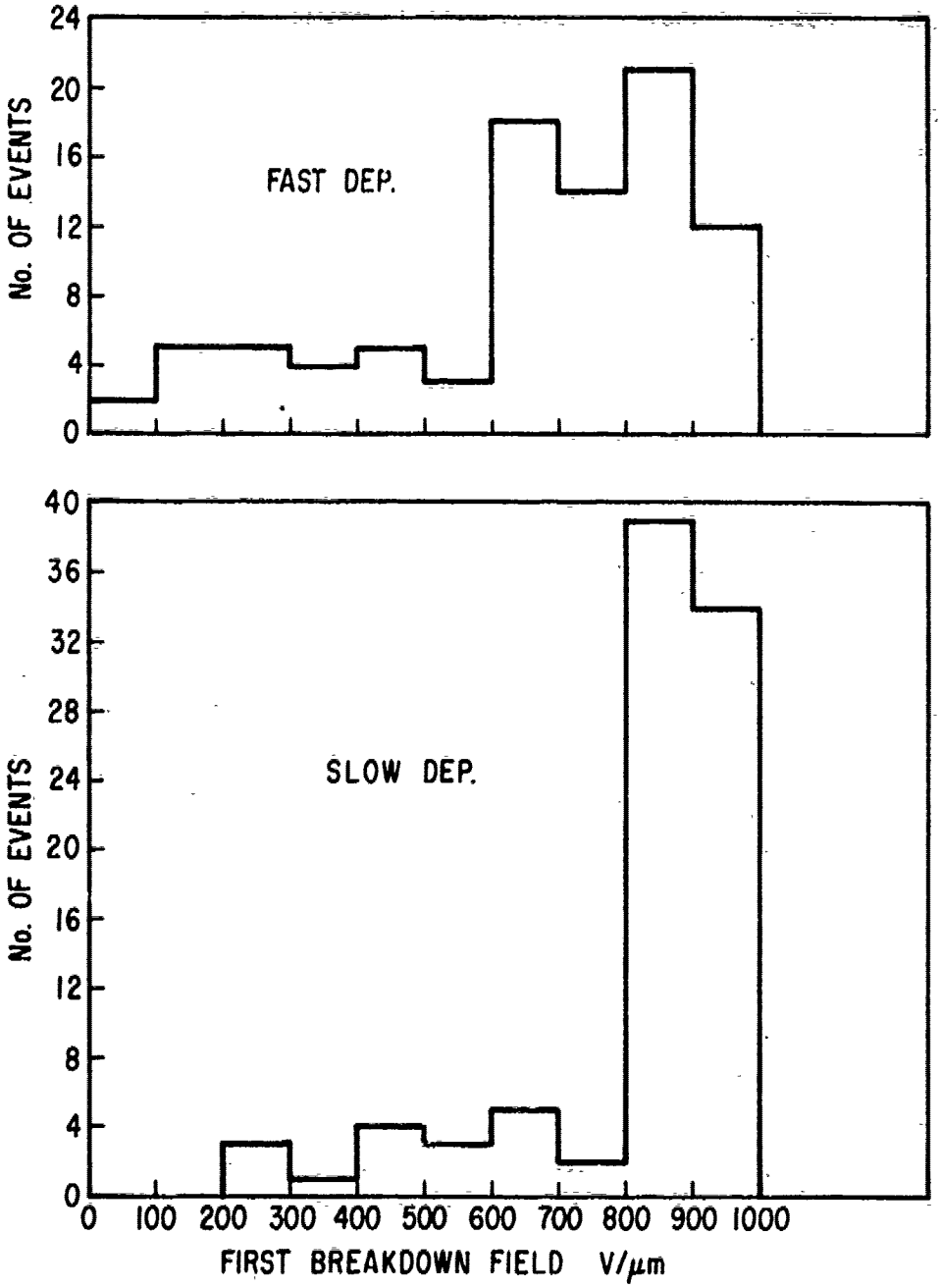


Figure 31. Frequency distribution of electric field of first breakdown event for CVD SiO_2, comparing fast and slow deposition rates. Same data as in Table 12 for 16-hr bake data.

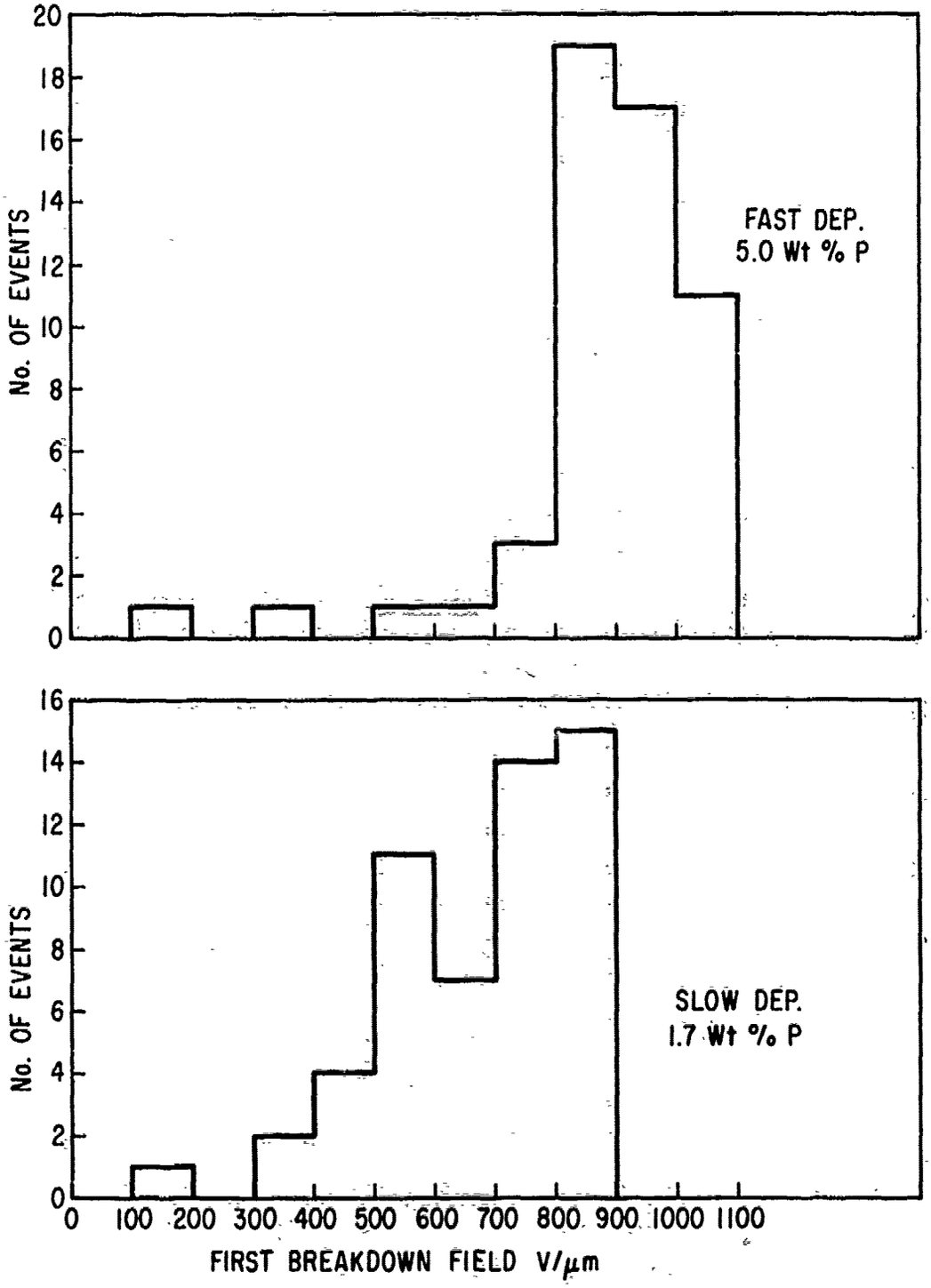


Figure 32. Frequency distribution of electric field of first breakdown event for CVD PSG, comparing deposition rates and phosphorus content. Same data as in Table 13.

3. Densification Treatments

As described in Section V, various post deposition densification treatments were tried, and tests were done to assess the effects on device electrical properties. Below are listed several device parameters and a brief description of the effect of densification on these parameters.

(1) Positive ions in gate oxide of MOS devices: In general, positive ion density increased after 1 hour in wet forming gas at 450°C and after 9 hours steam at 450°C. The shift in flatband voltage after bias-temperature stress at 220°C for 5 min was -0.3 to -0.8 V for PSG-passivated gate metal - thermal SiO_2 - Si capacitors. Without phosphorus, the shifts were much larger, about -5 V. For the structures tested, a 1-volt shift corresponds to 2.6×10^{11} ions/cm^2. The above data were taken on MOS transistor devices where the region under the gate metal has a relatively large perimeter-to-area ratio. For larger-area capacitors, the shifts after the same temperature-bias treatment were of the order of -20 to -35 V, irrespective of phosphorus content. Before densification, the shift in the C-V curve after bias-temperature treatment was about 0.2 V. These results indicate the importance of PSG gettering, and of lateral diffusion of ions at the perimeter.

(2) Also reflecting increased mobile positive ion density in the oxide was the behavior of lateral pnp devices on linear CA3747 wafers. The collector-base and emitter-base avalanche breakdown voltages of these devices showed very large walkout effects after the densification treatments described in (1) above. There was little effect on breakdown voltage of npn devices.

(3) Ten hours of steam at 450°C tended to decrease the leakage currents of both CMOS and linear bipolar devices.

(4) The breakdown voltage of MOS device gate oxides was not affected by 1 hour wet forming gas treatment. After 9 hours of steam treatment at 450°C, the average gate oxide breakdown voltage for CVD SiO_2 passivated devices increased from 50 to 62 V, while there was no change in PSG passivated devices.

(5) Threshold voltages of NMOS and PMOS transistors were determined. There were only slight changes (tenths of volts) in the 10^{-6} A threshold voltage, as expected from the results of (1) above.

In summary, there are small changes after densification treatments. It is felt that the changes are small enough that if special circumstances warrant

the densification treatments described, it would be possible to adjust device or circuit design to render these changes inconsequential.

4. Double vs Triple Passivation Layers

As described in Section VII, there is no advantage relative to corrosion effects in having a CVD SiO_2 layer between the aluminum and the PSG. To see if there might be other advantages or disadvantages, a comparison of double-layer and triple-layer passivated devices (8 % PSG) was made using both linear and CMOS circuits. As shown in Table 15, no advantage was found.

Table 15. Comparison of Double and Triple Passivation Layers

				Linear CA3045		COS/MOS CD4011A
Passivation Layers	SiO_2 Bottom (Å)	PSG (Å)	SiO_2 Top (Å)	I_{CBO}(10V) (A)	BV_{EBO}(1mA) (V)	I_{LEAK}(V_{DS}=10 V) (A)
Double	0	4500	2500	1.5×10^{-10}	6.92	5.6×10^{-9}
Triple	2000	4000	2000	2.1×10^{-10}	7.01	1.7×10^{-8}

VII. ALUMINUM CORROSION STUDIES

A. INTRODUCTION

Corrosion of glass-passivated aluminum interconnections during device operation is a common cause of integrated circuit failure, especially with integrated circuits packaged in plastic. This type of corrosion frequently occurs at the cathode, where $Al(OH)_3$ forms.

Systematic experiments were conducted to determine the exact cause of cathodic aluminum corrosion. Variables investigated include phosphorus content of the deposited PSG film, the moisture content of the ambient, applied dc bias, and the effects of cracks or pinholes over the aluminum.

The experimental studies on aluminum corrosion were conducted along two main approaches: (1) Induced corrosion of test structures followed by selective etching of the aluminum and microscopic examination of the exposed defects; and (2) induced corrosion of test structures monitored by electrical measurements of the test devices. Each of these approaches, and the results obtained, are discussed below. All electrical bias conditions noted in this Section are dc bias.

B. SELECTIVE ETCHING STUDY OF INDUCED CORROSION

1. Test Structures

Photomicrographs of the test structures used in these experiments are shown and described in Figs. 33 and 34.

2. Relation of Corrosion and Structural Glass Defects

Starting with an oxidized silicon wafer, a 1-μm-thick layer of aluminum was evaporated onto the wafer and delineated into the barbell-type test pattern shown in Fig. 33. The pattern was then glassed with a 5000-Å-thick layer of PSG containing 8.5 wt % phosphorus, followed by a 2000-Å-thick layer of undoped SiO_2. Contact areas were then opened at the ends of the barbell.

To determine the integrity of the glass passivating layers, patterns were taken, after contact opening, and subjected to aluminum etch at 55°C for periods of 6 and 12 minutes. Pinholes or cracks in the overlying oxide layer will allow the etch to penetrate to the metal, causing it to etch away. This experiment revealed that the glass layers had numerous cracks and pinholes.

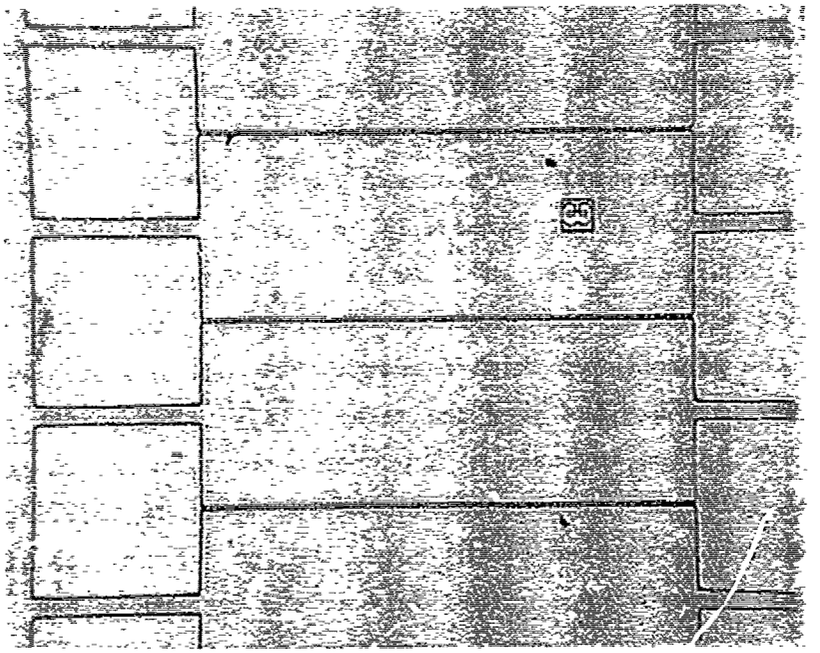


Figure 33. Aluminum metallization barbell test pattern (100X) overcoated with PSG. Bond pads were opened by photolithography and etching. Aluminum stripes are 7.5-μm wide and 750-μm long. An identical structure with 12.5-μm-wide stripes was also used.

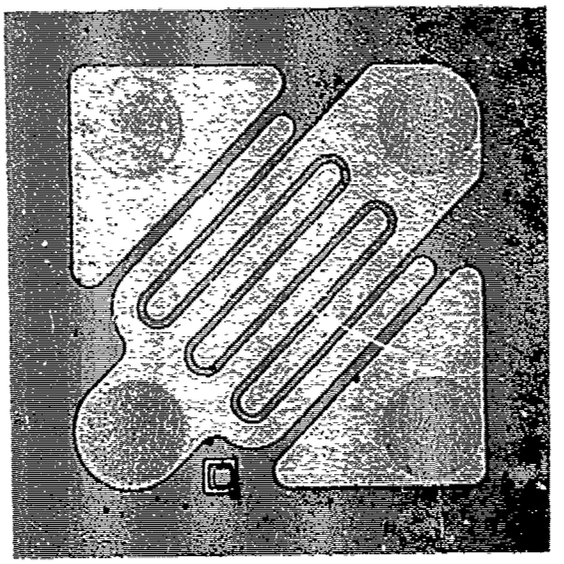


Figure 34. Aluminum interdigitated test pattern (100X) overcoated with PSG. Circular bond pad areas were defined in glass by photolithography and etching. Aluminum stripes are 42-μm wide; separation between stripes is 10 μm.

To test for corrosion, unetched samples were taken and two adjacent electrodes were biased at 50 V dc for 24 hours in room air (∿50 to 60% RH). Upon microscopic examination, no corrosion was observed. The sample was then placed into an autoclave and subjected to H_2O vapor at 15 psig and 121°C for 4 hours. The samples were next biased for an additional 24 hours. Now corrosion had occurred at the cathode to the extent that the line had opened. From these results, it was concluded that H_2O vapor is essential for corrosion.

Another series of test patterns was prepared, and great care was taken to reduce the pinhole and crack density. Hot aluminum etching did not reveal any pinholes in the glass over the metal. Only undercutting at the bond pads was observed, indicating that with proper deposition and photolithographic techniques, incidence of pinholes can be considerably reduced. Samples from this series were subjected to the autoclave for 4 hours and biased at 120 V for 24 hours. Corrosion occurred only at the cathode in the contact area.

An analogous test using an interdigitated aluminum pattern, shown in Fig. 34, exhibited similar results, i.e., no pinholes in the PSG layer over aluminum and undercutting only at contact areas (Fig. 35). To confirm that holes or scratches in the oxide were required to allow corrosion to occur, an interdigitated metallization pattern, previously subjected to the autoclave, was purposely scratched across the cathode and anode fingers. After biasing at 120 V for 48 hours in room air at 25°C, cathodic corrosion occurred at the cathode fingers and bond area (Fig. 36).

A subsequent experiment with another aluminum barbell test pattern, having 15-μm wide lines and glassed with a PSG layer containing 8.5 wt % phosphorus, also verified that pinholes and/or cracks had to be present to allow corrosion to occur. The contact mask for this test pattern was designed such that when contact pads were opened in the glass, holes were simultaneously opened over the aluminum lines. Holes of 12, 8, 5, and 2.5 μm in diameter were opened, simulating pinholes that could occur during processing. The samples were subjected to the autoclave for 4 hours at 121°C at 15 psig and then biased for 16 hours at 50 V. As before, corrosion occurred at contact areas and at the simulated pinholes on the cathode only (Fig. 37). This confirmed that without pinholes or cracks, corrosion will not occur anywhere except at bonding pads.

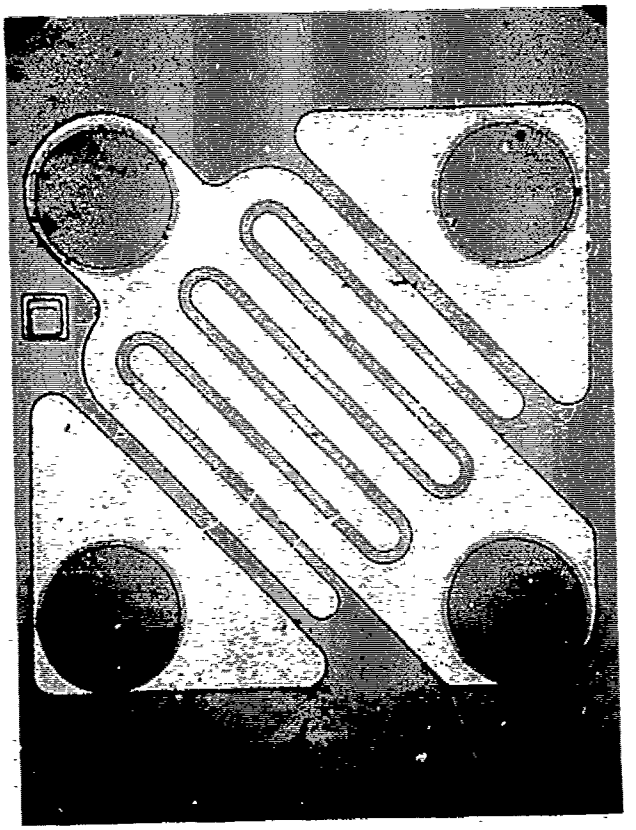


Figure 35. Glassed structure subjected to 55°C aluminum etch for 12 minutes. Pattern, with bond pads open, shows good glass integrity, i.e., no pinholes in glass over the aluminum.

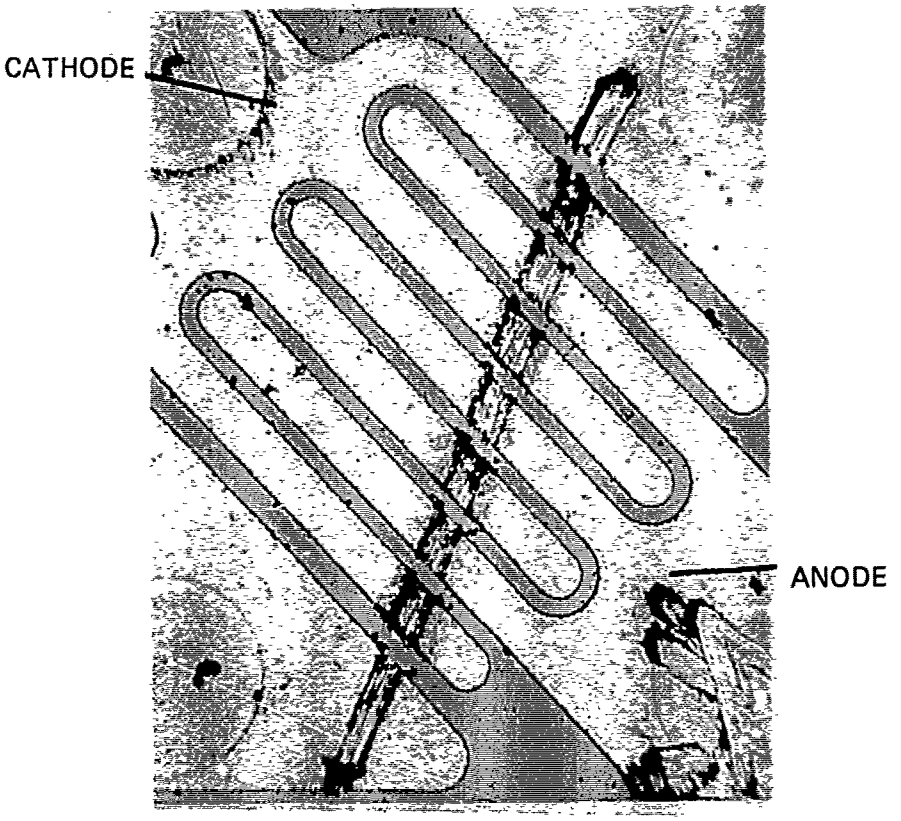
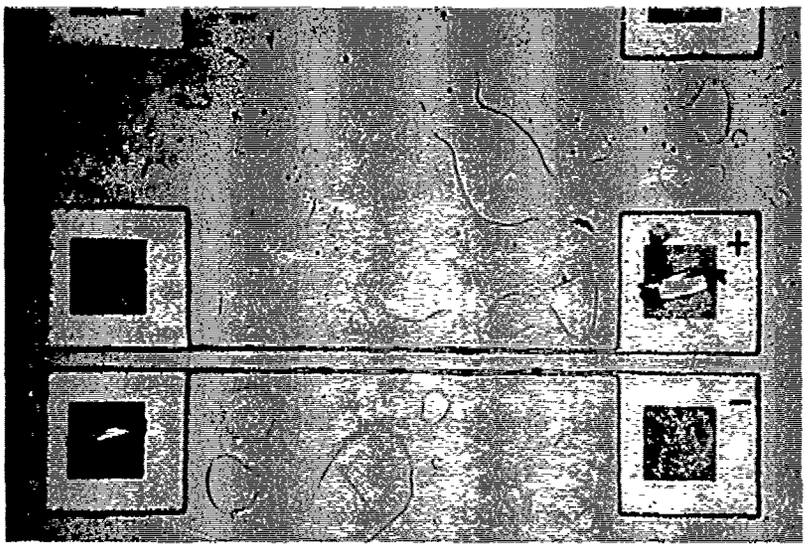
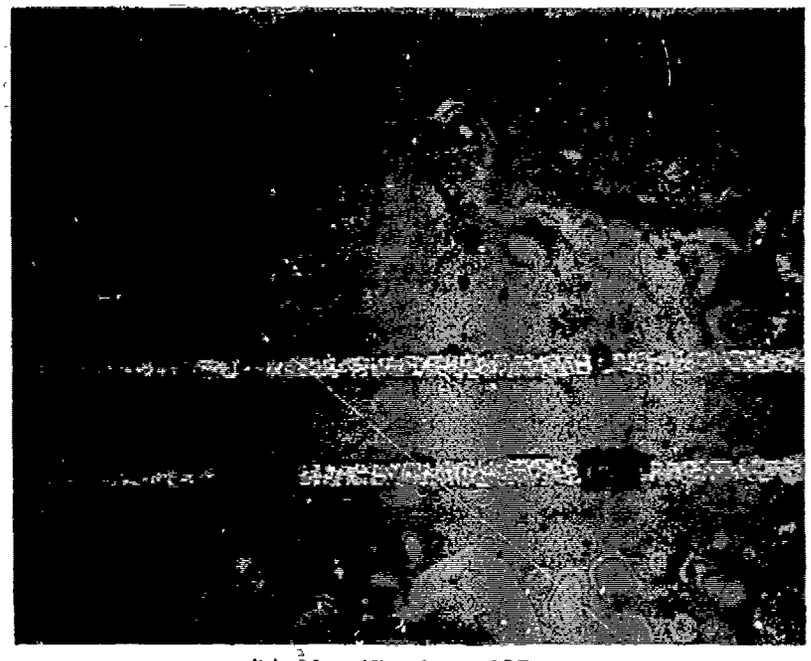


Figure 36. Purposely damaged PSG-SiO_2 glass overcoat on interdigitated aluminum pattern (100X) followed by bias at 120 V for 48 hr. Corrosion occurred at the contact areas and the damaged areas of the cathode only.



(a) Magnification X 78.



(b) Magnification X 385.

Figure 37. Cathodic corrosion on PSG overcoated aluminum test pattern. Aluminum pattern was glassed with a 5000-Å PSG layer containing 8.5 wt % phosphorus, and capped with a 2000-Å layer of SiO_2. Samples were subjected to autoclave for 4 hr and biased at 50 V for 16 hr. Line width is 15 μm.

3. Relation of Corrosion and Phosphorous Content in the Glass

To determine the effect of phosphorus content on aluminum corrosion, samples were prepared where the PSG layer contained 3 to 4 wt % instead of the 8.5 wt % phosphorus contained in the first sample. The samples were subjected to the autoclave for 5 hours at 121°C 15 psig and then biased at 100 V. After 70 hours no corrosion was observed. The samples were then returned to the autoclave for 5 additional hours and re-biased for an additional 168 hours at 100 V. Corrosion still did not occur. Next, samples were biased at 100 V in 100% relative humidity air at room temperature for 18 hours. Under these conditions, aluminum corrosion occurred at the cathode, and the cathode stripe was completely converted to $Al(OH)_3$ in some regions. Apparently, corrosion conditions are worse when the relative humidity is maintained at a high level. The results confirm other information which indicated that high concentrations of phosphorus allow corrosion to occur readily, and that at lower concentrations such as 3 to 4 wt % phosphorus, corrosion will occur only under very high humidity conditions.

4. Photolithographically Caused Glass Damage Leading to Corrosion

Many pinholes in the passivating glass over the aluminum are due to particulate matter that can be incorporated into the glass during chemical vapor deposition [75,76], or may arise during etching to open the bonding pads (because of holes in the photoresist layer). However, some pinholes and cracks are generated by other means. They may be created by the contact printing operation or by impact during chip handling [57]. When the photomask comes in contact with the glass-passivated aluminum pattern, large pressures occur at points of contact. The result is that the aluminum flows slightly and the glass may crack. Hillocks present in the aluminum also flatten and cause glass damage. To confirm this mechanism, a silicon wafer

75. V. Y. Doo and V. M. L. Sun, Metallurg. Trans. 1, 741 (1970).
76. W. C. Benzing, R. S. Rosler, and R. W. East, Solid State Technology 16, No. 11, 37 (1973).

with a glassed aluminum pattern was sequentially etched in hot aluminum etch to reveal cracks and pinholes following contact printing steps. The etching studies showed that more cracks and pinholes developed each time the glassed pattern was brought into contact with the photomask.

It should be pointed out in this connection that our evaluation of passivation overcoats on commercial ICs (Appendix F) has shown that in a substantial portion of the integrated circuits manufactured in the last several years, the passivation layer contains pinholes, cracks, or a combination of these. (A number of publications also confirm this finding [77-82].) The more common class was pinholes in the central regions of aluminum lines. Another type observed was pinholes along the edge of the delineated metal lines [82]. The edge pinholes are attributed to inadequate coverage of metal edges by the photoresist, and can generally be avoided by the use of thicker photoresist layers or improved photoresist application techniques. Those pinholes which occurred in the central areas of delineated lines are, to a large extent, believed to be attributable to the presence of hillocks in the aluminum, which occur because of recrystallization of the aluminum during the contact alloying step. It should be noted that even if a hillock is completely covered with dielectric during the subsequent step of deposition of the passivation layer, the hillock may not be adequately covered by photoresist, the photoresist may be pushed away from the peak of the hillock during contact printing, or the contact printing step may fracture the dielectric over the hillock. Any of these three conditions, or a combination, will result in a pinhole through the passivation layer, exposing a region of aluminum.

77. G. L. Schnable and R. S. Keen, in *Advances in Electronics and Electron Physics*, Vol. 30, L. Marton, Ed., (Academic Press, New York, 1971), pp. 79-138.
78. V. C. Kapfer and J. J. Bart, 10th Ann. Proc. Reliability Physics, (IEEE, New York, 1972), pp. 175-182.
79. W. F. Keenan and W. R. Runyan, Microelectron. and Reliability 12, 125 (1973).
80. P. B. Mee, Honeywell Computer J. 5, 115 (1973).
81. G. H. Ebel and H. A. Engelke, 11th Ann. Proc. Reliability Physics, (IEEE, New York, 1973), pp. 108-116.
82. W. Kern, RCA Review 34, 655 (1973); Solid State Technology 17, No. 3, 35 (1974) and No. 4, 78 (1974).

5. Discussion and Summary of Conclusions

A number of authors have pointed out that phosphosilicate layers with an excessively high concentration of phosphorus are hygroscopic, and can lead to aluminum corrosion problems. One author also indicated that cracking in low phosphorus content PSG can lead to reliability problems [69].

Our experiments revealed that three factors are directly involved and lead to corrosion of aluminum in glass-passivated ICs. The first factor is the presence of H_2O vapor in the package; the second is an excessive amount of phosphorus in the passivating layer; and the third is the presence of cracks and pinholes in the passivating layer over or at the edges of the aluminum interconnection. Any one of these factors does not lead to corrosion by itself; all three are necessary to generate cathodic corrosion of the type frequently observed in field failures. Our work has shown that in the absence of localized defects, corrosion occurs only at exposed bonding pad areas.

C. ELECTRICAL MEASUREMENT STUDY OF INDUCED CORROSION

1. Preliminary Tests

As pointed out in Subsection B, cathodic aluminum corrosion takes place in the presence of water vapor, high phosphorus content (>8 wt % phosphorus in the CVD PSG), and applied bias, and is most severe at cracks, pinholes, or bond pad openings as described in Section VI. In preliminary measurements with unencapsulated devices mounted on headers and wire bonded, we found that application of bias to aluminum patterns overcoated with PSG while in water vapor in an autoclave at 121°C, 15 psig, resulted in complete corrosion of a 1.8-μm thick, 10-μm wide line in tens of hours. This drastic corrosion was found in all layers tested, including those coated with low phosphorus content (∿2 wt %) PSG and even CVD SiO_2. In these cases delamination of the CVD layer was found, and the films peeled away in large sections. This gross failure was accompanied by metal corrosion. In order to find a less destructive test that would exhibit the differences known to exist depending on phosphorus content, the following program was carried out. The objectives include the establishment of a useful test procedure for studying aluminum corrosion, the evaluation of various passivation layer parameters, and the correlation of previous predictions based on PSG electrical properties with test results.

2. Preparation of Test Devices

Line patterns of aluminum on thermal SiO_2 overcoated with PSG layers of various composition and thickness, and encapsulated in a novolac epoxy molding compound, were used to study the corrosion. The metal line was 7.5×10^{-2} cm long and had three gap widths (5.0, 7.5, and 10.0 μm). The line pattern used is shown in Fig. 38. Double layers of CVD PSG capped with CVD SiO_2, and triple layers of CVD SiO_2, CVD PSG, and CVD SiO_2 were studied. Phosphorus content in the PSG layers ranged from 2 to 7.7 wt %.

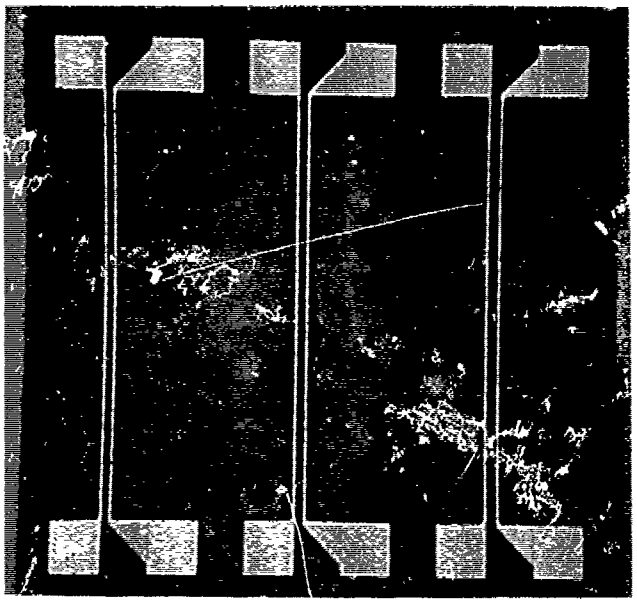


Figure 38. Photomicrograph of line pattern used in corrosion study.

3. Results of Electrical Measurements

Two series of measurements were done to establish relative corrosion rates. In the first series, current between line pairs at 100 V was measured at 95°C in dry nitrogen as a function of prior time in an autoclave. Results of the first series of measurements show a large increase in current for the high-phosphorus samples. A typical result is shown in Fig. 39. Table 16 summarizes results at 35 hours autoclave exposure.

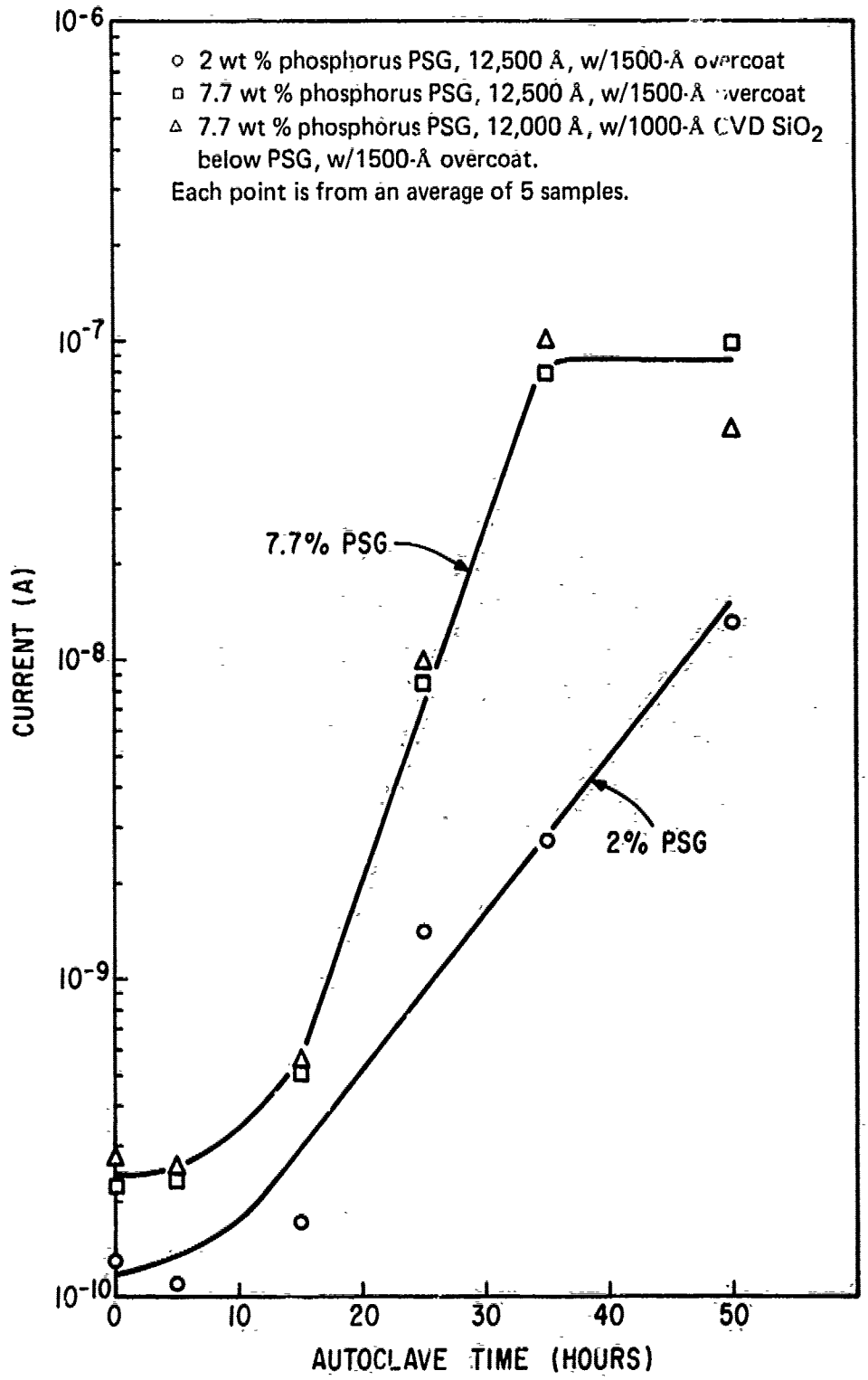


Figure 39. Current between aluminum line pairs 7.5 μm apart at 95°C, 100 V as a function of cumulative autoclave exposure.

Table 16. Steady State Current between Line Pairs at 95°C, 100 V*

Sample No.	Layer Thickness (Å) SiO_2 (1)	PSG (2)	SiO_2 (3)	Wt % P	I (A)
1A	0	12,500	1,500	2.6	4.2×10^{-9}
2A	0	12,500	1,500	2.0	2.7×10^{-9}
4A	0	12,500	1,500	4.6	4.2×10^{-9}
6A	0	12,500	1,500	7.7	7.8×10^{-8}
18A	1,000	12,000	1,500	7.7	1.0×10^{-7}

*7.5-μm Line Spacing
35-Hours Autoclave
Average of 5 Measurements

(1) CVD SiO_2 over metal
(2) CVD PSG over (1)
(3) CVD SiO_2 over (2)

In the second series, the resistance of the aluminum lines was monitored as a corrosion-related parameter after autoclave exposure without bias, and after heat exposure (90°C) with 20-V bias applied between lines. Some line pairs were left floating. A complete cycle of line resistance measurements in the second series consisted of the following procedure:

(1) Measure initial line resistance.
(2) Place in autoclave at 121°C, 15 psig in vapor phase for 20 hours.
(3) Measure line resistance.
(4) Place in room air, 90°C with 20-V bias applied between line pairs for 5 hours.
(5) Measure line resistance.

In the second series of measurements, it was found that the line resistance increased only after both autoclave stress and 90°C, 20-V bias were applied to a line pair. There was no increase after autoclave stress alone, and only the negatively biased lines showed the increase. A typical result is shown in Fig. 40 for three full cycles. Table 17 shows results at the end of three cycles for five sample types. Note the large increase in resistance for the 7.7 wt % phosphorus PSG, negative bias lines.

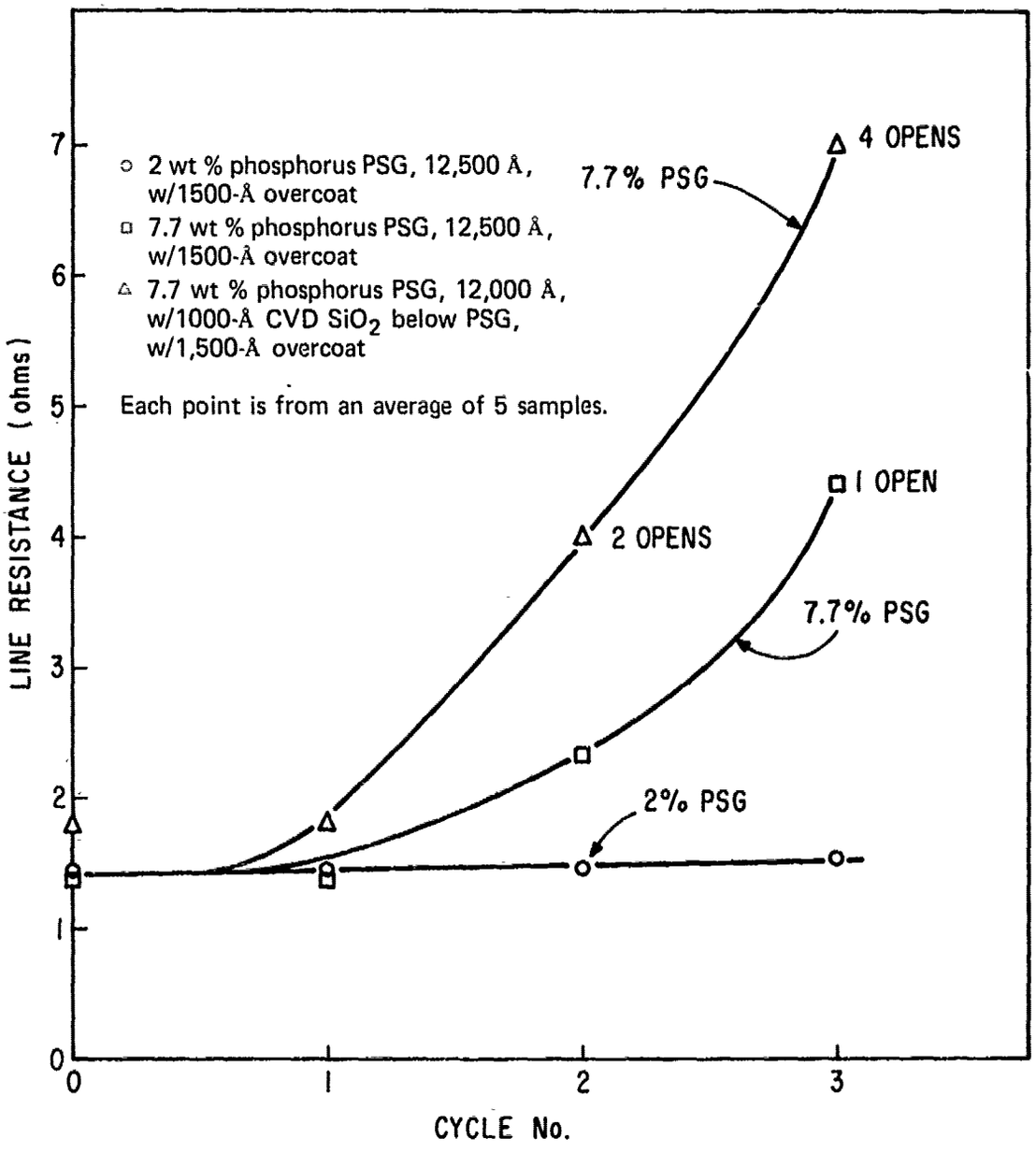


Figure 40. Aluminum line resistance after three full cycles of autoclave followed by bias at 20 V at 90°C in room air.

Table 17. Aluminum Line Resistance Values before Stress Testing*

Sample No.	Wt % P	Resistance (Ohms) of Lines with Following Bias Conditions: Floating Initial	Floating Final*	Positive Bias Initial	Positive Bias Final*	Negative Bias Initial	Negative Bias Final*
1A	2.6	1.481	1.474	1.502	1.503	1.505	1.541
		1.416	1.410	1.464	1.463	1.376	1.402
2A	2.0	1.537	1.534	1.531	1.541	1.474	1.542
		1.472	1.467	1.540	1.547	1.451	1.547
4A	4.6	1.494	1.491	1.505	1.510	1.455	1.512
		1.433	1.431	1.500	1.502	1.415	1.456
6A	7.7	1.459	1.458	1.475	1.477	1.420	5.216
		1.392	1.395	1.456	1.459	1.373	4.409
18A	7.7*	1.889	1.889	1.903	1.918	1.796	5.980
		1.787	1.793	1.933	1.967	1.795	6.990

*After 3 cycles of 20-hour autoclave followed by 5 hours at 90°C, 20 V. Average of five measurements.
**Trilayer

In another experiment, the influence of phosphorus concentration and epoxy resin overcoats was determined using CD4009A circuit metallization patterns without connection to silicon. Samples with the metal deposited on thermally grown SiO_2 and overcoated with PSG (phosphorus concentrations of about 5% and 8% by weight) with and without epoxy resin overcoat, were subjected to 24 hours in an autoclave (steam, 121°C, 15 psig). Measurements of interelectrode current were then made at 60°C, dry nitrogen ambient, with 15 volts applied bias. Table 18 shows averaged values of current (in amperes) 1 minute after voltage application for 30 to 40 measurements for each entry.

The current measured for the 8 wt % phosphorus PSG samples with epoxy overcoat shows a dependence on bonding pad position. That is, current is higher when the voltage is across two bonding pads which are near each other than when the pads are at opposite sides of the chip. This is not observed

Table 18. Interelectrode Current at 60°C, 15 V on CD4009A Patterns

	Current 4 wt % P in PSG (A)	Current 8 wt % P in PSG (A)
No overcoat	4.1×10^{-12}	1.3×10^{-11}
With overcoat	4.2×10^{-12}	6.5×10^{-10}

for the same PSG without epoxy coat or for the 4 wt % phosphorus PSG with or without epoxy coat. This indicates that the enhanced conduction is due to surface conduction at the passivation glass-epoxy interface from one exposed wire bonding pad to the other. If the enhanced conduction were through the PSG bulk, there would be no dependence on pad-to-pad spacing, since the individual circuit patterns are identical. If the enhanced conduction were through the bulk of the resin, then the 4 wt % phosphorus PSG sample should also show a large increase due to the resin, but this was not found, as shown in Table 18.

4. Conclusions

In these measurements the importance of phosphorus content on the corrosion rate is strongly evident. In addition, the presence of a CVD SiO_2 layer between the aluminum and the PSG apparently increased the corrosion rate, which is a somewhat surprising result. Also, it should be pointed out that the current levels of Fig. 38 or Table 16 for the 7.7 wt % phosphorus PSG layers are about 20X the value calculated from the electrical properties of the PSG as described in the previous section. This may be due to the presence of the encapsulating plastic as discussed (Table 18), or to conduction at the interface between the thermal oxide and the PSG.

Based on measurements with the CD4009A patterns the following conclusions can be made:

(1) With 4 wt % phosphorus in PSG, the presence of the epoxy coating has little effect.

(2) 8 wt % phosphorus PSG shows higher currents than 4 wt % phosphorus PSG independent of epoxy overcoat.

(3) With 8 wt % phosphorus in PSG there is a very large increase in current due to the epoxy overcoat.

5. Discussion

Assuming a Faraday efficiency of one, degrees of aluminum corrosion based on observed or estimated currents can be made. For the line pattern used, 4.7×10^{-4} C are needed for complete corrosion. Using the peak current of 10^{-7} A at 100 V (Fig. 39), a corrosion time of about 7 hours is calculated at 20 V, 90°C, assuming linear I-V dependence. While this time agrees with data of Fig. 40, it is not suggested that uniform corrosion of the cathode takes place, since, as will be described later, mostly localized corrosion is found. Rather, as described in Section VI, the current decays drastically during the corrosion process. Thus, as is shown in Table 17, essentially no anodic corrosion takes place, since the anode corrosion product is Al_2O_3, a good insulator which is stable in the absence of chloride ions. This distributes the corrosion over the entire available anode. No such limiting process occurs at the cathode, and thus localized corrosion (at defects) leads to high resistance and open lines in the presence of high-phosphorus-content PSG.

Certain devices were decapsulated for microscopic examination upon completion of three full cycles. It was found that only the negative line had corroded, and that in most cases, the corrosion was localized (presumably at a defect). Also, it was found that in many samples the PSG had again delaminated from the thermal SiO_2. The delamination reflects decreased adhesion of the PSG to the SiO_2. This delamination is found on certain sample lots, and may indicate contamination at the interface, perhaps due to traces of photoresist residue. It is also possible that the contamination leads to increased interface conductivity which will enhance the measured currents. These are important questions relating to reliability which need to be answered by further research.

Stress-corrosion cracking [83] may be a factor in accelerating cathodic corrosion of aluminum metallization lines at grain boundaries. Aluminum on

83. W. W. Binger, E. H. Hollingsworth, and D. O. Sprowls, in *Aluminum, Properties, Physical Metallurgy and Phase Diagrams*, Vol. 1, K. R. Van Horn, Ed., (Amer. Soc. for Metals, Metals Park, Ohio, 1967), pp. 2009-276.

silicon wafers, after heat treating at a temperature of 450°C has been shown to be in tension at room temperature [43], and would remain in tension under device usage conditions.

VIII. ANALYTICAL CONTROL METHODS

A. INTRODUCTION

Exploratory studies have been performed on practical analytical techniques for control of passivation processing and evaluation of passivation layers. In this section we briefly review pertinent methods and report on the experimental results and methodological innovations achieved.

Also included are several additional analytical results that have not yet been described in the previous sections of this report; these results were obtained by application of standard instrumental analytical methods.

B. SURVEY OF PRACTICAL MEASUREMENT METHODS

Practical methods and measurement techniques suitable for setup and in-process control of production-type CVD passivation work, as well as for detection of structural layer defects, are outlined in Table 19. All of these chemical, optical, electrical, and mechanical test methods have been discussed and literature sources have been referenced in the passivation survey paper presented in Appendix A, and thus will not be repeated here. An extended discussion of additional methods for detecting and characterizing localized structural defects was recently presented in a separate paper [82]. By applying such tests for analyzing defective devices before and after the passivation of wafers, and at succeeding steps, the mechanisms leading to degradation, immediate or long term, can be defined. Steps can then be taken to modify the processing sequence used so that these mechanisms do not take place.

C. ANALYTICAL METHODS FOR EXPERIMENTAL RESEARCH

Instrumental methods used in research applications involving the electrical, physical, and chemical characterization of dielectric films are reviewed in Appendix A. Several detailed treatises [45,82,84-87] are available on this

84. P. F. Kane and G. B. Larrabee, *Characterization of Semiconductor Materials*, (McGraw-Hill Book Co., New York, 1970).
85. P. F. Kane and G. B. Larrabee, "Trace Analysis Techniques for Solids," in *Annual Review of Materials Science*, Vol. 2, (1972), pp. 33-65.
86. *Handbook of Thin Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw-Hill Book Co., New York, 1970).
87. *Thin Film Dielectrics*, F. Vratny, Ed., (The Electrochemical Society, New York, 1969).

Table 19. Measurement Techniques for Setup and In-Process Control of Production-Type CVD Passivation-Glass Deposition

Characteristic	Substrate to be Used	Measurement Technique	Deposition Condition to be Adjusted as Required
Thickness	Si wafer	Interferometric technique; stylus-type instrument	Time of deposition
Density	Si wafer	Etch rate (as deposited)	Deposition rate, deposition temperature
Phosphorus content	p-type Si wafer	Sheet resistivity after high-temperature bake; etch rate after densification	PH_3/SiH_3 ratio
Total stress	0.14-mm-thick Si wafer	Wafer warpage by optical microscopy	Deposition rate, deposition temperature, SiH_4/O_2 ratio
Interfacial stress	0.6- to 1-mm-thick Si wafer	Surface temperature measurements; pyrometry	Deposition temperature
Surface topography	Si wafer	Nomarski interference contrast microscopy; stylus-type instrument	Substrate cleanliness, system maintenance, cooling of system parts above the substrate
Pinholes	Patterned Al on oxidized Si wafer	Preferential Al etch, inspect	Substrate conditions, system maintenance
Cracks	Patterned Al on oxidized Si wafer	Inspect, Al etch, inspect, heat treat, Al etch, inspect	Deposition rate, deposition temperature, SiH_4/O_2 ratio
Edge coverage	Patterned Al on oxidized Si wafer	SiO_2 etch, Al etch, inspect	Reactant flow rate, edge topography of substrate

subject. A survey of instrumental techniques for elemental composition profiling of thin films has been recently presented [88].

D. EXPERIMENTAL RESULTS ON DEVELOPMENT OF ANALYTICAL METHODS

Innovative work to be described was done on the following methods: (1) chemical etch rate analysis; (2) passivation overcoat analysis on single ICs; pellets; (3) surface resistance from diffused layers; (4) measurement of film stress; (5) x-ray fluorescence analysis for phosphorus; (6) infrared absorption spectroscopy; and (7) corona-charging techniques.

1. Chemical Etch Rate Method

The etch rate of silicate glasses in suitable etchants is generally a sensitive measure of the chemical composition of the film, and can be utilized as the basis of convenient control tests. We have found that determination of the PSG composition during setting up and optimizing the CVD conditions for a given system is most readily done by the etch rate method because it is fast, simple, and convenient. It is reliable and sufficiently accurate and precise for most practical requirements if it is carried out under controlled conditions, and if suitable calibration curves are established.

In addition to film composition, the etch rate is also sensitive, to a lesser extent, to structural film properties, especially density, porosity, and stress, which makes the method a valuable tool in process control for monitoring these film properties. The effects of these physical film properties can be largely eliminated by a high-temperature annealing treatment at, typically, 800°C. The etch rate then becomes a unique function of the chemical film composition.

Determination of the etch rate of films as-deposited and also after densification furnishes valuable information on both physical and chemical film properties. The calibration graph presented in Fig. 41 exemplifies the use of etch rate testing for determining the glass composition. It shows the etch rate of SiO_2 (0 wt % phosphorus) and PSG films as-deposited under various conditions, and also after densification at 800°C. It can be clearly seen that

88. J. W. Coburn and E. Kay, "Techniques for Elemental Composition Profiling in Thin Films," in *Critical Reviews in Solid State Sciences*, September 1974, pp. 561-590.

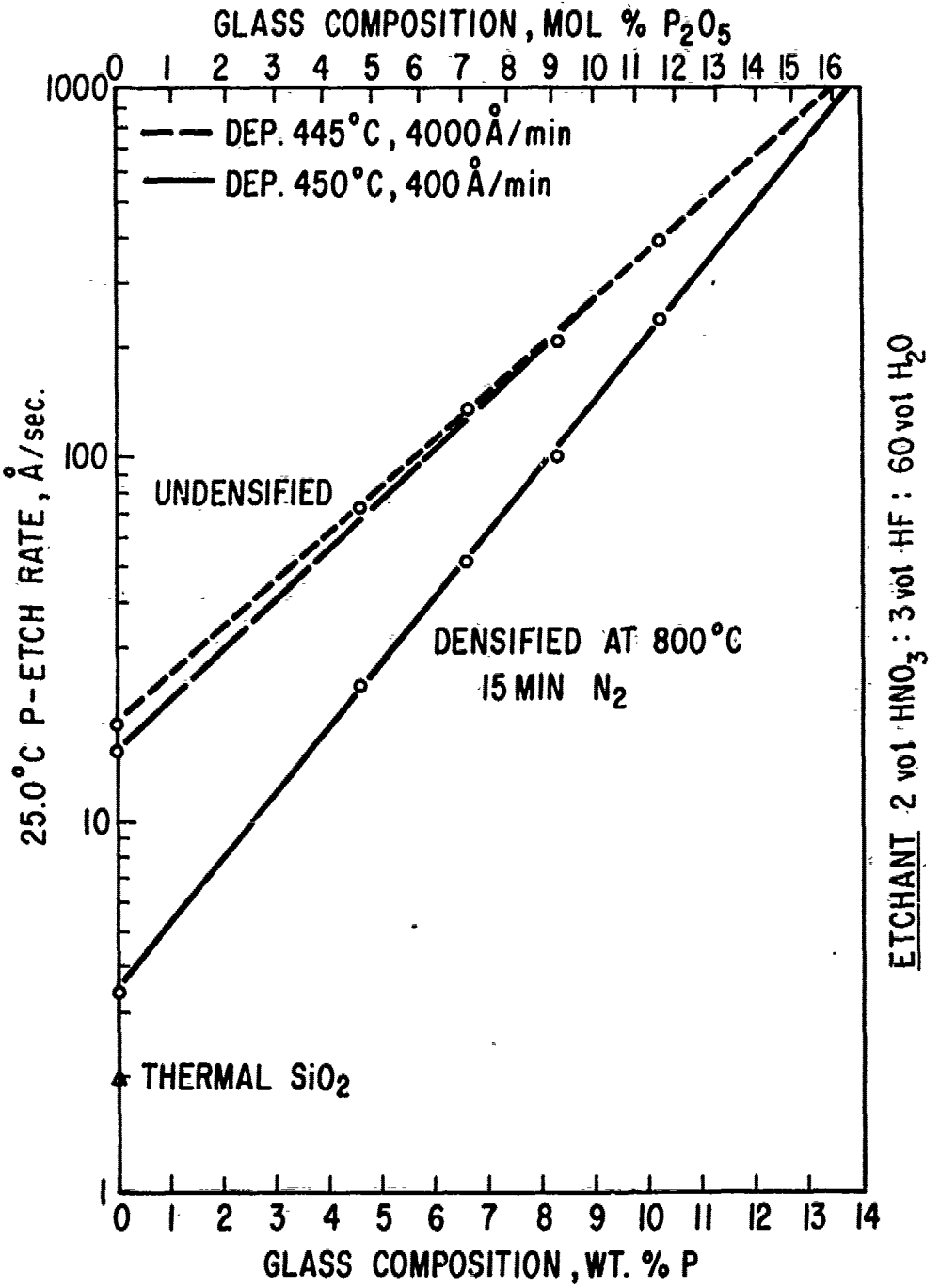


Figure 41. Etch rates of CVD PSG films as a function of glass composition, deposition conditions, and densification treatment.

the etch rate of as-deposited films depends not only on film composition but also on density and stress, which vary with CVD conditions, whereas the etch rate of densified films is a unique function of composition. With increasing phosphorus concentration in the PSG, the curves for as-deposited films approach the curve for densified films, indicating that at higher phosphorus concentrations a substantial degree of densification occurs during film deposition. Although curves of different slopes result for films of different density, the logarithm of the etch rate varies in all cases linearly with the wt % phosphorus in the film.

Primary calibration of phosphorus concentration in PSG for all our analytical work was based on wet chemical colorimetric analysis utilizing ammonium molybdate reagent. For this purpose the films were first dissolved in HF solution followed by elimination of all dissolved silicon to prevent its interference in the molybdate reaction. Two or three colorimetric tests were made per sample to obtain an average value.

Examples of how much the etch rate of CVD films is influenced by densification treatments of the films at intermediate temperature (400°C) and at room temperature under both dry and humid ambient conditions have been described in Section V. The effect of CVD conditions (deposition temperature and deposition rate) on the etch rate has also been demonstrated in Fig. 20 and Table 11. These results serve as additional examples of the sensitivity and use of the chemical etch rate method.

Determination of etch rate is carried out by measuring the film thickness and by measuring the dissolution time in the etch solution under isothermal conditons. Direct interferometric techniques of thickness measurement can be employed (see, for example, Appendix F) if the refractive index of the film is known. Multiple-beam interferometry of metal-coated samples yields the thickness independent of refractive index. Alternatively, ellipsometry can be used, it yields both thickness and refractive index of the film. One of the simplest absolute techniques if profilometry of a step etched down to the substrate as described in Appendix F. Diluted HF solutions can be used as etchants. We found an etch temperature of 25° $\pm$ 0.2°C and a mixture of 2 vol HNO_3 (70%), 3 vol HF (49%), and 60 vol H_2O ("P-etch") [89] convenient for CVD films of typically 1-μm thickness. Ammonium fluoride buffered HF solutions

89. W. A. Pliskin and R. P. Gnall, J. Electrochem. Soc. 111, 872 (1964).

should not be used because their selectivity for phosphorus (or boron) in the glass is poor; the sensitivity of dilute HF solutions is considerably greater. Etching is performed either integrally until the entire film is dissolved, or differentially until a desired portion is etched off. In the first case, the hydrophobic property of silicon can be used as an endpoint if the substrate is silicon. In the second case, an additional thickness measurement is required to obtain the residual and incremental film thicknesses. Details of the technique, including the use of a convenient etch apparatus for automatic sample movement, were described in a previous publication [29].

It is often convenient to relate the etch rate of a PSG film directly to the silane/phosphine ratio used in the CVD of the film. A plot of data for this application is presented in Fig. 42; the same samples and CVD conditions as in Fig. 41 were used to construct this plot. Also shown for comparison are etch rates for various types of SiO_2 films. This type of calibration curve is particularly useful for setting up CVD conditions and for making immediate adjustments in CVD processing.

The etch rate method is also useful in more complex analytical applications where composite films must be resolved into their components [90]. It is possible to identify composition and thickness of film layers in multilayer structures from which the profile can be obtained by plotting composite film thickness vs time of etching. A schematic plot of two hypothetical cases of triple film structures is presented in Fig. 43 to exemplify the technique. Practical applications of this technique for IC overcoat analysis are described in Appendix F.

It is frequently necessary, in PSG evaluation and comparison with literature data, to convert etch rate results obtained by other methods from weight percent phosphorus to mole percent phosphorus pentoxide. A conversion graph is presented in Fig. 44 for this purpose to obviate tedious computations.

2. Passivation Overcoat Analysis on Single IC Pellets

Several methods were tested for their suitability to microanalytical applications for determining the structure and composition of overcoat layers on single IC pellets. Instrumental composition profiling microprobe techniques

90. W. A. Pliskin, J. Electrochem. Soc. 114, 620 (1967).

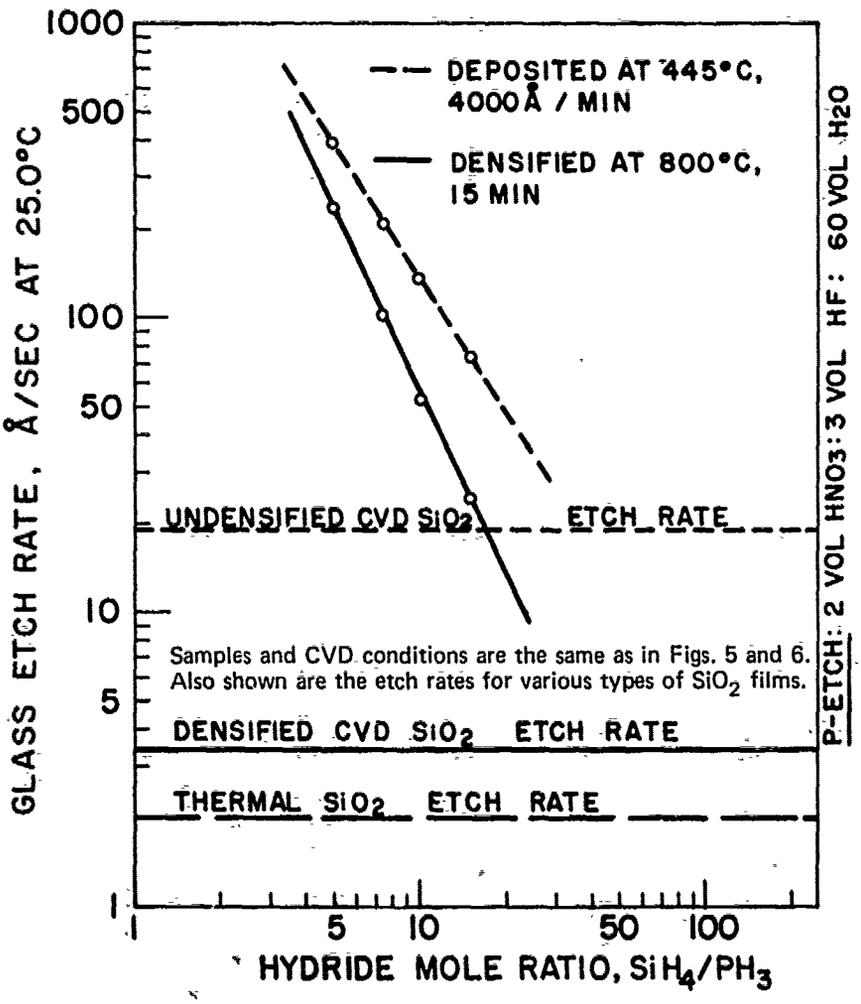


Figure 42. Etch rate of PSG films vs silane/phosphine ratio in the hydride gas mixture.

[88], particularly those based on electron probe microanalysis [91], Auger electron spectrometry [92,93] and MeV ion backscattering spectrometry [93], are certainly the methods of choice from a purely analytical research point of view, but these sophisticated methods are far too complicated for routine use in a control laboratory in a manufacturing facility where large numbers of samples must be analyzed rapidly. After exploratory work on quantizing electron probe microanalytical techniques and scanning Auger electron spectrometry,

91. G. DiGiacomo, J. Electrochem. Soc. 121, 419 (1974).
92. D. F. Stein, J. Vac. Sci. Technol. 12, No. 1, 268 (1975).
93. C. A. Evans, Jr., J. Vac. Sci. Technol. 12, No. 1, 144 (1975).

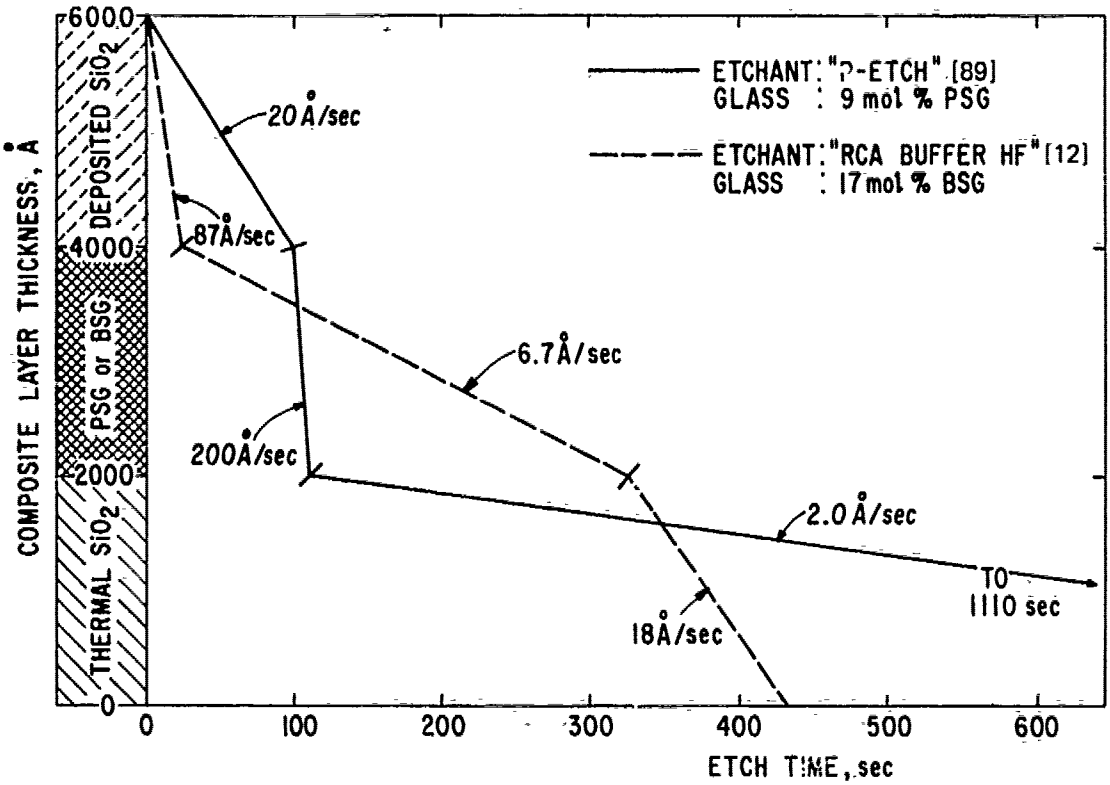


Figure 43. Application of selective etch method for analyzing multilayer dielectric structures.

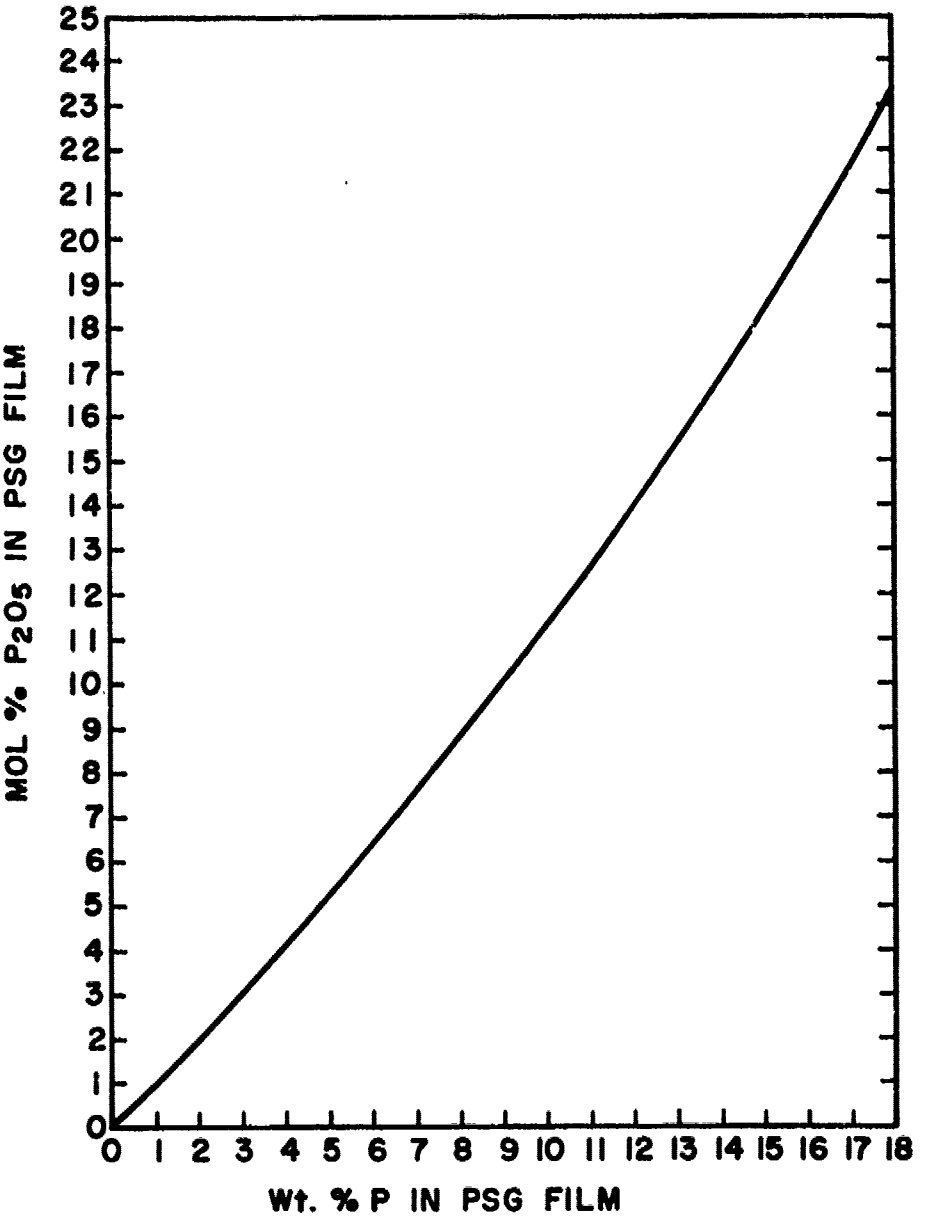


Figure 44. Correlation of mol % P_2O_5 and wt % phosphorus in PSG films.

we decided to devise a method based on etch rate analysis using the principles discussed in the preceding subsection.

If combined with aluminum marker-etching techniques, the resulting method can be used to determine the chemical composition, the component layer structure, the component thicknesses, the integrity of the dielectric overcoat, and the density of localized structural defects over aluminum metallization. Two techniques were developed: one based on graphical resolution of layer thickness vs etch time plots, and one based on step etching combined with profilometry. A complete description of these techniques is presented in Appendix F, which also includes results of applications in survey studies of commercial ICs.

3. Surface Resistance as a Monitor of Phosphorus Content

Measurements of surface (sheet) resistance of heat-treated wafers of PSG on silicon, using a four-point probe, can be employed as a production control monitor of phosphorus content in PSG layers. After PSG deposition on a high-resistivity p-type test wafer, a drive-in diffusion in dry nitrogen is done during which the PSG source reacts with the silicon, resulting in diffusion of phosphorus into the silicon substrate [94]. The PSG is then removed by etching, and the surface resistance measurement is performed. The surface (or sheet) resistance (ohms/square) will be related to the phosphorus content in the silicon, which in turn depends on the phosphorus content in the CVD glass and the drive-in temperature and time.

Based on surface resistance measurements vs drive-in conditions, a drive-in at 1200°C for 30 min was established. Shorter times and/or lower temperatures show a very strong dependence on exact drive-in conditions and lead to greater inaccuracies.

Using etch rate and x-ray fluorescence analysis to determine phosphorus content, the relation between surface resistance and wt % phosphorus was correlated in the linear coordinate plot shown in Fig. 45. Note that at low wt % phosphorus the surface resistance is extremely sensitive to phosphorus

94. I. Fränz and W. Langheinrich, Solid State Electronics 18, 209 (1975).

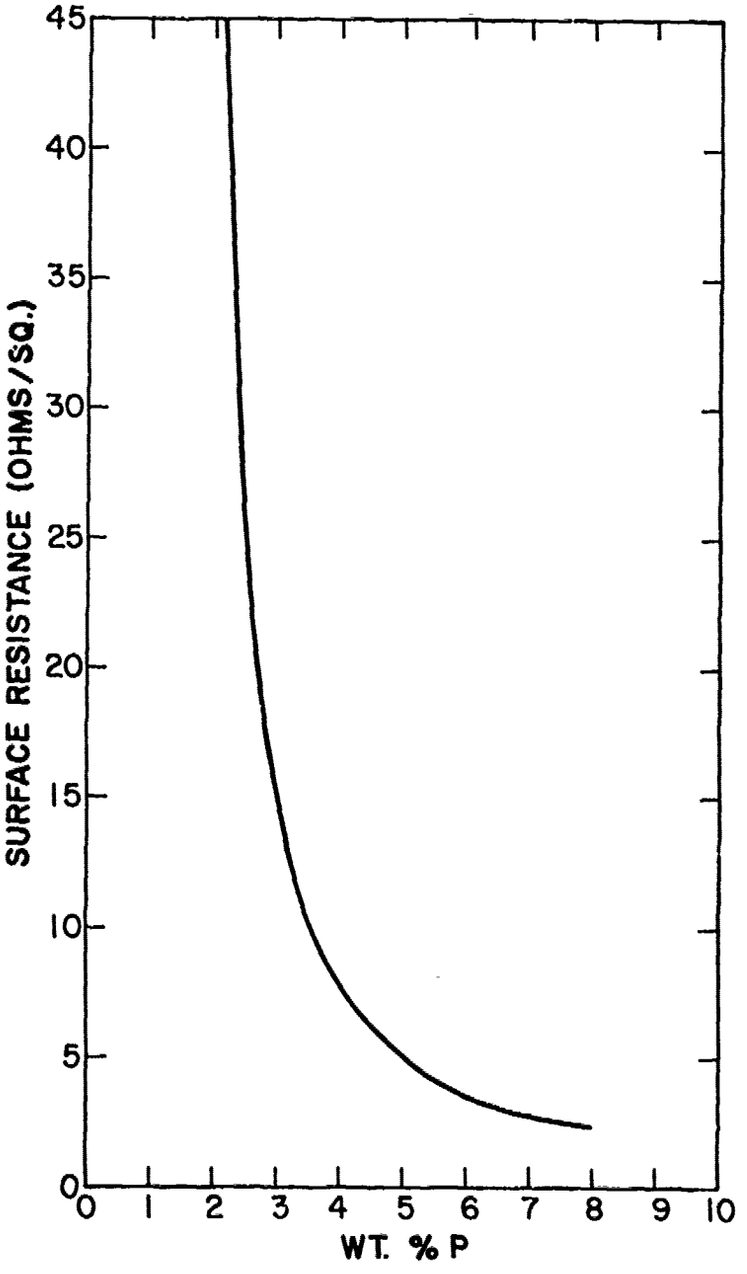


Figure 45. Typical linear coordinate plot of surface resistance vs wt % phosphorus in PSG for 1200°C, 30-min diffusion in dry N_2.

concentration. At high concentrations, there is a flattening of the curve, due to solid solubility limitations. If the data are shown on a log-linear plot, as in Fig. 46, an approximate straight line is obtained up to about 5 wt % phosphorus PSG. In either case, surface resistance measurements are useful for phosphorus concentration monitoring in the range of about 1 to 7 wt % phosphorus PSG. The accuracy for higher concentrations of phosphorus in the glass is poor because of solid solubility saturation effects.

It should be realized that these data are not standard since the exact value of surface resistance depends on wafer quality, crystallographic orientation, pre-deposition treatment, and diffusion conditions. The graphs shown illustrate typical data obtained under the conditions stated.

4. Measurements of Film Stress

The method devised for measuring stress in CVD films on silicon wafers has been described and exemplified in Subsections IV.C, and IV.E.

We have also employed a convenient test based on step-wise heating of overcoat passivated aluminum-metallized IC device wafers to relatively high temperatures (500° to 550°C) for typically 20 minutes per heating cycle to bring out latent stresses or weaknesses in the glass. These will increase in number with increasing temperature and give a realistic picture, suitable for statistical evaluation, of the potential stress levels and the specific location and distribution of excessive stress regions. This approach is akin to step-stress accelerated life-testing and constitutes a useful, practical test method, particularly in conjunction with aluminum marker-etching to enhance the detection sensitivity of localized structural defects, especially microcracks, in the glass overcoat. The largest areas of undelineated aluminum within a circuit, such as those over large capacitors in linear bipolar ICs, are particularly sensitive to the onset of crack formation as a function of heat treatment temperature. These areas are also most suitable for estimating the crack density, or for counting the number of cracks for quantitative statistical computations.

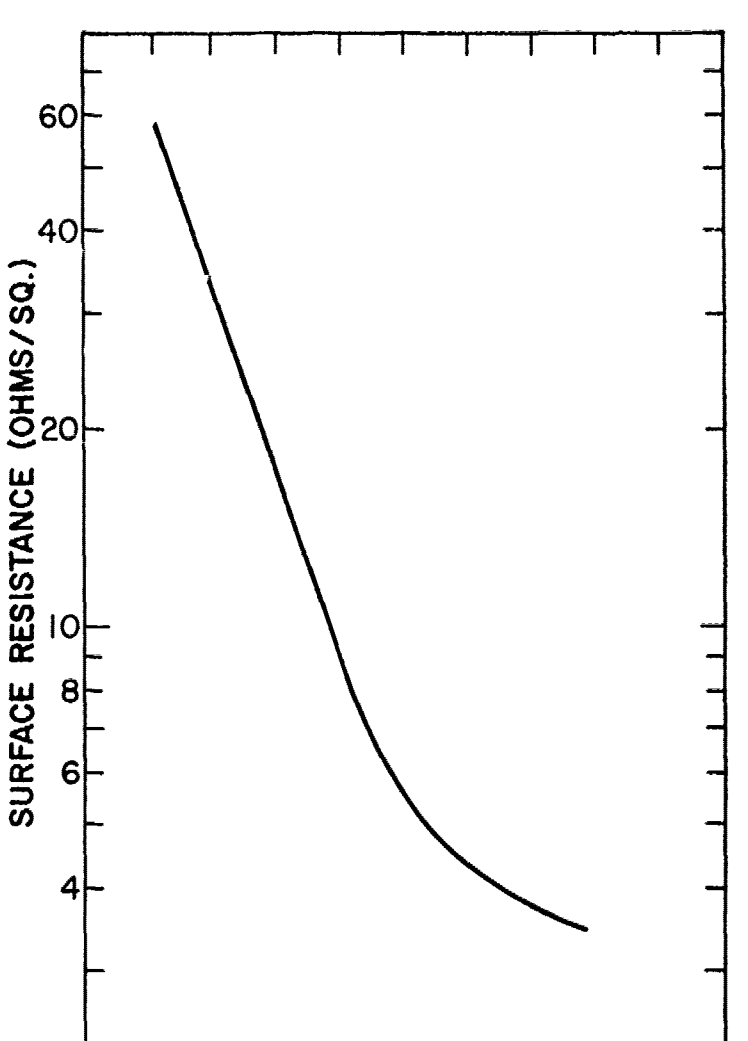


Figure 46. Typical log-linear plot of surface resistance vs wt % phosphorus in PSG for 1200°C, 30-min diffusion in dry N_2.

5. X-Ray Fluorescence Analysis of PSG Films

a. Background Information. - A nondestructive, fast, and quantitative instrumental method for determining the composition of PSG layers would be particularly desirable for rapidly analyzing large numbers of glassed wafers in production process-control applications. X-ray fluorescence analysis, also known as x-ray spectrometric analysis, x-ray emission spectroscopy, or x-ray spectrochemical analysis, is uniquely qualified to meet these requirements and, in addition, offers the possibility of automation [95]. Principles and methodology of this method have been recently discussed in detail by several authors [96-98]. Application of the method for multi-element analysis in refractories may serve as a typical example of its capability for analyzing many elements in a sample [99]. Determination of low-concentration phosphorus-doped SiO_2 layers for diffusion sources was reported several years ago [100] and has served as a starting point for further work. The SiK_α/PK_α ratio technique to be discussed was previously presented by us [101].

The main innovation of the new work described here is the extension of the x-ray fluorescence analysis to higher concentrations of phosphorus in PSG, and to layers thicker than 0.5 μm, which require suitable corrections because of radiation self-absorption.

b. Experimental Techniques. - PSG films of various phosphorus concentrations and layer thicknesses were deposited on polished, high-resistivity phosphorus-free silicon wafers, and also on phosphorus-free and silicon-free germanium wafers by the CVD techniques described in Section III. Colorimetric microanalysis of phosphorus by the molybdenum-blue reaction on concurrently deposited

95. J. A. Keenan, Amer. Laboratory 7, No. 2, 23 (1975).
96. E. P. Bertin, *Principles and Practice of X-Ray Spectrometric Analysis*, (Plenum Press, New York, 1975).
97. W. A. Pliskin and S. J. Zanin, "Film Thickness and Composition," in *Handbook of Thin Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw-Hill Book Company, New York, 1970), pp. 11-1 to 11-54.
98. J. V. Gilfrich, "X-Ray Fluorescence Analysis," in *Characterization of Solid Surfaces*, P. F. Kane and G. B. Larrabee, Eds., (Plenum Press, New York, 1974), pp. 275-306.
99. L. A. Winger and E. L. McKinley, Ceramic Bull. 53, 638 (1974).
100. F. X. Pink and V. Lyn, Electrochem. Technol. 6, 258 (1968).
101. W. Kern, "Recent Trends in Determining Composition and Imperfections of Dielectric Films," T. D. Callinan Award Address, Electrochem. Soc. Mtg., Houston, Texas, May 1972.

PSG films was used as the primary standardization of the x-ray fluorescence working curves. X-ray fluorescence radiation measurements were carried out using a Siemens Crystalloflex 4 x-ray generator with a chromium target x-ray tube (2000 W) and a Siemens Vacuum X-Ray Spectrometer Model VRS. Sample area of measurement was usually 0.50 cm^2.

Experimental results will be presented on the phosphorus emission intensity technique, on the silicon/phosphorus ratio technique, and on the analysis of PSG/SiO_2 double layers on IC device wafers.

c. Technique Based on Phosphorus Emission Intensity. - Figure 47 shows typical measurements of phosphorus K_α net radiation intensity as a function of the phosphorus concentrations calculated for each data point for 2.2-μm-thick (±0.1 μm) PSG films. It is seen that the relationship is linear over the range of 0 to at least 55 $\mu g/cm^2$. Calculation of the phosphorus concentration of a film from Fig. 47 requires knowledge of the film thickness and density, since the total amount of phosphorus is measured within a given test area. A density of 2.3 g/cm^3 was taken as a mean value for these CVD PSG films for establishing the curve. Calibration curves of this type are useful, but are valid only if the film thicknesses of samples to be measured are closely similar to those of the standard samples from which the calibration curve was established.

Figure 48 shows that the PK_α radiation intensity is not linear with film thickness. This is caused by self-absorption of some of the radiation by the film itself. The four curves are for PSG films of approximately 1, 3, 5, and 9 wt % phosphorus in thicknesses up to 25,000 Å. The portions of the curves from 0 to 4000 Å are seen to be linear in all cases, indicating that all of the PK_α radiation from the film is emitted. Beyond 5000 Å, the curve slope decreases as the thickness increases. For example, a 2-μm-thick 9 wt % phosphorus film yields only 68 percent of the PK_α intensity it should have if the relationship were linear.

Closer inspection of Fig. 48 reveals that the degree of nonlinearity varies also with composition, becoming worse with increasing phosphorus content. A plot of curves whose PK_α intensities are normalized to the 4000 Å point of the curve (to prevent cross-over of curves) is presented in Fig. 49, which now shows the nonlinearity vs composition dependence more clearly. The

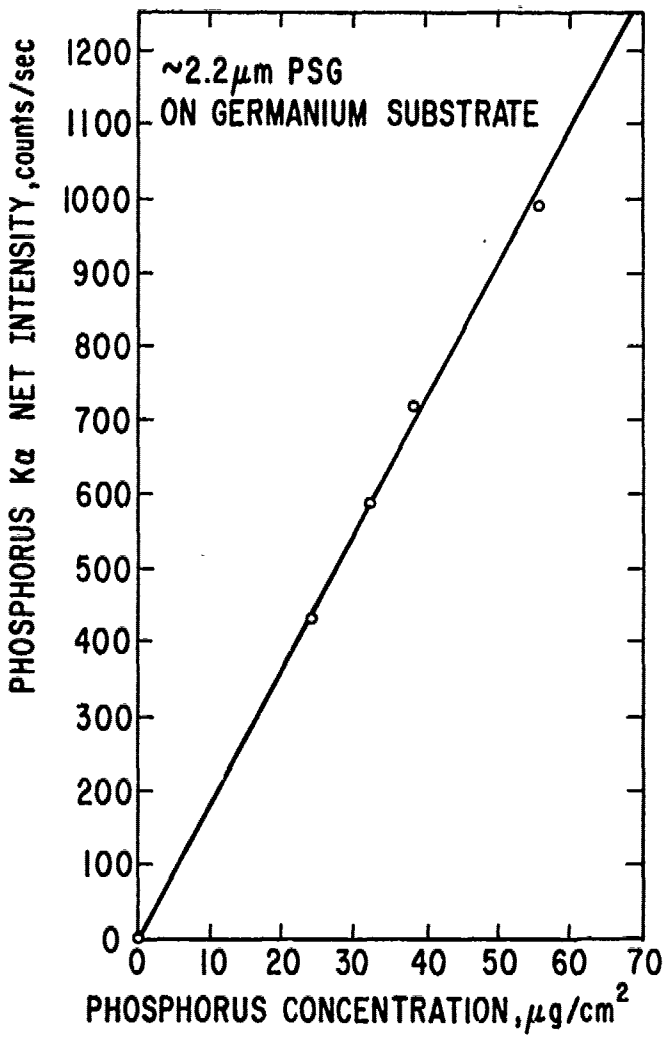


Figure 47. Typical measurements of phosphorus K_α net radiation intensity as a function of the calculated phosphorus concentrations.

intensity of the 1 to 3 wt % phosphorus curve falls off moderately with increasing thickness, whereas the 5 and 9 wt % phosphorus curves fall off quite strongly.

Table 20 lists the PSG standard samples included with each series of analyses to serve as reference base. The thickness correlation factors shown are needed to normalize the measured PK_α radiation to the exact film thicknesses of 5,000 and 10,000 Å.

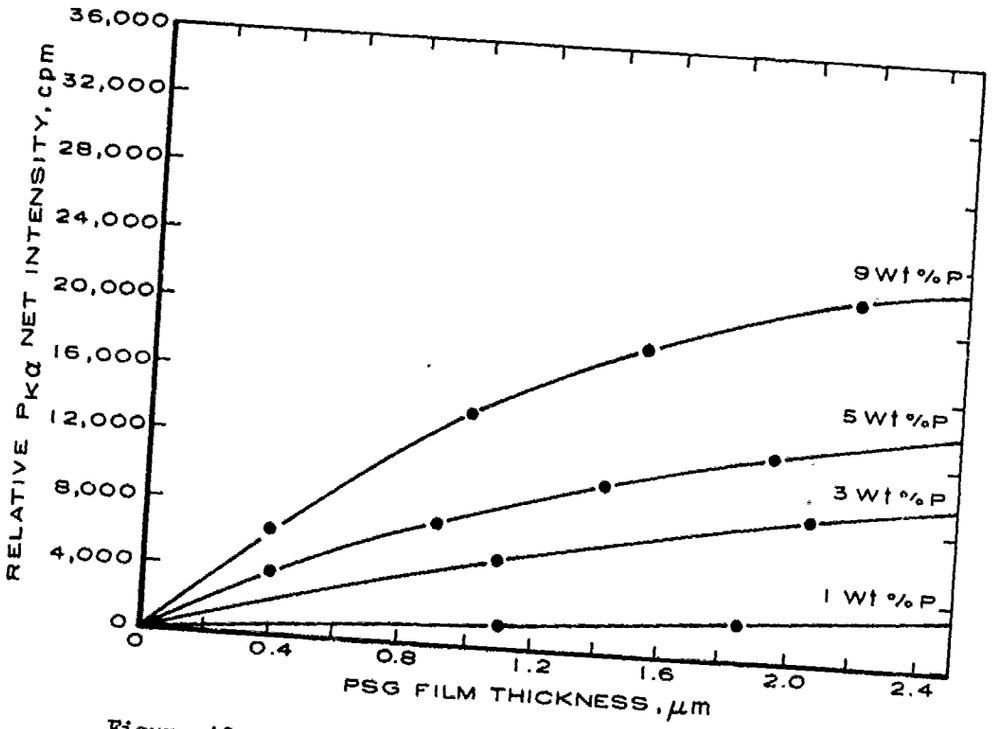


Figure 48. Effect of film thickness and composition on PK_α radiation intensity.

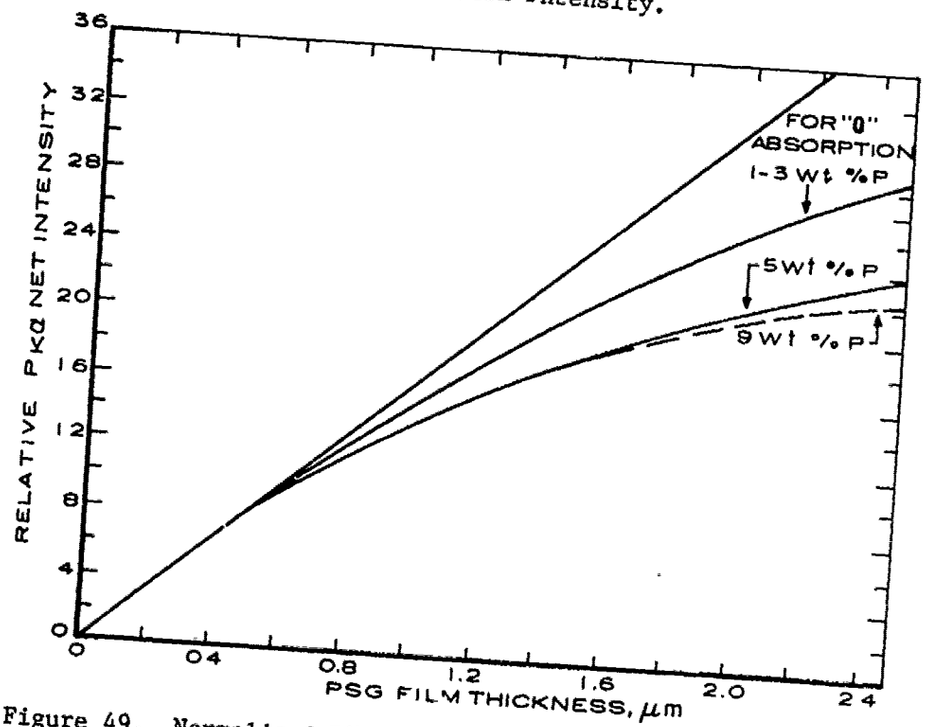


Figure 49. Normalized PK_α radiation intensity as a function of film thickness and composition.

The correlation factors in Table 20 were derived from the curves in Fig. 49. The same is done for the samples analyzed concurrently with the standards normalizing to either 5,000 or 10,000 Å (whichever is closer to the sample thickness). The curve in Fig. 49 closest to the estimated wt % phosphorus is selected for this purpose. Estimation of the normalization factors is straightforward, as shown in the example in Table 20. The wt % phosphorus in the samples is then read directly from the calibration curve.

Figure 50 shows typical standard calibration curves of PK_{α} radiation intensity as a function of wt % phosphorus in PSG films normalized to 5,000- and 10,000-Å thickness using the correlation factors in Table 20. The excellent linearity of the curves through the zero point demonstrates that the radiation intensity is directly proportional to the phosphorus concentration in the range of 0 to at least 8 wt % phosphorus. The calibration curve shown

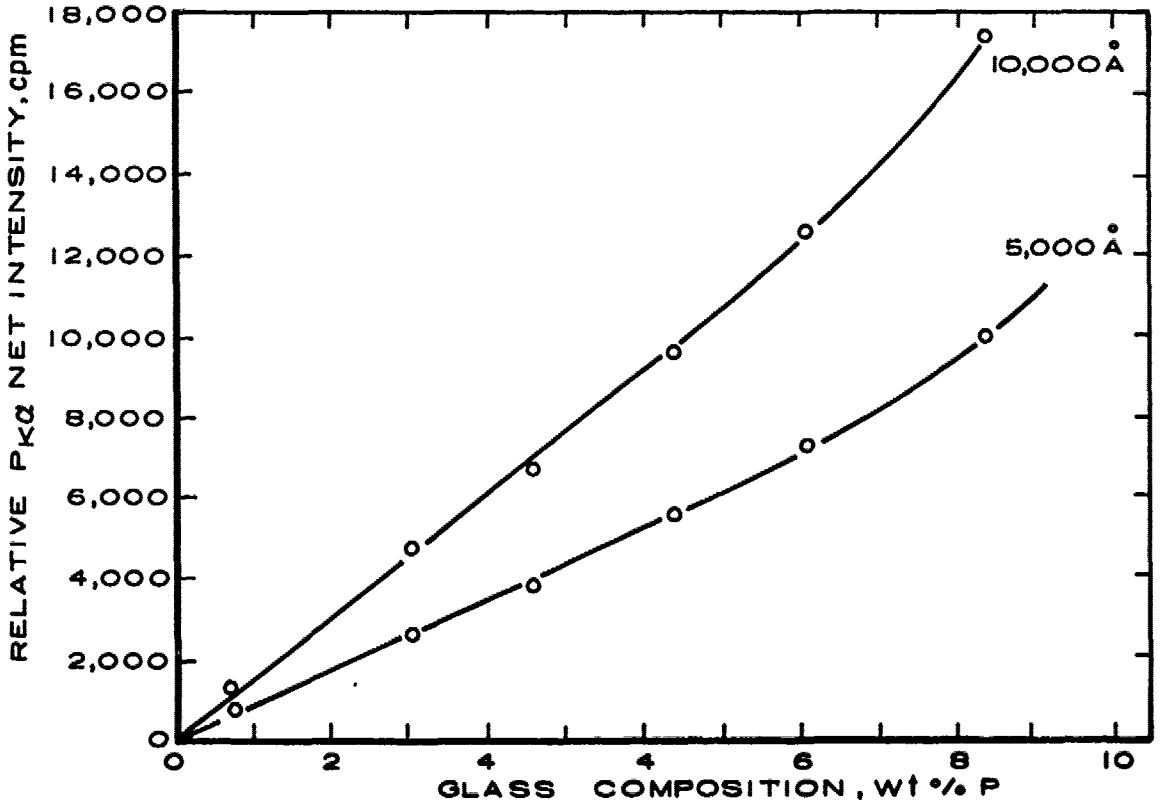


Figure 50. PK_{α} radiation intensity normalized to 5,000- and 10,000-Å thickness as a function of wt % phosphorus in standard PSG films.

Table 20. X-Ray Fluorescence Standards: Factors for Normalizing PK_α Net Intensities to 5,000- and 10,000-Å Film Thickness

PSG Standard[1] No.	Film Thickness[2] (Å)	Composition[3] (wt % P)	PK_α Net Intensity[4] Correlation Factors[5] for 5,000 Å	10,000 Å
Si-A	11,000	10.35	0.537	0.932
Si-B	10,750	8.05	0.547	0.947
Si-C	11,200	6.4	0.531	0.919
Si-D	12,300	4.6	0.490	0.858
Si-E	10,950	3.1	0.491	0.930
Si-F	11,150	0.74	0.482	0.912

1 PSG films prepared by CVD using high-resistivity silicon wafers as substrates.

2 Film thickness measured by reflection spectrophotometry.

3 Composition by modified wet chemical molybdenum-blue colorimetric assay.

4 X-ray fluorescence instrumentation as defined in the text.

5 Correlation factors were computed from the graphs shown in Fig. 49. Typical calibration curves using the above data for normalizing the measured PK_α radiation intensity to film thicknesses of 5,000 and 10,000 Å are plotted in Fig. 50. Estimation of these factors is done as shown in the following example for PSG standard Si-C:

Film thickness measured	- 1.12 μm
PK_α intensity measured	- 10,490 cpm
Normalization curve selected from Fig. 49	- 5 wt % phosphorus
Relative PK_α read for 0.50 μm	- 7.9
Relative PK_α read for 1.12 μm	- 14.9
Correlation factor to normalize to 0.50 μm	- 7.9/14.9 = 0.531
Measured PK_α normalized to 0.50 μm	- 0.531 x 10,490 cpm = *5560 cpm*

is considered relative and strictly valid only for the particular analysis series run on that date because of instrumental fluctuations. A new calibration curve is therefore made for each analysis date by including several standard samples with the unknown.

The graphs presented demonstrate the effect of film thickness on the measured radiation intensity and provide experimentally determined curves for obtaining the correction factors necessary for proper determination of the wt % phosphorus in PSG samples of any given film thickness up to 25,000 Å. These useful and not previously reported curves should be universally applicable for evaluating data obtained by any of the ordinary x-ray fluorescence instruments of the type defined above, regardless of minor changes in instrumental settings.

d. Technique Based on Silicon/Phosphorus Emission Intensity Ratio. - It was reasoned that the complications due to film thickness and instrumental fluctuations could be minimized or eliminated if the radiation emission intensity *ratio* SiK_α/PK_α would be used for measuring the phosphorus content in PSG films. Instead of the SiK_α line, one may also use one of its satellite lines to reduce the intensity relative to the PK_α intensity. It is necessary in this analysis to use a substrate free of silicon or other interfering elements. Polished germanium wafers are a particularly suitable substrate for this purpose. Standard samples very similar in composition to those on silicon (Table 20) were used in this work. A film thickness of 22,000 Å was selected since the intent was to make this technique applicable to CVD process control where unusually thick (1.5 to 2.5 μm) PSG films are used.

Figure 51 depicts the linear relationship of the radiation intensity ratio SiK_α/PK_α as a function of the mole ratio SiO_2/P_2O_5 for 2.2-μm-thick PSG films on germanium wafers. If the logarithms of SiK_α/PK_α ratio are plotted as a function of mole % P_2O_5 or of wt % phosphorus, the curvature of the resulting curves approaches exponential.

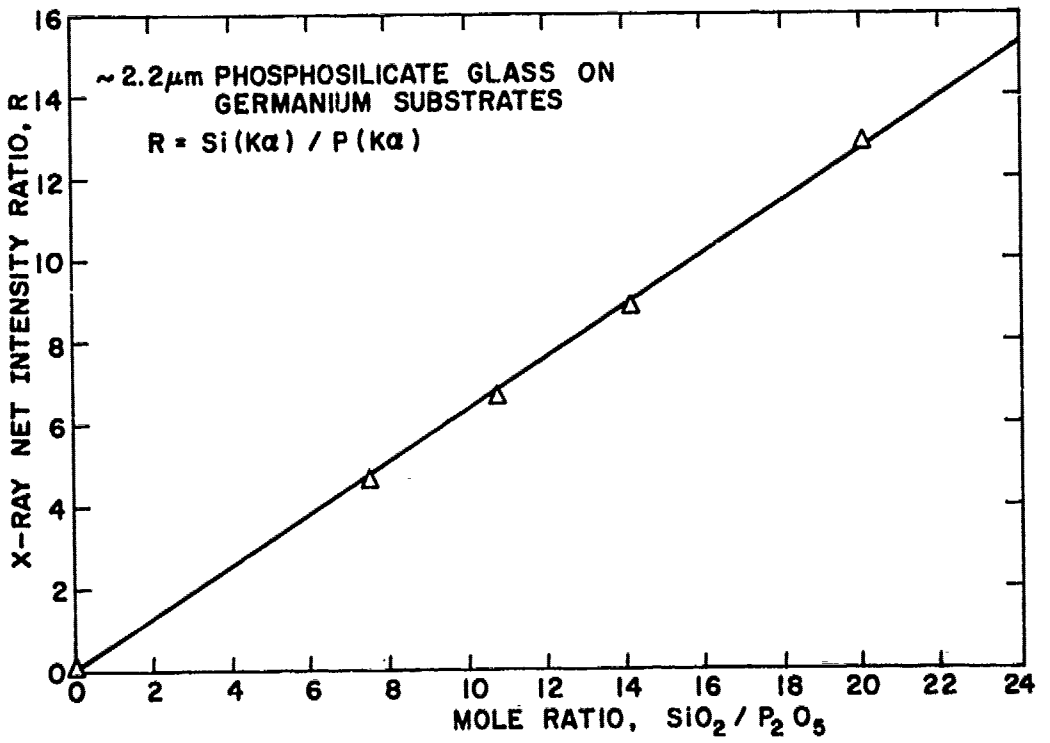


Figure 51. Linear relationship of the radiation intensity ratio SiK_α/PK_α as a function of the mole ratio SiO_2/P_2O_5 for PSG films on germanium wafers.

Plots of ratio values as a function of film thickness show that this technique is still not free of thickness complications, although it is considerably improved, to the extent that corrections can be neglected in many instances. Normalized plots for 5 wt % and 9 wt % phosphorus layers showed that, for example, a 2.5-fold reduction in thickness from 2.2 μm to 8,800 Å results in SiK_α/PK_α decreases of less than 10 percent, as compared with over 40 percent for the PK_α technique. As a second example, a film thickness of 2.2 μm ±10% gives a SiK_α/PK_α ratio deviation well within only ±2%, an accuracy that can be considered quite satisfactory for most applications, so that corrections are not needed within the film thickness range of 2.0 to 2.4 μm. For comparison, the deviations observed for the PK_α measuring technique for the same thickness and composition range are more than double (±4.5%) those achieved by the SiK_α/PK_α ratio technique.

In the light of these findings it can be concluded that, for accurate evaluation of PSG films greater than 0.5 μm in thickness, either method of x-ray fluorescence analysis requires appropriate corrections of the values obtained from the working curves to account for film thickness and composition deviations from the standards. The reasons for these problems lie, in addition to the phenomenon of radiation self-absorption by the film mass, in the x-ray fluorescence physics peculiar to the phosphorus-silicon system. It is therefore most desirable and simplest to settle for a constant film thickness for both standards and unknowns and analyze them concurrently so that these corrections, as well as systematic instrumental deviations, can be eliminated.

e. Analysis of PSG/SiO_2 Double Layers on IC Device Wafers. - All of the x-ray fluorescence work described thus far has been based on PSG films without SiO_2 top or bottom layers, deposited on phosphorus-free silicon and germanium substrate wafers. Frequently it is necessary, however, to determine the PSG composition of samples of control wafers with an SiO_2 top layer, or of such layers on actual aluminum-metallized IC wafers from production runs, and the question of possible interferences from the substrate arises.

An SiO_2 capping layer over PSG reduces the PK_α emission intensity through radiation absorption [32,100] and requires an appropriate correction.

Measurements on actual CMOS IC wafers having phosphorus-diffused regions, with and without PSG overcoats, and with and without SiO_2 capping layers, showed that neither silicon nor aluminum interferes with the determination of the phosphorus in the PSG layer. As shown in Table 21, the PK_α intensity of an uncoated IC wafer is not more than a few percent of the intensity obtained from a typical PSG overcoat. However, a 3300-Å-thick SiO_2 capping layer reduces the PK_α intensity by 18 percent, which agrees with the attenuation factor estimated from the thickness correlation curves presented in Fig. 43.

An additional source of error, if not accounted for properly, is the effect of etched-out PSG areas being excluded from x-ray fluorescence contribution. In the case of the CMOS IC CD4011A, this PSG-free area amounts to

Table 21. Application of X-Ray Fluorescence Analysis of PSG on Finished IC Wafers

Exper. No.		Sample Measured (Overcoats not pattern-etched)	PK_α Radiation Intensity net cpm	net intensity (%)	net attenuation (%)
IC Device Wafer	(1)	CMOS IC wafer (CD4017), prior to glassing	30	-	-
	(2)	Sample (1) overcoated with 7400 Å-PSG (4 wt % P)	2429	100.0	0
	(3)	Sample (1) overcoated with 7400 Å-PSG (4 wt % P) + 3300 Å SiO_2	1986	81.7	18.3
Silicon Control Wafer	(4)	Si control wafer prior to glassing	0	-	-
	(5)	Sample (4) overcoated with 7400-Å PSG (4 wt % P)	2333	100.0	0
	(6)	Sample (4) overcoated with 7400-Å PSG (4 wt % P) + 3300-Å SiO_2	1927	82.6	17.4

22 percent (grid lines = 14.7%, bond pads = 7.6%) of the total pellet area of 1.34 mm x 1.42 mm (53 mils x 56 mils). Computations are required for each type of circuit to determine the PSG-free wafer area being analyzed.

It is important to realize that the x-ray fluorescence method measures the total amount of phosphorus (with the corrections noted above) contained in and below the measured sample area. For example, a 5000-Å-thick film containing 2 wt % phosphorus yields the same signal as a 1000-Å-thick film containing 10 wt % phosphorus. It is obvious that the film thickness value needed to determine wt % phosphorus is just as important as the quantity of

phosphorus measured. Mechanical stylus techniques or methods based on interferometry can be used to measure the overcoat thickness of step-etched samples by the techniques already described and detailed in Appendix F.

f. Summary of Results.

(1) X-ray fluorescence analysis of phosphorus in PSG films based on measurement of the PK_α radiation intensity has been demonstrated to be precise and accurate if standards of known composition and film thickness are analyzed concurrently with a series of unknown samples. The films can be analyzed on silicon or germanium substrate wafers low in phosphorus.

(2) The PK_α radiation intensity can be considered linear with film thickness up to 5000 Å. Whenever possible, samples in the thickness range of 4000 to 5000 Å should be analyzed to obviate self-absorption corrections.

(3) Films thicker than 5000 Å exhibit radiation losses caused by self-absorption becoming worse with increasing thickness.

(4) The degree of self-absorption loss is also affected by the phosphorus content in the film.

(5) Suitable corrections should be used for films thicker than 5000 Å to allow accurate determination of the phosphorus content. Normalization curves have been presented to serve as a basis for estimating the appropriate correction factors.

(6) It has been demonstrated that the use of the SiK_α/PK_α intensity ratio can be used to minimize effects of self-absorption. This technique is particularly useful where thick films (1.5 to 2.5 μm) must be analyzed. However, the films must be deposited on a silicon-free and noninterfering substrate, such as germanium.

(7) The evaluation techniques and graphs presented should be useful and universally applicable for evaluating data obtained by any of the usual types of x-ray fluorescence equipment.

(8) The composition of PSG layers capped with SiO_2 can be measured by x-ray fluorescence but corrections are required for the radiation absorption losses caused by the SiO_2 top layer.

(9) X-ray fluorescence analysis for determining the wt % phosphorus in SiO_2-capped PSG overcoats on aluminum metallized IC wafers is fast, accurate, and reliable if the corrections that have been pointed out for layers

on simple substrates are made, and if the film thicknesses are either known or can be validly assumed. It was demonstrated that no interference results from the aluminum or other elements present in the substrate of CMOS IC wafers. However, bipolar IC device wafers would require a proper blank correction because of the phosphorus introduced during formation of the emitter glass and the emitter diffused regions.

6. Infrared Absorption Spectroscopy

The infrared absorption spectrum of as-deposited PSG films is of limited use for quantitative composition analysis, but it is very useful in structural studies of the films, such as in densification and leaching experiments, as will be demonstrated. The main limitation of infrared spectroscopic methods is the restriction to certain film thickness ranges and to composition in which the infrared absorbing constituents can be sufficiently resolved spectrally. Absorption spectra cannot be obtained for films on IC device wafers by transmission techniques because of absorption of infrared radiation by the substrate; suitable film substrates are needed that transmit infrared radiation uniformly in the wavelength range of interest. Oxygen-free high-resistivity silicon wafers of 0.6- to 1-mm thickness and polished on both sides are particularly suitable for studying CVD dielectric films.

A set of absorption spectra of ∿1.2-μm-thick CVD PSG films deposited at 450°C is presented as typical examples in Fig. 52. Films with several concentrations of phosphorus are shown for comparison; the absorbance intensity of the P=O band is seen to increase with the phosphorus concentration. The ratio of the intensity of the P=O absorbance band at ∿1325 cm^{-1} to that of the major Si-O band at ∿1050 cm^{-1} is approximately linearly related to the concentration of phosphorus in the glass and can be used with empirical calibration curves to estimate the film composition [101-104]. The sensitivity of films as-deposited is not as good as that for the previously published [23,105] analogous

102. E. A. Corl, S. L. Silverman, and Y. S. Kim, Solid-State Electronics 9, 1009 (1966).
103. R. P. Esch, J. M. Eldridge, P. Balk, and W. A. Pliskin, "Quantitative Determination of Phosphorus in Thin Phosphosilicate Films," Abstract No. 95, Electrochem. Soc. Mtg., Detroit, Fall 1969.
104. A. S. Tenny and M. Ghezzo, J. Electrochem. Soc. 120, 1276 (1973).
105. W. Kern, RCA Review 32, 429 (1971).

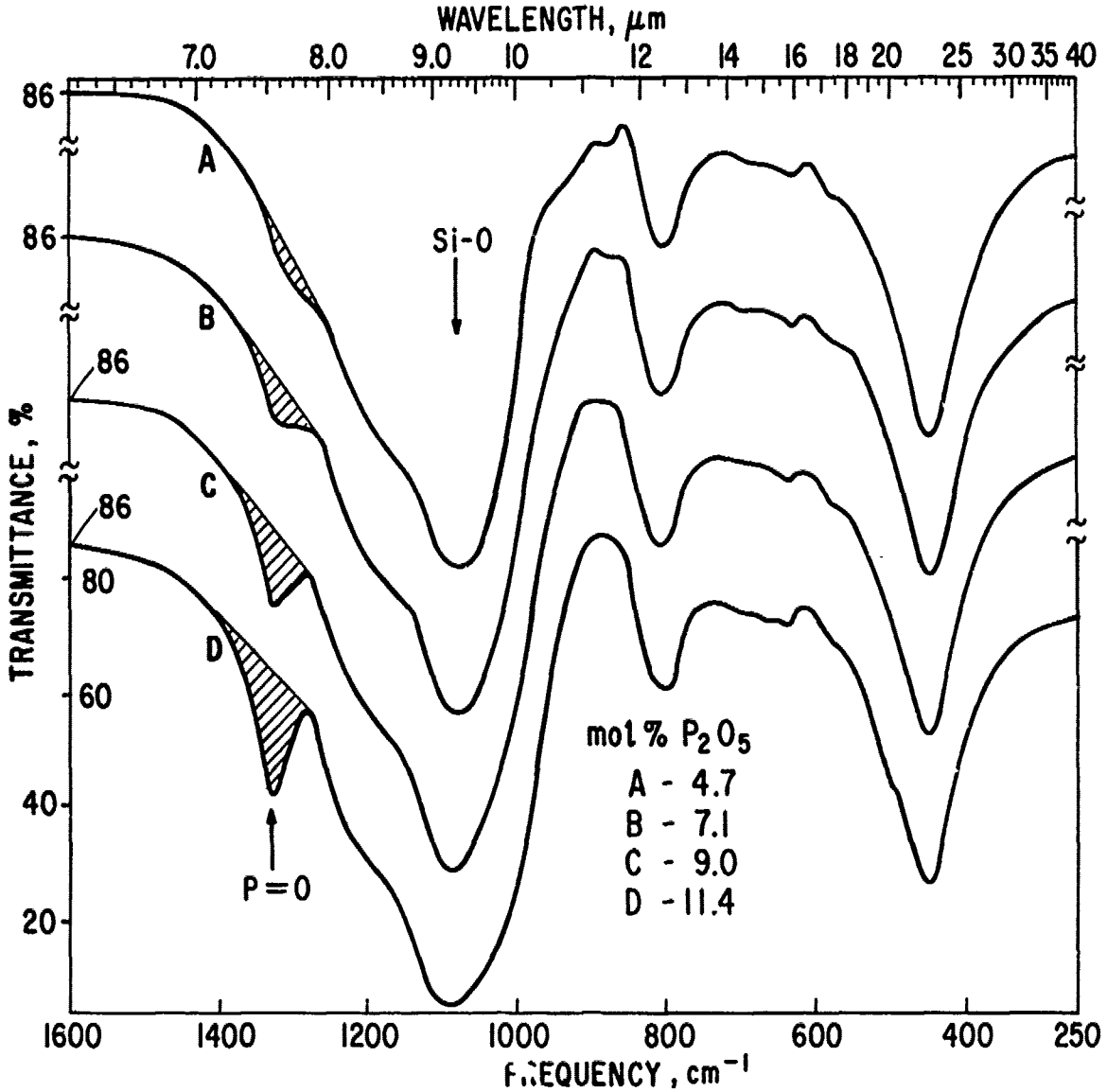


Figure 52. Infrared absorption spectra of PSG films of various phosphorus contents.

method for B_2O_3 in BSG, mainly because of the relatively weak absorptivity of P=0. This poses a severe shortcoming of the method for application to the analysis of PSG films in the compositional range of main interest (a few percent phosphorus). Previously, we had reported [23] that a densification treatment (typically 15 min at 800°C in N_2) causes spectral shifts in the P=0 and Si-O bands, which result in a considerable increase in resolution. It is now realized that utilization of this effect offers the means of extending

substantially the sensitivity of the method for measuring P=0 absorption in PSG films. Furthermore, the densification of samples prior to infrared spectroscopy eliminates the reported [23,104] dependence of the absorbance ratio on deposition temperature, and results in annealing of stress and strain that are introduced during CVD and that also affect the infrared absorption. (The technique for determining linear net absorbance is noted in Table 22, which also defines details of the measuring technique we used for obtaining the results listed on leaching studies to be discussed.)

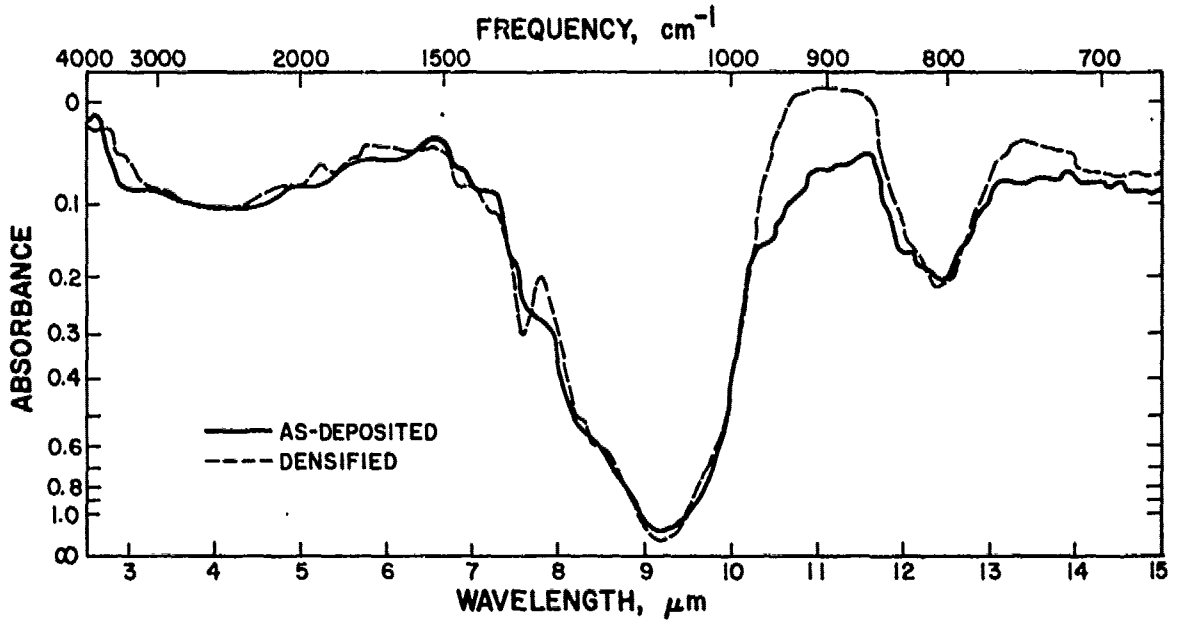
A pair of spectra is presented in Fig. 53 as an illustration. The film contained 4.5 wt % phosphorus and was 14,000-Å thick. The spectrum of the film before densification shows only a weak band in the wavelength region of 7.7 μm, only slightly separated from the Si-O major stretching vibration band. In contrast, the same film after densification shows a well-resolved band of P=O at 7.57 μm (1321 cm^{-1}).

Table 22. Infrared Absorption Data of Consecutive Leaching Treatments of PSG Films

Treatment	"Undensified Absorbance*"			"Densified Absorbance**"		
	Maximum	Minimum	Net	Maximum	Minimum	Net
Initial	0.44	0.20	0.24	0.51	0.20	0.31
6 min in deionized distilled H_2O at room temperature	0.46	0.22	0.24	0.52	0.19	0.33
60 min in deionized distilled H_2O at room temperature	0.45	0.22	0.23	0.54	0.20	0.34
6 min in deionized distilled H_2O at 100°C	0.44	0.22	0.22	0.53	0.20	0.33
60 min in deionized distilled H_2O at 100°C	0.46	0.22	0.24	0.55	0.22	0.33
60 min in pressure cooker in vapor phase at 15 psig, 121°C	0.40	0.19	0.21	0.48	0.15	0.33

*Refers to the linear net absorbance of the P=O band maximum at about 7.6 μm (1316 cm^{-1}) in the infrared vibrational absorption spectrum of a 19,000-Å-thick PSG film deposited at 371°C, and containing 7.7 wt % phosphorus. Absorbance was measured with a silicon blank wafer in a reference beam of a Perkin-Elmer Model 137B spectrophotometer.

**Same as * and for an identical film but after densification at 800°C in dry N_2 for 15 min.



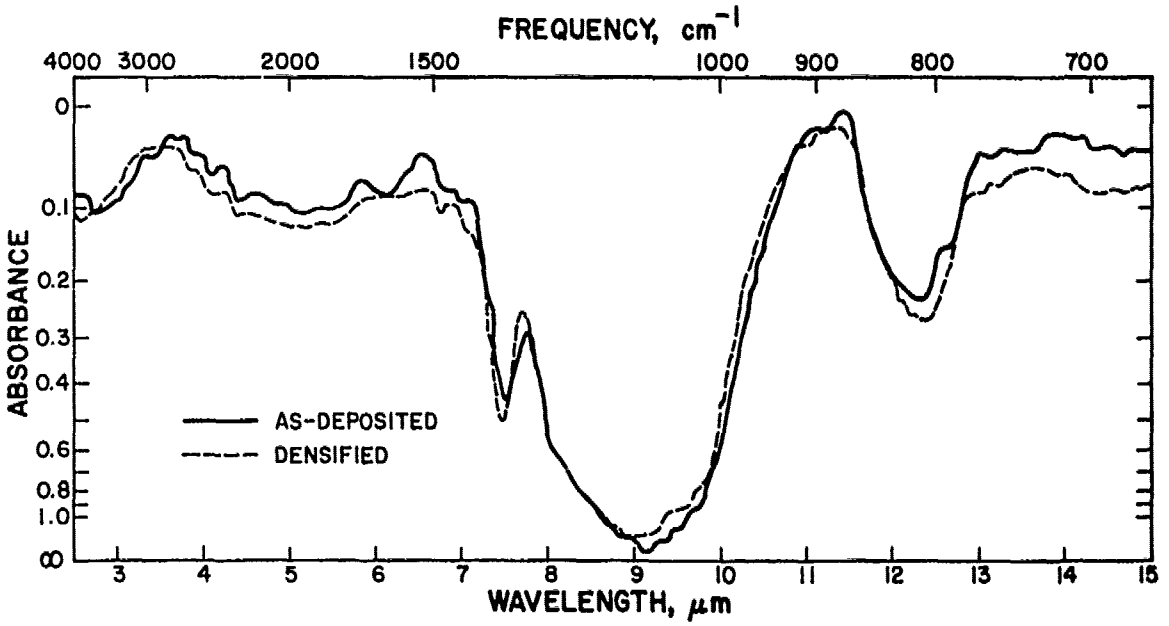
The film was 4.5 wt % phosphorus, 14,000 Å thick. Note the weak band at about 7.7 μm for the undensified film, and the strong, well-resolved band at 7.55 μm, created by the 800°C densification treatment of the second film. The film deposition temperature was 371°C.

Figure 53. IR absorption spectra of PSG film before and after densification.

A relatively high-concentration phosphorus glass (7.7 wt % phosphorus) of 19,000-Å thickness was prepared for leaching tests using the net absorbance of the P=O band as a quantitative measure. Half of the sample wafer was treated as deposited, the other half was first densified (15 min in N_2 at 800°C) before the leaching tests. The data after the consecutive treatments are presented in Table 22. It can be seen that the P=O net absorbance remained essentially unchanged, indicating no loss of phosphorus in either the densified or the undensified sample. This result was confirmed by x-ray fluorescence analysis of the same samples. The finding is in agreement with recently published data on PSG leachability [73, 74, 106] which have demonstrated the stability of PSG films containing less than about 8 mol % P_2O_5 (7.4 wt % phosphorus).

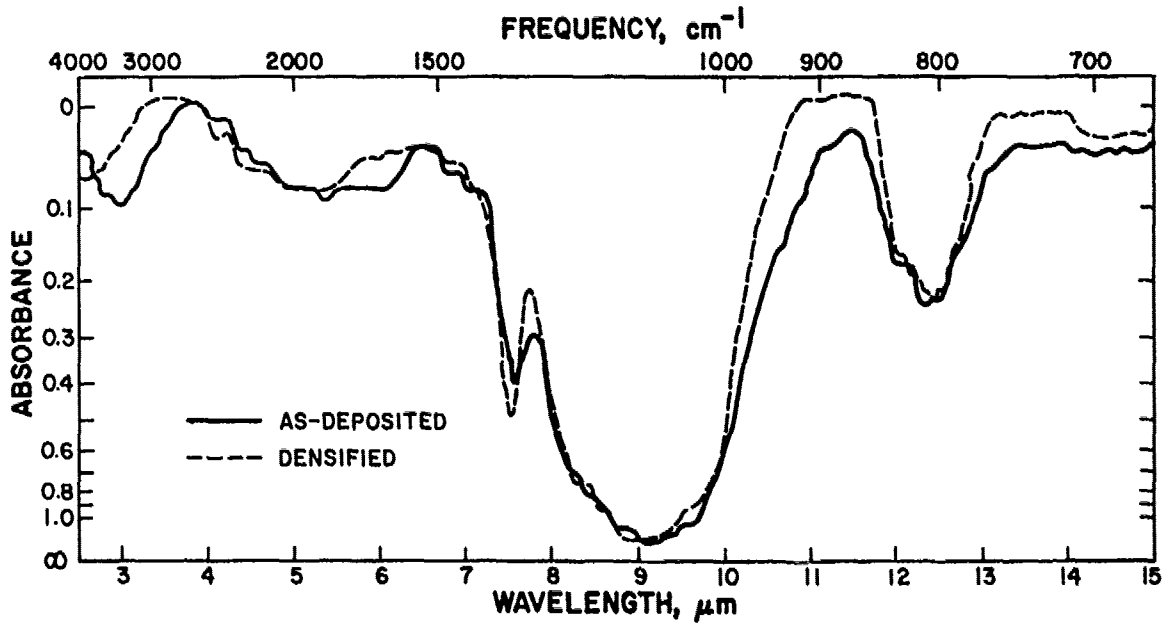
IR absorption spectra of thin films before and after the leaching treatments described above are presented in Figs. 54 and 55. To determine the linear net absorbance, a base line is drawn across the P=O band as a straight

106. E. A. Corl and W. E. Reese, Metallurg. Trans. 1, 747 (1970).



The films were 7.7 wt % phosphorus, 19,000 Å thick. The spectrum with a small P=O band at 7.6 μm is for the undensified film; the spectrum with a large peak at 7.6 μm is for the 800°C-densified film. Film deposition temperature was 371°C.

Figure 54. Initial IR absorption spectra of PSG films before leaching treatments.



The experimental conditions were the same as described under Fig. 54. Leaching treatments are listed in Table 22.

Figure 55. Final IR absorption spectra of PSG films after all leaching treatments.

line tangent to the absorption spectrum at points ("maximum" and "minimum" in Table 22) on either side of the P=O band at 7.6 μm. The net absorbance is determined as the difference between the maximum absorbance and the base line absorbance at the same wavelength.

7. Corona Charging for Conductivity Measurements of Passivation Layers

The use of a corona discharge for depositing ions on the surface of an insulator represents an alternative technique for determination of conductivity, breakdown strength, and layer quality. In this method, the corona device (fine wires at about 6000 V potential) generates ions in the gas ambient. These ions are swept to the sample and deposit on the insulating surface, charging it to the breakdown potential. A potential probe is used to monitor the surface potential. A preliminary evaluation of this technique was done with layers of 0, 4.8, and 8.5 wt % phosphorus in PSG about 10^{-4} cm thick, on degenerately doped n-type silicon wafers.

The coated wafers were charged with negative ions in dry nitrogen ambient at room temperature, and were then placed on a grounded aluminum block beneath the surface potential probe. The temperature of the grounded block is variable; measurements were done at 20° and 100°C.

A relatively rapid decay of surface potential is found for 0 wt % phosphorus layers, while the decay rate of the phosphorus-containing layers is much slower. Presumably, this is due to Na^+ or other ionic motion in the 0 wt % phosphorus glass. The effect is quite dramatic, as shown in Table 23.

Table 23. Surface Voltage Decay after Corona Charging

Phosphorus in PSG (wt %)	Surface Voltage			
	20°C		100°C	
	Initial (V)	After 5 min (V)	Initial (V)	After 5 min (V)
0	200	50	200	20 (in 5 sec)
4.8	1260	1170	1190	940
8.5	870	780	880	730

The initial potential in the table is measured several seconds after termination of corona charging. The delay is necessary to move the sample to the probe station. During the charging (about 15 to 30 sec) and the interval between charging and measurement, the surface voltage decays markedly for the 0 wt % phosphorus sample due to polarization by ionic motion. This is why the initial surface potential for this sample is so low.

For the phosphorus-containing samples, the initial potential is close to the intrinsic breakdown potential. Since there is no metallic contact on the surface of the sample, localized defects do not affect the observed initial voltage, and intrinsic strength can be determined.

Further experiments are needed to fully assess the usefulness of this technique in passivation studies.

E. TRACE IMPURITIES IN CVD SiO_2 AND PSG FILMS

SiO_2 and PSG films were deposited on high-purity polished germanium wafers in the single-rotation CVD hotplate reactor under specified conditions. Variables selected were temperature of deposition, rate of film deposition, and oxygen-to-hydride ratio, as shown in the headings of Tables 24 and 25. Film thicknesses were 1 to 2 μm.

Spark source solids mass spectrographic analyses were conducted to obtain a survey of trace impurities present and approximate concentration levels. Due to the thinness of the films, the spark penetrated into the germanium substrate, which made the determination of concentrations difficult and uncertain As a result, all samples were referenced to Pt, an external standard, as being 10^6 ppma. The values stated in Table 24 are based on the assumption of equal sensitivity for all elements. For most elements in most matrices this assumption produces results accurate to within a factor of three. Several analyses were usually made for the more important impurities (Cu, Ca, K, Na, Cr, B). In the case of Cu, 4 to 6 determinations were made to improve the precision; the concentration ranges from which the average was calculated are shown in parentheses.

The major impurity found was copper, at a concentration of 2 to 6 times greater than found in the unheated substrate germanium wafer, suggesting that

Table 24. Mass Spectrographic Analysis of Trace Impurities in CVD SiO_2 and PSG Films

Impurity Elements (concentrations in ppm atomic)	SiO_2 #91-1; 300°C, 300 Å/min	SiO_2 #91-3; 450°C, 2000 Å/min	SiO_2 #91-4; 450°C, 400 Å/min	PSG #D-1; 450°C, O_2/Hy* = 20:1	PSG #G-1; 450°C, O_2/Hy* = 6:1	Ge Substrate Control (unheated)
P	<0.68	0.36	1.3	Major	Major	<0.25
Cu (Range)	36 (31 - 42)	45 (33 - 62)	38 (30 - 47)	45 (33 - 60)	19 (8.1 - 44)	8.0 (7.4 - 8.6)
Ca	4.7	2.6	13.0	8.7	2.4	1.0
K	7.3	1.5	6.3	2.8	10.0	-
Na	5.6	1.8	4.3	1.5	9.3	-
Mg	<6.0	<1.6	8.8	-	-	-
Al	<0.63	<0.17	1.1	<0.21	0.73	-
B	0.76	0.26	1.1	1.4	0.27	-
Ag	-	-	-	-	-	2.8
Cr	<0.22	0.71	2.3	3.8	1.2	-
S	-	-	5.2	-	-	-

*O_2/Hy denotes oxygen-to-hydride ratio, $O_2/(SiH_4 + PH_3)$.

Table 25. Optical Emission Spectrographic and Atomic Absorption Analyses of Trace Impurities in CVD SiO_2 and PSG Films

Impurity Elements (concentrations in ppm by wt)	SiO_2 #91-1; 300°C, 300 Å/min	SiO_2 #91-3; 450°C, 2000 Å/min	SiO_2 #91-4; 450°C, 400 Å/min	PSG #D-1; 450°C, O_2/Hy^* = 20:1	PSG #G-1; 450°C, O_2/Hy^* = 6:1
Emission Spectrography					
Cu	10-100	6-60	6-60	0.6-6	10-100
Ga	3-30	3-30	3-30	-	3-30
Fe	1-10	2-20	3-30	<1	2-20
Mg	0.3-3	1-10	0.1-1	0.03-0.3	0.3-3
Quantitative Atomic Absorption					
Cu	1.4	0.92	0.89	0.63	1.3
Na	5.5	4.7	5.5	2.3	6.4
K	2.4	1.7	2.7	1.1	-

*O_2/Hy denotes oxygen-to-hydride ratio, $O_2/(SiH_4 + PH_3)$.

copper contamination may occur from the hotplate disc serving as sample stage in the CVD apparatus. Much lower concentrations of calcium, potassium, sodium, and magnesium were found.

Optical emission spectrographic analysis of the film material removed from the substrate again detected copper, but also detected gallium at substantial trace concentration levels. Some iron and magnesium were also found.

Quantitative atomic absorption analysis was next carried out for the three most important impurities: Copper, sodium, and potassium. The films were dissolved from the substrate for these analyses. The results show that the true absolute concentration of copper is much lower than suggested by the spectrographic analyses and ranged from 0.6 to 1.4 ppm by weight. The sodium and potassium levels ranged from 1 to 6 ppm.

F. SUMMARY OF MAJOR RESULTS AND CONCLUSIONS

Several analytical methods have been critically examined for their suitability as practical process control techniques for monitoring the composition and quality of CVD PSG passivation films. A number of innovations have been achieved to improve these techniques for this specific purpose. For compositional analysis of PSG films, we have found etch rate determination, x-ray fluorescence analysis, and sheet resistivity measurement particularly useful.

It has been shown that isothermal etch rates are the simplest and most convenient; densifying the films before etching renders the etch rate a unique function of the composition only, since dynamic effects in the as-deposited films due to film stress and density anneal on heating. Calibration curves have been presented relating etch rates of as-deposited and of densified CVD films with composition established by primary wet chemical analysis, and also with relative film density. Furthermore, the etch rate method has been successfully refined for analyzing the overcoat composition on single IC pellets, as detailed in Appendix F.

X-ray fluorescence analysis based on the PK_α radiation emission has been shown to be a fast, nondestructive instrumental technique for PSG analysis. However, it requires corrections for radiation self-absorption losses in thicknesses greater than 0.5 μm, or if SiO_2 top layers are present. The ratio of emission intensity SiK_α/PK_α is less affected by variation in film thickness,

but requires noninterfering substrates such as germanium. It has also been demonstrated that the method is applicable for analyzing the phosphorus content in overcoat layers deposited on aluminum-metallized CMOS IC device wafers.

Measurement of the sheet resistance of diffused PSG layers is a useful alternative method of analysis applicable to films in the composition range of 1 to 7 wt % phosphorus.

Techniques for measuring film stress have been refined, and a step stress thermal test has been developed and applied to visualize the numerical density and distribution of localized stress-induced defects on glassed IC device wafers.

The use of infrared spectroscopy in leaching and densification studies has been demonstrated and applied, and a thermal technique of enhancing the resolution of the P=O vibrational band has been shown to substantially improve the sensitivity of the infrared method for low concentrations of phosphorus in PSG films.

It has been pointed out that corona charging for conductivity measurements, by depositing ions on the surface of an insulator, is a promising and useful alternative technique for characterizing passivating films that merits further investigation.

Analyses of trace impurities in CVD films by emission spectrographic, mass spectrographic, and atomic absorption analyses of CVD SiO_2 and PSG films have been presented as typical examples of the type and concentration of contaminants in such films.

IX. GENERAL DISCUSSION, ACCOMPLISHMENTS, AND CONCLUSIONS

A. BASELINE FOR EXPERIMENTAL STUDIES TO IMPROVE PASSIVATION

In view of the wide variety of conditions being used to passivate commercially available ICs at the start of the contract, experimental studies were performed using a range of conditions that were intended to bracket production usage conditions, rather that a single deposition condition. The specific range of conditions used to deposit passivation glass layers on test wafers was as follows: deposition temperature, 325° to 450°C; oxygen-to-hydride ratio, 5:1 to 50:1; deposition rate, 0.1 to 1 μm/min; gas composition adjusted to produce deposits containing 0 to 8 wt % phosphorus in PSG.

Commonly used production type photoresists were employed, with the exposure of patterns obtained by contact printing techniques using commercial alignment fixtures. Delineation of patterns in the overcoat layers were performed by application of both standard buffered HF solutions and proprietary etchant compositions.

B. COMPARISON OF IMPROVED CVD LAYERS WITH BASELINE PASSIVATION

As information was developed on the effect of various deposition conditions on film properties, various improved deposition conditions were established, and additional test wafers were run. The properties of test devices passivated with improved glasses were then compared with those of baseline test devices, using appropriate test wafers that provided the best sensitivity for the parameter under study.

It is concluded that the best overall passivation layer properties are achieved if deposition is performed at a wafer temperature of 450°C under conditions which result in a PSG film containing approximately 3 wt % of phosphorus. The oxygen-to-hydride ratio should be approximately 20:1, which corresponds to the ratio producing a maximum deposition rate at 450°C. These conditions produce films with high density but with relatively low intrinsic tensile stress. We have also shown, during the final month of the contract, that additional reduction in intrinsic film stress can be achieved by adding moisture to the nitrogen carrier gas during the CVD processing.

It was clearly demonstrated that passivation films containing the recommended phosphorus content have no cracks, whereas SiO_2 films or PSG films with substantially less phosphorus frequently contain a significant number of cracks if deposited over typical IC wafers. Moreover, test devices with passivation films containing too much phosphorus (8 wt %) were shown to have less desirable electrical properties and far greater susceptibility to cathodic aluminum corrosion than devices made under the recommended conditions.

Devices prepared under conditions specifically selected to produce fewer pinholes not only contained far fewer pinholes than similar patterns on baseline wafers prepared by conventional contact printing techniques, but also were orders of magnitude less susceptible to adverse cathodic corrosion effects.

A comparison was made of the electrical properties of ICs fabricated with passivation glass deposited at a temperature of 375°C and similar devices passivated at 450°C. It was concluded that the level and distribution of electrical characteristics of the two groups of devices were essentially equal.

Tests with single, double, and triple layers of PSG plus SiO_2 passivation glass showed that the triple-layer structure had no advantages in terms of susceptibility to corrosion. Accelerated corrosion tests showed excellent stability for aluminum-metallized devices passivated with the double-layer structure consisting of 0.5-μm PSG (3 wt % phosphorus) capped with 0.3-μm of SiO_2.

C. STATE-OF-THE-ART IN GLASSING PRIOR TO START OF THE CONTRACT

At the start of the contract, an assessment was made of the state-of-the-art of glass passivation of commercially available aluminum-metallized integrated circuits. Products from five manufacturers, fabricated during the preceding several years, were studied to determine the type and quality of passivation glass. It was found that most manufacturers were using a phosphosilicate type passivating glass, although there was considerable variation in the thickness, phosphorus content, and localized structural defect density. Some products were passivated with SiO_2 containing no phosphorus, and some combined two or more passivation layers of distinctly different composition. The variation in glass properties is not particularly surprising in view of the fact that the principal reason for using the passivation glass was to attain scratch protection during chip handling, plus the fact that most of the

devices were made before the period of adverse publicity concerning aluminum corrosion due to excessively high phosphorus concentration in PSG passivation layers.

The fact that some products contained no phosphorus in the SiO_2 would imply that the manufacturer chose a simpler process (SiO_2 deposition rather than PSG deposition).

Some devices contained over 8 wt % phosphorus in PSG layers. It must be concluded that some manufacturers, not having available concrete experimental evidence at that time, felt it was not necessary to control phosphorus content at lower levels. Since the most severe type of cathodic aluminum corrosion occurs only when devices simultaneously have localized defects (cracks or pinholes) plus electrical bias plus high phosphorus content, small-scale qualification tests with high-phosphorus-concentration PSG may not have shown the possible adverse effects of PSG with 8 wt % phosphorus.

Several other reasons could be advanced for the use of excessively high phosphorus concentrations in PSG glasses in commercial ICs. For example, some manufacturers may have believed that the use of fixed PH_3/SiH_4 ratios in CVD gas streams, or the use of premixed PH_3-SiH_4 gases, ensured a fixed P_2O_5/SiO_2 ratio in the deposited glass. It has now been shown that for fixed PH_3/SiH_4 ratios, phosphorus content in the deposit changes appreciably with deposition temperature, oxygen/hydride ratio, and other factors.

It is possible, by comparing densified vs undensified etch rates or by performing pinhole determinations with the aluminum etch before and after heat treatments such as 400° to 500°C bakes, to obtain information which relates to the temperature of deposition of the passivation layer. Using this type of analysis, we infer that some of the CVD layers on commercial devices were applied at temperatures on the order of 350°C rather than at the recommended temperature of 450°C. The use of lower temperatures is not surprising, particularly in view of the fact that some commercial CVD equipment, without modification, is not capable of producing wafer temperatures above 350°C.

It should be pointed out that, concurrent with performance of experimental studies during this contract, a considerable amount of pertinent information on CVD and on aluminum corrosion was presented at technical meetings and/or was

published in scientific papers. Included were two invited presentations and two detailed technical publications (see Appendices A and E) on work that was in part supported by this contract. The work by scientists and engineers at organizations other than RCA Corporation has also been reviewed in these publications. The net result of information dissemination by all of these presentations and publications has been to greatly increase available knowledge of possible failure mechanisms, and of the necessity and the means for controlling the phosphorus content in CVD PSG passivation layers.

D. OVERALL CONCLUSIONS

(1) The effects of various deposition conditions on the properties of CVD PSG films have been studied in detail, and the relative importance of ten critical conditions has been established. It has been concluded that the most important conditions to control, in declining order of importance, are: substrate temperature of deposition, oxygen-to-hydride ratio, hydride input, silane-to-phosphine ratio, and nitrogen input. Other important factors examined include reactor geometry, wall temperature of the reactor, system cleanliness and gas purity, substrate surface characteristics, and substrate surface topography. The essential effects of CVD key parameters on PSG film deposition rate, phosphorus content, and intrinsic film stress are shown in Table 26. This schematic also allows one to predict, at a glance, what results can be expected on combining the various parameters, or how to compensate an effect by increasing or decreasing the relative magnitude of some of the other factors.

(2) We have concluded that the best overall properties of PSG overcoat passivation layers are attained if CVD is carried out at a substrate temperature of 450°C and at a silane-to-phosphine ratio that results in a PSG film of approximately 3 wt % of phosphorus (or 3 mol % P_2O_5). The oxygen-to-hydride ratio should be approximately 20:1, which also corresponds to the ratio producing maximum deposition rate at 450°C. PSG layer thicknesses of 0.5 to 1.5 μm have been found useful. The addition of an SiO_2 top layer enhances photoresist adherence and pattern definition.

Table 26. Effects of CVD Key Parameters for Preparing PSG Films

DIRECTION OF ARROWS INDICATES RELATIVE INCREASE OR DECREASE

↗ ↘ STRONG; ≺ SLIGHT; → NONE

CVD PARAMETERS	EFFECTS ON FILM		
	DEPOSITION RATE	PHOSPHORUS CONTENT	INTRINSIC STRESS
HYDRIDE FLOW RATE $\frac{SiH_4 + PH_3}{Time}$ ↑	↗	→	↗
HYDRIDE RATIO $\frac{PH_3}{SiH_4}$ ↑	↗	↗	↘
OXYGEN RATIO $\frac{O_2}{SiH_4 + PH_3}$ ↑	∩	∩	↗
DEPOSITION TEMPERATURE T ↑	H / → / L	↘	↘
DILUENT GAS FLOW RATE $\frac{N_2}{Time}$ ↑	∩	→	→

H = HIGH, L = LOW OXYGEN RATIO

(3) Bulk and surface electrical conductivities of CVD PSG films have been measured at several temperatures, and the effect of water vapor on them has been determined. It has been concluded that the bulk resistivity of CVD PSG films with 2 to 4 wt % phosphorus is more than adequate for passivation purposes.

(4) A detailed study of cathodic corrosion of aluminum conductor lines in glass-passivated silicon devices has been made, and the relationship between aluminum corrosion and phosphorus content of the PSG film, moisture, electrical bias, and localized defects in the passivation film has been defined.

(5) A correlation has been demonstrated between intrinsic stress in deposited films and susceptibility to cracking during deposition or during subsequent exposure to thermal stress conditions, particularly at processing temperatures higher than the deposition temperature.

(6) A practical method has been developed for measuring stress in CVD films deposited on silicon wafers; the method requires no special fixtures for the wafer during deposition and is thus applicable to any type of deposition system.

(7) A fundamental understanding of the material aspects of glass passivation has been achieved, including the interrelationship between phosphorus content in the PSG film and electrical and stress properties of passivation layers. The importance of processing device wafers under conditions that minimize cracks, pinholes, and other localized defects in deposited glass layers has been demonstrated, and a fundamental understanding of the factors that lead to such defects has been provided. On the basis of these findings, conditions have been defined for chemical vapor deposition glassing of aluminum-metallized IC wafers with a crack-free phosphosilicate layer.

(8) It has been shown that with defect-free PSG films of controlled low phosphorus content, corrosion of aluminum metal interconnection lines in passivated test devices is not a problem, even under accelerated stress conditions.

(9) We have concluded that CVD phosphosilicate glass, deposited under controlled conditions, offers a number of significant advantages over SiO_2 for passivation of integrated circuits.

(10) Densification studies in various ambients have shown that PSG films can be densified appreciably in relatively short times at 450°C in moist ambients without increase in the moisture content of the film; kinetics of the process have been established for several ambients.

(11) A new technique for lowering stress in CVD SiO_2 and PSG films has been developed. By depositing films using moisture-containing nitrogen carrier, we have obtained films with lower stress.

(12) Various techniques for characterizing the physical and chemical properties of deposited SiO_2 and PSG layers were evaluated, and appropriate practical techniques were refined or devised for use in production process control to assure films with suitable chemical and physical properties. The recommended techniques have been outlined in Table 19 of Section VIII.

(13) It was demonstrated that isothermal etch rate measurement of passivation layers is a reliable, fast, and convenient tool for determining film composition. Generally applicable calibration graphs have been established and experimentally demonstrated.

(14) The usefulness and limitations of sheet-resistance measurements of silicon control wafers, following diffusion of CVD PSG films for determining the phosphorus concentration, have been discussed and exemplified with typical calibration graphs.

(15) In addition to the methods listed in Table 19, x-ray fluorescence analysis of phosphorus in PSG films has been investigated and refined for rapid in-process control applications. This nondestructive instrumental method of analysis has been found a very useful additional or alternative technique for semiautomated compositional control that is particularly well suited for rapidly testing large numbers of samples.

(16) New microanalytical methods have been devised for determining the layer structure, layer type, and chemical composition of passivation overcoat layers on single pellets of IC devices, including hermetically packaged and plastic encapsulated types. The validity and usefulness of these methods have been demonstrated experimentally by extensive applications for comparative evaluation of commercial ICs.

(17) The application of infrared absorption spectroscopy for studying molecular, structural, and compositional changes in PSG films, in corrosion and leaching studies and in densification treatments has been demonstrated with specific examples. Significant improvements in spectral resolution of the P=O absorption band by thermal densification have been attained.

(18) The state-of-the-art of integrated circuit passivation techniques had been reviewed in detail prior to the start of this contract. That information was refined and updated concurrently with performance of the contract, and has been organized into several technical papers.

(19) We have considered various possible glassing-related failure mechanisms of glass-passivated ICs, and have developed a detailed understanding of the factors that must be controlled to achieve integrated circuits of high reliability. To a large extent, these findings are also believed to be applicable to other types of passivation materials deposited by a variety of techniques.

(20) Commercially available production-type CVD equipment has been classified into four categories. Experiments with SiO_2 and PSG films have been conducted using representative commercial production-type continuous processing systems of the more important types. It has been concluded that the results obtained using these production-type systems not only agree in principle, but frequently relate on a semiquantitative basis, with results obtained using a pilot production-type vertical rotary deposition system.

(21) It is concluded that properly controlled chemical vapor-deposition of phosphosilicate glass as a passivation layer offers a number of significant technical and economical advantages relative to layers of other materials, or to layers deposited by other techniques, and that CVD PSG films will continue to be widely used in IC fabrication.

(22) Based on experimental results achieved during this contract, and on consideration of available published information, we have made several specific recommendations of programs for future study. The areas recommended for future study include programs to consolidate and implement the findings of this project in large-scale production of integrated circuits, programs to improve the passivation of gold-metallized ICs, and research programs to provide low-temperature passivation layers that can effectively serve as additional or alternative moisture- and alkali ion-barrier protective coatings.

(23) We believe that application of the findings of this program to production of glass-passivated ICs will result in less lot-to-lot variation and significant improvement in the reliability of devices.

(24) We conclude that the results of this program have fully met the overall contract objective of providing an increased understanding of the material and processing requirements for successfully glass-passivating silicon planar metallized integrated circuits to improve their performance and reliability.

X. PROCESSING RECOMMENDATIONS

A. GENERAL CONSIDERATIONS

The processing conditions defined in this section are based on the findings presented in the preceding sections of this report. They represent, in our opinion, the best conditions that can be recommended for successfully passivating aluminum-metallized silicon planar ICs with PSG, with or without SiO_2 CVD glass overcoats. It must be realized that the exact CVD optimum processing conditions may differ slightly for various types or requirements of ICs and for the specific deposition equipment used for CVD. The recommended processing conditions will therefore be stated in ranges rather than in absolute figures. The description of optimum passivation processing conditions is divided into three segments: (1) pre-deposition, (2) deposition, and (3) post-deposition.

B. PRE-DEPOSITION PROCESSING

(1) Make sure that all traces of photoresist polymer, photoresist stripping agent, and etch residues from delineating the aluminum interconnect metallization have been scrupulously removed by suitable dissolution treatments and exhaustive rinsing. It is important to conduct rinsing treatments without allowing the device wafers to dry between various rinsing steps, for reasons discussed in previous papers on semiconductor surface contamination [107-110]. Carefully controlled ultrasonic treatments are effective for dislodging particulate contaminants. Organic residues would impair good adhesion of CVD layers; etchant residues may lead to corrosion; and alkali traces could lead to electrical instabilities of the devices. All of these impurities must therefore be removed before CVD processing.

(2) The final rinsing and drying treatments are especially critical. High-purity deionized and distilled water of about 10 to 15 MΩ/cm specific electrical resistivity at 23°C for terminal rinsing treatments is needed, if

107. W. Kern, RCA Review 31, 207 (1970).
108. W. Kern, RCA Review 31, 234 (1970).
109. W. Kern, Solid State Technology 15, No. 1, 34 and No. 2, 39 (1972).
110. W. Kern and D. Puotinen, RCA Review 31, 187 (1970).

drying of the wafers is to be done by gentle whirling at low speed (to prevent atomizing water droplets) in a wafer centrifuge. Alternatively, a terminal rinse in high-purity sodium-free isopropyl alcohol can be applied immediately after the last water rinse, followed by draining and drying in dust-free air in a laminar flow hood.

(3) The cleaned and dried device wafers should be glassed as soon as possible after the terminal rinsing treatment. If storing is necessary, it should be done in a dust-free clean-room atmosphere. Storage in chemically cleaned glassware is acceptable, but plastic containers must not be used as they lead to immediate surface recontamination [110].

C. GLASS DEPOSITION

(1) The substrate temperature of deposition should be maintained at 450°C unless a lower temperature is dictated by a particular device type. Nearly all aluminum-metallized ICs can be processed at 450°C without problems. Temperatures lower than 450°C have disadvantages, as explained in Section III.

(2) Preheating the substrate wafers directly in the CVD system at the temperature of deposition for about 5 minutes is important for removal of volatile surface impurities and for thermal equilibration prior to CVD. Again, a temperature of 450°C is more effective than lower temperatures.

(3) The oxygen-to-hydride ratio $[O_2/(SiH_4 + PH_3)]$ should be about 20:1 (18:1 to 22:1) if a deposition temperature of 450°C is used. For lower temperatures this ratio should be adjusted for optimum deposition rate and compositional stability by referring to Figs. 1 to 4. For example, at 350°C, the optimum oxygen-to-hydride ratio is approximately 11:1, and at 400°C it is 16:1.

(4) The hydride ($SiH_4 + PH_3$) input (gas flowrate) should be selected to result in a film growth rate of about 1500 to 2500 Å per minute. The flow rate to be used depends upon the size and type of the CVD reactor and the other CVD conditions. An exception can be made in the case of continuous CVD reactors operating on the principle of close-spaced nozzle arrays (see Appendix B), where integrated deposition rates of up to 1 μm/min are acceptable.

(5) The silane-to-phosphine ratio (SiH_4/PH_3) should be adjusted, in conjunction with the temperature of deposition and the oxygen-to-hydride ratio, to result in a PSG film composition containing 2 to 4 wt % phosphorus, which is equivalent to 2 to 4 mol % P_2O_5. As a start, the graphs in Figs. 5 and 6 should be helpful in selecting an appropriate ratio.

(6) The nitrogen input (flowrate) should be selected on the basis of best film uniformity, combined with highest deposition rate for a given type of CVD system. For the rotary hotplate CVD reactor described in Appendix D, for example, we have typically used a total gas flowrate of 11 liters/min, of which 10 liters/min was contributed by the diluent flowrate; the remaining 1 liter/min consisted of nitrogen-diluted hydrides plus oxygen.

(7) Cooling of the deposition chamber walls or of the gas distributor head is a desirable feature of a CVD system, because homogeneous gas phase nucleation is suppressed, which leads to cleaner film deposits with a lower density of particulate contaminants.

(8) Cleanliness of the CVD system is of paramount importance for attaining films with the lowest possible amount of particulate impurities. These can lead to pinholes and other structural defects in CVD layers and must therefore be avoided. The formation of particulate (powdery or colloidal) impurities by premature gas phase reactions in low-temperature CVD systems operating on the principle of hydride oxidation cannot be entirely eliminated, and constitutes the major shortcoming of all known systems. This type of contamination can be greatly minimized by instituting frequent cleaning of the CVD system to remove built up powder deposits, and by on/off blasting out all terminal gas lines with pressurized nitrogen to dislodge and remove loose deposits. The use of large-area, high-efficiency submicrometer filters at the inlets of the deposition reactor is also recommended. Maximum flowrate of nitrogen and cooling of the reactor walls are useful in suppressing these undesirable reactions.

(9) The layer structure and thicknesses of the passivation overcoat layers can be chosen within a fairly wide range to suit specific requirements. For example, the thickness of the metallization layer varies for different types of devices; those having thick metallization layers also require a thicker overcoat layer to ensure good edge coverage, which becomes more critical with increasing thickness. We have found an overcoat layer thickness

of 1 μm to be a good target thickness, but the thickness can range from about 0.7 to 1.5 μm and can consist of a single-layer PSG or a double-layer PSG with SiO_2 on top. Thicker overcoat layers afford somewhat better mechanical protection of the aluminum interconnection, but they are susceptible to microcrack formation if post-deposition heat treatments at 450°C or above are applied.

(10) The main function of the (optional) SiO_2 top layer is to enhance photoresist adhesion, obviating the application of organosilane adhesion promoting coupling agents that may otherwise be required to maintain good resist adhesion during pattern etching. Furthermore, a SiO_2 top layer can act as a redundant layer in eliminating any pinholes that might be present in a thin, single PSG layer. It is desirable to deposit the SiO_2 layer at a low rate to reduce film stress.

(11) Water vapor may be introduced into the CVD reactor during deposition of the films. As described in Section IV, this technique lowers the stress in CVD films without having deleterious side effects on the film or the IC substrate wafers. This technique may be particularly useful in the deposition of PSG/SiO_2 bilayers. No further recommendations can be given at this time since feasibility of this new process was first demonstrated near the end of the contract.

D. POST-DEPOSITION PROCESSING

(1) Optional heat treatments at 450°C for the purpose of densifying the passivation glass and to release film stresses can be applied as discussed in Section V.

(2) Densification heat treatments are best conducted in an atmosphere of steam, which is much preferable to dry or moist gases. A treatment period of one to several hours can be used.

(3) Glass overcoated IC device wafers should be thoroughly baked out at about 200°C before applying the photoresist coating.

(4) Glass etching for pattern delineation can be performed with the usual ammonium fluoride buffered-HF etchants to maintain good resist adhesion and to achieve good pattern resolution.

(5) Photoresist processing should be conducted under carefully controlled conditions to avoid the introduction of glass defects, such as pinholes, during these operations. The contact printing step on aluminum-metallized devices is particularly critical and is best replaced by projection printing or other noncontact printing techniques, if at all possible.

(6) Photoresist removal can be accomplished by the usual techniques of chemical stripping, or by rf plasma ashing after its acceptability is demonstrated for each particular type of device.

E. PROCESS CONTROL

The physical and chemical properties of CVD overcoat layers should be controlled by periodic checks to ensure production within recommended specifications. Practical analytical control methods to achieve this have been presented in Section VIII.

XI. RECOMMENDATIONS FOR FUTURE STUDIES

In this section, recommendations are given for several specific areas where additional passivation studies should be performed.

A. PRODUCTION ENGINEERING PROGRAM TO IMPLEMENT THE DEPOSITION OF PHOSPHOSILICATE GLASS PASSIVATION LAYERS WITH CONTROLLED PROPERTIES

A production engineering program is recommended to establish conditions, on production-type CVD equipment, for deposition of phosphosilicate glass passivation layers with controlled physical and chemical properties. This program would be based on the results obtained on the present contract and would include development of quality control methods which are applicable to routine monitoring of production equipment for deposition of PSG films. Emphasis should be given to implementation of techniques for controlling phosphorus content and stress, and for greatly reducing the incidence of cracks and pinholes in the deposited films. Appropriate life test studies should be made to assess the degree of passivation attained on statistically significant groups of integrated circuits, and a detailed failure analysis should be made on any failed devices to establish the physical mechanisms of failure.

B. DEVELOPMENT OF TECHNIQUES FOR LOWERING STRESS IN CVD FILMS

CVD films of SiO_2 and of PSG are in intrinsic tensile stress as deposited. This intrinsic stress, combined with tensile stresses arising because of recrystallization of the underlying metal, can lead to crack formation in passivation layers. As demonstrated during the latter part of the present program, use of a nitrogen carrier gas saturated with moisture can result in significant reductions in intrinsic stress in both CVD SiO_2 and CVD PSG films deposited at 450°C. The use of moisture-containing ambients is expected to have even greater advantages for films deposited at temperatures such as 325°C (as required for certain types of devices), and is expected to result in improved adhesion between deposited films and oxide substrates. A program of studies is recommended to investigate in more detail the effects of moisture during CVD, to further improve conditions of deposition, and to determine the applicability of moisture-containing nitrogen carriers to production-type equipment.

C. STUDY OF INTERFACE PROPERTIES BETWEEN THE DEPOSITED PASSIVATION LAYER AND THE THERMALLY GROWN SILICON DIOXIDE LAYER

A study should be made to characterize the physical and chemical properties of the interface between deposited passivation layer and the underlying dielectric layer in integrated circuits. The exact nature of the bond between the deposited SiO_2 or PSG and the underlying thermally grown SiO_2 is an important determinant of the susceptibility of integrated circuits to several possible failure mechanisms, including excessive electrical conduction at the dielectric-dielectric interface; flaking, peeling, or blistering of the deposited dielectric during environmental stresses; and aluminum metal extending between adjacent conductor lines during electrical stresses. A major objective of such a study would be to develop techniques for characterizing interfacial conductivity, adhesion, and other significant properties of the dielectric-dielectric interface, and then to establish those materials and processing conditions which must be controlled to consistently obtain a satisfactory bond between the deposited passivation layer and the integrated-circuit dielectric material.

D. DEVELOPMENT OF IMPROVED TECHNIQUES FOR CHARACTERIZING LOCALIZED DEFECT DENSITY IN PASSIVATION LAYERS

There is a great need to develop improved techniques for characterizing localized defects in passivation layers, including cracks, pinholes, thin spots, and poor edge coverage. The possibility of developing nondestructive techniques should be investigated. Quantitative information should be obtained on the sensitivity of various methods. The best available methods should then be used to determine the origins of localized defects in typical production processes, and modifications in processing should be made to substantially lower the incidence of localized defects in passivation layers.

E. STUDY OF LOW-TEMPERATURE-DEPOSITED SILICON NITRIDE

Low-temperature-deposited silicon nitride layers have been shown to be feasible for passivation of Al- and Au-metallized integrated circuit wafers. When these films are deposited under suitable conditions, they can effectively serve as a moisture barrier and as an alkali ion barrier. Low-temperature Si_3N_4

films have been deposited by plasma deposition techniques, by reactive sputtering, and by photochemical deposition techniques. Considerable work is needed to correlate physical and chemical properties of low-temperature Si_3N_4 layers with passivated device reliability, and to develop production-type equipment and techniques for depositing and characterizing such films. Some of the deposition techniques can produce radiation damage in the underlying thermally grown SiO_2 layer, and, in these cases, techniques for minimizing radiation damage must be developed.

F. STUDY OF DEPOSITION OF INORGANIC DIELECTRIC FILMS OVER GOLD-METALLIZED DEVICES

A study should be made to establish suitable materials, processes, and conditions for deposition of inorganic dielectric passivation layers over Au-metallized transistors and integrated circuits. Devices with Au metallization, in contrast to Al-metallized devices, have several additional limitations, including the requirement that deposition temperature should not exceed approximately 350°C; the fact that gold is part of a bilayer or trilayer metallization system and the underlying metal layers may be undercut during metal pattern delineation; and the fact that deposited inorganic dielectrics tend not to adhere to gold surfaces. Passivation layers on Au-metallized devices are desirable for scratch protection during handling, for protection against loose conductive particles in packages containing a cavity, and for protection against electrolytic dendrite formation which can result in short circuits.

G. DEVELOPMENT OF LOW-TEMPERATURE-DEPOSITED ALUMINUM OXIDE PASSIVATION PROCESSES

A program of studies should be initiated to assess low-temperature-deposited aluminum oxide layers for passivation of Al-metallized and Au-metallized silicon devices. Aluminum oxide films, like Si_3N_4 films, can be effective alkali barriers, and can serve as a moisture barrier when deposited under suitable conditions. Since Al_2O_3 passivation films could have potential cost and adhesion advantages compared with low-temperature-deposited Si_3N_4 films, their capabilities and limitations should be investigated. Low-temperature deposition of aluminum oxide layers is possible by chemical vapor

deposition, by plasma reactions, and by rf sputtering techniques using a target of pure Al_2O_3.

H. STUDY OF LOW-TEMPERATURE CVD OF TERNARY PHOSPHOSILICATE GLASSES

The addition of a ternary component to the glass during its synthesis by CVD could further improve the properties of phosphosilicate glasses and thereby tend to produce glasses of lower reactivity due to chemical bonding of a much larger fraction of the phosphorus. Considerably higher percentages of phosphorus than are presently used could therefore be employed, with improved properties such as greater sodium-gettering. As an additional benefit the linear thermal expansion coefficient would be increased, leading to films of lower residual stress.

The ternary component could be taken from the group of glass forming elements, in particular Al, Ge, As, Pb, or B, or of silica-network modifiers such as Zn, Pb, or halogens. Compounds of all of these elements are available that have sufficiently high vapor pressure to make their introduction into the presently used hydride CVD process feasible so that their co-oxidation to a ternary homogeneous silicate glass could be achieved.

REFERENCES

1. G. L. Schnable, W. Kern, and R. B. Comizzoli, "Passivation Coatings on Silicon Devices," paper presented at the Fall Meeting of the Electro-Chemical Society, New York, N.Y., October 17, 1974 (Abstract No. 215); ECS Ext. Abstr. 74-2, 528-530 (1974), published in the J. Electrochem. Soc. 122, 1092 (August 1975), and included herein as Appendix A.

2. C. F. Powell, J. H. Oxley, and J. M. Blocher, Jr., Eds., *Vapor Deposition*, (John Wiley & Sons, New York, 1966).

3. W. M. Feist, S. R. Steele, and D. W. Ready, "The Preparation of Films by Chemical Vapor Deposition," in *Physics of Thin Films*, Vol. 5, G. Hass and R. E. Thun, Eds., (Academic Press, New York and London, 1969), pp. 237-314.

4. D. S. Campbell, "The Deposition of Thin Films by Chemical Methods," in *Handbook of Thin Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw-Hill Book Company, New York, 1970), pp. 5-1 to 5-25.

5. J. A. Amick and W. Kern, "Chemical Vapor Deposition Techniques for the Fabrication of Semiconductor Devices," in *Chemical Vapor Deposition*, J. M. Blocher, Jr. and J. C. Withers, Eds. - Second Intn'l Conf., The Electrochem. Soc., Inc., New York (1970), pp. 551-570.

6. T. L. Chu, "Dielectric Materials in Semiconductor Devices," J. Vac. Sci. Technol. 6, 25 (1970).

7. RCA Review, Special Issue: *Chemical Vapor Phase Deposition of Electronic Materials*, RCA Review 31, No. 4 (1970).

8. E. L. MacKenna, "Chemical Vapor Deposited Dielectrics - Properties and Deposition Methods," Proc. 1971 Semicond./IC Proc. and Prod. Conf., pp. 71-83, Ind. and Sci. Conf. Management, Chicago, Ill. (1971).

9. *Chemical Vapor Deposition* (International Conferences): J. M. Blocher, Jr. and J. C. Withers, Eds. - Second Intn'l Conf., The Electrochem. Soc., Inc., New York (1970); F. A. Glaski, Ed. - Third Intn'l Conf., The American Nuclear Society, Hinsdale, Ill., (1972); G. F. Wakefield and J. M. Blocher, Jr., Eds. - Fourth Intn'l Conf., The Electrochem. Soc., Inc., Princeton, N.J. (1973).

10. T. L. Chu and R. K. Schmeltzer, "Recent Advances in the Chemical Vapor Growth of Electronic Materials," J. Vac. Sci. Technol. 10, 1 (1973).

11. J. J. Tietjen, "Chemical Vapor Deposition of Electronic Materials," in *Ann. Rev. Matl. Sci.*, Vol. 3, R. A. Huggins, R. H. Bube, and W. Roberts, Eds., (published by Annual Reviews, 1973), pp. 317-326.

12. N. Goldsmith and W. Kern, "The Deposition of Vitreous Silicon Dioxide Films from Silane," RCA Review 28, 153 (1967).

13. H. J. Emeleus and K. Stewart, "Oxidation of the Silicon Hydrides," J. Chem. Soc. (London), Part I, 1182 (1935).

14. T. L. Chu, J. R. Szedon, and G. A. Gruber, "Silica Films by the Oxidation of Silane," Trans. Met. Soc. AIME 242, 532 (1968).

15. K. Strater, "Controlled Oxidation of Silane," RCA Review 29, 618 (1968).

16. B. J. Baliga and S. K. Ghandhi, "Growth of Silica and Phosphosilicate Films," J. Appl. Phys. 44, 990 (1973).

17. W. Kern and R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Semiconductor Devices," Electrochem. Soc. Ext. Abstr. 5, No. 1, pp. 234-235 (Spring 1968).

18. A. W. Fisher, J. A. Amick, H. Hyman, and J. H. Scott, Jr., "Diffusion Characteristics and Applications of Doped Silicon Dioxide Layers Deposited from Silane (SiH_4)," RCA Review 29, 533 (1968).

19. A. W. Fisher and J. A. Amick, "Diffusion Characteristics of Doped Silicon Dioxide Layers Deposited from Pre-Mixed Hydrides," RCA Review 29, 549 (1968).

20. K. Strater and A. Mayer, "Oxidation of Silane, Phosphine and Diborane During Deposition of Doped-Oxide Diffusion Sources," in *Semiconductor Silicon*, R. R. Haberecht and E. L. Kern, Eds., (The Electrochem. Soc., Inc., New York, 1969), pp. 469-480.

21. T. Tokuyama, T. Miyazaki, and M. Horiuchi, "Low-Temperature-Deposited Glass for Passivation of Semiconductor Devices," in *Thin Film Dielectrics*, F. Vratny, Ed., (The Electrochem. Soc., Inc., New York, 1969), pp. 297-326.

22. W. Kern and R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Use with Silicon Devices - I. Deposition Techniques," J. Electrochem. Soc. 117, 562 (1970).

23. W. Kern and R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Use with Silicon Devices - II. Film Properties," J. Electrochem. Soc. 117, 568 (1970).

24. W. Kern and A. W. Fisher, "Deposition and Properties of Silicon Dioxide and Silicate Films Prepared by Low-Temperature Oxidation of Hydrides," RCA Review 31, 715 (1970).

25. M. M. Schlacter, E. S. Schlegel, R. S. Keen, R. A. Lathlaen, and G. L. Schnable, "Advantages of Vapor-Plated Phosphosilicate Films in Large-Scale Integrated Circuit Arrays," IEEE Trans. Electron Devices ED-17, 1077 (1970).

26. G. L. Schnable, "Glass Passivation of Integrated Circuits by Chemical Vapor Deposition of Oxide Films," IEEE 1971 Intn'l Conv. Digest, pp. 586-587 (1971).

27. J. L. Vossen, A. W. Stephens, and G. L. Schnable, "Bibliography on Metallization Materials and Techniques for Silicon Devices," Monograph #2, Thin Film Division, American Vacuum Society (1974).

28. W. Kern, "Densification of Chemically Vapor Deposited Borosilicate Glasses," J. Electrochem. Soc. 116, 251C (Abstract) (1969).

29. W. Kern, "A Technique for Measuring Etch Rates of Dielectric Films," RCA Review 29, 557 (1968).

30. M. L. Hammond and G. M. Bowers, "Preparation and Properties of SiO_2 Films Deposited from SiH_4 and O_2," Trans. Met. Soc. AIME 242, 546 (1968).

31. M. Shibata and K. Sugawara, "Deposition Rate and Phosphorus Concentration of Phosphosilicate Glass Films in Relation to $O_2/SiH_4 + PH_3$ Mole Fraction," J. Electrochem. Soc. 122, 155 (1975).

32. A. Mayer, K. Strater, and D. A. Puotinen, *Manufacturing Techniques for Controlled Deposition and Application of Doped Oxides*, Tech. Rpt. AFML-70-TR-191 (September 1970).

33. M. Shibata, T. Yoshimi, and K. Sugawara, "Deposition Rate and Phosphorus Concentration of Phosphosilicate Glass Films in Relation to $PH_3/SiH_4 + PH_3$ Mole Fraction," J. Electrochem. Soc. 122, 157 (1975).

34. W. Kern, J. L. Vossen, and G. L. Schnable, "Improved Reliability of Electron Devices Through Optimized Coverage of Surface Topography," 11th Ann. Proc. Reliability Physics, (IEEE, New York, 1973), pp. 214-223.

35. W. Kern, "Chemical Vapor Deposition Techniques for Glass Passivation of Semiconductor Devices," Proc. IEEE 1975 National Aerospace and Electronics Conf., NAECON '75 Record, pp. 93-100 (IEEE Cat. No. 75CH0956-3-NAECON).

36. D. S. Campbell, "Mechanical Properties of Thin Films," in *Handbook of Thin Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw-Hill Book Company, New York, 1970), pp. 12-3 to 12-50.

37. R. W. Hoffman, "The Mechanical Properties of Thin Condensed Films," in *Physics of Thin Films*, Vol. 3, G. Hass and R. E. Thun, Eds., (Academic Press, New York and London, 1966), p. 211.

38. R. Lathlaen and D. A. Diehl, "Stress in Thin Films of Silane Vapor-Deposited Silicon Dioxide," J. Electrochem. Soc. 116, 920 (1969).

39. R. Glang, R. Holmwood, and R. Rosenfeld, "Determination of Stress in Films on Single Crystalline Silicon Substrates," Rev. Sci. Instr. 36, 7 (1965).

40. H. Sunami, Y. Itoh, and K. Sato, "Low Stress CVD Glass Films in Multilevel Interconnection," Proc. 2nd Conf. Solid State Dev., Tokyo, 1970; Suppl. to J. Japan. Soc. Appl. Phys. 40, 67 (1971).

41. M. L. Barry, "A Continuous Process for the Deposition of Silicon Oxide of Silane," in *Chemical Vapor Deposition,* J. M. Blocher, Jr., and J. C. Withers, Eds. - Second Intn'l Conf., The Electrochem. Soc., New York (1970), pp. 595-617.

42. H. Sunami, Y. Itoh, and K. Sato, "Stress and Thermal Expansion Coefficient of Chemical-Vapor-Deposited Glass Films," J. Appl. Phys. 41, 5115 (1970).

43. P. B. Ghate and L. H. Hall, "Internal Stresses in Multilayered Structures," J. Electrochem. Soc. 119, 491 (1972).

44. R. Jaccodine and W. Schlegel, "Measurements of Strain at Si-SiO_2 Interface," J. Appl. Phys. 37, 2429 (1966).

45. W. A. Pliskin, "Use of Infrared Spectroscopy for Characterization of Dielectric Films in Silicon," in *Semiconductor Silicon 1973*, H. R. Huff and R. R. Burgess, Eds., (The Electrochem. Soc., Princeton, NJ, 1973), pp. 506-529.

46. B. Swaroop, "Low-Temperature Densification of Silica Films," in *Thin Film Dielectrics*, F. Vratny, Ed., (The Electrochem. Soc., New York, 1969), pp. 407-431.

47. B. E. Deal, E. L. MacKenna, and P. L. Castro, "Characteristics of Fast Surface States Associated with SiO_2-Si and Si_3N_4-SiO_2-Si Structures," J. Electrochem. Soc. 116, 997 (1969).

48. W. Kellner and A. Goetzberger, "Current Gain in Silicon Nitride Passivation Planar Transistors by Hydrogen Implantation," IEEE Trans. Electron Devices ED-22, 531 (1975).

49. E. P. EerNisse and C. B. Norris, "Introduction Rates and Annealing of Defects in Ion-implanted SiO_2 Layers on Si," J. Appl. Phys. 45, 5196 (1974).

50. I. J. Hodgkinson and A. R. Walker, "Stress Relief Induced in Oxide Films by Ultraviolet Radiation," Thin Solid Films 17, 185 (1973).

51. D. R. Kerr, J. S. Logan, P. J. Burkhardt, and W. A. Pliskin, "Stabilization of SiO_2 Passivation Layers with P_2O_5," IBM J. Res. Develop. 8, 376 (1964).

52. P. Balk and J. M. Eldridge, "Phosphosilicate Glass Stabilization of FET Devices," Proc. IEEE 57, 1558 (1969).

53. J. M. Eldridge and D. R. Kerr, "Sodium Ion Drift through Phosphosilicate Glass-SiO_2 Films," J. Electrochem. Soc. 118, 986 (1971).

54. E. H. Snow and B. E. Deal, "Polarization Phenomena and Other Properties of Phosphosilicate Glass Films on Silicon," J. Electrochem. Soc. 113, 263 (1966).

55. J. M. Eldridge, R. B. Laibowitz, and P. Balk, "Polarization of Thin Phosphosilicate Glass Films in MGOS Structures," J. Appl. Phys. 40, 1922 (1969).

56. L. Kasprzak and A. Hornung, "Polarization and Depolarization in PSG Films," IBM J. Res. Develop. 19, 127 (1975).

57. L. K. Karstadt, W. G. Burger, C. M. Hsieh, and W. A. Cosgrove, "Large IC Chip Impact Analysis and Handling Protection," Solid State Tech. 16, No. 8, 41 (1973).

58. W. McQuitty and C. R. Lively, "IC Failure and the Packaging Process," Electronic Packaging and Production 11, No. 11, 112 (November 1971).

59. T. W. Hickmott, "Effect of Bombardment by Glass-forming Ions on Thermally Stimulated Ionic Conductivity of Sodium in SiO_2," Phys. Rev. Letters 32, 65 (1974).

60. W. Shockley, W. W. Hooper, H. J. Queisser, and W. Schroen, "Mobile Electric Charges on Insulating Oxides with Application to Oxide Covered Silicon p-n Junctions," Surface Science 2, 277 (1964).

61. E. S. Schlegel, G. L. Schnable, R. F. Schwarz, and J. P. Spratt, "Behavior of Surface Ions in Semiconductor Devices," IEEE Trans. Electron Devices ED-15, 973 (1968).

62. E. S. Schlegel and G. L. Schnable, "The Application of Test Structures for the Study of Surface Effects in LSI Circuitry," IEEE Trans. Electron Devices ED-16, 386 (1969).

63. E. S. Schlegel, R. S. Keen, and G. I. Schnable, "The Effects of Insulator Surface-Ion Migration on MOS and Bipolar Integrated Circuits," 8th Ann. Proc. Reliability Physics, (IEEE, New York, 1971), pp. 9-16.

64. R. Castagne, P. Hesto, and A. Vapaille, "Surface Conductivity of the Insulator of an MIS or MIM Device," Thin Solid Films 17, 253 (1973).

65. G. A. Brown, K. Lovelace, and C. Hutchins, "A Process Control Test for Lateral Charge Spreading Susceptibility," 11th Ann. Proc. Reliability Physics, (IEEE, New York, 1973), pp. 203-207.

66. R. S. Alwitt, "The Growth of Hydrous Oxide Films on Aluminum," J. Electrochem. Soc. 121, 1322 (1974).

67. S. C. Kolesar, "Principles of Corrosion," 12th Ann. Proc. Reliability Physics, (IEEE, New York, 1974), pp. 155-167.

68. H. Koelmans, "Metallization Corrosion in Silicon Devices by Moisture-Induced Electrolysis," 12th Ann. Proc. Reliability Physics, (IEEE, New York, 1974), pp. 168-171.

69. W. M. Paulson and R. W. Kirk, "The Effects of Phosphorus-Doped Passivation Glass on the Corrosion of Aluminum," 12th Ann. Proc. Reliability Physics, (IEEE, New York, 1974), pp. 172-179.

70. W. Kern, "Apparatus for Chemical Vapor Deposition of Oxide and Glass Films," RCA Review 29, 525 (1968).

71. M. Kuhn and D. J. Silversmith, "Ionic Contamination and Transport of Mobile Ions in MOS Structures," J. Electrochem. Soc. 118, 966 (1971).

72. P. F. Schmidt, W. VanGelder, and J. Drobek, "Phosphorus Concentration Profile and Phase Segregation in Phosphosilicate Glass on SiO_2 Films," J. Electrochem. Soc. 115, 79 (1968).

73. J. Sato, Y. Ban, and K. Maeda, "Durability and Stability of Various Insulating Films against the High Temperature in an Autoclave," 9th Ann. Proc. Reliability Physics, (IEEE, New York, 1971), pp. 96-106.

74. N. Nagasima, H. Suzuki, K. Tanaka, and S. Nishida, "Interaction between Phosphosilicate Glass Films and Water," J. Electrochem. Soc. 121, 434 (1974).

75. V. Y. Doo and V. M. L. Sun, "Pinholes in Pyrolytic Oxide Deposited on Silicon and Metals," Metallurg. Trans. 1, 741 (1970).

76. W. C. Benzing, R. S. Rosler, and R. W. East, "A P oduction Reactor for Continuous Deposition of Silicon Dioxide," Solid State Technology, 16, No. 11, 37 (1973).

77. G. L. Schnable and R. S. Keen, "On Failure Mechanisms in Large-Scale Integrated Circuits," in *Advances in Electronics and Electron Physics*, Vol. 30, L. Marton, Ed., (Academic Press, New York, 1971), pp. 79-138.

78. V. C. Kapfer and J. J. Bart, "Thin Film Nickel-Chromium Resistor Failures in Integrated Circuits," 10th Ann. Proc. Reliability Physics, (IEEE, New York, 1972), pp. 175-182.

79. W. F. Keenan and W. R. Runyan, "Nickel-Chromium Resistor Failure Modes and their Identification," Microelectron. and Reliability 12, 125 (1973).

80. P. B. Mee, "Microscopy and Its Contribution to Computer Technology," Honeywell Computer Journal 7, 115 (1973).

81. G. H. Ebel and H. A. Engelke, "Failure Analysis of Oxide Defects," 11th Ann. Proc. Reliability Physics, (IEEE, New York, 1973), pp. 108-116.

82. W. Kern, "Detection and Characterization of Localized Defects in Dielectric Films," RCA Review 34, 655 (1973); also, Solid State Technology 17, No. 3, 35 (1974) and No. 4, 78 (1974).

83. W. W. Binger, E. H. Hollingsworth, and D. O. Sprowls, "Resistance to Corrosion and Stress Corrosion," in *Aluminum, Properties, Physical Metallurgy and Phase Diagrams*, Vol. 1, K. R. Van Horn, Ed., (Amer. Soc. for Metals, Metals Park, Ohio, 1967), pp. 209-276.

84. P. F. Kane and G. B. Larrabee, *Characterization of Semiconductor Materials*, (McGraw-Hill Book Co., New York, 1970).

85. P. F. Kane and G. B. Larrabee, "Trace Analysis Techniques for Solids," in *Annual Review of Materials Science*, Vol. 2, (1972), pp. 33-65.

86. *Handbook of Thin Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw-Hill Book Co., New York, 1970).

87. *Thin Film Dielectrics*, F. Vratny, Ed., (The Electrochemical Society, New York, 1969).

88. J. W. Coburn and E. Kay, "Techniques for Elemental Composition Profiling in Thin Films," in *Critical Reviews in Solid State Sciences*, September 1974, pp. 561-590.

89. W. A. Pliskin and R. P. Gnall, "Evidence for Oxidation Growth at the Oxide-Silicon Interface from Controlled Etch Studies," J. Electrochem. Soc. 111, 872 (1964).

90. W. A. Pliskin, "Fused Glass Penetration into Thermally Grown Silicon Dioxide Films," J. Electrochem. Soc. 114, 620 (1967).

91. G. DiGiacomo, "Microprobe Technique for Determination of Thickness and Phosphorus Concentration of Gate Oxide Phosphosilicate Glass in FET Devices," J. Electrochem. Soc. 121, 419 (1974).

92. D. F. Stein, "Applications of Auger Spectroscopy to Materials Research," J. Vac. Sci. Technol. 12, No. 1, 268 (1975).

93. C. A. Evans, Jr., "Thin Film Compositional Analysis - A Comparison of Techniques," J. Vac. Sci. Technol. 12, No. 1, 144 (1975).

94. I. Fränz and W. Langheinrich, Solid State Electronics 18, 209 (1975).

95. J. A. Keenan, "Computer-Coupled System for X-Ray Fluorescence Analysis," American Laboratory 7, No. 2, 23 (1975).

96. E. P. Bertin, *Principles and Practice of X-Ray Spectrometric Analysis*, (Plenum Press, New York, 1975).

97. W. A. Pliskin and S. J. Zanin, "Film Thickness and Composition," in *Handbook of Thin-Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw-Hill Book Co., New York, 1970), pp. 11-1 to 11-54.

98. J. V. Gilfrich, "X-Ray Fluorescence Analysis," in *Characterization of Solid Surfaces*, P. F. Kane and G. B. Larrabee, Eds., (Plenum Press, New York, 1974), pp. 275-306.

99. L. A. Winger and E. L. McKinley, "Chemical Analysis of Refractories by X-Ray Fluorescence of Glass Pellets," Ceramic Bull. 53, 638 (1974).

100. F. X. Pink and V. Lyn, "Non-destructive Determination of Phosphorus in Phospho-Silica Films on Silicon Substrates," Electrochem. Technol. 6, 258 (1968).

101. W. Kern, "Recent Trends in Determining Composition and Imperfections of Dielectric Films," T. D. Callinan Award Address, Electrochem. Soc. Mtg., Houston, Texas, May 1972.

102. E. A. Corl, S. L. Silverman, and Y. S. Kim, "Non-Destructive Detection of Phosphorus Oxide Layers on Semiconductor Wafers," Solid-State Electron. 9, 1009 (1966).

103. R. P. Esch, J. M. Eldridge, P. Balk, and W. A. Pliskin, "Quantitative Determination of Phosphorus in Thin Phosphosilicate Films," Abstract No. 95, Electrochem. Soc. Meeting, Detroit, Fall 1969.

104. A. S. Tenney and M. Ghezzo, "Composition of Phosphosilicate Glass by Infrared Absorption," J. Electrochem. Soc., 120, 1276 (1973).

105. W. Kern, "Infrared Spectroscopic Method for Compositional Determination of Vapor Deposited Borosilicate Glass Films and Results of its Application," RCA Review 32, 429 (1971).

106. E. A. Corl and W. E. Reese, "Infrared Adsorption Characteristics of Soluble and Insoluble Phosphorus-Bearing Oxide Layers," Metallurg. Trans. 1, 747 (1970).

107. W. Kern, "Radiochemical Studies of Semiconductor Surface Contamination - I. Adsorption of Reagent Components," RCA Review 31, 207 (1970).

108. W. Kern, "Radiochemical Studies of Semiconductor Surface Contamination -. II. Deposition of Trace Impurities on Silicon and Silica," RCA Review 31, 234 (1970).

109. W. Kern, "Semiconductor Surface Contamination Investigated by Radioactive Tracer Techniques," Solid State Technology 15, No. 1, 34, and No. 2, 39 (1972).

110. W. Kern and D. Puotinen, "Cleaning Solutions Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology," RCA Review 31, 187 (1970).

APPENDICES

NOTE TO READER:

The paper below, included herein as Appendix A, has been published in the August issue of the *Journal of the Electrochemical Society*, Vol. 122, pp. 1092-1103. It is reprinted in this report because it is pertinent to the contract and includes a substantial bibliography on the subject of passivation coatings.

APPENDIX A

Passivation Coatings on Silicon Devices

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ABSTRACT

Passivation coatings are widely used to improve the performance and reliability of silicon devices of various types, ranging from discrete mesa-type diodes and transistors to complex planar silicon integrated circuits, and including both hermetic and plastic-encapsulated devices. This paper reviews the materials and techniques used to apply passivation coatings to completed silicon devices. Principal production techniques used in passivation of silicon devices include thermal oxidation, high-temperature diffusion, high-temperature chemical vapor deposition of Si_3N_4 or Al_2O_3, low-temperature chemical vapor deposition of glasslike SiO_2 or phosphosilicate layers (deposited at approximately 400°C), rf sputtering of SiO_2, mechanical deposition of glass frit layers which are subsequently fused, and application of organic polymer films.

The effects of passivation layers on silicon device reliability are discussed, and the interrelationships among the silicon device, the passivation layer or layers used and the final encapsulation are indicated. Pertinent references on passivation and on related topics are cited in the text.

Passivation coatings are widely used to improve the performance and reliability of silicon devices of various types, ranging from discrete mesa-type diodes and transistors to complex planar integrated circuits, and including both hermetic and plastic-encapsulated devices. This paper outlines the materials and techniques used in the semiconductor device industry to achieve silicon device passivation.

Passivation coatings may be classified as primary if they are directly in contact with the single-crystal silicon from which the device is fabricated, and as secondary if they are separated from the silicon by an underlying dielectric layer. The function of the primary passivation layer is to provide good dielectric properties, low surface recombination velocity, controlled immobile charge density, and device stability at elevated temperatures under bias or operating conditions. The functions which are served by the secondary passivation layer are to provide additional stability in various ambients, in both production and use, and to serve as getter, impurity barrier, or mechanical shield.

This paper reviews primary and secondary passivation materials and the techniques used to obtain them, including thermal oxidation, high-temperature diffusion, low-temperature deposition of SiO_2 and binary silicates, deposition of alkali barrier-type layers, and deposition of glass frit or application of preforms followed by fusion. The effect of passivation layers on silicon device reliability is discussed, and the interrelationship among the techniques used for final encapsulation, the passivation layers used, and device reliability is indicated. Emphasis is given to those proc-

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Key words: silicon device passivation, silicon dioxide, glass passivation, phosphosilicate glass, silicon device reliability.

esses and materials which have been widely used to fabricate semiconductor devices in production, rather than to processes used only to fabricate exploratory developmental devices. A total of 363 references (listed alphabetically) have been cited to indicate the type of information which has been published on passivation layers and on related topics (1-363).

Thermally Grown Silicon Dioxides

The most commonly used primary passivation material is thermally grown SiO_2, with thickness ranging typically from 0.5 to 1.5 μm. In addition to passivation, two other very important functions of thermal oxides on silicon wafers are to serve as diffusion masks, and to serve as the insulator between the expanded metallization pattern and the underlying silicon in planar devices. Thermally grown oxides are prepared by high-temperature oxidation, at atmospheric pressure, of silicon wafers in atmospheres of dry oxygen, wet oxygen, or steam (11, 70, 114, 259, 72, 226, 348). For surface-sensitive devices, oxidation is frequently followed by one or more annealing steps (heat-treatments) in appropriate nonoxidizing atmospheres to improve the electrical properties of the Si-SiO_2 interface (259, 47, 220, 361, 307).

The cleanliness of the silicon surface is of great practical importance in device processing. Organic and inorganic surface contaminants (159, 149, 150, 137, 199, 152) are frequently introduced during many of the wafer processing steps and must be removed effectively to achieve high-quality oxide layers and interfaces. Decontamination is especially important just prior to heat-treatments and can be carried out by wet chemical methods (159, 124, 213).

The presence of alkali ions in thermally grown SiO_2 can result in device instability (296, 130, 114, 236, 173). Also alkali ions are undesirable because they can lead to devitrification of SiO_2 (202, 224, 212) and are a factor in SiO_2 dielectric breakdown (346, 83, 233). Accordingly, precautions are taken to minimize the level of alkali ion contamination during oxidation, and in some cases subsequent treatments are used to remove alkali ions (206). Whatever the process used, the results achieved are readily monitored by measuring stability of capacitance-voltage curves of metal-oxide-silicon capacitors subjected to bias at an elevated temperature (114, 362, 72, 226) such as 300°C.

In recent years, the technique of oxidation in atmospheres containing a small percentage of HCl (or Cl_2) has been widely used to getter alkali ions, thereby producing thermally grown oxides with very low levels of alkali ion contamination (260, 171, 172, 184, 231, 335, 173). The HCl gettering process, in addition to gettering alkali ions from SiO_2, also removes fast-diffusing interstitial contaminants from silicon, thus increasing bulk lifetime (260, 261, 53) and improving device properties (50, 192).

The thermally grown layer, which is amorphous, may be pure SiO_2, may contain boron if formed by oxidation of a boron-doped region (115), may contain hydroxyl if prepared by wet oxidation (25), or may contain chlorine if prepared using a chlorine-containing oxidizing ambient (211, 52, 334).

A very large body of literature exists concerning thermal oxides on silicon (11, 259, 226, 74, 334) and on the effects of oxidation conditions on the electrical properties and stability of the Si-SiO_2 interface (259, 71, 163, 72-74, 227). This information, to a large extent generated in connection with studies of MOS devices (270-272, 3), is applicable to a wide variety of oxide-passivated silicon devices. Considerable information has also been published on the radiation hardness of various types of SiO_2 (353, 132, 112). Accordingly, SiO_2 primary passivation phenomena will not be treated in detail in this paper. The ambient and temperature during application, or during subsequent fusion or heat-treatment of the secondary passivating layer may, however, modify the electrical properties of the Si-SiO_2 interface, including the mobile and immobile charge density and the fast surface-state density (75, 294, 309, 274, 76, 193, 361, 16). While this is particularly true of high-temperature depositions or heat-treatments (temperatures greater than approximately 800°C), it also occurs to some extent during low-temperature deposition processes [performed at 450°C or lower (274)].

Sequence of Application of Dielectric Layers

Figure 1 shows the sequence of application of passivation layers to various types of silicon devices. Passivation coatings may be applied before or after metallization, depending on the type of device. Some devices contain several different types of passivation layers, each having specific functions.

Table I, II, and III show some of the physical properties of commonly used passivation materials. Single-crystal silicon, thermally grown silicon dioxide, aluminum, and gold are included for comparison purposes.

Considerable information exists on the properties and stability of double dielectric structures such as MNOS memory devices (55, 272, 3, 16, 349). In such structures, the second dielectric layer serves primarily as part of the active device rather than as a secondary passivation layer, and thus is not considered in this paper.

Thermal oxides which have served as high-temperature diffusion masks will have an overlying layer of borosilicate glass and/or phosphosilicate glass. In NPN bipolar transistors and bipolar IC's, the thin layer of phosphosilicate glass (EPSG), formed on the surface of the thermally grown SiO_2 during emitter diffusion, remains on the device and serves as a getter for alkali ions present at that point (164) or introduced during later processing steps. In some processes, a phosphosilicate glass (206) or emitter diffusion layer (phosphorus-doped) (42) is used to getter alkali, and is subsequently removed by etching.

A very thin phosphosilicate layer has also been applied over gate oxides of some MOS transistors and IC's for gettering purposes (17, 266, 91, 141). Typically, this is accomplished at approximately 800°C using a diffusion source such as $POCl_3$. (Gettering of alkali

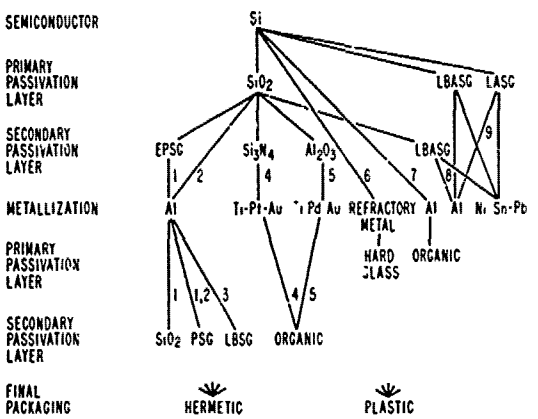

Fig. 1. Sequence of application of passivation layers to various types of silicon devices. Typical devices made by the sequences indicated by numbers are as follows: 1, NPN transistors, digital and linear bipolar IC's; 2, MOS transistors, p-channel MOS IC's, CMOS; 3, face-bonded chips; 4, beam-lead sealed-junction bipolar devices, plastic encapsulated Au-metallized devices; 5, beam-lead sealed-junction MOS IC's; 6, axial-lead diodes; 7, high-power diodes, high-power transistors, thyristors, devices with beveled junction; 8, high-voltage devices, high-voltage power devices; 9, high-voltage devices. Designations for glasses are as follows: EPSG, phosphosilicate glass formed by NPN bipolar transistor emitter diffusion; LASG, lead aluminosilicate glass; LBASG, lead boroaluminosilicate glass; LBSG, lead borosilicate glass; PSG, phosphosilicate glass.

Table I. Growth and properties of typical low-temperature passivation materials. Some of the properties of thermally grown SiO_2 are given for comparison purposes.

Film type	Source material	Growth temperature, °C	Growth rate, Å-min^{-1}	Film composition	Melting range, °C	IR band maxima, μm	Etch rate,* Å-sec^{-1}
Sputtered SiO_2	SiO_2	100-450	50-200	SiO_2	1600-1700	9.3-9.5	4-12
CVD SiO_2	$SiH_4 + O_2$	325-475	500-5000	SiO_2	1600-1700	9.3	16-20
CVD PSG	$PH_3 + SiH_4 + O_2$	350-450	1000-4000	3 m/o P_2O_5 (3 w/o P) in P_2O_5-SiO_2	900-1000	7.6, 9.3	40-50
CVD BSG	$B_2H_6 + SiH_4 + O_2$	400-450	1000-4000	17 m/o B_2O_3 in B_2O_3-SiO_2	850-950	7.4, 9.3	50-70
Thermal SiO_2	$Si + H_2O$	900-1250	17-170	SiO_2	1600-1700	9.2	1.8-2.0

* P-etch, 25.0°C: $2HNO_3.3HF.60\ H_2O$.

ions from thermally grown SiO_2 by an overlying phosphosilicate layer involves a different mechanism than the high-temperature process of gettering of interstitial impurities such as Au, Cu, Fe, and Ni from Si by phosphosilicate glasses in direct contact with silicon.) Where PSG is used over the gate oxide of MOS devices (under the gate metal), close control of the P-concentration and layer thickness is required to avoid undesirable polarization effects (293, 294, 92, 82).

For MOS and PNP bipolar transistor applications in which an underlying high-temperature phosphosilicate glass is not present, special precautions are taken to insure that deposited films do not contain alkali. For example, deposited Al metal must be alkali-free.

Thermally grown SiO_2 is not used for passivation of some discrete devices, particularly high-voltage devices, because of drift effects and high, immobile charge density. Primary passivation in these devices is achieved by use of a silicate glass or an organic polymer coating. When an organic polymer is applied directly to a silicon surface, it must be recognized that real silicon surfaces contain a native SiO_2 layer (9, 135) on the order of 20Å thick. The exact nature of the processing prior to application of the polymer material and of the polymer itself (135, 190) are significant factors in determining initial device properties, and also device stability.

With both Al- and Au-based metallization systems, the maximum temperature which can be used in processing after metallization is limited by the melting point of the eutectic formed between silicon and the metallization (the Al-Si eutectic temperature is 577°C; the Au-Si eutectic is 370°C) rather than the melting point of the metal itself.

Deposited Thin-Film SiO_2 and Silicates

With IC's and small-signal planar transistors, a secondary passivation coating is applied to completed devices after Al metallization (147, 197, 34, 275, 278, 142). Originally, functions of the deposited layer were to provide resistance to scratching of the metallization pattern during chip handling (142), and to provide immunity to effects of loose conductive particles in hermetic packages. It was subsequently realized that additional benefits could accrue from these coatings. These benefits include reduced effects of ion motion on the surface (273, 275, 280), lower susceptibility to metal corrosion (215, 275), decreased susceptibility of metal stripes to electromigration failure (31, 297, 32, 81), improved stability and reliability of thin-film resistors (144, 342, 234), and alkali-gettering capability in the case of phosphosilicate glasses (PSG). Anodic Al_2O_3 has also been reported to reduce susceptibility of Al metallization to electromigration (180, 77, 178, 263, 81).

Silicon devices in hermetically sealed packages are susceptible to the effects of loose conducting particles in the package (209, 207, 101) unless the devices are coated with a dielectric. In Al-metallized devices, deposited SiO_2 or PSG is quite effective. In Au-metallized devices, organic coatings are generally used (345, 239) since deposited oxides have low adhesion to gold (63).

Most commonly, chemical vapor deposition (CVD) of SiO_2 on Al-metallized circuits is accomplished at atmospheric pressure at a temperature of approximately 400°C using SiH_4 plus excess O_2 in N_2 as carrier (106, 145, 301, 147, 6, 19, 155, 191, 15, 27, 360, 154); PSG and BSG (borosilicate glass) are deposited using, respectively, PH_3- and B_2H_6-containing mixtures under similar conditions (321, 147, 157, 6, 155, 269, 275, 191, 15, 27, 360, 286, 287, 154). Typically, CVD layers are on the order of 1 μm thick. Tetraethyl orthosilicate (TEOS) has also been used as a source for CVD of SiO_2 (6). CVD SiO_2 layers are in tensile intrinsic stress as deposited (303, 104). Because silicon has a higher coefficient of thermal expansion (CTE) than silicon dioxide, the residual stress in CVD SiO_2 films on Si at room temperature is somewhat lower than the intrinsic stress of films as deposited, but the films are still in considerable tension (175, 19, 302, 303) (see Table II).

Deposited SiO_2 or PSG films, when heated above the deposition temperature, are put in additional tension, particularly in regions over the edges of delineated Al metal films. Accordingly, there is some correlation between the intrinsic tensile stress in deposited films and the temperature increment above deposition temperature which can be attained before cracks begin to form (269, 303).

SiO_2 secondary passivation layers on Si wafers have also been obtained by rf sputtering (251, 61, 188, 99). The sputtering conditions can be adjusted to produce good coverage of topography (188, 339, 161) and to result in low stress (compressive) at room temperature (251, 325). Sputtering processes produce radiation damage in the thermally grown SiO_2 which can adversely affect sensitive devices such as MOS transistors and integrated circuits (251, 188, 58, 187, 205, 318, 204). Most, but not all of the radiation-induced charge can be annealed out by suitable heat-treatments. Techniques which reduce the amount of radiation damage during sputtering have recently been described (58, 187, 205, 318).

Layers of PSG have been widely used because they are in less stress (tensile) than layers of SiO_2 as deposited by CVD (269, 302, 235) and have the ability to getter alkali ions (269). PSG is thus particularly ad-

Table II. Stress in low-temperature deposited passivation layers. Some of the properties of thermally grown SiO_2 and of Si, Al, and Au are given for comparison purposes.

Material	CTE, ×10^{-6}/°C	Internal stress, dynes/cm^2 (350°-400°C)	Total stress on Si (at 25°C)	Total stress over Al edges (450°C)
CVD SiO_2	0.5	High T* ($1\text{-}2 \times 10^9$)	High T* ($0.5\text{-}2 \times 10^9$)	Very high T*
Sputtered SiO_2	0.5	Low	C**	T
CVD PSG	0.5	Moderate T	T	High T
Thermal SiO_2	0.5	—	C	—
Si	3.5	—	—	—
Al	26.0	Low	T	—
Au	15.0	—	—	—

* T = tensile.
** C = compressive.

vantageous for MOS devices, which are more surface sensitive than digital bipolar IC's.

CVD has been more widely used than rf sputtering for depositing layers of SiO_2, PSG, or BSG, because it is faster (see Table I), requires simpler equipment, and, in contrast to rf sputtering, produces no radiation damage in the thermally grown SiO_2.

Deposited SiO_2 or silicate films are sometimes densified by a heat-treatment in a suitable ambient to improve their properties (148, 305, 158). Higher phosphorus contents in the CVD PSG glass reduce intrinsic tensile stress (which tends to cause cracking) (269, 303, 235) and increase the alkali-ion gettering capability of the passivation layer. On the other hand, PSG layers with excessively high phosphorus concentration tend to be hygroscopic and may have poor stability in humid atmospheres (225). These effects can be reduced by depositing a thin SiO_2 layer over the PSG layer (158).

Excessively thin passivation layers tend to contain more pinholes than thicker layers (85) and are less effective in covering topography such as delineated metal lines. Also, any charges which move along the surface of the passivation layer are closer to the Si-SiO_2 interface and thus exert more influence on device characteristics (273). Thicker layers, however, are more likely to contain nodules and are more likely to crack.

The effectiveness of a passivation layer in providing protection against metallization scratches increases with increasing passivation layer thickness (277). It is possible to deposit and delineate crack-free BSG or PSG layers 3 μm thick (157, 158) which afford very good scratch protection. With thicker layers, it is necessary to deposit the layers under conditions in which stress is not excessive. Consideration must also be given to the effects of mismatches in thermal coefficients of expansion. Borosilicate containing 17 mole per cent (m/o) B_2O_3 approximates the linear coefficient of thermal expansion (CTE) of silicon (158). Crack-free layers of BSG over 10 μm in thickness can readily be obtained by CVD at 450°C (157, 158).

Regardless of deposited passivation layer thickness, layers of deposited dielectrics must be applied to properly cleaned wafers under suitable conditions to avoid metal penetration (20) and lateral charge spreading or lateral ion migration effects at the interface between thermally grown SiO_2 and deposited dielectric (273, 118, 280, 39).

There is some reaction of Al metal with SiO_2, BSG, or PSG at relatively low temperatures (289), such as 400°C (277, 232, 253). Thus, an intermediate aluminosilicate film forms during SiO_2 deposition. Subsequent high-temperature processing steps such as chip-to-header eutectic bonding and package sealing, particularly in frit-sealed ceramic packages, which are sealed at temperatures on the order of 500°C (200, 343), can cause additional Al-glass interaction. The Al-SiO_2 reaction tends to be accelerated at localized oxide defects and thus is dependent on oxide quality (51, 232).

Low-temperature deposited films of SiO_2, PSG, and BSG are amorphous. Delineation of deposited SiO_2 and PSG films (to expose bonding pads and open scribe lines) is accomplished using buffered hydrofluoric acid. Delineation of BSG films is preferably performed using unbuffered hydrofluoric acid mixtures because of the higher etch rate (158).

In Si-gate MOS IC's, CVD phosphosilicate is frequently used as the dielectric between polycrystalline silicon and overlying metal; in these devices it also serves as a passivation layer. In some cases the PSG layer is subjected to a heat-treatment at a temperature such as 1000°C to obtain some flow of the PSG (222, 161, 153, 340, 10).

Characterization of Dielectric Films

The characterization of dielectric films used in silicon device passivation is based both on standard chemical, physical, and electrical methods established for surface and thin-film analysis (198, 199, 138, 139) and on methods developed specifically for the analysis of thin dielectric films (341, 137). Special electrical methods include metal-insulator-semiconductor (MIS) measurements of the capacitance-voltage (C-V) relationship before and after bias heat-treatment (116, 296, 259, 362, 72). From these measurements one can calculate the density of electronic states, interface charges, and bulk charges, all of which play important roles in the electrical properties and stability of deposited dielectrics (296, 114, 294, 309, 226). Measurements of the sheet resistivity of a silicon wafer after heat-treatment at temperatures over 1000°C is often used to estimate the composition of a deposited binary oxide film from the resulting doping concentration in the silicon (18, 38, 10). X-ray fluorescence analysis (246, 306, 82), backscattering (186), and Auger electron spectroscopy (292) have been used to determine the composition of deposited dielectric films. Infrared spectroscopy has been used extensively for compositional and structural analysis of deposited SiO_2 (251, 305, 158, 264, 265, 151, 37, 223, 247), PSG (60, 158, 265, 37, 64, 317, 247, 286, 287), and BSG (251, 148, 158, 264, 151, 315, 37, 247, 8, 312) films. Chemical etch rate measurements have also been used to determine film composition and relative density for films as deposited (251, 146, 54, 321, 305, 158, 282, 120, 136, 110, 316) or after densification heat-treatment (321, 305, 158, 156). Moisture absorption and adsorption, and resistance of deposited dielectric films to moisture are important aspects of passivating films and have been examined by various authors (265, 151, 64, 8). Measurements of surface conductivity (46), stress (129, 268, 267, 175, 302, 303, 104, 331), and index of refraction (251, 106, 305, 158) of various deposited dielectrics have been reported. Methods for characterizing localized structural defects in dielectric films have been reviewed recently (153). Coverage of topography by deposited films is important for device reliability (107, 140, 161, 10, 179).

Alkali Barrier Layers

In some high-reliability devices, silicon nitride (Si_3N_4), which serves as both a getter and an effective alkali barrier (322, 65, 100, 41), is applied over the thermally grown SiO_2 prior to metallization. Aluminum oxide (Al_2O_3), which is also an alkali ion barrier (329, 330), has been used in some MOS devices (49, 174, 105). Examples of devices with ion barriers include nitride-passivated bipolar devices (195, 279); beam-lead sealed-junction devices (279, 239), and MNOS devices (262). Silicon nitride can also be deposited over refractory metals (160) such as W and Mo, or over the polycrystalline silicon used in silicon-gate MOS devices. A considerable amount of information has been published on deposition (54, 109, 87, 208, 191, 216, 347, 258) and properties (75, 54, 109, 344, 168, 87, 265, 216, 194, 347, 193) of Si_3N_4, and on device applications (322, 279, 262, 109, 78, 310, 337, 351, 196, 160, 355, 195, 125, 12).

Typically, Si_3N_4 layers are formed by reaction of SiH_4 or of $SiCl_4$ with excess NH_3 at temperatures of 800°-900°C at atmospheric pressure. Layer thicknesses of 0.1-0.2 μm are generally used as alkali barrier layers in bipolar devices. Al_2O_3 is prepared by CVD from $Al_2Cl_6 + H_2 + CO_2$ (328, 329, 86, 326) at approximately 900°C.

Delineation of Si_3N_4 or Al_2O_3 films is performed using hot (180°C) phosphoric acid (336). In MOS devices in which the Si_3N_4 is used under the gate metal, the thickness of the Si_3N_4 is on the order of 0.03-0.05 μm (262, 12). Both thickness and dielectric constant must be closely controlled in this type of MOS application.

Although defect-free silicon nitride layers are effective diffusion barriers, it must be recognized that many

nitride-passivated devices have exposed underlying thermal oxide at each contact cut and at the periphery of the chip. Although procedures exist for sealing the edges with nitride, this is frequently not done because of the additional process complexity and the chip area penalty involved. With unsealed oxide edges, lateral migration of alkali is possible, and has been shown to adversely affect silicon device reliability (208). While the effects of alkali ions on stability of threshold voltage of MOS devices have been the subject of many studies, it has also been clearly established that alkali ions can adversely affect bipolar devices (279, 310, 208, 195, 77).

Fused Glass Layers

Fused glass films are used on various device types. Table III shows the composition and properties of typical fused glasses used in silicon device passivation. Planar, aluminum-metallized IC's have made use of a thin (~1 μm) fused glass layer applied over metal (68, 69, 323). The high CTE permits only very thin layers, which can be applied by careful sedimentation of fine powder as is described later. Pinholes in the glass film on such devices can lead to metal corrosion (7). Power devices of planar or mesa structure often use fused glass as a direct passivant on the high-voltage junction (169, 126). Various techniques for high-voltage axial-lead diode passivation make use of beads of fused glass powder (79, 80), glass sleeves with metal studs (56, 44), or glass sleeves with glass beads as end seals (67).

The composition of glass used to form fused layers for device passivation depends on the device processing restrictions and designed operating characteristics. Important properties of the starting glass are particle size (in the case of powders), fusion temperature, and melt viscosity. For the fused layer, the important properties are chemical durability, CTE, and dielectric properties, in particular, ionic mobility at intended device operating temperature. Since the CTE increases and chemical durability decreases with decreasing fusion temperature, tradeoffs based on device processing requirements and intended use must be made (214, 354). As an example, low melting glasses used over aluminum can be applied in thicknesses of only a few microns (242).

Because of their good chemical stability, lead oxide-containing glasses are widely used, but the high ionic mobility of the lead ion above about 125°C in some glasses of this type limits device operating temperature (162, 295, 40, 290). For example, lead aluminosilicate glasses (LASG) are used in mesa grooves for thyristor and other high power device passivation (351, 352, 62) where device operating temperature of 125°C is sufficient. The low CTE of such glasses permits the application of thick layers directly on silicon in the grooves (355, 356), and the chemical stability permits contact etching and nickel plating of the device after high-temperature fusion (~900°C) of the glass powder. The addition of boron oxide (LBASG) (40, 221, 357) permits further decrease of ionic mobility and also of fusion temperature (to about 700°C), rendering the glass suitable for use on higher operating temperature devices (88), such as power transistors. However, CTE is increased (see Table I). ZnO is usually added to such glasses (LAZBSG) to moderate the CTE increase. With boron-containing glass of high fusion temperature (≥900°C), it is not possible to fuse the glass directly on the silicon because of doping effects. An intermediate SiO_2 barrier layer is then necessary. Glasses with ZnO and B_2O_3 as major constituents have higher device operating temperature capability because of reduced ionic mobility (162, 45, 221). In some cases, however, reduced chemical resistance of such glasses limits subsequent processing options.

For scratch and ambient protection over metallization on planar IC's and small-signal transistors, where the glass is applied over the entire wafer, the glass must fuse at a temperature compatible with the metallization. This is an important restriction in the case of Al metallization since, as previously indicated, the Al-Si system forms a eutectic melting at 577°C. Also the low-melting glasses used have a high CTE, and therefore, to avoid cracking, only very thin layers can be used (240, 242, 133, 325, 88, 125).

Depending on thickness desired, the powdered glass may be deposited by several methods. For thin, pinhole-free films on the order of 1 or 2 μm thickness, sedimentation in a centrifuge is suitable. Procedures for dispersing the glass powder in the suspending liquid and choice of liquid(s) are important for obtaining thin, uniform, pinhole-free, and adherent glass films (248, 240, 250, 249) by this technique.

For thicker layers of about 5-25 μm, doctor-blading of a slurry, electrophoretic deposition, spinning on of photoresist-glass mixtures, application of beads of glass powder in a slurry, and silk screening (245) can be used. Doctor-blading requires a step- or groove-type geometry for the selective placement of the glass, and is suited to mesa-type devices. Electrophoretic deposition (123, 313, 217) is used for various power devices, and can be made selective by using insulator films to mask areas where no glass is desired (283-285). Photoresist-glass powder compositions permit removal of unwanted glass before fusion, thus eliminating an etching step (13).

For axial-lead diodes passivated with fused glass powder, a drop of slurry can be formed about the diode and stud lead assembly. In the case of preforms, the glass tubes for axial diodes are fitted over the device and fused into contact. High ambient pressure applied during fusion permits a lowering of fusion temperature (56). Combinations of glass powder as a bonding agent, and preforms as the passivating layer, have also been described (218).

Other glass application techniques include the use of various oxide thin films as a bonding layer between fused glass powder and the silicon surface (241, 244, 251, 243) and the formation of a glass *in situ* by firing of a silicon device with deposited glass-forming oxide powders (134).

The various analytical techniques already noted for grown or deposited layers are also useful for characterizing fused glass materials (247, 153). In addition, differential thermal analysis (102), microhardness testing (331), and particle size analysis (143) of the powder are valuable test methods to assure the attainment of high-quality layers.

Table III. Typical fused glasses. Some of the properties of silicon are given for comparison purposes.

Glass	Composition (% by wt) PbO	B_2O_3	Al_2O_3	ZnO	SiO_2	Other	Fusion temperature (°C)	CTE (°C)$^{-1}$	Devices	Deposited
LAZBSG	51	9	3	—	29	Na_2O:1.6; other oxides:5.4	570	8.2×10^{-6}	Planar IC's	Over metal on completed chip
LBASG	30	13	7	—	50	—	950	3.5×10^{-6}	Power devices	Over SiO_2 in mesa grooves
LASG	50	—	10	—	40	—	900	4.0×10^{-6}	High-voltage power devices	On Si in mesa grooves
LZABSG	46	10	3	2	39	—	700	4.6×10^{-6}	Power trans. and diodes	On Si; glass bead
ZBSG	2	25	—	60	10	CeO_2:3	700	4.5×10^{-6}	Power trans. and diodes	On Si; glass bead
Si	—	—	—	—	—	—	1410	3.5×10^{-6}	—	—

Passivation Layers and Silicon Device Reliability

Most of the presently available small-signal planar transistors and integrated circuits are Al-metallized and are passivated with a thin layer of SiO_2 or PSG. The primary purposes of this layer are to provide scratch protection during handling (142), to achieve immunity to shorts caused by loose particles in packages with a cavity, to reduce susceptibility of the Al metallization to corrosion (275), and to meet customer specification requirements. With complex IC's, increased electrical and visual inspection yields frequently more than compensate for the costs of applying and delineating a passivation layer. Glass passivation layers, deposited over the metallization pattern, have also been shown to significantly increase device reliability (197, 97, 276, 125, 185, 324, 127).

Glass passivation is frequently performed on all wafers by the same process, without regard to whether the final product will be commercial or high-reliability, in plastic or in hermetic packages, or will be rated for limited temperature or full temperature operation. Obviously, the thickness and composition of the passivation layer which meet all of these diverse requirements involve some tradeoffs and compromises. Our experimental studies (156) have shown that in a substantial portion of the integrated circuits manufactured in the last several years, the passivation layer contains pinholes, cracks, or a combination of these. A number of publications also confirm this finding (157, 278, 140, 144, 210, 89, 153, 338, 21).

Cracks in passivation layers, when present, frequently occur at and run along topographic steps or along the edges of delineated metal conductors or thin-film resistors (140, 144), and thus cannot be seen by optical microscopy. Pinholes in the dielectric over alloyed metal are generally very difficult to see by optical microscopy because of the rough topography of the recrystallized aluminum. Both cracks and pinholes can be revealed by scanning electron microscopy (SEM), or by subjecting the chip to immersion in an etchant which does not dissolve the dielectric but is capable of dissolving the underlying material (85, 254, 144, 89, 153). After chemical etching to undercut the Al, the actual pinhole in the dielectric is generally visible, by optical microscopy, in the center of the undercut area (153).

Pinholes in the passivating glass can occur for a variety of reasons. They may be present in the passivation layer as deposited (85, 27), may arise during etching to open the bonding pads (because of holes in the photoresist layer), or may be created by the contact printing operation or by impact during chip handling (142).

In a recent study (156), two classes of pinholes were evident in samples of IC's from six manufacturers. The more common class was pinholes in the central regions of aluminum lines. Another type observed was pinholes along the edge of the delineated metal lines (153). The edge pinholes are attributed to inadequate coverage of metal edges by the photoresist and can generally be avoided by the use of thicker photoresist layers or improved photoresist application techniques. Those pinholes which occurred in the central areas of delineated lines are to a large extent believed to be attributable to the presence of hillocks in the aluminum which occur because of recrystallization of the aluminum during the contact alloying step (188, 179, 156). Even if a hillock is completely covered with dielectric during the subsequent step of deposition of the passivation layer, the hillock may not be adequately covered by photoresist, the photoresist may be pushed away from the peak of the hillock during contact printing, or the contact printing step may fracture the dielectric over the hillock. Any of these three conditions, or a combination, will result in a pinhole through the passivation layer, exposing a region of underlying metal. Handling of wafers can result in impact cracks and scratches (142).

Al-metallized IC's are considerably more susceptible to failure due to opens as a result of Al corrosion during operation if the passivation layer contains cracks (235, 358) or pinholes (156) over the metal lines. Defects in passivation layers also increase susceptibility to ionic contaminant effects (156, 111). The requirements for attaining crack-free, pinhole-free passivation layers are very similar to the requirements for a first-layer deposited dielectric in multilevel-metallized integrated circuits. These include minimizing hillocks, low-stress dielectric deposition conditions, good coverage of the edges of delineated metal, and proper photolithographic procedures (303, 278, 104, 161, 103, 153, 340).

Phosphosilicate layers with an excessively high concentration of phosphorus are hygroscopic and have led to aluminum corrosion problems (235, 358, 93, 359). On the other hand, the use of low-phosphorus glass compositions which result in cracks over or along the edges of aluminum metal lines can lead to localized metal corrosion problems (235). The density and structure of phosphosilicate films are factors which influence the optimum phosphorus content (225).

The effectiveness of a passivation layer can be assessed by accelerated techniques in which the devices are exposed to high relative humidities. One commonly used condition is reverse bias or operating life at 85% relative humidity at 85°C. A considerably more severe test is to apply bias to devices which are in a pressure cooker, for example, at 15 psig (121°C).

Moisture plus bias can result in electrochemical corrosion of metal. Electrochemical corrosion normally would be expected to result in open metal lines which have positive (anodic) bias relative to adjacent lines (298, 166); with Al-metallized integrated circuits, corrosion of circuit lines which are cathodic has also been reported (166, 235). Stress-corrosion cracking (30) may be a factor in accelerating cathodic corrosion of Al metallization lines at grain boundaries. Corrosion mechanisms of Al can be chemical as well as electrochemical, and in either case temperature (5), pH (252, 170), and presence of chlorides (252, 170) are important factors in determining corrosion rate and corrosion products.

The more costly metallization system Ti-Pt-Au, with Au wire bonds, has been shown to be superior to Al for corrosion resistance (350, 119, 165). With Au metallization systems, electrolytic corrosion can, however, result in formation of dendrites which form shorts between conductors (170, 203, 288, 117).

Device Encapsulation

Final encapsulation of silicon devices may be in hermetically sealed packages (181, 94, 35, 22, 200, 343, 255), in molded plastic packages (181, 22, 4, 165, 113, 189, 23), in cast plastic, or by conformal plastic coating of chips mounted on hybrid substrates (345, 122). The encapsulation process provides the final means for passivation of the device. The device reliability, in terms of both stability of electrical characteristics and susceptibility to catastrophic failure, is a complex function of the device design and processing techniques and materials used, including the metallization, the passivation layer or layers, and the final encapsulation.

Early silicon devices were primarily sealed in hermetic packages. The plastic-encapsulated silicon devices initially offered had reliability limitations (183, 215, 310, 36, 276, 98, 108, 304) which, to a large extent, have now been overcome (24, 95, 98, 165, 113). Plastic encapsulation does permit lower costs, provides mechanically rugged packages, provides freedom from loose particle problems, and permits smaller package size.

Hermetically sealed devices are not totally immune to ionic contamination and moisture effects (20, 209, 140, 319, 332, 239). Ionic contaminants may be inadvertently sealed in the package (319, 320). Also, a percentage of the devices in completed electronic equip-

ment are not actually hermetically sealed (300, 209, 1), either because they escaped hermeticity screening tests, or because the hermetic seal became damaged during device handling or equipment assembly (1). In such cases, a suitable passivation layer can provide some protection against Al corrosion or electrolytic Au migration reactions.

The plastic formulations initially used for molding silicon devices were based on phenolics, epoxies, and silicones (128, 36, 28, 200, 97, 121, 201, 165, 113). In many cases a junction coat (layer of plastic such as an epoxy, silicone varnish, or room-temperature vulcanizing silicone elastomer) was applied prior to molding (84, 97, 121, 311, 165, 2). Plastics can be a source of ions (182, 128, 230, 228, 29, 166, 177, 308) or impurities (183, 230, 135, 298, 176) which adversely affect silicon devices, particularly in moist atmospheres and under bias conditions. In the last several years, a considerable number of process and materials changes has been made to improve the reliability of plastic-encapsulated silicon integrated circuits (96, 24, 95, 98, 165, 113). Most notable of the improvements is the use of novolac epoxy formulations with high glass transition temperatures (165).

Silicones are extensively used for encapsulation of power devices (201, 26) and for beam-lead devices (345, 237). In general, silicones permit high in-process temperatures and higher maximum storage temperatures (201, 257) than epoxy- or phenolic-based encapsulating compounds.

Various test devices and accelerated testing techniques have been developed for evaluating the stability of passivated devices under severe environmental conditions (314, 256, 238, 257). For plastic-encapsulated devices, a moisture-containing ambient constitutes an effective means for accelerating ion migration effects or chemical or galvanic corrosion of the metallization pattern on the chip (182, 28, 237, 33, 7, 90, 256, 121, 29, 238, 229, 291, 236, 257, 189, 23, 166, 176, 177). Moisture is an important factor since surface conductivity of SiO_2 and of other passivation materials increases by several orders of magnitude with increase in relative humidity (131, 46).

In general, passivation techniques provide only partial protection against ambient effects. For example, silicon nitride-passivated devices may be protected against alkali penetration into the underlying SiO_2, but may be influenced by potential buildup at insulator-insulator interfaces or at the ambient-upper dielectric interface. Increased device stability is frequently obtained by specific device construction features which make the device less surface sensitive. Examples include resistive overlays (57), use of diffused channel stoppers (273, 49), field plates (48, 43, 363, 59), ion implanted surfaces (299, 219), and use of beveled junctions (66, 167, 327, 14, 62) in high-voltage devices.

The most reliable silicon devices are those in which device design, wafer processing, metallization, passivation, assembly, encapsulation, and electrical testing are all specified to minimize the incidence of conditions which result in known failure mechanisms, and adequate in-process controls (39) are applied during the entire device fabrication sequence; thus reliability (278, 333, 281, 324, 236, 239) is designed into the product.

Acknowledgments

The authors gratefully acknowledge the contributions of A. W. Fisher and R. D. Vibronek to the experimental results presented in this paper, and the assistance of R. E Allen and P. L. Pado in preparation of the manuscript. We also thank A. W. Fisher, K. W. Hang, and J. L Vossen for the helpful discussions and for reviewing the manuscript. We also thank F. P. Jones, S. Merrin, and G. S. Sheldon for bringing several references on fused glass to our attention, and M. H. Woods for supplying several references on double dielectric structures.

This work was in part supported by the Air Force Materials Laboratory, Wright-Patterson Air Force Base, Ohio, under Contract No. F33615-74-C-5146.

Manuscript submitted Nov. 22, 1974; revised manuscript received Feb. 26, 1975. This was Paper 215 presented at the New York, New York, Meeting of the Society, Oct. 13-17, 1974.

Any discussion of this paper will appear in a Discussion Section to be published in the June 1976 JOURNAL. All discussions for the June 1976 Discussion Section should be submitted by Feb. 1, 1976.

Publication costs of this article were partially assisted by RCA Corporation.

REFERENCES

1. G. E. Adams, 11th Ann. Proc. Reliab. Phys., pp. 95-97 (1973).
2. J. D. Adams, 1/4-1 to 1/4-7 in IEEE 1974 INTERCON—Improving Producibility II, IEEE Cat. No. 74CHO904-3 (1974).
3. A. H. Agajanian, *IEEE Trans. Electron. Devices*, **ED-20**, 757 (1973); IBM Technical Report No. TR 22.1559 (November 1972).
4. L. Altman, *Electronics*, **46**, No. 9, 85 (April 26, 1973).
5. R. S. Alwitt, *This Journal*, **121**, 1322 (1974).
6. J. A. Amick and W. Kern, in "Chemical Vapor Deposition," J. M. Blocher, Jr. and J. C. Withers, Editors, pp. 551-570, The Electrochemical Society Softbound Symposium Series, New York (1970).
7. E. S. Anolick, A. Amendola, and P. J. Levitz, 9th Ann. Proc. Reliab. Phys., pp. 228-232 (1971).
8. E. Arai and Y. Terunuma, *This Journal*, **121**, 676 (1974).
9. J. R. Archer, *ibid.*, **104**, 619 (1957).
10. W. E. Armstrong and D. L. Tolliver, *ibid.*, **121**, 307 (1974).
11. M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, *Bell System Tech. J.*, **38**, 749 (1959).
12. T. G. Athanas, *Solid State Technol.*, **17**, No. 6, 54 (1974).
13. S. S. Baird and J. A. Cunningham, U.S. Pat. 3,355,291 (1967).
14. M. Bakowski and K. I. Lundstrom, *IEEE Trans. Electron. Devices*, **ED-20**, 550 (1973).
15. B. J. Baliga and S. K. Ghandhi, *J. Appl. Phys.*, **44**, 990 (1973).
16. P. Balk, Review paper prepared for inclusion in Proc. ESSDERC 1973 (European Solid State Device Research Conference), Munich (September 18-21, 1973) (Preprint).
17. P. Balk and J. M. Eldridge, *Proc. IEEE*, **57**, 1558 (1969).
18. M. L. Barry, *This Journal*, **117**, 1405 (1970).
19. M. L. Barry, in "Chemical Vapor Deposition," J. M. Blocher, Jr. and J. C. Withers, Editors, pp. 595-617, The Electrochemical Society Softbound Symposium Series, New York (1970).
20. J. J. Bart, *IEEE Trans. Electron. Devices*, **ED-16**, 351 (1969).
21. J. J. Bart, Paper No. 3.6 presented at the International Reliability Physics Symposium, Las Vegas, Nevada, April 2, 1975.
22. A. T. Batch, *Electronic Pkg. Prod.*, **11**, No. 3, 45, (1971).
23. D. M. Baugher and L. J. Gallace. 1/2-1 to 1/2-8 in IEEE 1974 INTERCON—Improving Producibility II, IEEE Cat. No. 74CHO904-3 (1974).
24. R. Beard, 10th Ann. Proc. Reliab. Phys., pp. 72-77 (1972).
25. K. H. Beckmann and N. J. Harrick, *This Journal*, **118**, 614 (1971).
26. W. P. Bennett and L. J. Gallace, IEEE Trans. Broadcast Television Receivers, **BTR-20**, 322 (1974).
27. W. C. Benzing, R. S. Rosler, and R. W. East, *Solid State Technol.*, **16**, No. 11, 37 (1973).
28. J. R. Bevington, J. P. Cook, and D. R. Little, 8th Ann. Proc. Reliab. Phys., pp. 73-80 (1970).
29. A. Bimson, in "Mikroelektronik 5," L. Steipe, Editor, pp. 395-421, R. Oldenbourg Verlag, München (1973).
30. W. W. Binger, E. H. Hollingsworth, and D. O. Sprowls, in "Aluminum, Vol. 1, Properties, Physical Metallurgy and Phase Diagrams," K. R.

Van Horn, Editor, pp. 209-276, American Society for Metals, Metals Park, Ohio, 1967.
31. J. R. Black, *IEEE Trans. Electron. Devices*, **ED-16**, 338 (1969).
32. J. R. Black, *Proc. IEEE*, **57**, 1587 (1969).
33. B. L. Blair and E. A. Herr, 8th Ann. Proc. Reliab. Phys., pp. 110-113 (1970).
34. I. Blech, H. Sello, and L. V. Gregor, in "Handbook of Thin Film Technology," L. I. Maissel and R. Glang, Editors, pp. 23-1 to 23-23, McGraw-Hill Book Co., New York (1970).
35. F. H. Bower, *Solid State Technol.*, **13**, No. 8, 56 (1970).
36. J. B. Brauer, V. C. Kapfer, and A. L. Tamburrino, 8th Ann. Proc. Reliab. Phys., pp. 61-72 (1970).
37. D. M. Brown, M. Garfinkel, M. Ghezzo, E. A. Taft, A. Tenney, and J. Wong, *J. Crystal Growth*, **17**, 276 (1972).
38. D. M. Brown and P. R. Kennicott, *This Journal*, **118**, 293 (1971).
39. G. A. Brown, K. Lovelace, and C. Hutchins, 11th Ann. Proc. Reliab. Phys., pp. 203-207 (1973).
40. R. C. Buchanan and M. A. Zuegel, *J. Am. Ceram. Soc.*, **51**, 28 (1968).
41. T. E. Burgess, J. C. Baum, F. M. Fowkes, R. Holmstrom, and G. A. Shirn, *This Journal*, **116**, 1005 (1969).
42. R. S. Buritz, A. Fafarman, R. F. McGowan, and S. L. Webster, Proc. 1969 Electron. Comp. Conf., pp. 304-321 (1969).
43. H. R. Camenzind, B. Polata, and J. Kocsis, *Electronics*, **42**, No. 7, 90 (March 31, 1969).
44. J. N. Carman, U.S. Pat. 3,200,310 (1965).
45. J. N. Carman, U.S. Pat. 3,392,312 (1968).
46. R. Castagne, P. Hesto, and A. Vapaille, *Thin Solid Films*, **17**, 253 (1973).
47. P. L. Castro and B. E. Deal, *This Journal*, **118**, 280 (1971).
48. P. P. Castrucci and J. S. Logan, *IBM J. Res. Develop.*, **8**, 396 (1964).
49. G. T. Cheney, R. L. Freyman, and A. A. Mammele, 9th Ann. Proc. Reliab. Phys., pp. 62-66 (1971).
50. Y. C. Cheng, J. W. Haslett, E. J. M. Kendall, R. J. Kriegler, and F. J. Scholz, *Proc. IEEE*, **62**, 859 (1974).
51. N. J. Chou and J. M. Eldridge, *This Journal*, **117**, 1287 (1970).
52. N. J. Chou, C. M. Osburn, Y. J. van der Meulen, and R. Hammer, *Appl. Phys. Letters*, **22**, 380 (1973).
53. C. K. Chu, J. E. Johnson, and A. J. Riding, Abstract 30, p. 86, The Electrochemical Society Extended Abstracts, Spring Meeting, San Francisco, California, May 12-17, 1974.
54. T. L. Chu, *J. Vacuum Sci. Technol.*, **6**, 25 (1969).
55. T. L. Chu, J. R. Szedon, and C. H. Lee, *Solid-State Electron.*, **10**, 897 (1967).
56. J. E. Clark, U.S. Pat. 3,193,366 (1965).
57. L. E. Clark and D. S. Zoroglu, *Solid-State Electron.*, **15**, 653 (1972).
58. R. H. Collins and J. S. Logan, U.S. Pat. 3,616,403 (1971).
59. F. Conti and M. Conti, *Solid-State Electron.*, **15**, 93 (1972).
60. E. A. Corl and W. E. Reese, *Metallurg. Trans.*, **1**, 747 (1970).
61. R. L. Cormia, *Solid State Technol.*, **12**, No. 12, 56 (December 1969).
62. J. Cornu, S. Schweitzer, and O. Kuhn, *IEEE Trans. Electron. Devices*, **ED-21**, 181 (1974).
63. H. E. Culver, H. Schilling, and R. E. Thun, *J. Vacuum Sci. Technol.*, **10**, 170 (1973).
64. K. S. Daghir, Abstract 268, p. 666, The Electrochemical Society Extended Abstracts, Fall Meeting, Miami Beach, Florida, Oct. 8-13, 1972.
65. J. V. Dalton and J. Drobek, *This Journal*, **115**, 865 (1968).
66. R. L. Davies and F. E. Gentry, *IEEE Trans. Electron. Devices*, **ED-11**, 313 (1964).
67. E. K. Davis and K. W. Hansen, U.S. Pat. 3,723,835 (1973).
68. E. M. Davis, W. E. Harding, and R. S. Schwartz, Wescon 1963, San Francisco, August 1963, Part 2, Paper 13.1.
69. E. M. Davis W. E. Harding, R. S. Schwartz, and J. J. Corning, *IBM J. Res. Develop.*, **8**, 102 (1964).
70. B. E. Deal, *This Journal*, **110**, 527 (1963).
71. B. E. Deal, Abstract 93, p. 259, The Electrochemical Society Extended Abstracts, Fall Meeting, Detroit, Michigan, Oct. 5-9, 1969.
72. B. E. Deal, in Silicon Device Processing, NBS Spec. Pub. 337, pp. 36-50, November 1970.
73. B. E. Deal, Abstract 39, p. 108, The Electrochemical Society Extended Abstracts, Spring Meeting, San Francisco, California, May 12-17, 1974.
74. B. E. Deal, *This Journal*, **121**, 198C (1974).
75. B. E. Deal, R. J. Fleming, and P. L. Castro, *ibid.*, **115**, 300 (1968).
76. B. E. Deal, E. L. MacKenna, and P. L. Castro, *ibid.*, **116**, 997 (1969).
77. C. J. Dell'Oca and M. L. Barry, *Solid-State Electron.*, **15**, 659 (1972).
78. R. Denning and C. L. Tollin, U.S. Pat. 3,465,209 (1969).
79. N. E. DeVolder, U.S. Pat. 3,505,571 (1970).
80. N. E. DeVolder, U.S. Pat. 3,533,832 (1970).
81. F. M. d'Heurle and R. Rosenberg, in "Physics of Thin Films," Vol. 7, G. Hass, M. H. Francombe, and R. W. Hoffman, Editors, pp. 257-310, Academic Press, New York (1973)
82. G. DiGiacomo, *This Journal*, **121**, 419 (1974).
83. T. H. DiStefano, *J. Appl. Phys.*, **44**, 527 (1973).
84. O. Dobson, *Electron. Eng. (London)*, **43**, No. 3, 47 (March 1971).
85. V. Y. Doo and V. M. L. Sun, *Metallurg. Trans.*, **1**, 741 (1970).
86. V. Y. Doo and P. J. Tsang, *This Journal*, **116**, 116C, (1969).
87. M. T. Duffy and W. Kern, *RCA Rev.*, **31**, 742 (1970).
88. M. Dumesnil and R. Hewitt, *This Journal*, **117**, 100 (1970).
89. G. H. Ebel and H. A. Engelke, 11th Ann. Proc. Reliab. Phys., pp. 108-116 (1973).
90. H. C. Edfors, Proc. 1972 Ann. Rel. & Maint. Symp., pp. 479-491 (January 1972).
91. J. M. Eldridge and D. R. Kerr, *This Journal*, **118**, 986 (1971).
92. J. M. Eldridge, R. B. Laibowitz, and P. Balk, *J. Appl. Phys.*, **40**, 1922 (1969).
93. C. J. Elia, *Wall Street Journal*, p. 31, May 2, 1974.
94. G. K. Fehr, *Solid State Technol.*, **13**, No. 8, 41 (1970).
95. J. E. Feldt and E. R. Hnatek, 10th Ann. Proc. Reliab. Phys., pp. 78-81 (1972).
96. F. Fischer, 8th Ann. Proc. Reliab. Phys., pp. 94-100 (1970).
97. P. Flaskerud, Proc. 1971 Semicond./IC Proc. and Prod. Conf., pp. 40-47, Ind. and Sci. Conf. Mtg., Chicago, Ill. (1971).
98. J. L. Flood, 10th Ann. Proc. Reliab. Phys., pp. 95-99 (1972).
99. P. Z. Fox and W. J. Nestork, *IBM J. Res. Develop.*, **15**, 384 (1971).
100. I. Franz and W. Langheinrich, *Solid-State Electron.*, **12**, 145 (1969).
101. B. T. French, J. E. Mann, and G. E. Ereckson, 10th Ann. Proc. Reliab. Phys., pp. 26-31 (1972).
102. R. G. Frieser, R. R. Tummala, and W. Fedrowitz, Abstract 5, p. 18, The Electrochemical Society Extended Abstracts, Spring Meeting, San Francisco, California, May 12-17, 1974.
103. P. B. Ghate, W. R. Gardner, and D. L. Crosthwait, *IEEE Trans. Reliability*, **R-22**, 186 (1973).
104. P. B. Ghate and L. H. Hall, *This Journal*, **119**, 491 (1972).
105. A. P. Gnadinger and W. Rosenzweig, *ibid.*, **121**, 700 (1974).
106. N. Goldsmith and W. Kern, *RCA Rev.*, **28**, 153 (1967).
107. A. J. Gonzales, 9th Ann. Proc. Reliab. Phys., pp. 142-148 (1971).
108. C. R. Gray, 10th Ann. Proc. Reliab. Phys., pp. 100-101 (1972).
109. L. V. Gregor, in "Thin Film Dielectrics," F. Vratny, Editor, pp. 447-488, The Electrochemical Society Softbound Symposium Series, New York (1969).
110. L. V. Gregor, *Proc. IEEE*, **59**, 1390 (1971).
111. A. J. Gregoritsch and R. G. Berger, Paper No. 3.5 presented at the International Reliability Phys-

ics Symposium, Las Vegas, Nevada, April 2, 1975.
112. B. L. Gregory and C. W. Gwyn, *Proc. IEEE*, **62**, 1264 (1974).
113. S. E. Grossman, *Electronics*, **46**, No. 21, 80 (Oct. 11, 1973).
114. A. S. Grove, "Physics and Technology of Semiconductor Devices," John Wiley and Sons, New York (1967).
115. A. S. Grove, O. Leistiko, Jr., and C. T. Sah, *J. Appl. Phys.*, **35**, 2695 (1964).
116. A. S. Grove, E. H. Snow, B. E. Deal, and C. T. Sah, *ibid.*, **35**, 2458 (1964).
117. F. J. Grunthaner, T. Griswold, and H. Bright, Paper No. 3.2 presented at the International Reliability Physics Symposium, Las Vegas, Nevada, April 2, 1975.
118. J. R. Haberer and J. J. Bart, 10th Ann. Proc. Reliab. Phys., pp. 106-111 (1972).
119. E. B. Hakim, G. Malinowski, and R. Holevinski, 11th Ann. Proc. Reliab. Phys., pp. 230-235 (1973).
120. L. Hall, *This Journal*, **118**, 1506 (1971).
121. M. C. Halleck, 10th Ann. Proc. Reliab. Phys., pp. 88-94 (1972).
122. D. W. Hamer and J. V. Biggers, in "Thick Film Hybrid Microcircuit Technology," pp. 277-302, Wiley-Interscience, New York (1972).
123. W. E. Harding and R. S. Schwartz, U.S. Pat. 3,280,019 (1966).
124. R. C. Henderson, *This Journal*, **119**, 772 (1972).
125. E. A. Herr, 10th Ann. Proc. Reliab. Phys., pp. 69-71 (1972).
126. E. A. Herr, A. Fox, and J. S. Read, G.E. Report No. R73 EGP8, November 19, 1973; Annual IEEE Chicago Fall Conference, December 1973.
127. E. A. Herr, A. Fox, and J. S. Read, *IEEE Trans. Broadcast Television Receivers*, **BTR-20**, 117 (1974).
128. H. Hirsch, *Solid State Technol.*, **13**, No. 8, 48 (1970).
129. R. W. Hoffman, in "Measurement Techniques for Thin Films," B. Schwartz and N. Schwartz, Editors, pp. 312-333, The Electrochemical Society Softbound Symposium Series, New York (1967).
130. S. R. Hofstein, *IEEE Trans. Electron Devices*, **ED-14**, 749 (1967).
131. L. Holland, in "The Properties of Glass Surfaces," pp. 448-528, Chapman and Hall, London (1964).
132. A. G. Holmes-Siedle, *Proc. IEEE*, **62**, 1198 (1974).
133. H. M. Hoogendorn and S. Merrin, U.S. Pat. 3,303,399 (1967).
134. G. C. Huth, U.S. Pat. 3,669,731 (1972).
135. J. A. Jackson, J. R. Szedon, and T. A. Temofonte, *This Journal*, **119**, 1424 (1972).
136. J. S. Judge, *ibid.*, **118**, 1772 (1971).
137. P. F. Kane and G. B. Larrabee, Editors, "Characterization of Semiconductor Materials," pp. 33-65, McGraw-Hill Book Co., New York (1970).
138. P. F. Kane and G. B. Larrabee, in *Annual Review of Materials Science*, **2**, 33 (1972).
139. P. F. Kane and G. B. Larrabee, "Characterization of Solid Surfaces," Plenum Press, New York (1974).
140. V. C. Kapfer and J. J. Bart, 10th Ann. Proc. Reliab. Phys., pp. 175-182 (1972).
141. L. H. Kaplan and M. E. Lowe, *This Journal*, **118**, 1649 (1971).
142. L. K. Karstadt, W. G. Burger, C. M. Hsieh, and W. A. Cosgrove, *Solid State Technol.*, **16**, No. 8, 41 (August 1973).
143. B. Kaye, *Int. Sci. and Technol.*, No. 27, 40-48 (March 1964).
144. W. F. Keenan and W. R. Runyan, *Microelectron. Reliab.*, **12**, 125 (1973).
145. W. Kern, *RCA Rev.*, **29**, 525 (1968).
146. W. Kern., *ibid.*, **29**, 557 (1968).
147. W. Kern, U.S. Pat. 3,481,781 (1969).
148. W. Kern, *This Journal*, **116**, 251C, (1969).
149. W. Kern, *RCA Rev.*, **31** 207 (1970).
150. W. Kern, *ibid.*, **31**, 234 (1970).
151. W. Kern, *ibid.*, **32**, 429 (1971).
152. W. Kern, *Solid State Technol.*, **15**, No. 1, 34 (1972), and **15**, No. 2, 39 (1972).
153. W. Kern, *RCA Rev.*, **34**, 655 (1973); *Solid State Technol.*, **17**, No. 3, 35, and No. 4, 78, 89 (1974).
154. W. Kern, Proc. Natl. Aerosp. Electr. Conf., pp. 93-100 (IEEE Cat. No. 75CHO936-3 NAECON), June 1975.
155. W. Kern and A. W. Fisher, *RCA Rev.*, **31**, 715 (1970).
156. W. Kern, A. W. Fisher, and R. D. Vibronek, Unpublished work (1974).
157. W. Kern and R. C. Heim, *This Journal*, **117**, 562 (1970).
158. W. Kern and R. C. Heim, *ibid.*, **117**, 568 (1970).
159. W. Kern and D. Puotinen, *RCA Rev.*, **31** 187 (1970).
160. W. Kern and J. M. Shaw, *This Journal*, **118**, 1699 (1971).
161. W. Kern, J. L. Vossen, and G. L. Schnable, 11th Ann. Proc. Reliab. Phys., pp. 214-223 (1973).
162. D. R. Kerr, *IBM J. Res. Develop.*, **8**, 385 (1964).
163. D. R. Kerr, 8th Ann. Proc. Reliab. Phys., pp. 1-8 (1970).
164. D. R. Kerr, J. S. Logan, P. J. Burkhardt, and W. A. Pliskin, *IBM J. Res. Develop.*, **8**, 376 (1964).
165. H. Khajezadeh, 11th Ann. Proc. Reliab. Phys., pp. 236-244 (1973); *Microelectronics (London)*, **5**, No. 2, 28 (1973).
166. H. Koelmans, 12th Ann. Proc. Reliab. Phys., pp. 168-171 (1974).
167. G. Kohl, *Solid-State Electron.*, **11**, 501 (1968).
168. W. A. Kohler, *Metallurg. Trans.*, **1**, 735 (1970).
169. R. A. Kokosa, B. R. Tuft, and E. D. Wolley, IEEE Industry Applications Meeting Proceedings, Milwaukee, Wisc., p. 87 (October 1973).
170. S. C. Kolesar, 12th Ann. Proc. Reliab. Phys., pp. 155-167 (1974).
171. R. J. Kriegler, *Thin Solid Films*, **13**, 11 (1972).
172. R. J. Kriegler, in "Semiconductor Silicon 1973," H. R. Huff and R. R. Burgess, Editors, pp. 363-375, The Electrochemical Society Softbound Symposium Series, Princeton, N.J. (1973).
173. R. J. Kriegler, 12th Ann. Proc. Reliab. Phys., pp. 250-258 (1974).
174. E. E. Lampi and E. F. Labuda, 10th Ann. Proc. Reliab. Phys., pp. 112-119 (1972).
175. R. Lathlaen and D. A. Diehl, *This Journal*, **116**, 620 (1969).
176. R. W. Lawson, 12th Ann. Proc. Reliab. Phys., pp. 243-249 (1974).
177. R. W. Lawson and J. C. Harrison, Paper No. 6, presented at the First International Conference on Plastics in Telecommunications (IEE), London, November 26-27, 1974 (preprint).
178. A. J. Learn, *J. Appl. Phys.*, **44**, 1251 (1973).
179. A. J. Learn, *Thin Solid Films*, **20**, 261 (1974).
180. A. J. Learn and W. H. Shepherd, 9th Ann. Proc. Reliab. Phys., pp. 129-134 (1971).
181. I. A. Lesk and E. D. Metz, in "Handbook of Semiconductor Electronics," 3rd ed., L. P. Hunter, Editor, pp. 9-1 to 9-25, McGraw-Hill Book Co., New York (1970).
182. J. J. Licari, in "Plastic Coatings for Electronics," pp. 278-313, McGraw-Hill Book Co., New York (1970).
183. J. J. Licari and G. V. Browning, *Electronics*, **40**, No. 4, 101 (April 17, 1967).
184. J. R. Ligenza, Paper presented at Solid State Device Physics and Technology Seminar, Dept. of Elec. Eng., Princeton Univ., Princeton, N.J., November 20, 1973.
185. J. H. Lindwedel, Final Report to RADC by Autonetics Div., North American Rockwell Corp., RADC-TR-73-127, May 1973.
186. G. Linker, O. Meyer, and W. Scherber, *Phys. Status Solidi (a)*, **16**, 377 (1973).
187. P. Lloyd, *Thin Solid Films*, **10**, 159 (1972).
188. J. S. Logan, F. S. Maddocks, and P. D. Davidse, *IBM J. Res. Develop.*, **14**, 182 (1970).
189. R. L. Lohn, 1/1-1 to 1/1-18 in IEEE 1974 INTERCON Improving Producibility II, IEEE Cat. No. 74CHO904-3 (1974).
190. C. P. Lue, J. A. Jackson, and Y. P. Han, Abstract 199, p. 490, The Electrochemical Society Extended Abstracts, Fall Meeting, New York, New York, Oct. 13-17, 1974.
191. E. L. MacKenna, Proc. 1971 Semicond./IC Proc. and Prod. Conf., 71-83, Ind. and Sci. Conf. Mtg., Chicago, Ill. (1971).
192. E. L. MacKenna, Abstract 216, p. 531, The Electrochemical Society Extended Abstracts, Fall

Meeting, New York, New York, Oct. 13-17, 1974.
193. E. M. MacKenna and P. Kodama, *This Journal*, **119**, 1094 (1972).
194. H. G. Maguire and P. D. Augustus, *ibid.*, **119**, 791 (1972).
195. C. F. Maguire, Q. T. Jarrett, and C. Y. Bartholomew, *Solid State Technol.*, **15**, No. 4, 46 (1972).
196. C. F. Maguire, F. J. Koons, and Q. T. Jarrett, *ibid.*, **14**, No. 8, 37 (1971).
197. C. C. Mai and T. S. Whitehouse, IEEE Trans. Reliability, **R-19**, 71 (1970).
198. "*Handbook of Thin Film Technology*," L. I. Maissel and R. Glang, Editors, McGraw-Hill Book Co., New York (1970).
199. Proc. of the Symp. on Modern Methods of Surface Analysis 1970, in "Modern Methods of Surface Analysis," P. Mark and J. D. Levine, Editors, North-Holland Publishing Co., Amsterdam (1971).
200. H. W. Markstein, *Electronic Pkg. Prod.*, **10**, No. 10, 20 (October 1970).
201. H. W. Markstein, *Electronic Pkg. Prod.*, **13**, No. 3, 25 (March 1973).
202. J. R. Mathews, W. A. Griffin, and K. H. Olson, *This Journal*, **112**, 899 (1965).
203. J. J. Mazenko, ISHM Symp. Proc. 1974, pp. 450-459 (1974).
204. D. V. McCaughan and R. A. Kushner, *Proc. IEEE*, **62**, 1236 (1974).
205. D. V. McCaughan, R. A. Kushner, and V. T. Murphy, in "Semiconductor Silicon 1973," H. R. Huff and R. R. Burgess, Editors, pp. 376-384, The Electrochemical Society Softbound Symposium Series, Princeton, N. J. (1973).
206. D. V. McCaughan, R. A. Kushner, and S. Wagner, *This Journal*, **121**, 724 (1974).
207. R. E. McCullough, 10th Ann Proc. Reliab. Phys., pp. 19-22 (1972).
208. B. A. McDonald, *Solid-State Electron.*, **14**, 17 (1971).
209. W. McQuitty and C. R. Lively, *Electronic Pkg. Prod.*, **11**, No. 11, 112 (November 1971).
210. P. B. Mee, *Honeywell Computer Journal*, **5**, 115 (1971).
211. R. L. Meek, *This Journal*, **120**, 308 (1973).
212. R. L. Meek and R. H. Braun, *ibid.*, **119**, 1538 (1972).
213. R. L. Meek, T. M. Buck, and C. F. Gibbon, *ibid.*, **120**, 1241 (1973).
214. S. Merrin, *EDN*, **15**, No. 23, 35 (December 1, 1970).
215. E. D. Metz, *Proc. IEEE*, **57**, 1606 (1969).
216. J. T. Milek, "Silicon Nitride for Microelectronic Applications. Part 1. Preparation and Properties," p. 1-118, IFI/Plenum, New York (1971).
217. K. Miwa, M. Kanno, S. Kawashima, S. Kawamura, and T. Shibuya, *Denki Kagaku*, **40**, 478 (1972).
218. J. P. Mize, U. S. Pat. 3,689,243 (1972).
219. R. A. Moline and G. W. Reutlinger, *IEEE Trans. Electron Devices*, **ED-20**, 1129 (1973).
220. F. Montillo and P. Balk, *This Journal*, **118**, 1463 (1971).
221. W. J. Morrissey, U.S. Pat. 3,752,701 (1973).
222. C. T. Naber, *This Journal*, **119**, 301C, (1972).
223. N. Nagasima, *J. Appl. Phys.*, **43**, 3378 (1972).
224. N. Nagasima and H. Enari, *Jap. J. Appl. Phys.*, **10**, 441 (1971).
225. N. Nagasima, H. Suzuki, K. Tanaka, and S. Nishida, *This Journal*, **121**, 434 (1974).
226. E. H. Nicollian, *J. Vacuum Sci. Technol.*, **8**, S39 (1971).
227. E. H. Nicollian, 12th Ann. Proc. Reliab. Phys., pp. 267-272 (1974).
228. R. W. Nufer and L. C. Anderson, *Solid State Technol.*, **14**, No. 8, 33 (1971).
229. T. Ohtsuki, O. Shintaku, and H. Fukuwatari, Abstract 158, p. 400, The Electrochemical Society Extended Abstracts, Fall Meeting, Boston, Massachusetts, Oct 7-11, 1973.
230. R. C. Olberg, *This Journal*, **118**, 129 (1971).
231. C. M. Osburn, *ibid.*, **121**, 809 (1974).
232. C. M. Osburn and N. J. Chou, *ibid.*, **120**, 1377 (1973).
233. C. M. Osburn and S. I. Raider, *ibid.*, **120**, 1369 (1973).
234. W. M. Paulson, 11th Ann. Proc. Reliab. Phys., pp. 61-68 (1973).
235. W. M. Paulson and R. W. Kirk, 12th Ann. Proc. Reliab. Phys., pp. 172-179 (1974).
236. C. G. Peattie, J. D. Adams, S. L. Carrell, T. D. George, and M. H. Valek, *Proc. IEEE*, **62**, 149 (1974).
237. D. S. Peck, 8th Ann. Proc. Reliab. Phys., pp. 81-93 (1970).
238. D. S. Peck and C. H. Zierdt, Jr., 11th Ann. Proc. Reliab. Phys., pp. 146-152 (1973).
239. D. S. Peck and C. H. Zierdt, Jr., *Proc. IEEE*, **62**, 185 (1974).
240. J. A. Perri, *Solid State Technol.*, **8**, No. 5, 19 (1965).
241. J. A. Perri and J. Riseman, U.S. Pat. 3,247,428 (1966).
242. J. A. Perri and J. Riseman, *Electronics*, **39**, No. 20, 108 (October 3, 1966).
243. J. A. Perri and J. Riseman, U.S. Pat. 3,546,013 (1970).
244. J. A. Perri, J. Riseman, and R. L. Ruggles, Jr., U.S. Pat. 3,300,339 (1967).
245. A. J. Pikor, Abstract 34, p. 96, The Electrochemical Society Extended Abstracts, Spring Meeting, San Francisco, California, May 12-17, 1974.
246. F. X. Pink and V. Lyn, *Electrochem. Technology*, **6**, 258 (1968).
247. W. A. Pliskin, in "Semiconductor Silicon 1973," H. R. Huff and R. R. Burgess, Editors, pp. 506-509, The Electrochemical Society Softbound Symposium Series, Princeton, N. J. (1973).
248. W. A. Pliskin and E. E. Conrad, *Electrochem. Technol.*, **2**, 196 (1964).
249. W. A. Pliskin and E. E. Conrad, U.S. Pat. 3,212,921 (1965).
250. W. A. Pliskin and E. E. Conrad, U.S. Pat. 3,212,929 (1965).
251. W. A. Pliskin, P. H. Davidse, H. S. Lehman, and L. I. Maissel, *IBM J. Res. Develop.*, **11**, 461 (1967).
252. M. Pourbaix, "Lectures on Electrochemical Corrosion," translated by J. A. S. Green, pp. 145-146, 165-171, Plenum Press, New York (1973).
253. K. Prabriputaloong and M. R. Piggott, *This Journal*, **121**, 430 (1974).
254. I. J. Pugacz-Muraszkiewicz, *IBM J. Res. Develop.*, **16**, 523 (1972).
255. T. H. Ramsey, Jr., *Solid State Technol.*, **17**, No. 9, 51 (September 1974).
256. B. Reich and E. B. Hakim, 10th Ann. Proc. Reliab. Phys., pp. 82-87 (1972).
257. B. Reich and E. B. Hakim, Proc. 1974 Ann. Reliab. and Maint. Symp., pp. 396-402 (January 1974).
258. A. R. Reinberg, Abstract 6, p. 19, The Electrochemical Society Extended Abstracts, Spring Meeting, San Francisco, California, May 12-17, 1974.
259. A. G. Revesz and K. H. Zaininger, *RCA Rev.*, **29**, 22 (1968).
260. P. H. Robinson and F. P. Heiman, *This Journal*, **118**, 141 (1971).
261. R. S. Ronen and P. H. Robinson, *ibid.*, **119**, 747 (1972).
262. J. C. Sarace, R. E. Kerwin, D. L. Klein, and R. Edwards, *Solid-State Electron.*, **11**, 653 (1968).
263. T. Satake, K. Yokoyama, S. Shirakawa, and K. Sawaguchi, *Jap. J. Appl. Phys.*, **12**, 518 (1973).
264. K. Sato, *This Journal*, **117**, 1065 (1970).
265. J. Sato, Y. Ban, and K. Maeda, 9th Ann. Proc. Rel. Phys., pp. 96-106 (1971).
266. K. Sato, Y. Nishi, and T. Abe, in "Thin Film Dielectrics," F. Vratny, Editor, pp. 378-406, The Electrochemical Society Softbound Symposium Series, New York (1969).
267. P. M. Schaible and R. Glang, in "Thin Film Dieelctrics," F. Vratny, Editor, pp. 577-594, The Electrochemical Society Softbound Symposium Series, New York (1969).
268. R. J. Scheuerman, in "Thin Film Dielectrics," F. Vratny, Editor, pp. 561-576, The Electrochemical Society Softbound Symposium Series, New York (1969).
269. M. M. Schlacter, E. S. Schlegel, R. S. Keen, R. A. Lathlaen, and G. L. Schnable, *IEEE Trans. Electron Devices*, **ED-17**, 1077 (1970).
270. E. S. Schlegel, *ibid.*, **ED-14**, 728 (1967).

271. E. S. Schlegel, *ibid.*, **ED-15**, 951 (1968).
272. E. S. Schlegel, "A Categorized MIS Bibliography," Philco-Ford Corp., Blue Bell, Pa. (1971).
273. E. S. Schlegel, R. S. Keen, and G. L. Schnable, 8th Ann. Proc. Reliab. Phys., pp. 9-16 (1971).
274. E. S. Schlegel and G. L. Schnable, *IEEE Trans. Electron Devices*, **ED-16**, 386 (1969).
275. G. L. Schnable, IEEE '71 Intern. Conv. Digest, pp. 586-587 (1971).
276. G. L. Schnable, H. J. Ewald, and E. S. Schlegel, *IEEE Trans. Reliability*, **R-21**, 12 (1972).
277. G. L. Schnable and R. S. Keen, *Proc. IEEE*, **57**, 1570 (1969).
278. G. L. Schnable and R. S. Keen, in "Advances in Electronics and Electron Physics," Vol. 30, L. Marton, Editor, pp. 79-138 Academic Press, New York (1971).
279. G. H. Schneer, W. van Gelder, V. E. Hauser, and P. F. Schmidt, *IEEE Trans. Electron Devices*, **ED-15**, 290 (1968).
280. W. Schroen, 11th Ann. Proc. Reliab. Phys., pp. 117-123 (1973).
281 W. H. Schroen, J. G. Aiken, and G. A. Brown, 10th Ann. Proc. Reliab. Phys., pp. 42-48 (1972).
282. R. O. Schwenker, *This Journal*, **118**, 313 (1971).
283. G. S. Sheldon, U. S. Pat. 3,642,597 (1972).
284. G. S. Sheldon, U. S. Pat. 3,644,801 (1972).
285 G. S. Sheldon, U.S. Pat. 3,735,483 (1973).
286. M. Shibata and K. Sugawara, *This Journal*, **122**, 155 (1975).
287. M. Shibata, T. Yoshimi, and K. Sugawara, *ibid.*, **122**, 157 (1975).
288. A. Shumka and R. R. Piety, Paper No. 3.1 presented at the Intl. Reliab. Phys. Symp., Las Vegas, Nevada, April 2, 1975.
289. R. Silverman, *This Journal*, **115**, 674 (1968).
290. B. R. Singh, *J. Phys. D: Appl. Phys.*, **7**, 443 (1974).
291. F. N. Sinnadurai, *Microelectron. Reliab.*, **13**, 23 (1974).
292. J. N. Smith, S. Thomas, and K. Ritchie, *This Journal*, **121**, 827 (1974).
293. E. H. Snow and B. E. Deal, *ibid.*, **113**, 263 (1966).
294. E. H. Snow and B. E. Deal, *Trans. Met. Soc. AIME*, **242**, 521 (1968).
295. E. H. Snow and M. E. Dumesnil, *J. Appl. Phys.*, **37**, 2123 (1966).
296. E. H. Snow, A. S. Grove, B. E. Deal, and C. T. Sah, *ibid.*, **36**, 1664 (1965).
297. S. M. Spitzer and S. Schwartz, *IEEE Trans. Electron Devices*, **ED-16**, 348 (1969).
298. R. S. Spriggs and A. H. Cronshagen, 10th Ann. Proc. Reliab. Phys., pp. 201-203 (1972).
299. J. D. Stansbury, *IEEE Trans. Electron Devices*, **ED-20**, 473 (1973).
300. R. L. Stewart and G. R. Neff, Proc. 1971 Semicond. IC Proc. and Prod. Conf., pp. 48-56, Ind. and Sci. Conf. Mtg., Chicago, Ill. (1971); *Evaluation Engineering*, **10**, No. 2, 32, (March/April 1971).
301. K. Strater, *RCA Rev.*, **29**, 618 (1968).
302. H. Sunami, Y. Itoh, and K. Sato, *J. Appl. Phys.*, **41**, 5115 (1970).
303. H. Sunami, Y. Itoh, and K. Sato, Proc. 2nd Conf. Sol. St. Dev., Tokyo, 1970, Suppl. to *J. Jap. Soc. Appl. Phys.*, **40**, 67 (1971).
304. R. E. Sundius, 10th Ann. Proc. Reliab. Phys., pp. 102-104 (1972).
305. B. Swaroop, in "Thin Film Dielectrics," F. Vratny, Editor, pp. 407-431, The Electrochemical Society Softbound Symposium Series, New York (1969).
306. B. Swaroop, *This Journal*, **118**, 913 (1971).
307. B. Swaroop, *IEEE Trans. Pts., Hybrids Pkg.*, **PHP-9**, 234 (1973).
308. J. R. Szedon, *ibid.*, **PHP-10**, 251 (1974).
309. J. R. Szedon and R. M. Handy, *J. Vacuum Sci. Technol.*, **6**, 1 (1969).
310. J. R. Szedon and J. P. Stelmak, *IEEE Trans. Elec. Insulation*, **EI-5**, 3 (1970).
311. J. R. Szedon, T. A. Temofonte, J. A. Jackson, and D. C. Philips, *J. Vacuum Sci. Technol.* **10**, 284 (1973).
312. E. A. Taft, *This Journal*, **118**, 1985 (1974).
313. E. G. Tefft, U.S. Pat. 3,639,975 (1972).
314. T. A. Temofonte and J. R. Szedon, 9th Ann. Proc. Reliab. Phys., pp. 107-113 (1971).
315. A. S. Tenney, *This Journal.*, **118**, 1658 (1971).
316. A. S. Tenney and M. Ghezzo, *ibid.*, **120**, 1091 (1973).
317. A. S. Tenney and M. Ghezzo, *ibid.*, **120**, 1276 (1973).
318. L. Terry, Abstract 228, p. 533, The Electrochemical Society Extended Abstracts, Spring Meeting, San Francisco, California, May 12-17. 1974.
319. R. W. Thomas, Proc. Govt. Microcirc. Appl. Conf. (GOMAC), pp. 31-36, October 1972.
320. R. W. Thomas and D. E. Meyer, *Solid State Technol.* **17**, No. 9, 56 (September 1974).
321. T. Tokuyama, T. Miyazaki, and M. Horiuchi, in "Thin Film Dielectrics," F. Vratny, Editor, pp. 297-326, The Electrochemical Society Softbound Symposium Series, New York (1969).
322. N. C. Tombs, H. A. R. Wegener, R. Newman, B. T. Kenney, and A. J. Coppola, *Proc. IEEE*, **54**, 87 (1966).
323. P. A. Totta, Proc. 1971 Electronic Components Conf., pp. 275-284 (IEEE 71C7-PMP) (May 1971).
324. P. A. Totta, 11th Ann. Proc. Reliab. Phys., p. 92 (1973).
325. P. A. Totta and R. P. Sopher, *IBM J. Res. Develop.*, **13**, 226 (1969).
326. T. Tsujide, S. Nakanuma, and Y. Ikushima, *This Journal*, **117**, 703(1970).
327. B. R. Tuft, U.S. Pat. 3,643,136 (1972).
328. S. K. Tung and R. E. Caffrey, *Trans. Met. Soc. AIME*, **233**, 572 (1965).
329. S. K. Tung and R. E. Caffrey, *This Journal*, **114**, 275C (1967).
330. S. K. Tung and R. E. Caffrey, in "Thin Film Dielectrics," F. Vratny, Editor, pp. 286-296, The Electrochemical Society Softbound Symposium Series, New York (1969).
331. M. N. Turetzky, J. B. Jenkins, and H. R. Fraser, Jr., *This Journal*, **121**, 1098 (1974).
332. J. Vaccaro, Proc. IEEE, **62**, 169 (1974).
333. H. W. van Beek, 10th Ann. Proc. Reliab. Phys., pp. 36-41 (1972).
334. Y. J. van der Meulen, *J. Vacuum Sci. Technol.*, **11**, 985 (1974).
335. Y. J. van der Meulen and J. G. Cahill, *J. Electronic Materials*, **3**, 371 (1974).
336. W. van Gelder and V. E. Hauser, *This Journal*, **114**, 869 (1967).
337. R. R. Verderber, G. A. Gruber, J. W. Ostroski, J. E. Johnson, K. S. Tarneja, D. M. Gillott, and B. J. Coverston, *IEEE Trans. Electron Devices*, **ED-17**, 797 (1970).
338. A. A. Viele, 12th Ann. Proc. Reliab. Phys., pp. 16-21 (1974).
339. J. L. Vossen, *J. Vacuum Sci. Technol.*, **8**, S12 (1971).
340. J. L. Vossen, G. L. Schnable, and W. Kern, *ibid.*, **11**, 60 (1974).
341. "Thin Film Dielectrics," F. Vratny, Editor, The Electrochemical Society Softbound Symposium Series, New York (1969).
342. R. K. Waits, *J. Vacuum Sci. Technol.*, **10**, 285 (1973).
343. C. H. Wang and W. T. Wakely, 18/1-1 to 18/1-3 in 1974 IEEE INTERCON Technical Program Papers, IEEE Cat. No. 74CHO898-7 (1974).
344. W. A. Westdorp and G. H. Schwuttke, in "Thin Film Dielectrics," F. Vratny, Editor, pp. 546-560, The Electrochemical Society Softbound Symposium Series, New York (1969).
345. M. L. White, *Proc. IEEE*, **57**, 1610 (1969).
346. R. Williams and M. H. Woods, *J. Appl. Phys.*, **43**, 4142 (1972).
347. V. D. Wohlheiter and R. A. Whitner, *This Journal* **119**, 945 (1972).
348. H. F. Wolf, in "Semiconductors," pp. 342-362, Wiley-Interscience, New York (1971).
349. M. H. Woods, 12th Ann. Proc. Reliab. Phys., pp. 259-266 (1974).
350. J. C. Wright, 11th Ann. Proc. Reliab. Phys., pp. 224-229 (1973).
351. Staff Article, "Fabrication Changes Soup Up Power Devices," *Electronics*, **44**, No. 10, 43 (May 10, 1971).
352. Staff Article. "Double Mesa is Key to Triac Chip Process," *ibid.*, **44**, No. 15, 28 (July 19, 1971).
353. See, for example, *IEEE Trans. Nuclear Science*, **NS-18**, No. 6 (December 1971); **NS-19**, No. 6 (December 1972), **NS-20**, No. 6 (December 1973); and **NS-21**, No. 6 (December 1974).

354. Staff Article, "Tailor-Made Glasses Can be Made Strong, Flexible, and Inert," *Product Engineering*, **43**, No. 2 (February 1972).
355. Staff Article, "Westinghouse Speeds High-Power Device," *Electronics*, **45**, No. 4, 41 (February 14, 1972).
356. Staff Article, "Diode Chips are Glass Passivated," *ibid.*, **46**, No. 2, 207 (January 18, 1973).
357. Staff Article, "GI Pushes High-Voltage Technology," *ibid.*, **46**, No. 21, p. 36 (October 11, 1973).
358. Staff Article, "How Phosphorus Abets IC Destruction," *ibid.*, **47**, No. 8, 34 (April 18, 1974).
359. Staff Article, "Defective ICs Halted Philco TV Output," *Electronic News*, p. 34 (May 20, 1974).
360. Staff Article, "Vapor Deposition Unit is Modular," *Electronics*, **47**, No. 18, p. 138 (September 5, 1974).
361. Y. T. Yeow, J. W. Clancy, and D. R. Lamb, *Int. J. Electronics*, **34**, 115 (1973).
362. K. H. Zaininger and F. P. Heiman, *Solid State Technol.*, **13**, No. 5, p. 49, and No. 6, 46 (1970).
363. D. S. Zoroglu and L. E. Clark, *IEEE Trans. Electron Devices*, **ED-19**, 4 (1972).

APPENDIX B

SURVEY OF CVD REACTOR SYSTEMS AND EQUIPMENT

by

W. Kern

A. REQUIREMENTS FOR REACTOR SYSTEMS

A CVD system for depositing passivating films of the type described must provide equipment that accomplishes the following functions [B-1 to B-5]:

(1) Transport, meter, and time the diluent and reactant gases entering the reactor;

(2) provide heat to the site of reaction, namely, the substrate material being coated, and control this temperature by automatic feedback to the heat source; and

(3) remove the by-product exhaust gases from the deposition zone and safely dispose of them.

The reactor system should be designed to fulfill these three primary functions with maximum effectiveness and simplicity of construction. It must consistently yield glass films of high quality; good thickness and compositional uniformity from wafer to wafer and from run to run; and high purity with a minimum of structural imperfections such as pinholes, cracks, and particulate contaminants. For research applications these requirements are usually quite sufficient, but for large-scale production applications the system should, in addition, perform with high throughput, be simple and safe to operate, and be

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B-1. C. F. Powell, J. H. Oxley, and J. M. Blocher, Jr., Eds., *Vapor Deposition*, (John Wiley and Sons, Inc., New York, 1966).

B-2. D. S. Campbell, in *Handbook of Thin-Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw-Hill Book Co., New York, 1970), pp. 5-1 to 5-25.

B-3. E. L. MacKenna, Proc. 1971 Semiconductor/IC Proc. and Prod. Conf., Ind. and Sci. Conf. Mtg., Chicago, Ill., (1971), pp. 71-83.

B-4. *Chemical Vapor Deposition* (Intn'l Conf.): J. M. Blocher, Jr., and J. C. Withers, Eds., - Second Intn'l Conf., The Electrochemical Soc., New York, 1970; F. A. Glaski, Ed. - Third Intn'l Conf., The American Nuclear Society, Hinsdale, Ill., 1972; and G. F. Wakefield and J. M. Blocher, Jr., - Fourth Intn'l Conf., The Electrochemical Soc., Princeton, N.J., 1973.

B-5. M. L. Hammond, J. Vac. Sci. Technol. 10, 268 (1973).

easy to maintain routinely. Labor-saving automation [B-6] and computerization are attractive additional options that can be well worth the increased capital cost in reducing labor costs, resulting in net savings. Similar considerations concern the capital cost of the equipment, which ranges from less than $3,000 for an in-house built research or pilot production unit to over $70,000 for a high-capacity production system. The capital cost must be carefully evaluated in terms of the system's actual product output, operator and maintenance labor required, consumed gases, power consumption, and parts replacement cost.

A considerable degree of sophistication and refinement has been engineered into present-day commercial reactor systems, emphasizing maximum product throughput, improved process control, and convenience and economy in processing and equipment maintenance. Various techniques for process automation have been developed, including full computer automation with separate digital control of each of the various parameters such as temperature control, gas composition, and timing sequence. Heating is usually effected by resistance-heating techniques, and operation is at nominally atmospheric pressure. Provisions have been made in several of the commercial reactors for cooling of the reactor walls or the gas distributor to suppress homogeneous gas phase nucleation.

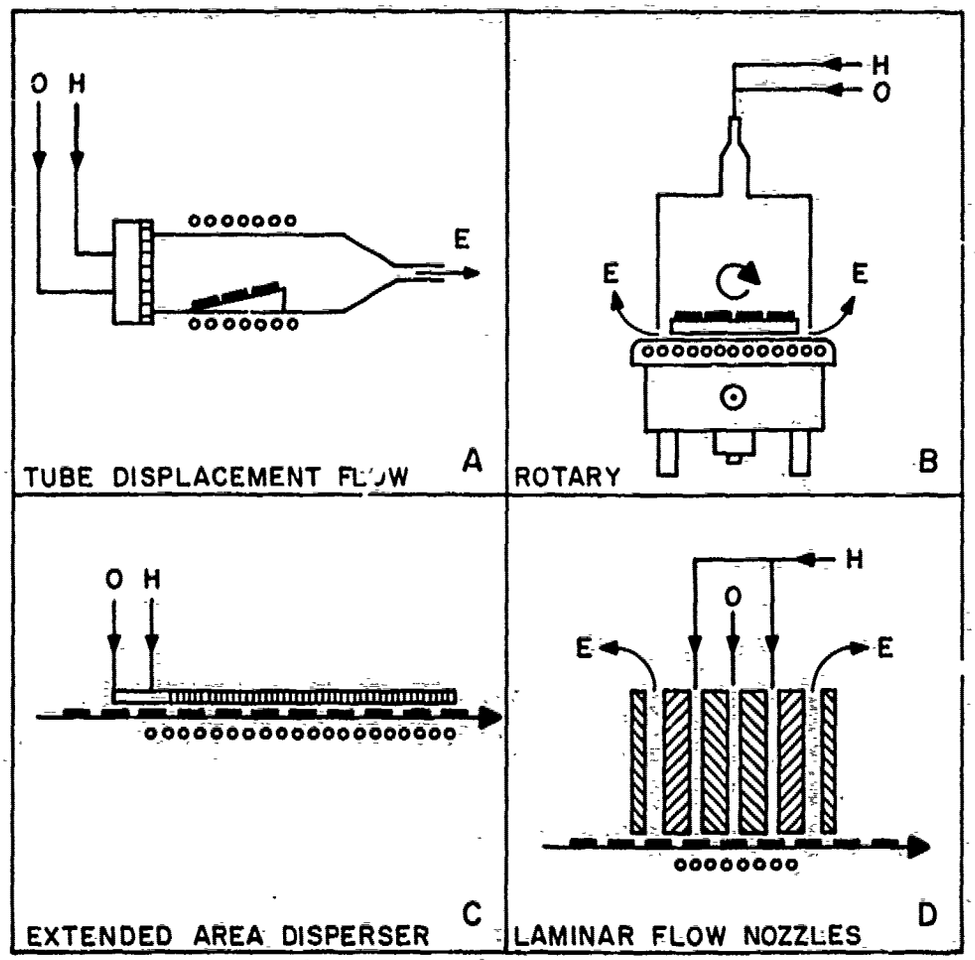
B. BASIC TYPES OF REACTORS

Reactors can be classified in essentially four main categories, according to their gas flow characteristics and principle of operation:

(1) Horizontal tube displacement flow reactors.
(2) Rotary vertical batch-type reactors.
(3) Continuous reactors employing premixed gas flow fed through an extended area slotted disperser plate.
(4) Continuous reactors employing separate, nitrogen-diluted oxygen and hydride streams that are directed toward the substrate by laminar flow nozzles.

The schematic diagrams presented in Fig. B-1 show the basic features of these four types. Each system and its variants are briefly discussed and

B-6. W. C. Benzing and R. Fisk, Solid State Technol. 18, No. 1, 39 (1975).



O = $O_2 + N_2$ H = $SiH_4 + N_2 \pm PH_3$ E = EXHAUST GASES

oooooo = RESISTANCE HEATER ▬ = SUBSTRATE WAFER

⟶ = DIRECTION OF GAS FLOW

⟶ = DIRECTION OF TRAVEL

A. Horizontal tube displacement flow reactors.
B. Rotary vertical batch-type reactors.
C. Continuous reactors employing premixed gas flow fed through an extended area slotted disperser plate.
D. Continuous reactors employing separate, nitrogen-diluted oxygen and hydride streams that are directed toward the substrate by laminar flow nozzles.

Figure B-1. Operating principles of the basic types of CVD reactors for preparing passivation overcoat layers.

exemplified. Data on commercially available equipment to be described were derived from information supplied by the manufacturer rather than by experimental studies by the author other than inspection of the equipment. (This statement applies only to the CVD reactor system and equipment section, not to the subsequent experimental section where results of original research are presented.)

C. HORIZONTAL DISPLACEMENT FLOW REACTORS

Horizontal tube reactors consisting of an elongated quartz tube of circular or rectangular cross section, as used in high-temperature semiconductor processing, were the first types used in CVD of oxides at low temperature. The diluent and reactive gases are continually being supplied, and are usually mixed and dispersed at the point of entry into the tube. The mixed gas stream passes over the heated substrates which rest on a tilted wafer carrier. Heat may be supplied resistively from outside the tube or from within the wafer carrier. Displacement-type forced laminar gas flow of this type features a low degree of gas mixing, requiring careful optimization of the gas dynamics to obtain good film uniformity in thickness and composition. Critical factors affecting film uniformity are substrate positioning, temperature profile of the deposition zone, geometry of reactor, and exhaust configuration. Several types of CVD systems based on horizontal displacement flow reactors are commercially available. A schematic of the basic system is shown in Fig. B-1A.

A horizontal, internally resistance-heated flow reactor manufactured by Applied Materials Technology, Inc.* has a capacity for ten 5-cm-diameter wafers per batch. Cycle time for a 5000-Å-thick SiO_2 deposition is approximately 15 minutes. Uniformity of film thickness is specified as typically $\pm$7.5% within a wafer, $\pm$10% from wafer to wafer within a run.

A tubeless horizontal production reactor of entirely different design is manufactured by Thermco.** It utilizes a resistance-heating block with the gases introduced across its width to minimize depletion of the gas

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*AMS-2600 Silox System, Applied Materials Technology, Inc., 2999 San Ysidro Way, Santa Clara, CA 95051.

**Thermco Thor II Oxide Reactor, Thermco Products Corp., Box 1875, Orange, CA 92667.

reactants moving across the heating platen. The gas delivery system has provision for bi-directional gas entry/exhaust. The unit has a loading capacity for 27 5-cm wafers and a deposition rate capability of 1000 Å/min. The film uniformity within a wafer is ±5%, and ±10% from wafer to wafer.

A developmental close-spaced horizontal cold-wall reactor has also been described [B-7]. A high-velocity stream of the premixed gases passes over the resistance-heated substrate wafers parallel to their surface. The reactor can accommodate 28 wafers of 5-cm diameter.

D. ROTARY VERTICAL BATCH REACTORS

In rotary vertical reactors for batch processing, the substrate wafers are placed on a plate rotating above a resistance heater (Fig. B-1B). The reaction chamber consists of a cylindrical, conical, or hemispherical bell jar that may have provisions for cooling. The gases enter through single or multiple inlets from the top or side of the belljar, pass over the substrates, and exit at the bottom of the chamber below the rotating plate. The incoming gases mix gradually with the partially reacted gas before passing over the substrates. Intentional changes in gas composition therefore proceed gradually (rather than abruptly as in the case of horizontal flow reactors), which for the present application is advantageous, particularly if double layers (PSG + SiO_2) with a graded interface are desired. The geometry of the reaction chamber and the configurations of the gas inlet and exit openings are critical in attaining the most effective gas flow dynamic conditions required for producing uniform deposits.

The construction and performance of a reactor of this type designed for research applications was described previously [B-8]. The unit consists of gear-driven discs heated by conduction from a hotplate. Planetary motion of the substrates promotes maximum uniformity of the film deposits by thermal and gas dynamic averaging effects over a wide range of operating conditions. A modified single-rotation reactor* we have built for research and pilot

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B-7. A. Mayer, K. Strater, and D. A. Puotinen, *Manufacturing Techniques for Controlled Deposition and Application of Doped Oxides*, Tech. Rpt. AFML-70-TR-91 (September 1970).

B-8. W. Kern, RCA Review 29, 525 (1968).

*W. Kern and A. W. Fisher, unpublished work.

production use is described in greater detail in Appendix D. Five wafers of 5-cm diameter can be coated simultaneously with a uniformity that is indistinguishable by visual inspection (±2% at 1-μm film thickness) from wafer to wafer, if the nitrogen diluent flow is properly balanced. Nine wafers can be coated simultaneously if thickness uniformity is less critical. Very high deposition rates (up to 1 μm/min) can be obtained, although these are not normally used.

Several important considerations should be noted for designing and constructing the gas-handling equipment associated with in-house built units. Heliarc-welded and leak-checked stainless-steel tubing is recommended for hydrides of high concentration (greater than 5 percent). Leak-tested polyethylene tubing is advantageous for oxygen, nitrogen, and diluted hydrides, particularly in the terminal parts of the installation where flexibility and quick removability for clean-up is important. Metering of the hydride gases is best done with calibrated mass flowmeters and controllers. Float-type flowmeters are perfectly adequate for oxygen and nitrogen. It is very important to have provision for nitrogen purging of the entire hydride line system, including the pressure regulators back to the source tanks, to be able to remove residual hydrides after deposition work is terminated at the end of the day, or to use nitrogen flow during setup to conserve expensive hydride gases. Additional recommendations, including valves, temperature measurement, and safety considerations were noted in previous publications [B-8 to B-10]. A variety of gas flow control panels are now available commercially* or can be obtained custom built for any desired requirements.**

A commercial rotary, resistance-heated vertical reactor system for semi-continuous operation is sold by Unicorp, Inc.† It features premixed gas input through four tubes inside the conical deposition chamber for uniform distribution, and has separate stations on a carrier disc for wafer loading/unloading, preheating, deposition, and cooldown. Up to seven 5-cm

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B-9. N. Goldsmith and W. Kern, RCA Review 28, 153 (1967).
B-10. J. A. DeNicola and R. D. Mastropiero, Solid State Technology 15, No. 2, 51 (1972).

*For example, Matheson Gas Products, P. O. Box 85, 932 Paterson Plank Rd., East Rutherford, NJ 07073.

**For example, Tylan Corp., 4203 Spencer St., Torrance, CA 90503.

†Rotox-60, Unicorp Inc., 625 N. Pastoria Dr., Sunnyvale, CA 94086.

wafers can be accommodated per station. The maximum oxide deposition rate is 1700 Å/min, with a conservatively estimated overall uniformity of ±5%.

An oxide reactor* featuring two planetary systems arranged concentrically was described in 1971 [B-11]. In this complex reactor, the driver element is a cylinder rotating within an annular spacing between a circular inner resistance-heated block and an outer heater ring. The gases are dispensed in a counter-rotating array to ensure good mixing of the gas flows, resulting in a thickness uniformity of ±1.5%.

Vertical CVD reactor systems with rotating gas feed over a stationary, resistance-heated plate are manufactured by Phoenix Materials Corporation.** Units for processing either 26 or 70 5-cm wafers are available.

A vertical cold wall reactor system by HLS Industries†, featuring a periphase gas injection arrangement that introduces the gases into the reactor through two concentric wall sections, was described recently. Low gas depletion losses and elimination of static boundary conditions result in uniform deposits.

E. CONTINUOUS REACTOR SYSTEMS

Application of continuous processing concepts to CVD reactor systems makes large-scale production of oxide and glass films possible at lower operating cost than the use of batch-type reactors, especially if combined with automation that is particularly suitable for such systems. A CVD processor of this type is manufactured by Applied Materials Technology, Inc.[B-12].†† The substrate wafers are moved conveyor-fashion on Inconel trays through the reactor at constant speed. Heating is by radiation from a resistance heater.

B-11. J. Wollam, Solid State Technology 14, No. 12, 72 (1971).
B.12. W. C. Benzing, R. S. Rosler, and R. W. East, Solid State Technology 16, No. 11, 37 (1973).

*Oxide Reactor 315 (no longer manufactured), Materials Research Corp., Orangeburg, NY 10962.

**Phoenix Materials Corp. Vapor Deposition Systems, 500 and 1500 Series, M.R. 10, Kittatinny, PA 16202.

†Univax Reactor Model 100-60-30, HLS Industries, 762 Palomar Ave., Sunnyvale, CA 94086; described in *Cold Wall Semicon Reactor*, Circuit Manuf., 14, 47 (November 1974).

††AMS-2000 Continuous Silox Reactor, Applied Materials Technology, Inc., 2999 San Ysidro Way, Santa Clara, CA 95051.

The nitrogen, oxygen, and hydride gas streams are combined before entering the manifolds to the slotted disperser plate from which the gas mixture passes by laminar flow over the wafers. The cross-flow gas dispersion and the relatively close spacing (approximately 1 cm) of the substrate to the water-cooled, extended area disperser plate minimize undesirable homogeneous gas phase nucleation. Wafer-to-wafer uniformity of film thickness is better than ±5%, with unusually low densities of particulate inclusions and pinholes. The machine has a throughput capacity of 400 5-cm wafers per hour with a 1-μm-thick SiO_2 deposit. A schematic is shown in Fig. B-1C.

In nozzle reactors, separate streams of nitrogen-diluted hydrides and oxygen impinge on the substrate surface where they mix and react, forming the oxide or glass films. The effects of numerous nozzle geometries on the resulting oxide deposition pattern has been examined in detail by several investigators [B-13,B-14]. An open horizontal circular compound nozzle was empirically found most desirable, with the deposition occurring where the heated moving wafer intersected the unconfined jet of the reacting gases, while the exhaust gases were removed by a pump. Uniformity of ±5% was obtained across a 5-cm wafer [B-13].

A commercially available continuous reactor system based on nozzle-type gas dispersion is manufactured by Pacific Western Systems, Inc.[B-15].* In this unit the nitrogen-diluted oxygen and hydrides are directed to the substrate surface as separate streams flowing through the laminar flow slots forming the nozzles. The water-cooled nozzle array unit is 4-cm wide and 25-cm long, extending over the width of the heater block assembly. The space between the nozzle array and the wafer surface during deposition is only about 2.5 mm and defines the reaction zone where the gases mix and react forming the oxide or glass films. Exhaust gases are removed through

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B-13. S. S. Flaschen, H. C. Evitts, and J. R. Black, *Large Area Semiconductor Surface Passivation Production Refinement Program*, Contract DA-36-039-AMC-02280(E), Final Tech. Rpt. (1965).

B-14. M. L. Barry, in *Chemical Vapor Deposition*, J. M. Blocher, Jr., and J. C. Withers, Eds., (The Electrochemical Society, New York, 1970), pp. 595-617.

B-15. Pacific Western Systems, Inc.; Electronics 47, 138 (Sept. 5, 1974).

*PWS Model 2000 Vapor Deposition System, Pacific Western Systems, Inc., 855 Maude Ave., Mountain View, CA 94040.

separate slots at the periphery of the nozzle array. The wafers traverse under the nozzle unit on a resistance-heated conveyor plate at a variable speed. The wafer plate (18 cm x 41 cm) accepts 21 5-cm wafers. Unusually high film deposition rates are obtainable with this system, and the density of particulate impurities in the film deposits is low. The thickness uniformity for SiO_2 films is $\pm 5\%$, with a deposition of 1 μm at a rate of 6.3 cm/min travel speed. Figure B-1D depicts schematically the construction of this type of nozzle reactor.

A continuous nozzle reactor system is also marketed by Chemical Reactor Equipment, Inc.[B-16].* A high-velocity nozzle is used, through which the gases are mixed and impinged over a relatively small area of deposition surface. A continuous mode of operation results from the reciprocating motion of the substrate under the nozzle. A five-nozzle system is capable of depositing 0.5-μm SiO_2 on up to 350 5-cm wafers per hour, with excellent uniformity.

B-16. Chemical Reactor Equipment, Inc.; Electronic News p. 60, June 5, 1972.
*CRE 1101, 1103, 1105, Chemical Reactor Equipment, Inc., 1080 HE Duane Ave., Sunnyvale, CA 94086.

REFERENCES

B-1. C. F. Powell, J. H. Oxley, and J. M. Blocher, Jr., Eds., *Vapor Deposition*, (John Wiley and Sons, Inc., New York, 1966).

B-2. D. S. Campbell, in *Handbook of Thin-Film Technology*, L. I. Maissel and R. Glang, Eds., (McGraw-Hill Book Co., New York, 1970), pp. 5-1 - 5-25.

B-3. E. L. MacKenna, Proc. 1971 Semiconductor/IC Proc. and Prod. Conf., Ind. and Sci. Conf. Mtg., Chicago, Ill., (1971) pp. 71-83.

B-4. *Chemical Vapor Deposition* (Intn'l Conf.): J. M. Blocher, Jr., and J. C. Withers, Eds., - Second Intn'l Conf., The Electrochemical Soc., New York, 1970; F. A. Glaski, Ed. - Third Intn'l Conf., The American Nuclear Society, Hinsdale, Ill., 1972; and G. F. Wakefield and J. M Blocher, Jr., - Fourth Intn'l Conf., The Electrochemical Soc., Inc., Princeton, N.J., 1973.

B-5 M. L. Hammond, J. Vac. Sci. Technol. 10, 268 (1973).

B-6. W. C. Benzing and R. Fisk, Solid State Technology 18, No. 1, 39 (1975).

B-7. A. Mayer, K. Strater, and D. A. Puotinen, *Manufacturing Techniques for Controlled Deposition and Application of Doped Oxides*, Tech. Rpt. AFML-70-TR-91 (September 1970).

B-8. W. Kern, RCA Review 29, 525 (1968).

B-9. N. Goldsmith and W. Kern, RCA Review 28, 153 (1967).

B-10. J. A. DeNicola and R. D. Mastropiero, Solid State Technology 15, No. 2, 51 (1972).

B-11. J. Wollam, Solid State Technology 14, No. 12, 72, (1971).

B-12. W. C. Benzing, R. S. Rosler, and R. W. East, Solid State Technology 16, No. 11, 37 (1973).

B-13. S. S. Flaschen, H. C. Evitts, and J. R. Black, *Large Area Semiconductor Surface Passivation Production Refinement Program*, Contract DA-36-039-AMC-02280(E), Final Tech. Rpt. (1965).

B-14. M. L. Barry, in *Chemical Vapor Deposition*, J. M. Blocher, Jr., and J. C. Withers, Eds., (The Electrochemical Society, New York, 1970), pp. 595-617.

B-15. Pacific Western Systems, Inc.; Electronics 47, 138 (Sept. 5, 1974).

B-16. Chemical Reactor Equipment, Inc.; Electronic News p. 60, June 5, 1972.

APPENDIX C

DIELECTRIC-RELATED AND GLASSING-RELATED FAILURE MECHANISMS OF INTEGRATED CIRCUITS

by

G. L. Schnable and W. Kern

A. INTRODUCTION

Failure mechanisms that are related to the dielectric or are caused by glass overcoating of metallized ICs can be divided into the following major groups:

(1) Localized structural and compositional defects in dielectric.

(2) Nonlocalized chemical and physical defects in dielectric.

(3) Chemical interactions of dielectric with metallization and moisture.

(4) Ionic and electronic charge motion and conductivity in glass and oxide films, on their surfaces, and along their various interfaces.

(5) Assorted defects introduced during passivation processing.

A more detailed outline of general dielectric-related failure mechanisms is presented in Table C-1; types of specific glassing-related failures of integrated circuits are listed in Table C-2. Many of these defects arise from improper processing or from inherent mutual incompatibility of the films with the metallization. It is important that they be detected and identified so that steps can be taken to eliminate them.

B. LOCALIZED STRUCTURAL AND LOCALIZED COMPOSITIONAL DEFECTS IN DIELECTRIC FILMS

Particulate contaminants (dust or reaction products) in the gas or vapor streams or on the substrate surface during chemical vapor deposition interfere with film nucleation and proper growth, resulting in voids, thin spots, partial or complete pinholes, or hillocks. Particulate impurities that become embedded in the film constitute a potential device failure due to local weakening of the dielectrical strength.

Pinholes in the films can also be caused by problems in photolithographic processing if the photoresist protects the film incompletely, or if the

Table C-1. General Dielectric-Related Failure Causes

No.	Basic Failure Cause
1	Localized structural defects
2	Localized deviation in chemical composition
3	Nonlocalized defects arising from incorrect physical and chemical film properties
4	Chemical interaction of dielectric with moisture
5	Electrolytic corrosion of metallization (interaction with dielectric, moisture, and ions)
6	Electronic and ionic charge motion on surface, in bulk, and at interfaces
7	Polarization instability of PSG caused by excessive P_2O_5 concentration
8	Excessive residual tensile stress
9	Insufficient impurity-gettering effectiveness of passivation layer(s)
10	Depletion of P_2O_5 from PSG by Al at Al/PSG interface, leading to Na^+ permeable Al/SiO_2 interface structure

Table C-2. Glassing-Related Failure Causes of Integrated Circuits

No.	Basic Failure Cause
1	Insufficient passivating film thickness
2	Insufficient P_2O_5 content in PSG
3	Excessive P_2O_5 content in PSG
4	Incorrect dielectric layer structure
5	Organic residual impurities on device surface prior to CVD
6	Ionic contaminants on device surface prior to CVD
7	Formation of hard-to-etch aluminosilicate interface on Al bonding pads
8	Particulate contaminants in gas stream during CVD
9	Photoresist and etching defects leading to pinholes
10	Microcracks due to incorrect material choice or processing
11	Nonuniform substrate heating (warped wafers) during CVD
12	Na^+ in CVD SiO_2 not sufficiently gettered by PSG
13	Inherently poor adhesion of CVD dielectric films to certain metals (such as gold)
14	Excessively high temperature during CVD or densification

etchants used in the chemical patterning process penetrate through pinholes or thin spots in the resist coating itself.

Gas bubbles that weaken the dielectric strength in an insulator may form during chemical vapor deposition in the presence of nucleating particulate contaminants. Unacceptable topographical defects, such as excessive surface roughness, may also arise during film deposition under incorrect process conditions.

Microfractures are a very common and important mode of a localized defect which is caused by excessive stress (see Section IV). Other localized defects include embedded foreign particles, microcrystallites, or precipitates caused by reactions in the solid state. Oxides and glasses may devitrify in local regions under certain conditions, and may deleteriously affect film integrity and dielectric strength.

The topography of the substrate being coated with a dielectric film may cause defects in the film deposit, such as thin spots over sharp edges, or film discontinuities in corners at the base of steep steps that may lead to electrical short-circuits. A survey of failure modes [C-1] and discussion of methods specifically designed to improve the reliability of electron devices by optimized coverage of surface topography [C-2] were presented recently.

C. NONLOCALIZED CHEMICAL AND PHYSICAL DEFECTS IN DIELECTRIC FILMS

Chemical imperfections include deviations in film composition, which may be nonstoichiometry in the case of single-component dielectric films, or incorrect percentages of one or several components in a binary or multiple component material. Chemical impurities in the bulk or the surface of a film are another common chemical imperfection which may deleteriously affect device performance due to current conduction across the contaminated film surface, for example. Incorrect layer composite structures, such as an inappropriate sequence, thickness, or composition of various dielectric layers,

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C-1. G. L. Schnable and R. S. Keen, in *Advances in Electronics and Electron Physics*, Vol. 30, L. Marton, Ed., (Academic Press, New York, 1971), p. 79.

C-2. W. Kern, J. L. Vossen, and G. L. Schnable, 11th Ann. Proc. Reliability Physics, p. 214 (1973).

may give rise to excessive stresses and/or a variety of other problems, such as poor adherence, instability in composition, or intolerable degrees of hygroscopicity (in the case of excess B_2O_3 or P_2O_5 in a glass) [C-3 - C-5]. These basic causes may deleteriously affect important mechanical and electrical film properties, such as thermal expansion and stress, bulk and surface resistivity, dielectric strength and dissipation, charge density, and polarizability.

Of particular concern in IC glassing is the presence of residual stress in the films, which may lead to cracks in the glass. Thermal expansion is one major factor determining the magnitude and the sign of the residual stresses at interfaces between dielectric layers or at the interface between a dielectric and the metallization, and, of course, between the thermal SiO_2 primary passivating layer and the thick silicon substrate crystal. A summary of stress data for various dielectric films of interest here was presented in Table VI [C-6]. The stress inversion data for CVD SiO_2 shown in the table illustrate the complexity of the mechanical stresses inherent in device wafers. However, variations in CVD processing parameters and subsequent heat treatment of the amorphous dielectric films can significantly reduce these stresses. For example, for a given growth rate and thickness, the tensile stress is greatest for pure SiO_2 films and decreases with increasing P_2O_5 concentration in the glass. Similar results are observed with borosilicates and other CVD glass films. Temperature and film deposition rate are also factors that affect the stress level in a complicated manner. Part of this contract involved work on minimizing residual stresses through control of CVD parameters and heat treatment.

Microfractures can be caused by these stresses between the dielectric film and the substrate, or between different types of films. Stress in films may develop during growth, deposition, pattern etching or heat treatments, especially if the linear thermal expansions of the components are mismatched.

C-3. E. Arai and Y. Terunuma, J. Electrochem. Soc. 121, 676 (1974).
C-4. Staff article, Electronics 47, No. 8, 34 (1974).
C-5. W. M. Paulson and R. W. Kirk, 12th Ann. Proc. Reliability Physics, p. 172 (1974).
C-6. J. L. Vossen, G. L. Schnable, and W. Kern, J. Vac. Sci. and Technol. 11, No. 1, 60 (1974).

Cracks may form particularly during thermal shocking preceding or following high-temperature processing, excessive thermal contraction on cooling, or temperature stress cycling and life testing of devices.

D. CHEMICAL INTERACTION OF DIELECTRIC WITH METALLIZATION

The most commonly encountered failure mode of this type is metal corrosion at the glass-aluminum interface. This is brought about by the leaching of P_2O_5 from PSG, or of B_2O_3 from BSG [C-3] by moisture, especially during pressure cooker testing or life tests under electrical bias in high humidity. These oxides react with moisture forming phosphoric and boric acids, respectively. The acids readily attack the aluminum, especially the phosphoric acid. To remedy this, the glass composition or the densification may need to be changed, or a protective interlayer of SiO_2 or Si_3N_4 may have to be deposited.

It should be recalled in this connection that aluminum is extremely prone to corrosion in the presence of certain impurities, even during its deposition and processing. One of the more serious problems of aluminum corrosion occurs in plastic-encapsulated devices [C-5,C-7,C-8], especially during life testing at high humidity.

With gold metallization systems, one problem caused by electrolysis is shorts due to dendrite formation [C-9,C-10]; compatible glass passivation layers would be expected to greatly reduce susceptibility to corrosion in such devices.

E. ELECTRICAL EFFECTS CAUSED BY INTERACTION OF MOISTURE WITH DIELECTRIC

Penetration of water vapor through the glass passivation layers can give rise to several types of failure mechanisms, especially in the presence of

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C-7. H. Koelmans, 12th Ann. Proc. Reliability Physics, p. 168 (1974).

C-8. R. A. Kokosa, B. R. Tuft, and E. D. Wolley, "Progress in High Voltage, High Frequency Planar SCR Technology," IEEE Industry Applications Mtg. Proc., Milwaukee, Wisc., p. 87 (October 1973).

C-9. B. Reich and E. B. Hakim, Proc. 1974 Ann. Reliab. and Maint. Symp., p. 396 (January 1974).

C-10. J. J. Mazenko, Proc. Intn'l Soc. for Hybrid Microelectronics Symposium, p. 450 (1974).

ionic contaminants [C-11]. Electrochemical corrosion of aluminum by moisture, as pointed out above, can cause partial or complete circuit breakdown [C-4, C-5,C-7,C-8,C-12].

Moisture on the surface or in dielectric interfaces of field-effect devices can provide mobility to insulator surface charges, thereby extending the gate potential over neighboring surface regions.

Experimental studies have shown that passivation glasses containing a high moisture content can have appreciable bulk conductivity. In integrated circuits, electrical leakage conduction through the glass can, for certain geometries and glass compositions, exceed leakage in the silicon itself. Some reported cases of pattern sensitivity in MOS LSI arrays may be in part attributable to conduction through passivation layers.

The amount of moisture absorbed or adsorbed determines the conductivity of the dielectric surface or its interfaces. This in turn affects the electrolytic conduction between electrically biased metallization paths, leading to current leakage or electrical opens, depending on polarity.

Effects of lateral surface ion migration are directly related to the degree of humidity to which the device is exposed, as noted by Temofonte and Szedon [C-13]. Current conduction across the dielectric surface may result.

In general, the presence of an excess amount of moisture on or in dielectrics causes degradation of the dielectric properties with consequent electrical instability of the device.

F. AFFINITY OF DIELECTRICS FOR WATER

The affinity of different types of dielectrics for water varies, depending upon the dielectric composition [C-14]. For example, silicon nitride and aluminum oxide exhibit a lower affinity than silicon dioxide, which, in turn, has a much lower affinity than certain silicates such as BSG or PSG. In

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C-11. D. S. Peck and C. H. Zierdt, Jr., 10th Ann. Proc. Reliability Physics, p. 146 (1974).
C-12. F. N. Sinnadurai, Microelectronics and Reliab. 13, 23 (1974).
C-13. T. A. Temofonte and J. R. Szedon, 9th Ann. Proc. Reliability Physics, p. 107 (1972).
C-14. J. Sato, Y. Ban, and K. Mada, 9th Ann. Proc. Reliability Physics, p. 96 (1971).

these glasses, the affinity to water (or hygroscopicity) increases as the B_2O_3 [C-3] or P_2O_5 [C-5,C-15] concentration increases. We found that CVD undensified BSG containing more than 25 mol % B_2O_3 is sufficiently hygroscopic to devitrify in humid room air. Information published by Nagasima et al. [C-15] indicates that densification of PSG suppresses the tendency to devitrify.

G. IONIC AND ELECTRONIC CHARGE MOTION IN DIELECTRIC LAYERS

These two types of mechanisms, causes of potential failure, are of extreme importance in primary passivation, where the dielectric is directly in contact with the p-n junction and the silicon surface. Inversion layers and excessive leakage currents may form as a result of sodium ion contamination through insufficiently impermeable dielectrics, for example, and seriously impair or degrade device performance. Charge movement of this sort can be precisely measured by capacitance-voltage-bias-temperature (CVBT) testing [C-16 to C-18] on metal-insulator-semiconductor structures.

Mechanisms causing unwanted inversion layers and their effects on device parameters have been described recently [C-16,C-17,C-19 to C-22]. Mechanisms based on oxide bulk ion drift are most directly related to glass passivation because they can be controlled to a considerable extent by application of PSG gettering. Effects of inversion layers on device parameters may manifest themselves in parasitic MOS transistor action, decreased current gain, and increased reverse current.

A related charge phenomenon, known as bias-induced inversion layers, has been described by Haberer and Bart [C-22]. These layers have been found associated with defects in the primary passivation oxide or in the thermal

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C-15. N. Nagasima et al., J. Electrochem. Soc, 121, 434 (1974).
C-16. B. E. Deal, J. Electrochem. Soc, 121, 198C (1974).
C-17. E. H. Nicollian, J. Vac. Sci. and Technol. 8, No. 5, S39 (1971).
C-18. K. H. Zaininger, RCA Review 27, 341 (1966).
C-19. W. H. Schroen, J. G. Aiken, and G. A. Brown, 10th Ann. Proc. Reliability Phys., p. 42 (1972).
C-20. W. H. Schroen, 11th Ann. Proc. Reliability Phys., p. 117 (1973).
C-21. G. A. Brown, K. Lovelace and C. Hutchins, 11th Ann. Proc. Reliability Phys., p. 203 (1973).
C-22. J. R. Haberer and J. J. Bart, 10th Ann. Proc. Reliability Phys., p. 106 (1972).

oxide/CVD oxide- or glass interfaces. To attain a high degree of reliability of linear integrated circuits, it is essential to produce a primary SiO_2 passivating layer of very high quality and purity to minimize the tendency of the fields to accumulate electronic charge over the underlying silicon. Similarly, the interface between the primary passivation oxide and the CVD oxide or glass overcoats must be of high purity also to minimize any lateral charge movement along this interface that could induce inversion channels [C-22].

H. DEVICE FAILURES INTRODUCED DURING GLASS PASSIVATION PROCESSING

CVD glass passivation and its associated processing operations may inadvertently introduce certain types of defects, if not controlled properly. For example, too thin a glass layer may not prevent ion migration effects, and therefore lead to insufficient passivation and metal protection. A PSG with low P_2O_5 content may result in inadequate gettering of externally introduced contaminants such as sodium ions; it may also cause cracking of the glass because of excessive stress [C-5]. Too high a concentration of P_2O_5, on the other hand, may result in current leakage across the surface or even in a hygroscopic glass which may cause corrosion problems [C-5]. In the case of multilayered dielectric structures, incorrect film thicknesses can cause residual stresses that may lead to microcracks with consequent impairment of protection against external contaminants.

Silicon dioxide films deposited from semiconductor-grade silane (SiH_4) and oxygen are known to contain some sodium that may deleteriously affect MOS devices. PSG passivation of proper composition is capable of gettering this contaminant to the extent that instability problems are eliminated.

The quality of adhesion of the CVD glass to a substrate is dependent upon the cleanliness of the surface, the nature of the substrate material, and the exact condition of the surface. Peeling and blistering can generally be avoided by observing clean processing conditions, except in a few special cases which are material-dependent. One of these is gold metallization. There is no chemical bonding mechanism between gold and a glass or oxide, and peeling or flaking frequently result. A thin interlayer of chromium,

which bonds well to each class of material, will overcome this particular problem, but may decrease the conductivity of the metallization.

Incomplete removal of glass over the aluminum bonding pads during delineation etching is a failure mechanism associated with wire bonds. Excessively high temperatures during CVD can cause formation of an Al_2O_3-rich aluminosilicate glass at the interface, which can be extremely difficult to remove by chemical etching.

This discussion of possible and frequently observed types of failures is by no means complete but gives an illustration of the technical problems that must be constantly considered in the course of passivation work.

I. EFFECTS OF DENSIFICATION TREATMENTS

One specialized topic not included in the introductory list of failure causes is that of densification side effects, which can be desirable or deleterious. Heat treatments can have different effects on mechanical stresses. For example, heat treatments that are at a temperature above the chemical vapor deposition temperature result in initially increased tensile stress (because the thermal coefficient of expansion of SiO_2 or of PSG is less than that of aluminum or of silicon). Complete annealing at a heat-treatment temperature of 540°C, for example, would result, upon cooling the wafer to room temperature, in compressive stresses in the passivating glass. The degree of stress relief attainable in deposited PSG films as a function of densification had not been determined prior to the beginning of this contract. The influence of these residual stresses on the failure of devices must be determined, recognized, and further examined. Strongest effects should show up during thermal cycling and thermal shock testing, where the differential in thermal expansion coefficients may cause mechanical damage to the device.

J. GLASSING-RELATED FAILURE MECHANISMS OBSERVED ON COMMERCIAL INTEGRATED CIRCUITS

All of the failure modes discussed are observed in one form or another on commercial integrated circuits. An exact assessment of the percentage

of any particular type of glassing-related failure mechanism is very difficult to provide because of the multiplicity of factors involved in analyzing actual devices, especially if decapsulation and chip isolation are required to secure this information. Even excellent reviews of device reliability frequently contain no such data (see, for example, Peattie et al. [C-23] and Proc. IEEE, February 1974). Very recent papers have shown that passivation can improve the reliability of aluminum metallization in microwave power transistors [C-24] and that defects in passivation layers can adversely affect reliability [C-25,C-26] of bipolar and MOS devices available from a variety of sources. The largest class of MOS IC failures can be categorized as "bake-recoverable." The recovery process frequency has an activation energy of about 1 eV, an energy level indicative of motion for alkali ions or protons either in or on the surface of the dielectric. We suspect that this phenomenon is related to the quality of the glass layer, and experimental evidence appears to support this statement.

Silicon ICs packaged in frit-sealed ceramic packages have been susceptible to microcracks in the SiO_2 on PSG overcoat, particularly over large areas of aluminum such as those used as counterelectrode on top of a capacitor [C-27, C-28]. The cause of this failure is the relatively high temperature (530°C) needed for fusion of the glass frit sealing the ceramic package. The stress in the glass overcoat passivation becomes so great that stress release occurs by cracking, especially over large metal areas and along their edges. Device failure may occur subsequently, due to penetration of sodium ions through the cracks and lateral penetration along the metal/glass interface or in the field oxide. The sodium originates from the glass frit and cannot be avoided in the atmosphere of the package; it is normally gettered by the PSG. Similarly, tensile cracks can occur during eutectic bonding of devices, particularly when chip bonding temperature exceeds the glass deposition temperature.

C-23. C. G. Peattie et al., Proc. IEEE 62, 149 (1974).
C-24. A. C. MacPherson et al., Paper No. 3.4 for presentation at 1975 Intn'l Reliability Phys. Symp., IEEE, Las Vegas, Nev., April 2, 1975.
C-25. J. J. Bart, IEEE Trans. Electron Devices ED-16, 351 (1969).
C-26. L. V. Gregor, Proc. IEEE 59, 1390 (1971).
C-27. W. Kern, RCA Review 34, 655 (1973).
C-28. W. Kern, Solid State Technology 17, No. 3, 35 (1974) and No. 4, 78 (1974).

The appearance and dimensions of these cracks have been shown in metallurgical and SEM photomicrographs in two recent publications [C-27,C-28].

Pinholes in the CVD oxide or glass passivation over aluminum have been found in linear bipolar ICs to be the cause of increased susceptibility of metal corrosion during device operation which led to serious field failure [C-4,C-5]. Pits and microcracks in the passivation can have similarly disastrous effects. Structural defects of this sort often open the way to migrating ionic contaminants that are always present in plastic encapsulants or in the device surfaces after chip mounting, bonding, and normal processing operations.

Ionic contaminants that may get introduced during pre-passivation processing, or impurities such as incompletely removed photopolymer films, resist stripping agents, or highly corrosive aluminum etchants may remain as residues on the device wafer surfaces, especially if the aluminum has a large surface area due to graininess or surface roughness. As a consequence, gases may be evolved during CVD glassing and become entrapped at the interface, causing pinholes, blisters, and corrosion-susceptible defects.

In MOS read-only memories, one technique which is widely used in the industry is to prepare all memory transistors with thin (gate) oxides (for example, all 1024 memory transistors in a 1024-bit ROM) and to metallize. The desired bit pattern is then etched in the metallization pattern, with gates that remain metallized being permanent "1s" and unmetallized gates being permanent "0s". The circuit is glass passivated and packaged. If, due to improper processing procedures, the sheet conductivity of the interface between the thermally grown SiO_2 layer and the vapor-deposited passivating glass layers is high, or the sheet conductivity of the CVD glass bulk is high, the circuit will not be reliable. On operating life, charge will build up at the thermal oxide - CVD oxide interface over the gate regions of unmetallized memory transistors, particularly those transistors adjacent to memory transistors with metallized gates. When the potential at this interface (approximately 0.1 μm from the silicon) builds up to a potential in excess of the device threshold voltage (3 V, for example), the device turns on, and thus a functional failure of the circuit occurs. This type of failure mechanism is somewhat similar to that previously mentioned for other types of devices, but in

this case occurs because of inversion of a region in which the thermal oxide is thin (gate) oxide rather than thicker oxide (field oxide in MOS circuits or collector oxide in bipolar circuits).

Another type of MOS failure mechanism, somewhat similar to the ROM case, can occur when the metal is partially missing over the gate region of MOS transistors, leaving an unmetallized region extending from source to drain, as described by Forsythe [C-29]. This type of problem can arise because of design errors, photolithography problems, metal scratches or misalignment. Passivating glass, unless deposited under conditions which produce low interfacial and deposited glass sheet conductivity, will not prevent the problem.

Concise reliability data, not exclusively related to glass passivation, have been compiled for MOS and CMOS ICs and are available in recent papers [C-30].* Reliability aspects of plastic-encapsulated linear bipolar ICs have also been published recently [C-31,C-32].

K. LATERAL MIGRATION OF ALKALI IONS

It has been observed that in devices which had cracks in the phosphosilicate passivation glass (or had other localized dielectric integrity problems), passage of contaminant alkali ions to the underlying thermally grown SiO_2 layer resulted in subsequent instability problems. In one case, MOS integrated circuits containing p-channel enhancement-mode MOS transistors with relatively large source-to-drain spacings were involved, and high failure rates were experienced when devices were baked without bias, followed by operating life tests. In another case, circuits containing n-channel enhancement-mode MOS transistors were involved, and when operating life tests were run, higher incidence of excessive leakage was observed on unbiased inputs than on reverse-biased inputs. We interpret these as cases of lateral migration of assembly-introduced alkali ions under the gate oxide under a concentration

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C-29. D. D. Forsythe, Microelectronics and Reliability 8, 339 (1969).
C-30. G. L. Schnable, H. J. Ewald, and E. S. Schlegel, IEEE Trans. Reliability R-21, 12 (1972).
C-31. H. Khajezadeh, 11th Ann Proc. Reliability Physics, p. 236 (1973).
C-32. H. Khajezadeh and A. S. Rose, paper presented at 1975 Reliability Phys. Symp., IEEE, Las Vegas, April 1975.

*M. N. Vincoff and G. L. Schnable, "Reliability of Complementary MOS Integrated Circuits," paper to be published in IEEE Trans. Reliability, October 1975.

gradient in the case of no bias; with bias the ions are held at the surfaces of negatively-biased metal lines and thus tend not to move laterally.

L. POSSIBLE MECHANISM FOR LOSS OF PSG GETTERING EFFECTIVENESS

A possible new mechanism not previously recognized could provide an additional or alternative explanation of one type of failure mode. Aluminum may react with the P_2O_5 and the SiO_2 in the PSG under the thermal conditions used for CVD, forming Al_2O_3 and a P_2O_5-depleted glass interface layer consisting essentially of SiO_2. The sodium ion gettering effectiveness at this interface may thus be diminished or lost, allowing sodium ions to diffuse laterally into the sensitive substructure of the device, where they would cause electrical instability.

M. RELIABILITY IMPROVEMENT BY GLASSING

It has been shown by several manufacturers that frit-sealing of MOS integrated circuit arrays causes alkali-type threshold voltage instabilities when no passivation glass is used or when the passivating glass is undoped SiO_2, but does not result in instabilities when the passivating layer is phosphosilicate glass. The explanation of the observed difference is that the sealing glass frit composition contained an alkali compound, which became volatilized during sealing, condensing on the passivated device surface. The alkali contaminant in the sealing glass was an oxide added to lower the softening points of the glass; was present as an impurity in the glass, nucleating agent or binder; or a combination of these existed.

The improvement of reliability of surface-sensitive integrated circuits due to glass passivation under suitable conditions has been reported in a number of papers [C-5,C-20,C-33 to C-35].

C-33. P. Flaskerud, Proc. 1971 Semiconductor/IC Proc. and Prod. Conf., p. 40, Ind. and Sci. Conf. Mgt., Chicago, Ill. (1971).

C-34. J. H. Lindwedel, *Reliability Evaluation of LIS Microcircuits*, p. 181, Final Report, RADC-TR-73-127, May 1973.

C-35. M. M. Schlacter et al., IEEE Trans. Electron Devices ED-17, 1077 (1970).

REFERENCES

C-1. G. L. Schnable and R. S. Keen, "On Failure Mechanisms in Large-Scale Integrated Circuits," in *Advances in Electronics and Electron Physics*, Vol. 30, L. Marton, Ed., (Academic Press, New York, 1971), p. 79.

C-2. W. Kern, J. L. Vossen, and G. L. Schnable, "Improved Reliability of Electron Devices Through Optimized Coverage of Surface Topography," 11th Ann. Proc. Reliability Physics, (IEEE, New York, 1973) p. 214.

C-3. E. Arai and Y. Terunuma, "Water Adsorption in Chemically Vapor-Deposited Borosilicate Glass Films," J. Electrochem. Soc. 121, 676 (1974).

C-4. Staff article, "How Phosphorus Abets IC Destruction," Electronics 47, No. 8, 34 (1974).

C-5. W. M. Paulson and R. W. Kirk, "The Effects of Phosphorus-Doped Passivation Glass on the Corrosion of Aluminum," 12th Ann. Proc. Reliability Physics, (IEEE, New York, 1974), p. 172.

C-6. J. L. Vossen, G. L. Schnable, and W. Kern, "Processes for Multilevel Metallization," J. Vac. Sci. and Technol. 11, No. 1, 60 (1974).

C-7. H. Koelmans, "Metallization Corrosion in Silicon Devices by Moisture-Induced Electrolysis," 12th Ann. Proc. Reliability Physics Mtg., (IEEE, New York, 1974), p. 168.

C-8. R. A. Kokosa, B. R. Tuft, and E. D. Wolley, "Progress in High Voltage High Frequency Planar SCR Technology," IEEE Industry Applications Mtg. Proc., Milwaukee, Wisc., p. 87 (October 1973).

C-9. B. Reich and E. B. Hakim, "Can Plastic Semiconductor Devices by Used in Military Equipment," Proc. 1974 Ann. Reliab. and Maint. Symp., p. 396 (January 1974).

C-10. J. J. Mazenko, "The Reliability of Beam Lead Sealed Junction Devices," Proc. Intn'l Soc. for Hybrid Microelectronics Symposium, p. 450 (1974).

C-11. D. S. Peck and C. H. Zierdt, Jr., "Temperature-Humidity Acceleration of Metal-Electrolysis Failure in Semiconductor Devices," 11th Ann. Proc. Reliability Physics, (IEEE, New York, 1973), p. 146.

C-12. F. N. Sinnadurai, "The Accelerated Aging of Plastic Encapsulated Semiconductor Devices in Environments Containing a High Vapor Pressure of Water," Microelectronics and Reliab. 13, 23 (1974).

C-13. T. A. Temofonte and J. R. Szedon, "Effects of Humidity and Organic Coating on Surface Potential Propagation in Passivated Devices," 9th Ann. Proc. Reliability Physics, (IEEE, New York, 1972), p. 107.

C-14. J. Sato, Y. Ban, and K. Maeda, "Durability and Stability of Various Insulating Films against the High Temperature Water in an Autoclave," 9th Ann. Proc. Reliability Physics, (IEEE, New York, 1971), p. 96.

C-15. N. Nagasima, H. Suzuki, K. Tanaka, and S. Nishida, "Interaction between Phosphosilicate Glass Films and Water," J. Electrochem. Soc. 121, 434 (1974).

C-16. B. E. Deal, "The Current Understanding of Charges in the Thermally Oxidized Silicon Structure," J. Electrochem. Soc. 121, 198C (1974).

C-17. E. H. Nicollian, "Surface Passivation of Semiconductors," J. Vac. Sci. and Technol. 8, No. 5, S39 (1971).

C-18. K. H. Zaininger, "Automatic Display of MIS Capacitance versus Bias Characteristics," RCA Review 27, 341 (1966).

C-19. W. H. Schroen, J. G. Aiken, and G. A. Brown, "Reliability Improvement by Process Control," 10th Ann. Proc. Reliability Physics (IEEE, New York, 1972), p. 42.

C-20. W. H. Schroen, "Failure Analysis of Surface Inversion," 11th Ann. Proc. Reliability Physics, (IEEE, New York, 1973), p. 117.

C-21. G. A. Brown, K. Lovelace, and C. Hutchins, "A Process Control Test for Lateral Charge Spreading Susceptibility," 11th Ann. Proc. Reliability Physics, (IEEE, New York, 1973), p. 203.

C-22. J. R. Haberer and J. J. Bart, "Charge Induced Instability in 709 Operational Amplifiers," 10th Ann. Proc. Reliability Physics (IEEE, New York, 1972), p. 106.

C-23. C. G. Peattie, J. D. Adams, S. L. Carrell, T. D. George, and M. H. Valek, "Elements of Semiconductor-Device Reliability," Proc. IEEE 62, 149 (1974).

C-24. A. C. Macpherson, H. M. Day, W. H. Weisenberger, and A. Christou, "Effects of Fast Temperature Cycling on Aluminum and Gold Metal Systems," Paper No. 3.4 prepared for presentation at the 1975 Intn'l Reliability Physics Symposium, IEEE, Las Vegas, Nevada, April 2, 1975.

C-25. J. J. Bart, "The Analysis of Chemical and Metallurgical Changes in Microcircuit Metallization Systems," IEEE Trans. Electron Devices ED-16, 351 (1969).

C-26. L. V. Gregor, "Thin-Film Processes for Microelectronic Application," Proc. IEEE 59, 1390 (1971).

C-27. W. Kern, "Detection and Characterization of Localized Defects in Dielectric Films," RCA Review 34, 655 (1973).

C-28. W. Kern, "Characterization of Localized Defects in Dielectric Films for Electron Devices," Solid State Technology 17, No. 3, 35 (1974) No. 4, 78 (1974).

C-29. D. D. Forsythe, "Surface-Charge Induced Failures Observed on MOS Integrated Circuits," Microelectronics and Reliability 8, 339 (1969).

C-30. G. L. Schnable, H. J. Ewald, and E. S. Schlegel, "MOS Integrated Circuit Reliability," IEEE Trans. Reliability R-21, No. 1, 12 (1972).

C-31. H. Khajezadeh, "High-Reliability Plastic Package for Integrated Circuits," 11th Ann. Proc. Reliability Physics, (IEEE, New York, 1973), p. 236.

C-32. H. Khajezadeh and A. S. Rose, "Reliability Evaluation of Hermetic Integrated Circuits in Plastic Packages," Paper presented at the 1975 Reliability Physics Symposium, IEEE, Las Vegas, Nevada, April 1975.

C-33. P. Flaskerud, "MOS Devices in Plastic Packages -- A Reality," Proc. 1971 Semiconductor/IC Proc. and Prod. Conf. Mgt., p. 40, Ind. and Sci. Conf. Mgt., Chicago, Ill. (1971).

C-34. J. H. Lindwedel, *Reliability Evaluation of LSI Microcircuits*, p. 181, Final Report, RADC-TR-73-127, May 1973.

C-35. M. M. Schlacter, E. S. Schlegel, R. S. Keen, R. A. Lathlaen, and G. L. Schnable, "Advantages of Vapor-Plated Phosphosilicate Films in Large-Scale Integrated Circuit Arrays," IEEE Trans. Electron Devices ED-17, 1077 (1970).

APPENDIX D

SINGLE-ROTATION VERTICAL CVD REACTOR

by

W. Kern and A. W. Fisher

The relatively simple and inexpensive vertical CVD batch reactor noted in the section on reactor systems has proven useful in research and pilot production applications. Figure D-1 shows a photograph of the unit with the glass bell jar as reaction chamber.

A commercial high-temperature hotplate or electric stove element serves as a heat source. A 1.4-cm-thick, 20-cm-diameter disc of aluminum alloy 6061 is used as sample stage. A small depression in the center of the disc aids in positioning it freely on a support pedestal machined of a thermally insulating ceramic (AlSiMag 222). The pedestal fits in a rotating steel shaft which extends through the center of the hotplate directly to an instrument motor. The disc rotates at typically 6 rpm above the hotplate top, with a clearance of 2 to 3 mm. Construction details are shown schematically in Fig. D-2.

A chromel-alumel thermocouple serves as temperature sensor for the rotating substrate plate. The thermocouple wires are insulated by a ceramic tube and are inserted through the hotplate from below, extending through a small opening in the Pyroceram top toward the rotating metal disc, but without touching it. The thermocouple signal is relayed to an automatic temperature controller, which regulates the temperature of the hotplate. The rotary disc temperature is also monitored independently prior to deposition work, using calibrated bimetallic surface thermometers.

The deposition chamber shown consists of a Pyrex bell jar of 25-cm height and has an outside diameter of 22 cm. The geometry of the single gas inlet on top of the bell jar is clearly visible in Fig. D-1. Alternatively, a water-cooled, double-walled, stainless-steel chamber of similar dimension has been used for cold-wall CVD studies. The deposition chamber rests on a Transite plate that has four symmetrically located slots serving as exit openings for the exhaust gases. The entire apparatus is placed in a chemical exhaust hood whose air intake is regulated to avoid excessive air drafts, so as not to cause thermal disturbances of the hotplate's temperature equilibrium.

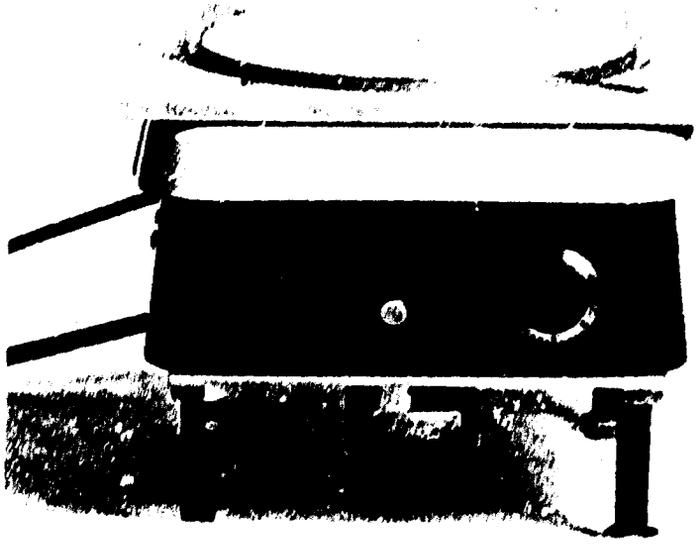
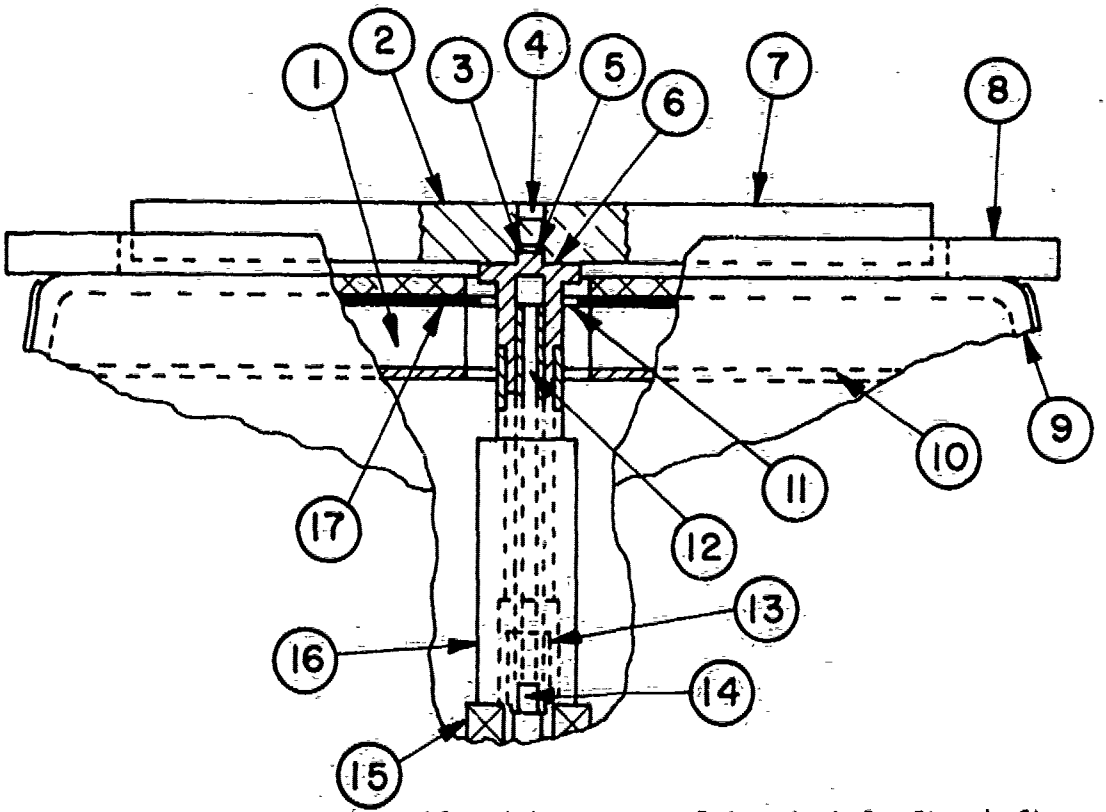


Figure D-1. Single-rotation vertical CVD reactor. Diameter of the glass bell jar is 21 cm.



1. Heater assembly with cut out clearance hole for shaft.
2. Aluminum alloy rotating disc (1.5 cm x 21 cm).
3. Centering insert of ceramic support pedestal.
4. Centering recess on both sides of disc.
5. Bushing.
6. Ceramic support pedestal and sleeve drive.
7. Surface of rotating disc for substrates.
8. Transite reaction chamber support plate.
9. Pyroceram hotplate top.
10. Backing plate.
11. Output for heating element.
12. Steel tubing centering shaft.
13. Boston sleeve coupling (#GR4).
14. Hexagonal socket head cap screw.
15. Thrust bearing (Aetna F-1).
16. Stainless steel sleeve-drive to motor shaft.
17. Mica insulation with cut out clearance hole for shaft.

Figure D-2. Sectional view of construction details for single-rotation CVD reactor center-portion of unit shown in Fig. D-1.

The oxide and glass deposits accumulating on the aluminum substrate disc should be removed periodically by immersion in diluted HF, followed by flushing with deionized water. Occasional mechanical cleaning with steel wool and detergent followed by immersion in concentrated HNO_3 for 3 to 5 minutes and thorough rinsing with deionized water is recommended. To avoid warping of the symmetrically machined plate on extended use at 450°C, it is simply inverted after cleaning when repositioning it on the support pedestal. This will effectively nullify the slight sagging that might otherwise occur.

NOTE TO READER:

The paper below was published in the Proceedings of the IEEE 1975 National Aerospace and Electronics Conference (NAECON '75 Record, IEEE Cat. No. 75 CH0956-3 NAECON), pp. 93-100, June 1975. As with Appendix A, it is pertinent to the contract.

APPENDIX E

CHEMICAL VAPOR DEPOSITION TECHNIQUES FOR GLASS PASSIVATION OF SEMICONDUCTOR DEVICES*

by

W. Kern

ABSTRACT

Chemical vapor deposition (CVD) has become the most widely used technique for producing glassy passivating layers over metallized semiconductor devices, particularly silicon integrated circuits. A considerable variety of reactor systems is now available, including horizontal tube-types, rotation reactors, and continuous processing units. Their capabilities and principles of operation are discussed. Experimental results are presented demonstrating variations in deposition conditions that critically affect film properties such as chemical composition, intrinsic stress, density, structure, and uniformity. To produce passivating films of consistently high quality, it is imperative to understand the effects of system and deposition variables and to effectively optimize the critical factors. Additional improvements of passivating films can be achieved by post-deposition densification treatments at low temperature.

INTRODUCTION

Chemical vapor deposition is a process by which gases or vapors are chemically reacted, leading to formation of a solid-phase reaction product on the substrate surface. Theoretical and practical aspects have been treated in recent reviews.[1-4] CVD has become one of the most widely used techniques for producing glassy passivating layers over metallized semiconductor devices, particularly discrete planar transistors and complex planar silicon integrated circuits for both hermetic or plastic encapsulation. The most commonly used passivating overcoat layers are SiO_2 and phosphosilicate glass (PSG), singly or in combination, deposited by oxidation of the nitrogen-diluted hydrides at a substrate temperature ranging from 325 to 450°C. The purpose of the paper is to discuss CVD equipment now available for producing passivating layers of this type, and to examine the effects of system and deposition variables on specific qualities of the films using examples from research in our laboratory.

The main functions of passivating overcoats are to protect against scratching of the vulnerable interconnect metallization during chip handling, to provide immunity to effects of loose conductive particles in hermetic packages, to improve device stability in various ambients, to lower susceptibility to metal corrosion and electromigration, and to reduce effects of ion motion on the device surface. PSG has, in addition, alkali-gettering capability which is of great importance in passivation and stabilization of devices, and exhibits less stress (tensile) than layers of CVD-SiO_2. We have just recently published a comprehensive survey[5] of passivation coatings for silicon devices in which many of these aspects are treated in greater detail.

The basic process for depositing SiO_2 films from silane and oxygen at low temperatures (250 to 550°C) was reported in 1968.[6] The exact details of this thermally-activated, surface-catalyzed, heterogeneous branching-chain reaction are complex. The overall reaction can be expressed as

$$SiH_4(g) + 2O_2(g) \rightarrow SiO_2(s) + 2H_2O(g),$$

but under some circumstances it may proceed as

$$SiH_4(g) + O_2(g) \rightarrow SiO_2(s) + 2H_2(g).$$

The reaction favored depends strongly on deposition temperature and silane concentration,[6-10] and probably also on the oxygen ratio and variations in reactor geometry. Phosphorus can be incorporated into the SiO_2 layers as an oxide of phosphorus by the reaction of phosphine with oxygen:

$$2PH_3(g) + 4O_2(g) \rightarrow P_2O_5(s) + 3H_2O(g)$$

forming PSG.[10-17] Effects of CVD parameters on the reaction chemistry will be discussed in a later section.

The theoretical maximum temperature which can be used in processing devices metallized with Al is limited by the melting point of the eutectic formed between Si and Al (577°C). In practice the maximum temperature during glassing is held below 500°C because solid-state reactions between Al and Si begin to exert degrading effects in many sensitive devices near 500°C. A bibliography covering related aspects of metallization for silicon devices has just been made available.[18]

*This work was in part supported by the Air Force Materials Laboratory, Wright-Patterson Air Force Base, Ohio, under Contract No. F33615-74-C-5146.

Combinations of PSG and SiO_2 layers can offer distinct advantages over any one single layer and can be readily prepared by CVD techniques, often in one continuous operation.[14] Furthermore, the properties of glass layers deposited at low temperature can be improved by a suitable densification treatment,[19] as will be described.

CVD REACTOR SYSTEMS AND EQUIPMENT

Requirements and Types of Reactor Systems

A CVD system for depositing passivating films of the type described must effect the following essential functions:[1-4,20] (1) Transporting, metering, and mixing the diluent and reactant gases entering the reactor; (2) providing heat to the substrate material being coated, and controlling this temperature by automatic feedback to the heat source, and (3) removing by-product and exhaust gases safely from the deposition zone. The reactor system should consistently yield glass films of high quality – good thickness and compositional uniformity, high purity with a minimum of structural imperfections such as pinholes, cracks, and particulate contaminants. For production applications the system should perform with high throughput, be simple and safe to operate, and easy to maintain. The capital cost of the equipment, which ranges from less than $5,000 for an in-house built research unit to over $70,000 for a high-capacity production system, must be evaluated in terms of averaged product output, operator and maintenance labor, consumed gases, power consumption, and parts replacement cost.

Reactors can be classified into essentially four main categories, according to their gas flow characteristics and principle of operation:

1. Horizontal tube displacement flow reactors.
2. Rotary vertical batch-type reactors.
3. Continuous reactors employing premixed gas flow fed through an extended area slotted disperser plate.
4. Continuous reactors employing separate N_2 + oxygen and hydride streams directed towards the substrate by laminar flow nozzles.

Data on commercially available equipment to be described was derived from citations by the manufacturers rather than by experimental studies by the author, other than inspection of the equipment.

Horizontal Displacement Flow Reactors

Horizontal tube reactors consisting of an elongated quartz tube of circular or rectangular cross-section were the first types used in CVD of oxides at low temperature. The diluent and reactive gases are continually being supplied, are usually mixed and dispersed at the point of entry into the tube, and pass over the heated substrates which rest on a tilted wafer carrier. Heat is supplied from outside the tube or from within the wafer carrier. Displacement-type forced laminar gas flow features a low degree of gas mixing, requiring careful optimization of the gas dynamics to obtain good film uniformity in thickness and composition.

A horizontal, internally resistance-heated flow reactor manufactured by Applied Materials Technology, Inc.[21] has a capacity for ten 5-cm diameter wafers per batch. Cycle time for a 5000Å-thick SiO_2 deposition is ½ minutes. Uniformity of film thickness is typically ± 7.5% within a wafer, ± 10% from wafer to wafer within a run.[21] A tubeless horizontal production reactor of entirely different design is manufactured by Thermco.[22] It utilizes a resistance heated block with the gases introduced across its width to minimize depletion of the gas reactants moving across the heating platen. The gas delivery system has provision for bi-directional gas entry/exhaust. The unit has a loading capacity for 27 5-cm wafers and a deposition rate capability of 1000Å/min. Uniformity within a wafer is ± 5%, and ± 10% from wafer to wafer.

A developmental close-spaced horizontal cold-wall reactor has also been described.[23] A high-velocity stream of the premixed gases passes over the resistance-heated substrate wafers parallel to their surface. The reactor can accommodate 28 wafers of 5-cm diameter.

Rotary Vertical Batch Reactors

In these reactors, the substrate wafers are placed on a plate rotating above a resistance heater. The reaction chamber consists of a cylindrical, conical, or hemispherical bell jar that may have provisions for cooling. The gases enter through single or multiple inlets from the top or side of the bell jar, pass over the substrates, and exit at the bottom below the level of the rotating plate. The incoming gas streams mix gradually with the partially reacted gas before passing over the substrates. The geometry of the reaction chamber and the gas inlet and exit openings critically influence the gas flow dynamics.

A reactor of this type, designed for research applications, was described in a previous paper.[24] The unit consists of gear-driven discs heated by conduction from a hotplate. Planetary motion of the substrates promotes maximum uniformity of the film deposits by thermal and gas dynamic averaging over a wide range of operating conditions. A modified single-rotation design[25] coats simultaneously five wafers of 5-cm diameter with a uniformity that is indistinguishable by visual inspection from wafer to wafer if the nitrogen diluent flow is properly balanced. Nine wafers can be coated simultaneously if thickness uniformity is less critical. Deposition rates of up to 1 μm/min can be obtained.

Several important considerations should be noted for designing and constructing the gas handling equipment associated with in-house built units. Heliarc-welded and leak-checked stainless steel tubing is recommended for hydrides of high concentration (greater than 5 percent). Leak tested polyethylene tubing is advantageous for oxygen, nitrogen, and diluted hydrides. Metering of the hydride gases is best done with calibrated mass flowmeters and controllers. Float-type flow meters are adequate for oxygen and nitrogen. It is important to have provision for nitrogen purging of the hydride lines back to the source tanks to remove residual hydrides after deposition work is terminated. Additional recommendations were noted

previously.[6,24,26] Gas flow control panels are now available commercially[27] or can be obtained custom built.[28]

A commercial rotary, resistance-heated vertical reactor system for semi-continuous operation is sold by Unicorp, Inc.[29] It features premixed gas input through four tubes inside the conical deposition chamber and has separate stations on a carrier disc for wafer loading/unloading, preheating, deposition, and cool down. Up to seven 5-cm wafers can be accommodated per station. The maximum oxide deposition rate is 1700Å/min with an overall uniformity of ± 5%.[29] An oxide reactor[30] featuring two planetary systems arranged concentrically was described in 1971.[31] In this complex reactor the driver element is a cylinder rotating within an annular spacing between a circular inner resistance heated block and an outer heater ring. The gases are dispensed in a counter rotating array, resulting in a thickness uniformity of ± 1.5%.

Vertical CVD reactor systems with rotating gas feed over a stationary, resistance heated plate are manufactured by Phoenix Materials Corporation.[32] Units for processing either 26 or 70 5-cm wafers are available.[32] A vertical cold wall reactor system by HLS Industries[33] featuring a periphase gas injection arrangement that introduces the gases into the reactor through two concentric wall sections was described recently.[33] Low gas depletion losses and elimination of static boundary conditions result in uniform deposits.

Continuous Reactor Systems

Application of continuous processing concepts to CVD systems makes large-scale production of oxide and glass films possible at lower operating cost than by use of batch-type reactors. A processor of this type is manufactured by Applied Materials Technology, Inc.[34,35] The substrate wafers are moved conveyor-fashion on Inconel trays through the reactor at constant speed. Heating is by radiation from a resistance heater. The nitrogen, oxygen, and hydride gas streams are combined before entering the manifolds to the dispenser plate from which the gas mixture passes by laminar flow over the wafers. The cross-flow gas dispersion and the relatively close spacing (approx. 1 cm) of the substrate to the water cooled, extended area slotted dispenser plate minimizes undesirable homogeneous gas phase nucleation. Wafer-to-wafer uniformity is better than ± 5%, with low densities of particulate inclusions and pinholes. The machine has a throughput capacity of 400 5-cm wafers per hour with 1-μm thick SiO_2 deposit.

In nozzle reactors, separate streams of nitrogen-diluted hydrides and oxygen impinge on the substrate surface where they mix and react, forming the films. The effects of nozzle geometries on the oxide deposition pattern has been examined in detail.[36,37] An open horizontal circular compound nozzle was empirically found most desirable, with the deposition occurring where the heated moving wafer intersected the unconfined jet of the reacting gases, while the exhaust gases were removed by a pump. Uniformity of ± 5% was obtained across a 5-cm wafer.[37] A commercially available continuous reactor system based on nozzle-type gas dispersion is manufactured by Pacific Western Systems, Inc.[38] In this unit the nitrogen-diluted oxygen and hydrides are directed to the substrate surface as separate streams flowing through the laminar flow slots forming the nozzles. The water-cooled nozzle array is either 3.8- or 7.6-cm wide and extends over the width (~20 cm) of the heater block assembly. The space between the nozzle array and the wafer surface during deposition is only about 2.5 mm, and defines the reaction zone where the gases mix and react, forming the films. Exhaust gases are removed through separate slots at the periphery of the nozzle array. The wafers traverse at an adjustable speed under the nozzle unit on a resistance heated conveyor plate that accepts 21 5-cm wafers. The thickness uniformity for SiO_2 films is ± 5% with a deposition of 1 μm at a rate of 6.3 cm/min travel speed; particle density is low, deposition rate high.

A continuous nozzle reactor system is also marketed by Chemical Reactor Equipment, Inc.[39] A high-velocity nozzle is used through which the gases are mixed and impinged over a relatively small area of deposition surface. Continuous mode of operation results from reciprocating motion of the substrate under the nozzle. A five-nozzle system is capable of depositing, with excellent uniformity, 0.5 μm SiO_2 on up to 350 5-cm wafers per hour.

CRITICAL CVD PARAMETERS

The exact conditions of the process can critically affect film growth rate and properties such as composition, intrinsic stress, density, structure, purity, uniformity, adhesion, and particulate contamination. These CVD conditions include: (1) Substrate temperature of deposition, (2) oxygen-to-hydride ratio, (3) hydride input, (4) silane-to-phosphine ratio, (5) nitrogen input, (6) geometry of reaction chamber and gas inlet/outlet configurations, (7) wall temperature of reaction chamber or gas disperser, (8) cleanliness of CVD system and purity of gases, (9) nature and cleanliness of substrate surface, and (10) surface topography of substrate. The parameters listed must be controlled by analysis of the film deposits, both initially and on a periodic control basis. We have recently surveyed suitable methods for analysis[5] and defect characterization[40] of dielectric films.

EXPERIMENTAL RESULTS AND DISCUSSION

Gases, Equipment, and Methods

The semiconductor-grade hydrides used were 1 vol % PH_3 and 3.5 vol % SiH_4 in high-purity N_2. The oxidant was O_2 of 99.9% purity, and the diluent was N_2 of 99.998% purity, both filtered through submicron filters. The single rotation vertical CVD reactor described in a previous section[25] was used with a glass deposition chamber. The hydrides and N_2 were introduced through the center inlet at the top of the chamber after having passed through a terminal submicron large-area filter. The O_2 was added separately on top of the bell jar after the filter. Surface temperatures were measured with bimetallic and thermocouple surface thermometers. The PSG composition was routinely analyzed by etch rate measurements of the densified films using the graph presented in Fig. 1, which was calibrated by wet chemical analysis.

Effects of Temperature and Oxygen-to-Hydride Ratio

The effects of substrate temperature of deposition and O_2:hydride ratio are closely interrelated and are therefore considered together, for both SiO_2 and PSG films. We have previously shown[6] that SiH_4 diluted with N_2 begins to form SiO_2 films at a temperature of about 240°C if the O_2:SiH_4 ratio is 3:1. The rate of film growth at constant SiH_4 input increases rapidly as the substrate temperature is increased to 310°C. Further increase to 450° results in a gradual increase in deposition rate. To attain a linear increase of deposition rate with temperature, the O_2:SiH_4 ratio must be increased as the temperature is increased. For example, at 475°C an O_2:SiH_4 ratio of at least 14:1 is required to achieve this. Larger ratios of up to 33:1 have no effect, but ratios beyond this limit inhibit the reaction, leading to decreased rates of film growth. Thus a plateau region exists that is insensitive to the O_2:SiH_4 ratio. Temperatures lower than 475° require a progressively smaller O_2:SiH_4 ratio to attain the plateau of maximum SiO_2 deposition rate.[6] At the same time the extent of the plateau region narrows as the temperature is decreased. These observations have since been confirmed by several other workers[7,10,41] and hold qualitatively even though different reactor geometries were used. The unusual reduction in SiO_2 deposition rate at high O_2:SiH_4 ratios has been explained by retardation theory where O_2 acts as the retardant by being adsorbed on the substrate.[10]

The corresponding observations for PSG formation by co-oxidation of SiH_4 + PH_3 with O_2 are essentially analogous to those discussed for SiO_2.[10,12,42] We have found that decreasing temperatures depress the PSG deposition rate and shift the maximum toward lower O_2: hydride ratios, narrowing the plateau region. The effect of substrate deposition temperature on PSG composition is shown in Fig. 2 for a fixed O_2:hydride ratio, and also for ratios corresponding to the maximum deposition rate estimated for each temperature as a function of the O_2:hydride ratio. The hydride composition used consisted of 11.5 mol % PH_3 + 88.5 mol % SiH_4; total gas flow rate was 8.8 liters/min. It is seen that the phosphorus content decreases with increasing temperature in both cases. The effects are less pronounced for PSG films of lower phosphorus concentrations. A practical consequence of the temperature effect is the need for isothermal conditions of the substrate. Good thermal contact of the wafer with the plate is essential to achieve uniform film thickness and composition.

Effects of Hydride Input

The quantity of SiH_4 or of SiH_4 + PH_3 introduced in the reaction chamber per unit time determines the rate of film deposition which follows a linear function up to some saturation level limited by the size of the chamber. We investigated effects of deposition rate variations on PSG film composition at a deposition temperature of 450°C. The O_2:hydride ratio was 18:1; SiH_4:PH_3 ratios were selected to yield films containing 3.5 and 7.5 wt % P. Deposition rates ranged from 2500Å/min to 6000Å/min. A very gradual increase of the phosphorus content with increase in deposition rate was noted, amounting to 16 percent for the low-P glass and to 11 percent for the high-P glass over this interval of deposition rate.

Effects of Silane-to-Phosphine Ratio

The SiH_4:PH_3 ratio under otherwise constant CVD conditions determines the composition of the resulting PSG. We have found that this relationship is nearly linear with glass composition, on a molar basis up to about 9 mol % P_2O_5, followed by a less than linear increase in P_2O_5 beyond this point. A PSG composition of 9 mol % PSG is obtained in our system at 445°C from a hydride composition of 12 mol % PH_3 in SiH_4 + PH_3 and the conditions stated in Fig. 1. Lower temperatures of deposition at constant SiH_4:PH_3 ratio increase the mol % P_2O_5 in the PSG if the O_2:hydride ratio is adjusted for the plateau region of maximum deposition rate for each temperature, in agreement with Fig. 2 and with data from the literature.[42] The PSG contains, therefore, more phosphorus than would be expected from stoichiometry, since two moles of PH_3 form one mole of P_2O_5. Up to about 9 mol % P_2O_5 the conversion efficiency of PH_3 to P_2O_5 at 445°C is 1.5 times greater than that of SiH_4 to SiO_2. At lower temperatures it is still greater. Stated differently, the conversion efficiency of SiH_4 to SiO_2 during co-oxidation of SiH_4 + PH_3 is lower than that of PH_3. Apart from kinetic[10] and thermodynamic[23] differences in the oxidation of the two hydrides, the previously mentioned retardation of SiH_4 oxidation by oxygen is responsible for at least part of the observed effect. In addition, PH_3 appears to have a retarding effect on SiH_4 oxidation also, since the film deposition rate is being depressed by the addition of PH_3.[43]

Incorrect SiH_4:PH_3 ratios can lead to several problems in the glass. A PSG with low phosphorus content may result in inadequate gettering of externally introduced contaminants such as sodium ions; it may also cause cracking of the glass because of excessive stress. Too high a concentration of phosphorus, on the other hand, may result in current leakage across the surface or in a hygroscopic glass which may cause metal corrosion problems.

Effects of Nitrogen Input

The functions of the nitrogen are (1) to dilute the hydrides to a sufficiently low concentration to prevent spontaneous combustion when combined with the oxygen and, in some systems, to permit premixing; (2) to force the reactive gas mixture over the heated substrate surface; and (3) to create gas flow conditions in the reaction chamber that result in good film uniformity across a maximum area of the substrate plate. Too low a nitrogen flow rate can severely depress the film deposition rate. Excessive nitrogen flow decreases the reaction time for the gases at the substrate surface and causes the plate temperature to drop due to cooling, thus leading to nonuniform deposits which, in the case of PSG, contain more phosphorus than obtained under normal conditions (because of the decreased temperature). A suitable flow rate for the reaction chamber we have used is in the range

of 7 to 11 liters of total N_2 (including hydride diluent N_2) per minute, the correct quantity being determined by the attainment of good film uniformity under the specific CVD conditions used.

Silane, despite its reactivity at higher concentrations with oxygen, can be conveniently premixed for production applications with oxygen and nitrogen at sufficiently high dilutions in both O_2 and N_2 (i.e., 0.5% SiH_4, 2.5% O_2, 97% N_2 by volume), forming a mixture that is inert until heated above 200°C.[9]

Effects of Reactor Geometry

The shape and dimensions of the reaction chamber and the gas inlet/outlet configuration are very critical with respect to thickness uniformity of the film deposits. We have constructed and tested many reaction chambers and found that small differences can cause gross effects, particularly in single-rotation reactors where a lesser degree of averaging is attainable than in planetary units.

Effects of Reaction Chamber Wall Temperature

The reactor wall, if hot, acts as a substrate for both glassy and powdery gas phase reaction products. Cooling the reactor parts that are not intended for heating the substrate results in a decrease of these undesirable coatings. Cooling also suppresses homogeneous gas phase nucleation, which is the cause of the powdery deposits, while at the same time promoting desirable heterogeneous reactions leading to glassy films. As a consequence, cleaner film deposits form and the deposition rate increases for the same reactant input. This means, in effect, that the yield of glassy product can increase considerably, since the input of expensive reactants can be reduced to attain the same deposition rate obtained with a hot-wall reactor. The composition of PSG films can be affected by this change, requiring readjustment of the SiH_4:PH_3 ratio.

Effects of Cleanliness of CVD System and Purity of Gases

The surface-catalyzed free-radical reaction mechanism underlying CVD of oxide and glass films is quite sensitive to contaminants on the substrate surface and in the gas phase. Particles on the substrate wafer (such as powder from scribing) or in the gas stream (such as colloidal oxides) can cause microbubbles, pinholes, and other localized structural defects in the glass layer. Extreme cleanliness is therefore imperative. As already noted, particulate contamination arises very often during CVD because of homogeneous gas phase nucleation reactions. Increasing the nitrogen diluent flow rate to a practical maximum suppresses this reaction, especially if combined with cooling of the reactor wall. SiO_2 films deposited from semiconductor-grade SiH_4 and O_2 are known to contain some sodium that may deleteriously affect MOS devices. PSG passivation of proper composition is capable of gettering this contaminant to the extent that instability problems are eliminated. Nevertheless, it is safest to employ only high-purity gases and to ensure removal of particulate impurities by use of large-area high-capacity submicron filters in all gas lines.

Effects of Substrate Surface

The type of material, the cleanliness, and the topographic structure — all affect the quality of the CVD films with respect to film growth and the presence or absence of structural defects. The quality of adhesion of the CVD glass to a substrate is dependent upon the cleanliness of the surface and the nature of the substrate material. Peeling and blistering can be avoided by observing clean processing conditions, such as complete removal of photoresist residues and chemical adsorbates after photolithographic delineation of the metallization patterns. Particulate contaminants left on the surface can inhibit proper nucleation of the glass film leading to structural defects such as pinholes and must be removed prior to CVD processing. The relation of film coverage and topography of the substrate surface is a specialized topic we have reviewed recently in detail.[44]

Applicability of Results to Other CVD Reactor Systems

We have conducted a limited number of experiments with other types of reactor systems, including several commercially available continuous processing units, to examine whether the experimental results presented in this section are applicable to other systems as well. We found that they not only agree in principle, but that they frequently relate on a semiquantitative basis, despite the remarkable differences in geometry and system operation. Nevertheless, the performance of each reactor must be carefully examined and adjusted to attain conditions for producing films of specified properties.

Post-Deposition Densification Treatments

Low temperature catalytic densification using water vapor in the furnace ambient makes it possible to improve the film properties to the point where they approach those of the bulk glasses.[28] We have found that under suitable conditions, a substantial degree of densification can be attained with CVD films of SiO_2, PSG, or borosilicates in a period of several hours at temperatures as low as 400 to 450°C without damage to the aluminum metallization. Two plots of densification achieved with PSG films are presented in Fig. 3 as examples. The films were 1-μm thick and contained 3.8 wt % phosphorus (equivalent to 3.8 mol % P_2O_5). Isothermal etch rates were used as the measure of densification effectiveness. The etch rates decrease with increasing density of the glass. Measurements were made at elapsed times from 90 seconds to 100 hours. Figure 3 demonstrates that densification of PSG films in steam for one hour decreases the etch rate to 56 percent of what it was initially. In 10% H_2-90% N_2 that was passed through water at 27°C, the etch rate decreased to 71 percent in one hour. For comparison, densification at 800°C decreases the etch rate of the same PSG to 28 percent of the as-deposited value (longer heat periods at 800°C have no significant effect). Catalyzed densification of PSG films at low temperature make it not only possible to improve the general qualities of the films deposited at 450°C, but also offers the option of conducting CVD processing at temperatures considerably below 450° and at very high rates of growth — conditions not recommended for films to be used as-deposited. Contrary to what one may

expect, infrared spectroscopy has shown that heating in steam does not introduce water into the films.

CONCLUSIONS

A considerable variety of CVD reactor systems for preparing SiO_2 and PSG passivating overcoats is now available. We have categorized and described the design, operation, and capability of these systems, which encompass designs from relatively simple to sophisticated automated concepts. Even though the principle of operation differs greatly for various types of systems, the basic CVD parameters underlying oxide and glass film formation by gas phase oxidation of the hydrides at temperatures below 500°C is in principle, and often semiquantitatively, applicable to a wide variety of systems.

The most critical factors determining PSG composition and film quality are substrate temperature of deposition, oxygen-to-hydride ratio, and silane-to-phosphine ratio. Experimental results have been presented to demonstrate the interrelationship of these three major factors and their effects on the deposition rate and composition of PSG films. The mechanism underlying these reactions has been interpreted on the basis of oxygen retardation of silane oxidation. These factors must be controlled and optimized for a given CVD system by analysis of the film product obtained.

The CVD process should be directed in a fashion conducive to heterogeneous gas phase nucleation to produce clear, glassy films free of defects. Homogeneous gas phase reactions produce particulate contaminants and must be suppressed. Even though the exact reaction mechanism of film formation is quite complex, and is influenced by many variables, the optimized CVD process for preparing high-quality SiO_2 and PSG films for IC overcoat passivation is well suited to large-scale production.

The feasibility of catalytically accelerated densification of PSG film at 450°C using water vapor as catalyst has been demonstrated experimentally. Substantial degrees of densification can be achieved, and consequent improvements in the film qualities can be expected.

ACKNOWLEDMENTS

I would like to thank especially Dr. G. L. Schnable for many valuable comments and suggestions he has made in the course of this project, and for critically reviewing and discussing the manuscript. A. W. Fisher contributed significantly to the design of the CVD reactor, and R. D. Vibronek proficiently carried out much of the experimental work. I would also like to thank Lt. D. Hutchens of AFML for his support and encouragement to produce this paper.

REFERENCES

1. W. M. Feist, S. R. Steele, and D. W. Ready, "The Preparation of Films by Chemical Vapor Deposition," 237-314 in Physics of Thin Films Vol. 5, G. Hass and R. E. Thun, Eds., Academic Press, New York and London (1969).

2. E. L. MacKenna, "Chemical Vapor Deposited Dielectrics - Properties and Deposition Methods," Proc. 1971 Semicond./IC Proc. and Prod. Conf., 71-83, Ind. and Sci. Conf. Mtg., Chicago, Ill. (1971).

3. Chemical Vapor Deposition (International Conferences): J. M. Blocher, Jr., and J. C. Withers, Eds. - Second Intl. Conf., The Electrochem. Soc., Inc., New York (1970); F. A. Glaski, Ed. - Third Intl. Conf., The American Nuclear Society, Hinsdale, Ill.(1972); G. F. Wakefield and J. M. Blocher, Jr. - Fourth Intl. Conf., The Electrochem. Soc., Inc. Princeton, N. J. (1973).

4. J. J. Tietjen, "Chemical Vapor Deposition of Electronic Materials," 317-326 in Ann. Rev. Matl. Sci., Vol. 3 (1973), edited by R. A. Huggins, R. H. Bube, and W. Roberts, published by Annual Reviews (1973).

5. G. L. Schnable, W. Kern, and R. B. Comizzoli, "Passivation Coatings on Silicon Devices," paper presented at the Fall Meeting of the Electrochemical Society, New York, N.Y., October 17, 1974. Abstract No. 215, ECS Ext. Abstr., 74-2, 528-530 (1974); manuscript accepted for publication in the J. Electrochem. Soc. (Spring 1975).

6. N. Goldsmith and W. Kern, "The Deposition of Vitreous Silicon Dioxide Films from Silane," RCA Review, 28, 153-165 (1967).

7. H. J. Emeleus and K. Stewart, "Oxidation of the Silicon Hydrides," J. Chem. Soc. (London); Part I: 1182-1189 (1935); Part II: 677-684 (1936).

8. T. L. Chu, J. R. Szedon, and G. A. Gruber, "Silica Films by the Oxidation of Silane," Trans. Met. Soc. AIME 272, 532-538 (1968).

9. K. Strater, "Controlled Oxidation of Silane," RCA Review, 29, 618-629 (1968).

10. B. J. Baliga and S. K. Ghandhi, "Growth of Silica and Phosphosilicate Films," J. Appl. Phys., 44, 990-994 (1973).

11. W. Kern and R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Semiconductor Devices," Electrochem. Soc. Ext. Abstr. 5, No. 1 234-235 (Spring 1968).

12. K. Strater and A. Mayer, "Oxidation of Silane, Phosphine and Diborane during Deposition of Doped-Oxide Diffusion Sources," in Semiconductor Silicon, 469-480, R. R. Haberecht and E. L. Kern, Eds., The Electrochem. Soc., Inc. New York (1969).

13. T. Tokuyama, T. Miyazaki and M. Horiuchi, "Low-Temperature-Deposited Glass for Passivation of Semiconductor Devices," 297-326 in Thin Film Dielectrics, edited by F. Vratny, The Electrochem. Soc., New York (1969).

14. W. Kern and R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Use with Silicon Devices - I. Deposition Techniques," J. Electrochem. Soc., 117, 562-568 (1970); "II. Film Properties," ibid, 117, 568-573 (1970).

15. W. Kern and A. W. Fisher, "Deposition and Properties of Silicon Dioxide and Silicate Films Prepared by Low-Temperature Oxidation of Hydrides, RCA Review, 31, 715-727 (1970).

16. M. M. Schlacter, E. S. Schlegel, R. S. Keen, R. A. Lathlaen, and G. L. Schnable, "Advantages of Vapor-Plated Phosphosilicate Films in Large-Scale Integrated Circuit Arrays," IEEE Trans. on Electron Devices, ED-17, 1077-1083 (1970).

17. G. L. Schnable, "Glass Passivation of Integrated Circuits by Chemical Vapor Deposition of Oxide Films," IEEE '71 Intern. Conv. Digest, 586-587 (1971).

18. J. L. Vossen, A. W. Stephens, and G. L. Schnable, "Bibliography on Metallization Materials and Techniques for Silicon Devices," Monograph #2, Thin Film Division, American Vacuum Society (November 1974).

19. W. Kern, "Densification of Chemically Vapor Deposited Borosilicate Glasses," J. Electrochem. Soc., 116, 251C (Abstract) (1969).

20. M. L. Hammond, "Thin Film Preparation by Chemical Vapor Deposition," (Abstract), J. Vac. Sci. Technol. 10, 268 (1973).

21. AMS-2600 Silox System, Applied Materials Technology, Inc., 2999 San Ysidro Way, Santa Clara, CA 95051.

22. Thermco Thor II Oxide Reactor, Thermco Products Corp., Box 1875, Orange, CA 92667.

23. A. Mayer, K. Strater, and D. A. Puotinen, "Manufacturing Techniques for Controlled Deposition and Application of Doped Oxides," Techn. Rep. AFML-70-TR-191 (September 1970).

24. W. Kern, "Apparatus for Chemical Vapor Deposition of Oxide and Glass Films," RCA Review, 29, 525-532 (1968).

25. W. Kern and A. W. Fisher, unpublished work.

26. J. A. DeNicola and R. D. Mastropiero, "Design and Maintenance of High Purity Gas-Handling Systems," Solid State Technol., 15, No. 2, 51-54 (1972).

27. For example: Matheson Gas Products, P. O. Box 85, 932 Paterson Plank Road, East Rutherford, N. J. 07073.

28. For example: Tylan Corporation, 4203 Spencer Street, Torrance, CA 90503.

29. Rotox-60, Unicorp. Incorporated, 625 North Pastoria Dr., Sunnyvale, CA 94086.

30. Oxide Reactor 315 (no longer manufactured), Materials Research Corporation, Orangeburg, NY 10962.

31. J. Wollam, "Equipment for the Chemical Vapor Deposition of Ultra-Uniform Silicon Dioxide Films," Solid State Technol., 14, No. 12, 72-73 (1971).

32. PMC Chemical Vapor Deposition Systems 500 Series and 1500 Series, Phoenix Materials Corp., M. R. 10, Kittanning, PA 16202.

33. Univax Reactor Model 100-60-30, HLS Industries, 762 Palomar Avenue, Sunnyvale, CA 94086; described in "Cold Wall Semicon Reactor," Circuit Mfg., 14, No. 11, 47

34. AMS-2000 Continuous Silox Reactor, Applied Materials Technology, Inc., 2999 San Ysidro Way, Santa Clara, CA 95051.

35. W. C. Benzing, R. S. Rosler, and R. W. East, "A Production Reactor for Continuous Deposition of Silicon Dioxide," Solid State Technol. 16, No. 11, 37-42 (1973).

36. S. S. Flaschen, H. C. Evitts, and J. R. Black, "Large Area Semiconductor Surface Passivation Production Refinement Program," DA-473-939 (June 1963-March 1965) AMC-02280(E), Final Techn. Rep. (1965).

37. M. L. Barry, "A Continuous Process for the Deposition of Silicon Oxide from the Oxidation of Silane," 595-617 in Chemical Vapor Deposition, edited by J. M. Blocher, Jr. and J. C. Withers, The Electrochem. Soc., New York (1970).

38. PWS Model 2000 Vapor Deposition System, Pacific Western Systems, Inc., 855 Maude Avenue, Mountain View, CA 94040; described in "Vapor Deposition Unit is Modular," Electronics, 47, 138 (September 5, 1974).

39. CRE 1101, 1103, and 1105, Chemical Reactor Equipment, Inc., 1080 HE Duane Avenue, Sunnyvale CA 94086; described in "Danish Firm offers Vapor System," Electronic News, 60 (June 5, 1972).

40. W. Kern, "Detection and Characterization of Localized Defects in Dielectric Films," RCA Review, 34, 655-690 (1973); Solid State Technology, 17, No. 3, 35-42, and No. 4, 78-84, 89 (1974).

41. M. L. Hammond and G. M. Bowers, "Preparation and Properties of SiO_2 Films Deposited from SiH_4 and O_2," Trans. Metallurg. Soc. AIME 242, 546-550 (1968).

42. M. Shibata and K. Sugawara, "Depcsition Rate and Phosphorus Concentration of Phosphosilicate Glass Films in Relation to $O_2/SiH_4 + PH_3$ Mole Fraction," J. Electrochem. Soc., 122, 155-156 (1975).

43. M. Shibata, T. Yoshimi and K. Sugawara, "Deposition Rate and Phosphorus Concentration of Phosphosilicate Glass Films in Relation to $PH_3/SiH_4 + PH_3$ Mole Fraction," J. Electrochem. Soc., 122, 157-158 (1975).

44. W. Kern, J. L. Vossen, and G. L. Schnable, "Improved Reliability of Electron Devices Through Optimized Coverage of Surface Topography," 11th Annual Proceedings Reliability Physics, 214-223, IEEE (1973).

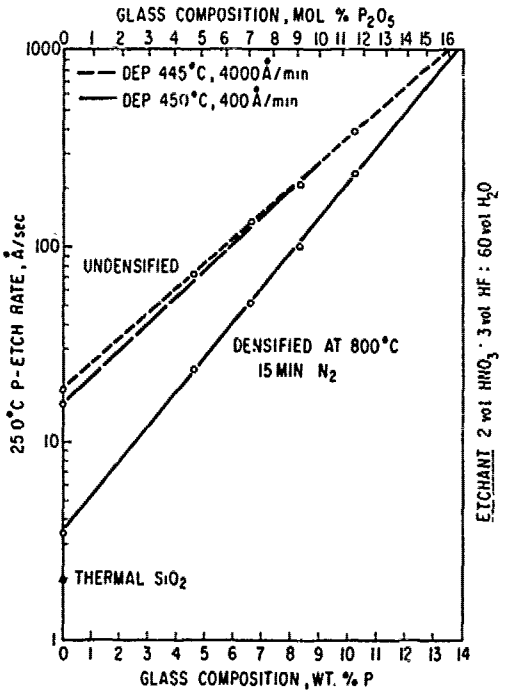


Figure 1

ETCH RATES OF SiO_2 AND PSG FILMS AS A FUNCTION OF DEPOSITION CONDITIONS, GLASS COMPOSITION, AND DENSIFICATION

Note that the etch rate of as-deposited films depends not only on film composition but also on density and stress, whereas the etch rate of densified films is a unique function of composition. With increasing % P the curves for as-deposited films approach the curve for densified films, indicating that at higher phosphorus concentrations a substantial degree of densification occurs during film deposition.

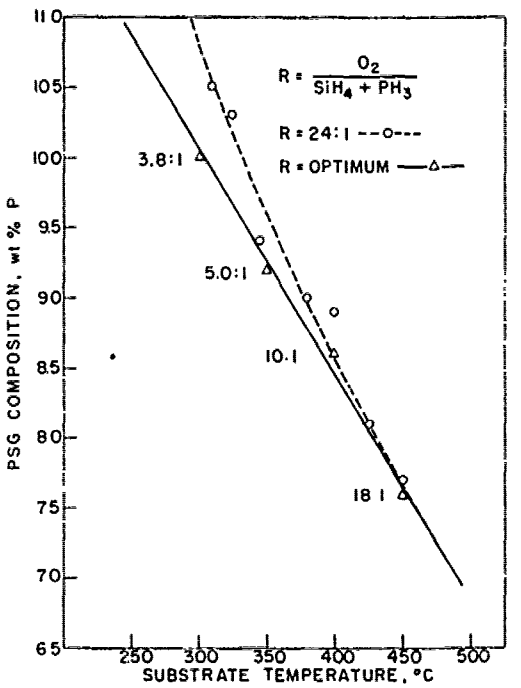


Figure 2

PSG COMPOSITION vs. SUBSTRATE DEPOSITION TEMPERATURE

The curves demonstrate the strong dependence of PSG composition on the substrate temperature during CVD.

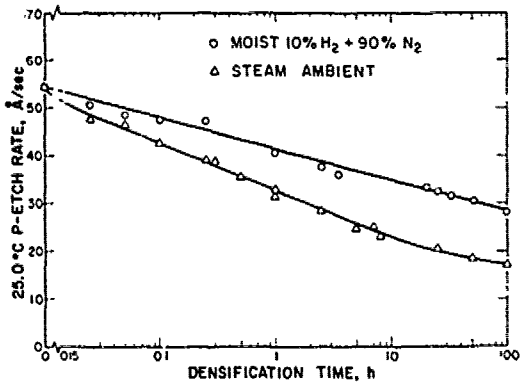


Figure 3

ETCH RATE OF PSG FILMS AS A FUNCTION OF HEAT TREATMENT CONDITIONS AT 450°C

The decrease in etch rate represents an increase in film density and shows that substantial degrees of densification can be achieved at 450°C in the presence of water vapor as catalyst.

APPENDIX F

ANALYTICAL METHODS FOR DETERMINING INTEGRITY, LAYER STRUCTURE AND COMPOSITION OF GLASS OVERCOATS ON ICs

by

W. Kern

A. INTRODUCTION

It is frequently necessary to assess the quality of passivating glass overcoats on both MOS or bipolar types of IC pellets for the purpose of in-house quality control, reliability testing, or evaluation of competitors' products. In most cases, the glass overcoat consists of SiO_2, phosphorus-doped SiO_2, phosphosilicate glass (PSG), or a combination of these layers over aluminum-metallized ICs. If the devices are encapsulated in epoxy molding compounds, exposure of the pellet without damage is required before analysis can be made. If the devices are contained in a hermetic enclosure, their exposure is readily accomplished by mechanically opening the container.

Three questions must usually be answered; what is the

(1) integrity of the glass layer (pinhole density, microcracks, blisters, and other localized defects)?

(2) layer structure (type, sequence, and thickness of the layers making up the glass coating)?

(3) chemical composition of each layer?

From the results, the quality of the glass overcoat can be assessed and the processing sequence inferred.

We have devised analytical techniques for these purposes and have used them with good results during the past year. It is the purpose of this Appendix to communicate these techniques in sufficient detail to enable others to apply them also. The method for determining thickness and composition is based mainly on selective chemical microetching and determination of the etch rate from which the layer structure and composition can be obtained by use of calibration curves. Two etch rate techniques have been developed by which to carry out the analysis. The first technique ("standard technique") is applicable to the analysis of practically all types of SiO_2/PSG overcoat structures, and is very accurate and reliable; but it is laborious because it requires many data points

to establish a graph of etch time as a function of overcoat thickness from which the component thicknesses and compositions are determined. The second technique ("simplified technique") is far less complicated and is faster in that it requires only a pair of thickness and contour measurements by Talysurf and a total etch time measurement. However, this technique works only if the composite layer contour is defined sharply enough by the etching and Talysurf tracing, which is not always the case. Both techniques are discussed and compared experimentally.

B. DETAILED PROCEDURE FOR STANDARD TECHNIQUE

1. Pellet Decapsulation

i. Grind down the entire top surface of the plastic package on a grinding wheel as close to the pellet as possible without damaging the pellet. Rinse with acetone and air-dry.

ii. Dissolve the epoxy molding compound by immersing the package in white fuming nitric acid (90%) at 90°C just long enough (typically 20 to 40 seconds) to remove all molding compound covering the pellet. Observe strict safety precautions (goggles, rubber gloves, exhaust hood). Remove, soak, and rinse in acetone, and inspect. If necessary, repeat etching until the chip surface is fully exposed.

iii. Dissolve the silicone junction coating (if present) by immersing the completely dried sample in concentrated (97%) sulfuric acid heated to 150°C under a stream of dry nitrogen (to exclude water vapor) until the device pellet is completely freed of organic materials; this may require extraction periods of typically 7 to 15 minutes. Rinse repeatedly with acetone, blot dry, and inspect after 6 to 7 minutes of extraction; continue acid treatment if necessary.

2. Initial Pellet Inspection

i. Examine the pellet under a microscope for gross visual defects and photograph the pellet areas of special interest under a microscope for later reference, if deemed necessary.

ii. If the type of glass used as the overcoat is not known, a separate pellet should be used to ascertain the elemental composition. In nearly all

cases, layers of SiO_2 and/or PSG are present. The presence of phcsphorus can be identified rapidly by qualitative electron probe microanalysis of the glass over large aluminum areas and over large dielectric areas between bonding pads.

3. Dielectric Integrity Testing

i. Immerse the package with the exposed pellet in aluminum etch [40 vol H_3PO_4 (85%):10 vol H_2O:4 vol HNO_3 (70%)] for twice the time required to dissolve the aluminum in the bonding pads [F-1]. Etchant temperature should be 50° to 55°C.

ii. Water-rinse and inspect microscopically for pinholes, microcracks, and other defects in the glass layer over aluminum. Record the type and frequency of defects.

4. Preparation of Glass Taper

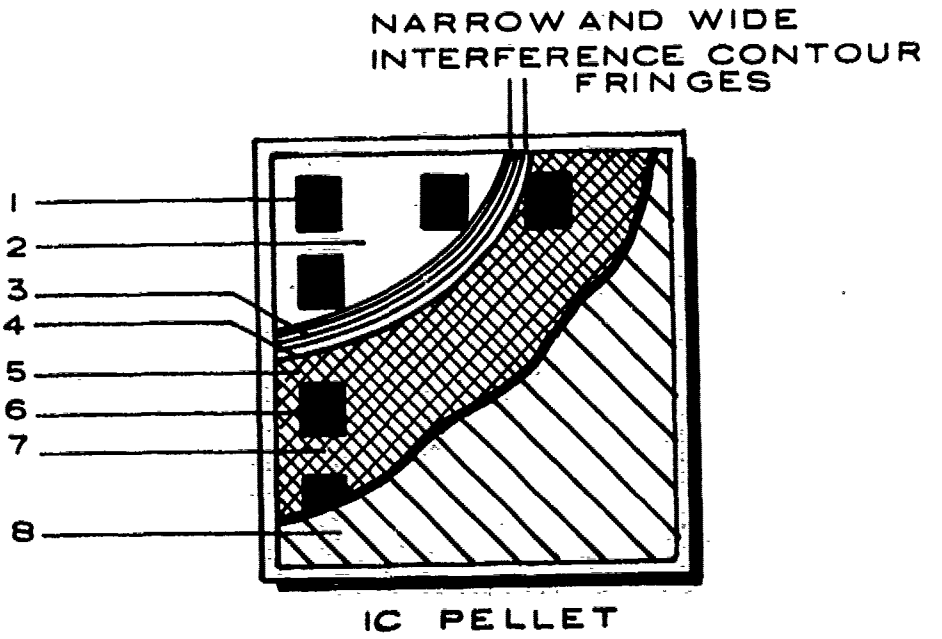
i. Place the aluminum-etched pellet under a binocular stereo-microscope and partially mask pellet with wax. Use a 50%-solution of Apiezon Hard Wax W* in trichlorethylene and apply with a fine sable paint brush. Cover about 80 to 90% of the pellet, leaving only one corner with several bonding pad areas exposed (Fig. F-1).

ii. Under a microscope examine in perpendicular white light, carefully noting the interference color of the oxide in the bonding pad areas, where the aluminum was etched away. These areas are usually thermal or densified SiO_2 and will serve as reference plane in all subsequent work.

iii. Etch the exposed overcoat layers in a solution of 1 vol HF (49%) + 4 vol H_2O until the interference color between bonding pads is the same as that noted initially for the bonding pads before this etch sequence. The glass etches very much more rapidly than the dense oxide in the bonding pad areas, which regions therefore change color only slightly during this glass etching. Etch in a series of 10-second steps, rinsing, blowing dry, and inspecting

F-1. W. Kern, "Detection and Characterization of Localized Defects in Dielectric Films," RCA Review 34, 655 (1973); Solid State Technology 17, No. 3, 35 and No. 4, 78 (1974).

*J. G. Biddle Co., Plymouth Meeting, PA 19462.



Bonding pad oxide area for taper etching	1
Area stripped of glass	2
Etched PSG taper (narrow)	3
Etched SiO_2 top layer taper (wide)	4
Area for etch rate determination	5
Bonding pad oxide area for precision etching	6
Original glassed area	7
Second masking for precision etching	8

Figure F-1. Schematic of IC pellet for glass analysis after preparation of glass taper for precision etching.

under the microscope after each etch step so as not to overshoot the glass removal end-point. Additional verification of the end-point is the beginning of dissolution of the aluminum interconnections as they become exposed. Total etch time is typically 30 to 60 seconds, depending on glass thickness and composition.

iv. Remove the wax mask in warm trichloroethylene and remask, covering only about 50 to 60% with wax so that the area with the etched glass taper is fully exposed (Fig. F-1). The masked half of the pellet is reserved for a possible repeat analysis.

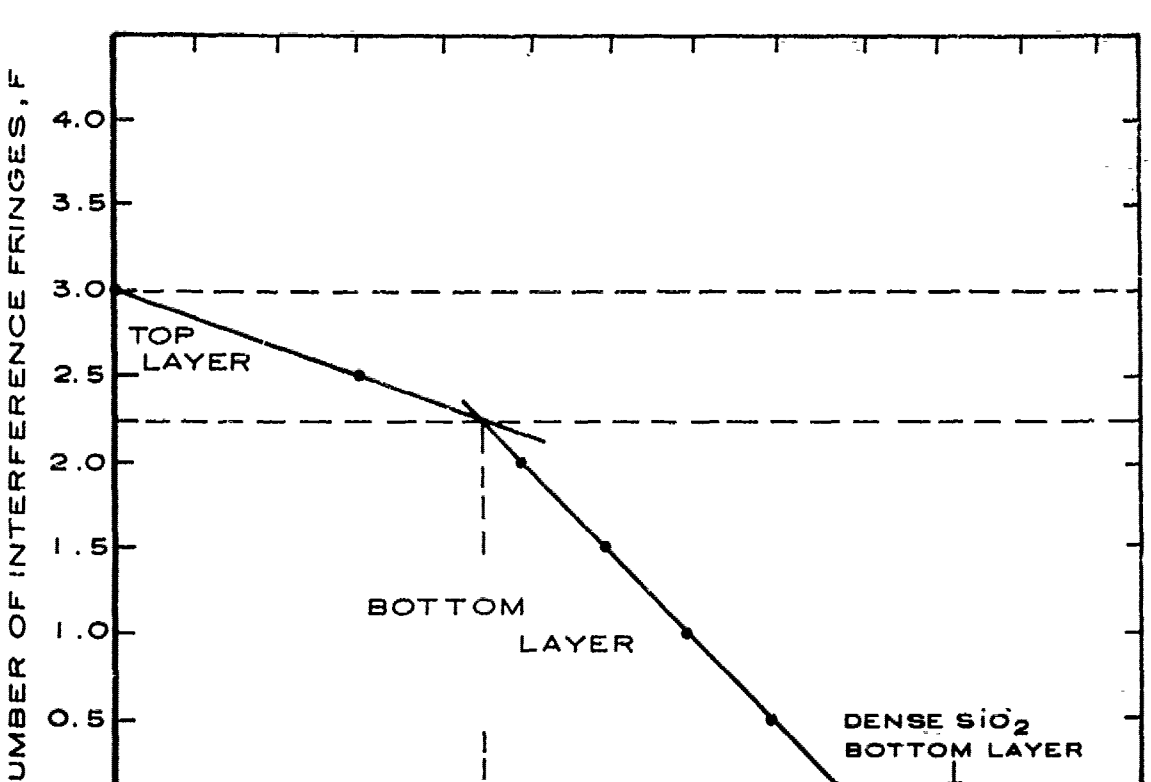
5. Precision Etching of Overcoat Layers

i. Measure the glass thickness by using the taper formed down to the dense oxide. Select an unobstructed, clear area of a well-defined taper portion between bonding pads for this and all subsequent measurements. A simple technique requiring only a microscope and monochromatic light source is interference fringe counting. Count the number of complete and partial dark contour fringes of the glass taper, including the top surface of the taper. This can be done quickly after brief training; a magnification of 200X or 500X is convenient. Be sure to count any partial top fringe (separated from the last complete fringe by a light fringe) by estimating the shade of darkness. A good description of the technique of fringe reading has been given by Booker and Benjamin [F-2].

ii. Immerse the masked device in P-etch [15 vol HF (49%), 300 vol H_2O, and 10 vol HNO_3 (70%)] maintained at 25°C (constant temperature bath) for 60 seconds. Rinse and dry. Remeasure the thickness of the etched glass layer.

iii. Repeat step ii. above several times, using shorter etch periods of 40 to 10 seconds as seen in the example in Fig. F-2. Continue until the glass is completely removed; oxide color is now the same as was noted under bonding pads before glass etching.

F-2. G. R. Booker and C. E. Benjamin, "Measurement of Thickness and Refractive Index of Oxide Films on Silicon," J. Electrochem. Soc. 109, 557 (1968).



Example of Calculations:

Top Layer

Net Fringes:	3.0 F - 2.25 F = 0.75 F
Thickness:	0.75 F x 1880 Å/F = 1410 Å
Net Etch Time:	90 sec
Etch Rate:	1410 Å/90 sec = 16 Å/sec
Layer Type:	undensified SiO_2

Bottom Layer

Net Fringes:	2.25 F - 0 F = 2.25 F
Thickness:	2.25 F x 1920 Å/F = 4300 Å
Net Etch Time:	180 sec - 90 sec = 90 sec
Etch Rate:	4300 Å/90 sec = 48 Å/sec
Layer Type:	CVD PSG (undensified)
Composition:	3.3 wt % P (from calibration curve)

Figure F-2. Determination of layer thicknesses, types, and composition from etching and fringe count data.

6. Determination of Layer Thicknesses, Layer Types, and PSG Composition

i. Plot the fringe counts versus etch time and draw straight lines of best fit through the points, as shown in Fig. F-2, which is an example of an actual analysis.

ii. Two lines of different slope indicate the presence of two different layers, such as SiO_2 over PSG. Determine the net thickness* and net etch time of each from the intercept, and calculate the etch rates (Å/sec) as shown in the example in Fig. F-2.

iii. Use the calibration curve for undensified PSG presented in Fig. 41 of Section VIII to relate the PSG glass etch rate to the phosphorus concentration.

iv. More accurate values can be obtained if the passivation glass is densified and the calibration curve for densified SiO_2 and PSG is used, since the etch rate of the undensified films is influenced to some extent by the CVD conditions used to prepare the overcoat layers. To achieve this, the isolated device pellet is heat-treated at 800°C in nitrogen for 15 minutes before the etch analysis is performed. The corresponding calibration curve for densified layers is then used to determine the composition.

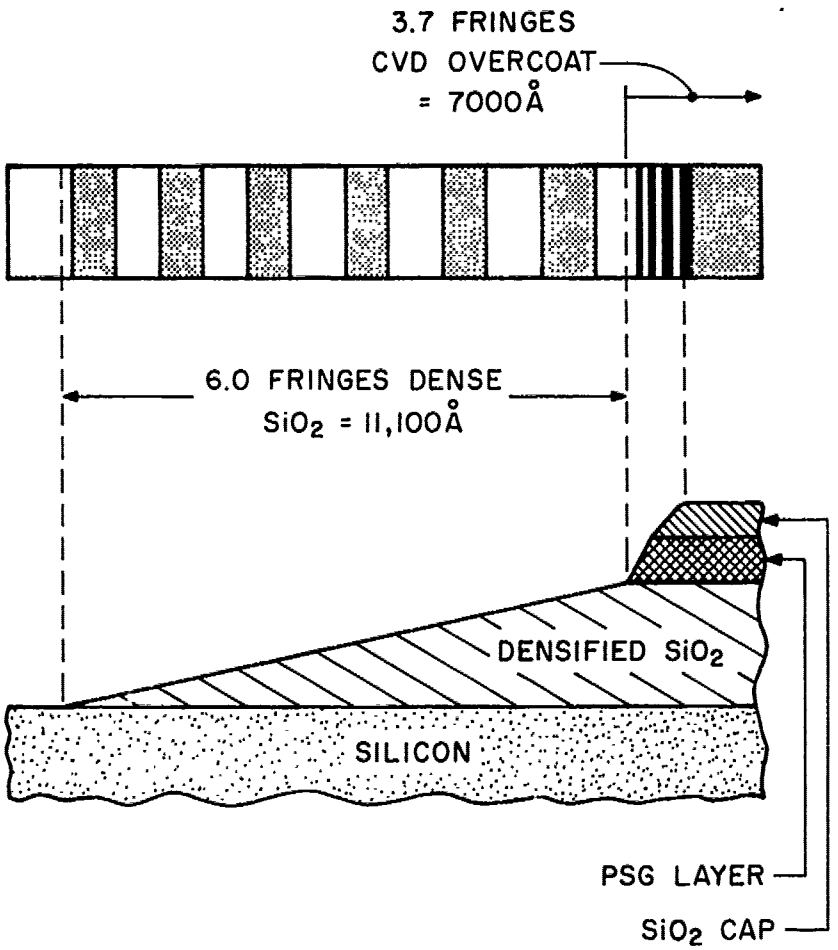
v. The thermal SiO_2 thickness underneath the aluminum metallization can be measured readily by repeating procedure 4, but using undiluted HF (49%) for the etching down to the silicon substrate surface. A taper contour as shown in Fig. F-3 will result. The SiO_2 film thickness can be readily determined from the fringe count by using a refractive index value of 1.48.

C. PROCEDURE FOR SIMPLIFIED TECHNIQUE

1. Pellet Preparation

Decapsulation, initial inspection, and dielectric integrity testing are performed as outlined in B. 1 - 3.

*The number of fringes (r) is related to film thickness (d) by the well-known relationship, $d = r\lambda/2n$, where n is the refractive index of the layer and λ is the wavelength of the monochromatic light used. Filtered mercury green light has a wavelength of 5461 Å; filtered sodium yellow light has one of 5890 Å. Undensified CVD SiO_2 has a refractive index of typically 1.45, PSG one of typically 1.42. For mercury light, one contour fringe therefore corresponds to approximately 1880-Å SiO_2 or to 1920-Å PSG; for sodium light the values are 2030-Å SiO_2 and 2070-Å PSG per fringe.



Top: Interference fringes of the taper contour shown below, as seen perpendicular to the surface in monochromatic light.

Bottom: Schematic cross section of taper contour: vertical dimensions to scale; horizontal dimension compressed approximately 15 times.

Figure F-3. HF-etched dielectric layer structure of a typical IC with overcoat.

2. Step Etching and Profilometry

i. Mask one-half or the IC pellet with Apiezon Hard Wax H.

ii. Determine total etching time (t) for P-etch at 25°C to remove the overcoat CVD layers using the oxide color under the aluminum bond pad areas as end-point.

iii. Dissolve the wax in trichloroethylene.

iv. Obtain a Talysurf trace across the etched step (20,000X vertical and at least 100X horizontal magnification). It is best to position the stylus in the area between the bond pads and the edge of the delineated IC pattern. Repeat the trace on the opposite side of the pellet.

v. Read the average film thicknesses (D) of SiO_2 and PSG from the traces at the intercept of the curves where the slope changes, as shown in Fig. F-4.

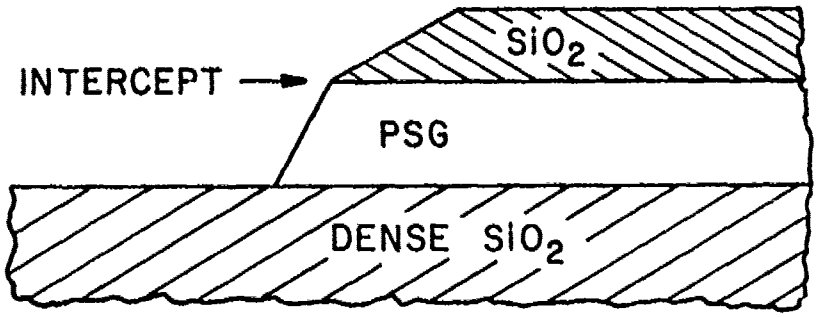


Figure F-4. Schematic cross section of typical CVD overcoat layers after step etching for profilometry.

3. Calculations

i. Calculate the PSG etch rate (R_{PSG}) from Eq. (F-1):

$$R_{PSG} = \frac{D_{PSG}}{t - (D_{SiO_2}/16)}, \qquad \text{(F-1)}$$

where R = etch rate (Å/sec),
D = film thickness (Å),
t = etch time (sec),
SiO_2 = silane oxide top layer (R_{SiO_2} = 16 Å/sec), and
PSG = phosphosilicate glass layer.

ii. Using the calculated value R_{PSG}, read off wt % phosphorus from calibration curve (Å/sec vs. wt % P) presented in Fig. 41 of Section VIII.

4. Precision

The results of repeatability tests of thickness measurements are presented in Table F-1. A reproduction of three typical Talysurf step-traces is shown in Fig. F-5.

5. Optional Measurements of Dense Oxide and Aluminum Thickness

The thickness of the dense, thermal SiO_2 layer beneath the glass passivation overcoat can be readily determined from the same Talysurf traces by measuring the thickness difference between the total dielectric layer thickness above the silicon plane (grid line) and the step-etched overcoat thickness. If desired, the thickness of the aluminum metallization can be measured from an additional trace across glassed interconnect lines. See Fig. F-5.

D. COMPARISON OF TECHNIQUES

The results of a comparison between the two techniques using PSG/SiO_2 layer structures on silicon substrate wafers are presented in Table F-2. Results comparing the techniques in actual IC analysis are given in Table F-3. The agreement can be seen to be satisfactory.

E. APPLICATIONS

A variety of commercially available and normally operating ICs from several different suppliers was selected for this comparative analysis. The integrity, layer structure, and composition of the overcoat layers were analyzed as described using the "standard" technique. In most cases two to six individual devices of a given passivation type were analyzed to derive the average values summarized in Table F-4. The column headings of this table are defined as follows:

(1) "Passivation type" refers to a given type of passivating overcoat, regardless of type of IC. Suppliers may use several types of passivating overcoats for different ICs, or for the same ICs of different

Table F-1. Repeatability of Talysurf Double-Layer-Thickness Measurements and Examples of Simplified Method Using PSG/SiO_2 Double Layers on Silicon

Sample No.	SiO_2 Top (Å)	PSG Bottom (Å)	P-Etch Time (sec) Total	SiO_2	PSG (diff.)	PSG Etch Rate (Å/sec)	wt % P	Mol % P_2O_5
A	3000	4400						
	2800	4900						
	3100	4500						
	2930 av.	4600 av.	317	183	134	34	2.3	2.3
B	3000	4800						
	2700	5200						
	2600	5000						
	2900 av.	5000 av.	328	181	147	34	2.3	2.3
C	2700	4200						
	3000	4000						
	3400	4000						
	3030 av.	4070 av.	258	190	68	60	4.1	4.2
D	3000	4000						
	2700	4000						
	2800	4000						
	2830 av.	4000 av.	254	177	77	52	3.7	3.7
E	1100	5800						
	1200	5800						
	1150 av.	5800 av.	167	72	95	61	4.2	4.3
AWF-1	2300	4600						
	2200	4900						
	2100	4700						
	2200 av.	4730 av.	165	138	27	175	7.5	8.1

Note: Total film thicknesses were also measured by contour fringe interferometry. The values were within 3% of those obtained by Talysurf averaged measurements.

A good description of Talysurf measuring techniques and of stylus techniques in general has been recently published [F-3].

F-3. D. J. Whitehouse, "Stylus Techniques," in *Characterization of Solid Surfaces*, P. F. Kane and G. B. Larrabee, Eds., (Plenum Press, New York, 1974), pp. 49-74.

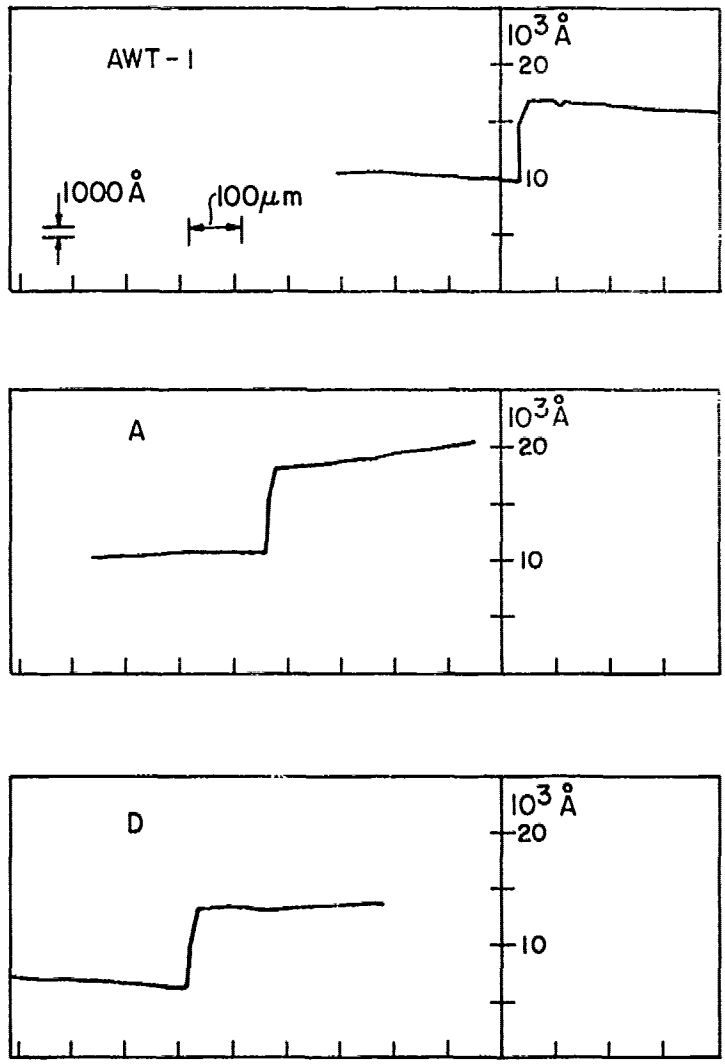


Figure F-5. Reproduction of three typical Talysurf traces from samples of step-etched PSG/SiO2 double layers on silicon selected from Table F-1. Top layer is SiO_2; bottom layer is PSG. Vertical magnification is 20,000X; horizontal magnification is 100X.

Table F-2. Comparison of Results Obtained by Standard (Long)* and Simplified (Short)** Methods of Analysis for PSG/SiO_2 Layer Structures

Sample No.	Analysis Method	Layer SiO_2 (Å)	Layer PSG (Å)	Phosphorus in PSG (wt %)
F	Long	1900	4610	4.1
	Short	1600	4300	3.7
G	Long	2185	4510	4.0
	Short	1800	4350	3.7
H	Long	1900	4220	4.6
	Short	2000	3550	4.0

*Data based on curves from 7 to 8 separate pairs of measurements of etch time and residual film thickness by fringe counting.

**Data based on single etch time and 2 to 3 Talysurf thickness traces.

Table F-3. Comparison of Results Obtained by Standard (Long)* and Simplified (Short)** Methods of Analysis for PSG/SiO_2 Structures on IC Chips

IC Pellet Analysis No.	Analysis Method	Layer SiO_2 (Å)	Layer PSG (Å)	Etch Rate (Å/sec)	Phosphorus in PSG (wt %)
1.	Long	1425	4300	48	3.3
	Short	1500	3500	41	2.8
2.	Long	2660	4610	51	3.5
	Short	2670	4000	72	4.6
3.	Long	4750	0	16†	0
	Short	5100	0	17†	0
4.	Long	4180	4400	42	3.0
	Short	4000	4000	44	3.2

*Data based on curves from 8 to 17 pairs of measurements of etch time and residual film thickness by fringe counting.
**Data based on single etch time and 2 to 3 Talysurf thickness traces.
†SiO_2, etch rate.

Table F-4. Comparative Analysis of IC Glass Overcoats

Manufacturer Code	Passivation Type(1)	Pinholes in Overcoat,(2) # per pellet	SiO_2 Top Layer Thickness (Å)	PSG Layer Thickness (Å)	Layer Composition(3) wt % P	Layer Composition(3) mol % P_2O_5
A	A-1	0 - many	7,500	7,500*	0 9.7*	0 10.8*
B	B-1	0 - 4	0	7,700	7.8	8.5
B	B-2	6 - many	0	7,750	4.2	4.3
B	B-3	40	≤1,000	5,500	0 1.9	0 1.9
C	C-1	many	4,750	0	0	0
C	C-2	0 - many	1,840	4,385	0 3.3	0 3.4
C	C-3	2	1,280	5,880	0 2.8	0 2.8
C	C-4	20 - many	4,180	4,400	0 2.9	0 2.9
D	D-1	0	2,000	12,000	0 3.8	0 3.8
E	E-1	15	13,000	0	0	0

Notes: See (1) - (3) under E (p. 230) for explanation of column headings.

*This PSG layer is underneath the aluminum metallization. The glass is in a densified state as it had been heated to fusion temperature to produce a gradually tapered slope. Etch rate analysis was based on PSG standards fused at 1000°C for 1 hour in N_2.

manufacturing dates. The grand average for a given supplier's product would not be meaningful because of the wide spread in the data due to the existing variations of overcoat systems. Averages were therefore taken only for groups of ICs whose passivating overcoats had closely similar characteristics.

(2) "Pinholes in overcoat" refers to those over the aluminum metallization only. They were made visible by immersing the devices in hot aluminum etch. A density greater than 50 pinholes per pellet is defined as "many".

(3) "Layer composition" was determined by the "standard" etch rate analytical method. Electron probe microanalysis with PSG standards was employed in some cases for preliminary measurements.

F. CONCLUSIONS

A method has been devised to determine the quality of passivation overcoat layers deposited over aluminum-metallized ICs. The method assesses the chemical composition, the component layer structure, and the integrity of the dielectric overcoat in terms of the number of defects such as pinholes and microcracks over the aluminum metallization. The method is applicable for analyzing single- and multilayer structures of both SiO_2 and PSG.

Two techniques for determining layer thickness and composition have been developed and applied. In the "standard" or "long" technique the types and thicknesses of combination layers are determined from graphical plots of differential etch rates. The phosphorus contents in PSG layers are determined graphically from plots of isothermal etch rate by means of a standard calibration curve. This technique is precise, accurate, and reliable, but time-consuming to perform. It can and has been applied for analyzing more complex structures, such as triple-layer structures and the composition of primary passivation layers underneath the metallization.

The "simplified" or "short" technique is less accurate but is fast. The Talysurf profiles at 20,000X vertical and 100X horizontal magnifications are adequate, if done with great care and read out under a magnifying glass, for resolving typical PSG/SiO_2 overcoat layer thicknesses. The repeatability (precision) of the profilometric technique is good; variations for single film

thicknesses are generally well within ±10%. The etch time determination is precise to within a few percent. For layers on silicon substrates, the final values in terms of wt % phosphorus were about 10% lower than that by the longer method. The film thicknesses were also similarly lower (Table F-1). For IC pellets, the results obtained were within ±25% of those obtained by the longer method (Table F-2). It can be concluded that the simplified fast method is adequate for some applications where lower precision (±25%) is acceptable. The time savings are considerable, and the procedure is not tedious. The thickness of the densified SiO_2 layer beneath the glass passivation overcoat can be determined by difference from the same Talysurf traces.

The method has been successfully applied to the analysis of commercial ICs from various manufacturers. The conclusions that can be derived from this limited number of representative devices shows that a wide variation of layer combinations, layer thicknesses, and PSG compositions exists, not only from one manufacturer to another, but also within the products of a given manufacturer. The same holds for the pinhole density, which ranges from zero to many per device pellet. All ICs evaluated were plastic-encapsulated types. No microcracks were found in any of the devices tested, probably because none of the devices had undergone high-temperature heat treatments subsequent to CVD glassing, which is usually needed only for hermetic types. Hermetically sealed ICs should be included in future comparative studies of glass passivation. It is apparent that, when the devices were fabricated, manufacturers of ICs lacked either the necessary knowledge to decide what properties of the overcoat passivation should be specified and employed, or the process control techniques for effectively monitoring of the CVD processes, or both. Process design engineers have only recently begun to realize the importance of these matters in achieving a consistently high degree of product reliability.

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