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January 1976

DIRECT DIGITAL MODULATION CONVERTER (DDMC)

Sherbrooke University

Rome Air Development Center
Air Force Systems Command
Griffiss Air Force Base, New York 13441

DIRECT DIGITAL MODULATION CONVERTER (DDMC)

This report has been reviewed and is approved for publication.

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This report describes the prototype of a Direct Digital Modulation Converter (DDMC). The codes considered are PCM (pulse code modulation) and ΔM (delta modulation) with sampling frequencies of 16, 19.2, 32, 38.4 for the later. The objective is to convert from one form of digitized voice signal to another without reconstruction of the original analog signal. The results obtained indicate that DDMC's can be designed with characteristics as good as the existing analog means for converting between different codes. The prototype

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EQUIPE MODULATION DELTA

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PREFACE

Our team is indeed very happy to present this second and final report on a direct digital modulation converter to convert from pulse code modulation to delta modulation or vice-versa. The development shown in this text is the result of an original approach to the subject, which was first presented in 1967 and was further developed in 1973 (phase 1 report).

We are firmly convinced that our findings lift one of the major difficulties raised against the introduction of delta modulation in the existing telecommunication network. This is valid for military systems (tactical or strategic) as well as for commercial networks.

ABSTRACT

This report describes the prototype of a *Direct Digital Modulation Converter (DDMC)*. The codes considered are PCM *(pulse code modulation)* and ΔM *(delta modulation)* with sampling frequencies of 16, 19.2, 32 and 38.4kHz for the latter.

The objective is to convert from one form of digitized voice signal to another without reconstruction of the original analog voice signal. A single channel system is considered and operating time is consequently only limited by the 125μsec. frame prescribed by the PCM sampling frequency.

The results obtained indicate that DDMC's can be designed with characteristics as good as the existing analog means for converting from one code to the other.

The prototype herein presented uses serial operation and is built with TTL logic. It works with a CVSD operating at four different sampling frequencies and in connection with five PCM channel banks.

CONTENTS

EVALUATION

DIRECT DIGITAL MODULATION CONVERTER

The value of this program was to show that direct digital code conversion between dissimilar digitized voice systems can be accomplished with no degradation in voice quality. Prior to the Direct Digital Modulation Converter (DDMC), no technique existed that made Pulse Code Modulation (PCM) and Continuously Variable Slope Delta (CVSD) modulation techniques directly compatible and interoperable. The DDMC can significantly improve Long Haul Voice communications by decreasing the number of Analog-to-Digital, Digital-to-Analog conversions to which the original signal would have been subjected.

Under TPO #9, which includes the development fo the Unified Digital Switch for future integrated Defense Communications Systems, interconnection between different types of digitized voice users will take place. In order to accommodate the aforementioned types of users, without degradation in voice quality, a DDMC will be an integral part of the switch. This will enable interoperability between otherwise incompatible digitized voice systems.

Julian Gitlin

JULIAN GITLIN
Project Engineer

1- INTRODUCTION

The objective of the present report is to present the results of a feasibility study on a *Direct digital Modulation Converter*, hereafter referred to as DDMC, and to describe the DDMC prototype design and implementation.

Direct Digital Modulation Conversion is defined as conversion from one form of digitized voice signal to another without reconstruction of the original analog voice signal. In this study, we will limit ourselves to two types of numerical formats for voice, *pulse code modulation* (PCM) and *delta modulation* (ΔM).

The scope of this program is to determine the feasibility of developing a *single* ΔM-PCM DDMC. Operating time is therefore not a parameter of importance as long as the DDMC operates within the 125μsec frame prescribed by the PCM sampling frequency; it is a technological problem, once the present efforts are rightly concluded, to bring the operating time to less than 5μsec which would allow multiplexing of several, possibly 24, communications and would render the DDMC highly competitive with other equipment when inserted in an *integrated telecommunication network*. Such a network includes possibly three types of switching offices-spatial, PCM and ΔM-; subscribers could have numerical transmission right from their set.

The minimum technical characteristics required from the DDMC are those of the available link (PCM coder-PCM decoder-analog-ΔM coder-ΔM decoder or vice versa). In the feasibility study, the *signal-to-noise* (S/N) ratio is the primary performance criterian. The ratio is obtained from test tones at various amplitudes (dynamic range).

The digital link that the DDMC provides has to give equal or better quality, in terms of S/N, than the voice quality obtained with the *analog* link, where signals are converted to analog form before being again coded digitally. The present study shall consider the CVSD type of delta codecs and the four different PCM channel banks: the D-1, TD968, TD660 and the European system.

In Chapter 2, the computer simulation of the CVSD and of the converter (DDMC) is described.

Chapter 3 deals with the implementation of the CVSD and of the DDMC. The structure of the DDMC is first analysed and the overall design is then described. Detailed circuit operation, drawings, diagrams and components are given in appendices A and B. Results of objective and subjective tests are given in Chapter 4. A general conclusion finally closes the study with a review of the main characteristics found.

2. THEORETICAL STUDIES

2.1. DELTA CODEC

The delta codec is an A/D converter. It is a closed loop system whereby the bit transmitted indicates the slope of the input signal between two sampling times. The transmitted digitized signal is reconstructed in the feedback loop which is the demodulator; this demodulator is the important part of the system and its design differentiates one codec from others.

2.1.1. DELTA CODEC PRINCIPLE

Figure 2.1 shows the block diagram of a non-adaptive delta codec.

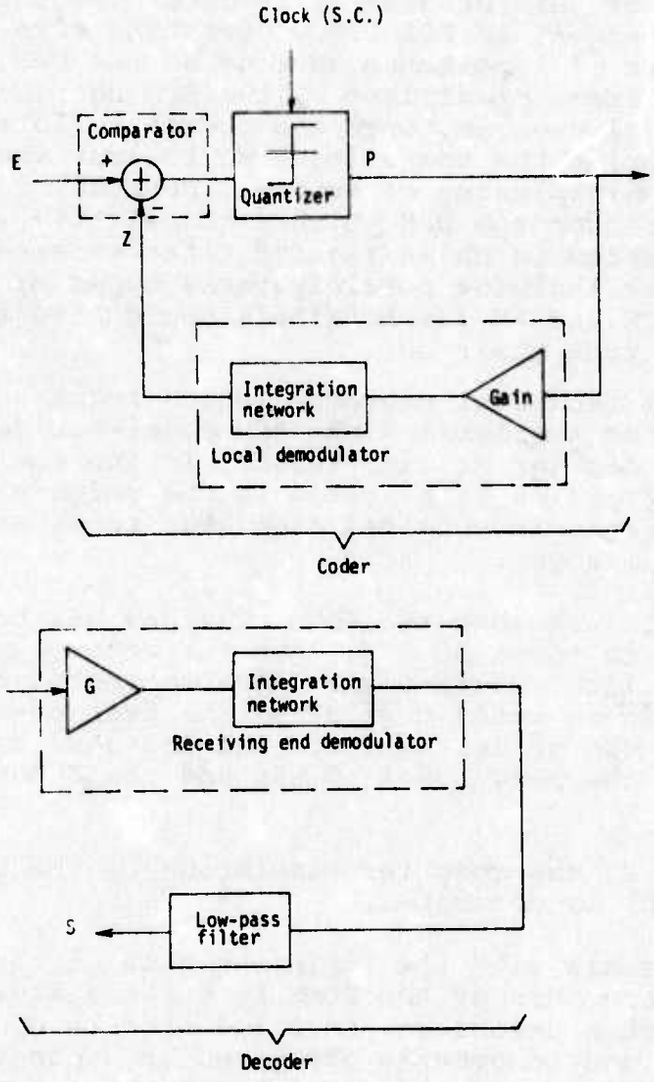


FIGURE 2.1.- Non adaptive delta codec principle.

The input signal (E) is compared to the reconstructed signal (Z) in the comparator; the difference or error (E-Z) is then passed through a two-level quantizer, which is controlled by a sampling clock (S.C.). At each clock time the quantizer gives the information on the sign of the error. The quantizer output is a "1" if the error is positive and a "-1" if the error is negative. The sequence (P) of "1" and "-1" is then integrated in the feedback loop; the gain (G) is the static gain of the integration network. The output of the "local" demodulator is a staircase signal (Z) called the reconstructed signal.

At the receiving end, the output of the demodulator (identical to the local demodulator in the feedback loop of the codec) or the reconstructed signal (Z) is passed through a low-pass filter which smoothes the staircase signal by removing the high frequency components.

2.1.2.C.V.S.D. PRINCIPLE

The continuous-variable-slope-delta (CVSD) modulation system is an adaptive type delta codec since the gain of the demodulator in the feedback loop is made variable in order to follow the amplitude or slope variation of the input signal.

In the CVSD, adaptation or companding is achieved through the past behaviour of the signal averaged over a rather long period of time, compared to the sampling period; the control is done with the digital description of the waveform (bit stream).

Figure 2.2 shows the block diagram of the CVSD.

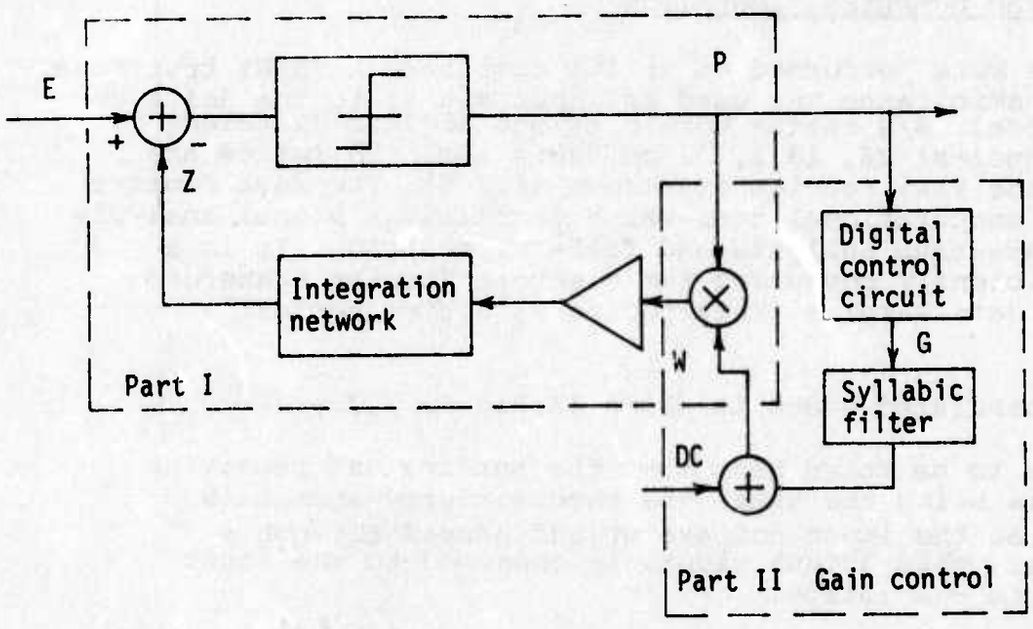


FIGURE 2.2.- CVSD block diagram.

An incoming analog signal E is compared with a reconstructed analog signal Z by means of a comparator which outputs either a logic 1 or a logic 0, depending on which of the signals E or Z is the larger. The result of this comparison is then clocked through the quantizer and transmitted as the encoded digital output P.

The reconstructed analog signal Z is produced by integrating the digital output P which has been multipled by a weighting factor (W) provided by a gain control incorporated thereon in order to produce a more accurate profile of the analog signal E. This weighting factor is initiated by detecting at least three like and consecutive bits in the binary sequence of P, by means of a digital control circuit. Upon this detection, a signal G is produced and furtheron filtered through a syllabic low-pass filter (usually at 25 Hz). The output of the syllabic filter is a continuous signal which is added to a DC voltage to increase the amplitude of the filter output and to improve its signal-to-noise ratio. This signal W is thereafter multiplied by the output digital signal P to obtain a delta step which is then integrated by means of the integrator network.

An important point with respect to gain control (Part II) is that the digital control circuit is controlled by a three-bit memory (A, B and C), whereby the following control logic is performed:

$$G = ABC + \bar{A}\bar{B}\bar{C}$$

2.1.3. CVSD COMPUTER SIMULATION

Studies were performed on an IBM computer. A 750Hz test tone with a 40db dynamic range was used as input signal to the delta codec computer model. S/N ratios were obtained at four different sampling frequencies: 16, 19.2, 32 and 38.4 kHz. S/N ratios are obtained from the fast Fourier transform (F.F.T). The fast Fourier transform is a computational tool which facilitates signal analysis such as power spectrum analysis and filter simulation. It is a method for efficiently computing the discrete Fourier transform of a series of data samples (referred to as a time series).

The simulated codec is shown in Figure 2.3.

It is to be noted here that the sending and receiving end demodulators being the same, the reconstructed signal is taken directly at the input comparator and passed through a smoothing filter. This output signal is compared to the input signal to compute S/N ratios.

In the simulation model all the blocks are represented in transfer function form, using the Laplace transformation.

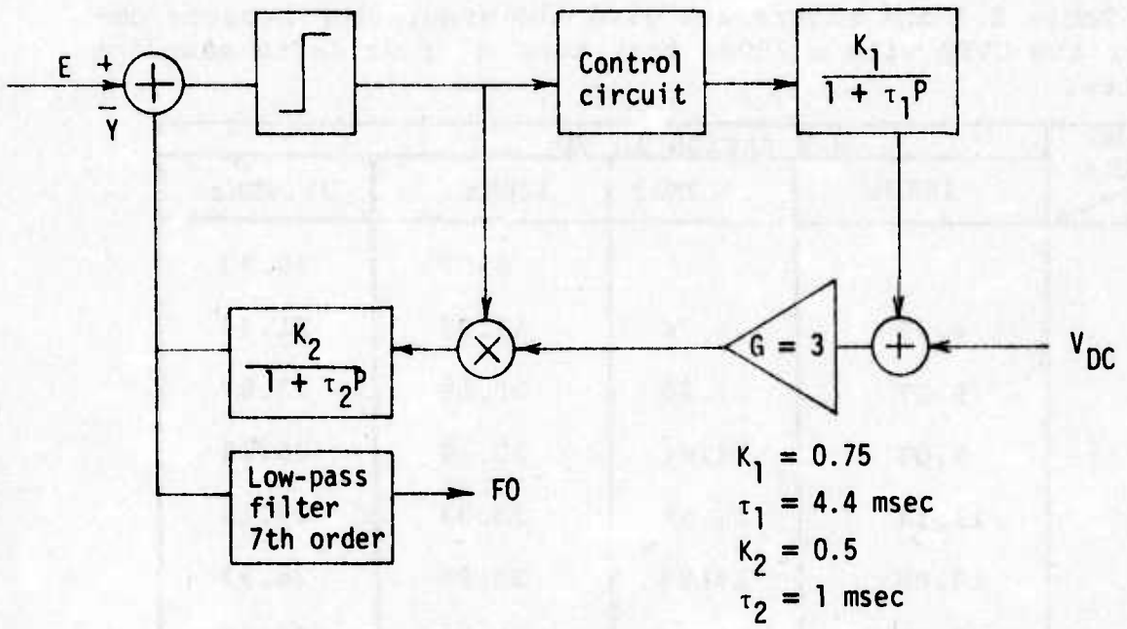


FIGURE 2.3.- CVSD simulation block diagram.

The Laplace transformation is a process of transforming a time domain function into the s (complex frequency) domain. The frequency response characteristic and the transfer function of the 7-th order low-pass filter are shown in Figure 2.4.

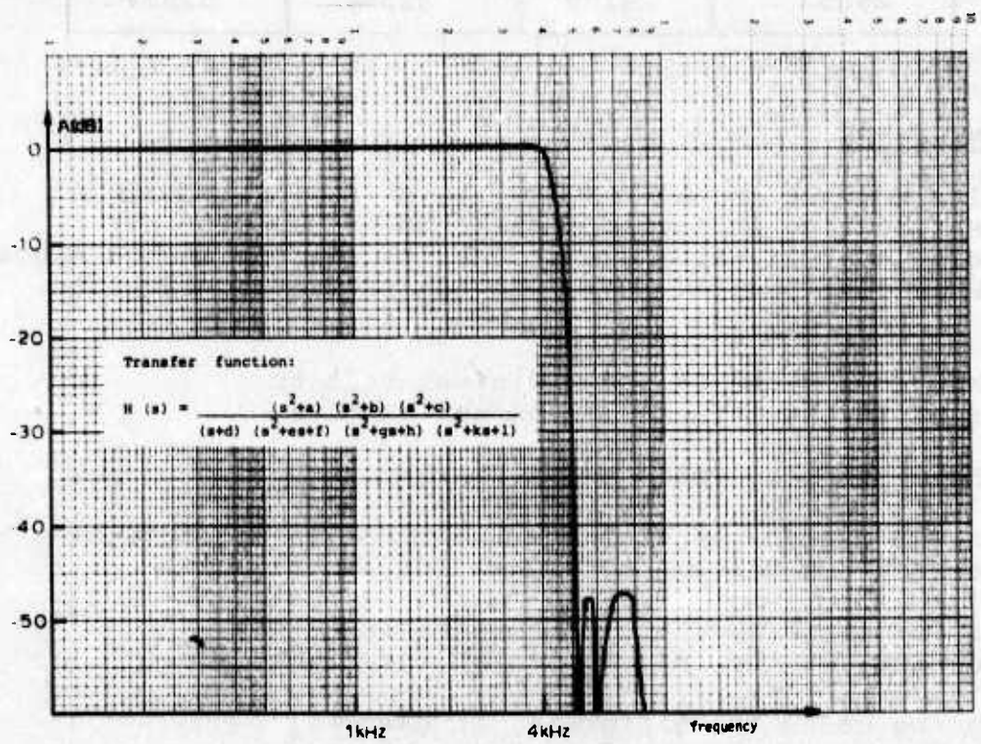


FIGURE 2.4.- Frequency response and transfer function of the 7th order low-pass filter.

Table 2.1 and Figure 2.5 give the simulation results obtained for the CVSD with a 750Hz test tone at four delta sampling frequencies.

SAMPLING FREQ. / INPUT AMPLITUDE	S/N ratios in db			
	16KHz	19.2Khz	32KHz	38.4KHz
0.01			6.87	10.93
0.03	4.78	5.76	17.22	21.44
0.10	9.27	14.95	20.59	23.07
0.30	9.07	14.84	22.16	26.28
0.60	11.14	13.59	25.34	28.15
1.00	12.89	14.03	23.90	26.91
2.00	13.97	16.18	21.85	23.40
3.00	14.08	15.96	20.20	21.69
6.00	13.77	14.90	16.65	17.04
V_{DC}	261mV	261mV	525mV	525mV

TABLE 2.1.- CVSD computed S/N ratios for a 750 test tone

2.2. CONVERTERS

Delta Modulation and PCM are two different methods of digitally representing an analog signal. Both transmit only samples of the input signal and thus the information on the signal is available only at sampling time. In the present application, they differ in two ways:

- -they do not use the same digital code to transmit the information on the samples.
- -their sampling rates are different.

Therefore, a PCM decoder receiving a binary delta sequence is unable to reconstruct the analog signal for two reasons:

- -as sampling rates are different, it is not looking for the information at the right time.
- -as the codes are different, it cannot "understand" the meaning of the binary words it is receiving.

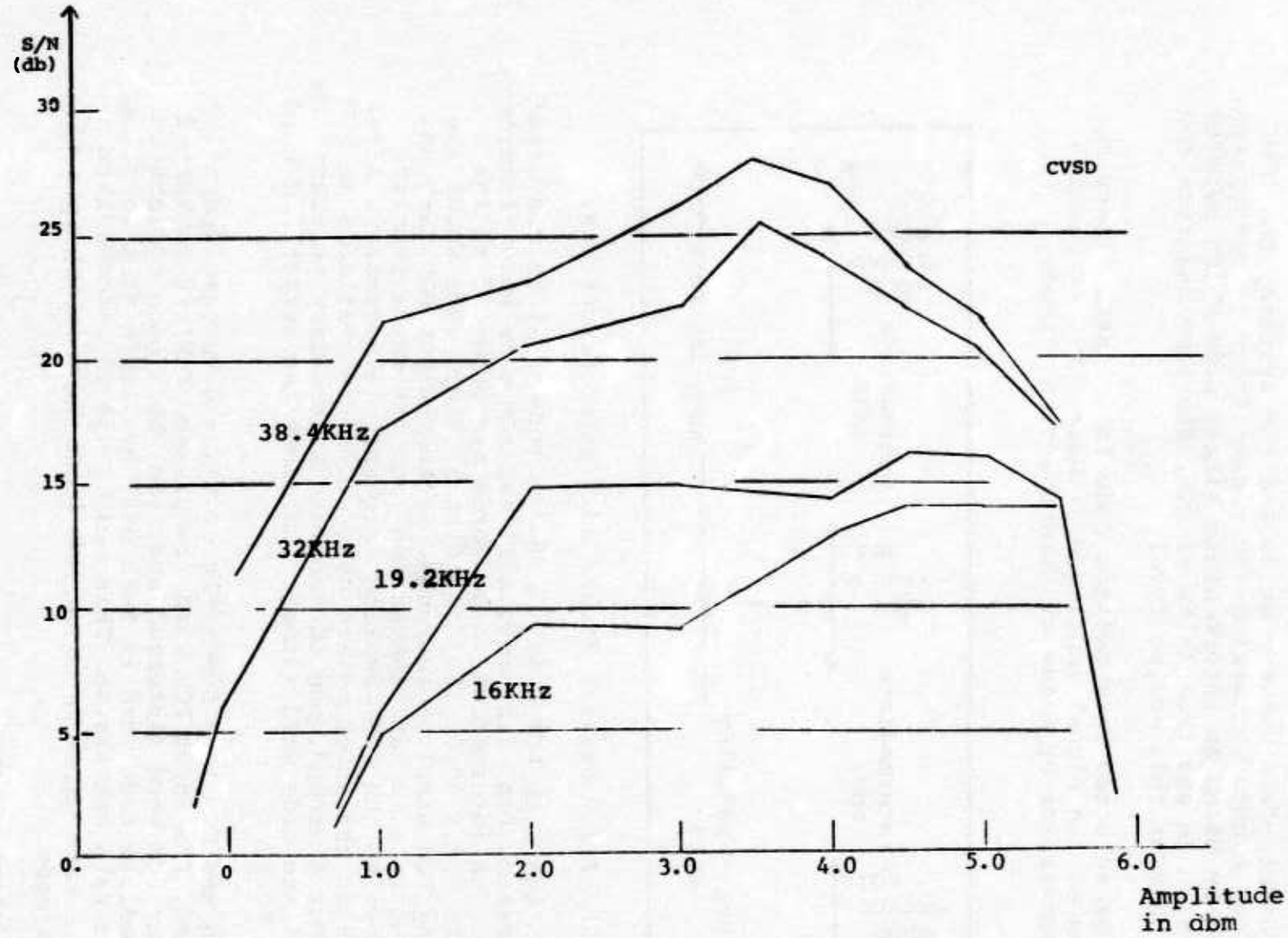


FIGURE 2.5.- CVSD computed S/N ratios for a 750 Hz test tone.

To interface between delta and PCM systems, the DDMC has to realize a code conversion and a sampling rate conversion. This is done by using an intermediate binary code which permits easy conversion to and from delta or PCM. The sampling rate conversion is made at this coding level.

The selected intermediate code is a linear binary representation of the signal amplitude (linear PCM). It permits easy rate conversion by means of interpolation methods.

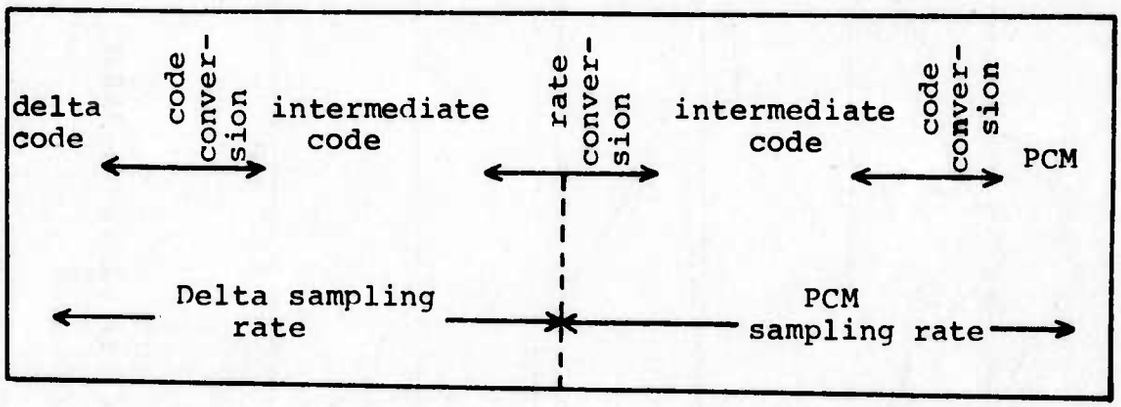


FIGURE 2.6.- General Method of Digital Conversion.

In the Δ to PCM DDMC, a delta code word is converted (code conversion, Fig. 2.6) into a linear PCM code word (intermediate code). The intermediate code words are produced at the Δ sampling rate (38.4 32.0, 19.2 or 16 kHz). These code words are needed at the PCM sampling instants. As the output PCM uses an 8kHz sampling rate, a rate conversion from the delta sampling frequency down to the PCM sampling frequency is necessary. After this conversion the intermediate code words are available at PCM sampling rate. A second code conversion is necessary to transform the intermediate code word (linear PCM) into the output PCM word (compressed PCM).

In the PCM to Δ DDMC (Fig. 2.6), the reverse operations are performed. The input PCM word (compressed PCM) is converted into a linear PCM word (intermediate code) by a code conversion. This intermediate code word is then made available at Δ sampling instant by a rate conversion. This result is an intermediate code at the Δ rate which is converted (code conversion) into the output delta code.

2.2.1 GENERAL MODELS

The delta to PCM and PCM to delta DDMC's are completely digital. They work with sampled signals expressed in binary form.

Therefore, once per sampling period each block in Figures 2.7(section 2.2.1.1.) and 2.9(section 2.2.1.2) receives

a binary number which represents the input value and uses it to compute the output value which is also a binary number.

2.2.1.1. DELTA MODULATION TO PCM CONVERSION

Figure 2.7 shows the general model of a Δ to PCM DDMC. The code conversion, from delta to linear PCM (intermediate code) is made by the gain control circuit and the digital integrator.

FIGURE 2.7.- General Model of a Δ to PCM DDMC.

The intermediate code represents the amplitude of the transmitted signal. To reconstruct this amplitude (at the delta sampling rate) the incoming delta sequence is first fed into the *gain control* circuit which determines the delta step size. This gain control circuit is a logic circuit which utilizes an algorithm similar to the algorithm of the delta modulator. Using the delta sequence, it generates once per Δ period a binary word which represents the value of the delta step at this instant. The digital *integrator* is another logic circuit which determines the amplitude of the transmitted signal by adding the delta step values. It is a digital addition and the output is a binary word: the intermediate code word.

The digital filter and the sampler at PCM rate realize the delta to PCM rate conversion. The digital *filter* is a logic circuit which transforms the digital version of the signal (represented by the binary intermediate code) in the same way as a continuous filter would transform the analog version of the same signal (represented by an analog voltage). It is a low-pass filter (cut-off frequency around 3.5 kHz) whose purpose is to attenuate high frequency components of the delta quantizing noise. The output of the filter is again a sequence of binary words which represents the transmitted signal smoothed by the low-pass characteristic.

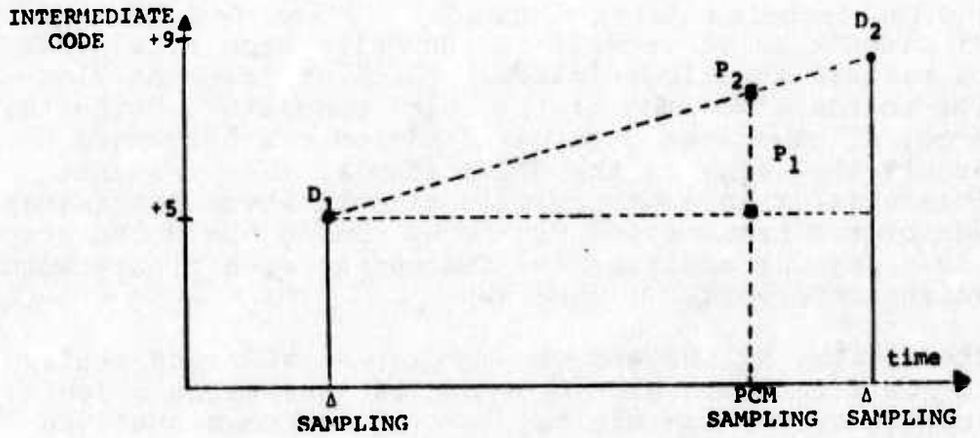
The rate reduction from delta frequency down to 8 kHz is made by the *sampler*. At the input of the sampler, the amplitude of the voice signal (intermediate code word) is known at each delta sampling instant. The sampler is a logic circuit which has to generate an intermediate code word at each PCM sampling time. The complexity of the circuit depends on the delta sampling rate.

At 32kHz, the sampler only needs to disregard three samples out of of four and keep the fourth one. At 19.2kHz and 38.4kHz the circuit is more complex because the delta rate is no longer a multiple of the PCM rate and the sampling instants are not coincident. In this case the PCM sampling time is generally in between two delta sampling times and as the value of the intermediate code is known only at delta sampling time, the value at PCM sampling time must be estimated by an interpolation method. The interpolation method depends on the system signal-to-noise ratio (i.e depends on the type of delta modulation and on the sampling frequency):

-when possible without degrading the system performance, a *zero-order digital holder* is used. In this case the latest available value is stored (hold) and used when needed (Figure 3.3).

-when a higher quality is necessary, a *linear interpolation* is used (Figure 2.8).

Such interpolations add noise to the system and in some cases a low-pass digital filter (cut-off frequency around 3.5kHz) must be placed after the interpolator to remove excessive out-of-voice-band noise.



D1 and D2 are two successive code words at Δ sampling time. P1 and P2 are two different estimates of the code value at PCM sampling time. P1 is obtained by zero-order holding and P2 by linear interpolation.

FIGURE 2.8.- Interpolation Methods

The intermediate code word which appears at the output of the sampler at PCM rate is a binary linear representation of the transmitted signal. This linear word is then *compressed* into the 7 or 8 bit PCM code according to the remote PCM channel bank characteristic.

2.2.1.2. PCM TO DELTA MODULATION CONVERSION

The general model of a PCM-delta DDMC is shown in Figure 2.9.

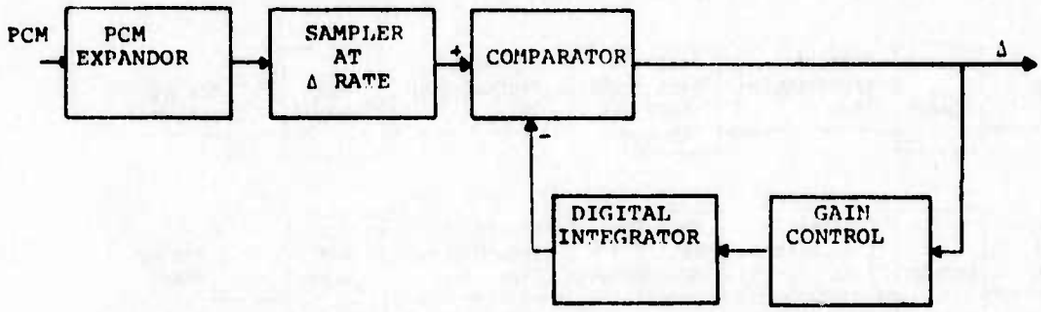


FIGURE 2.9.- General Model of a PCM to Δ DDMC.

The PCM *expandor* converts the incoming PCM word (compressed) into the intermediate code word (linear PCM, see Figure 2.6).

The *sampler* performs the rate conversion from PCM to delta sampling frequencies. The PCM sampling rate being smaller than the delta cne, intermediate code words (in between two PCM samples) are estimated by interpolation methods similar to those of section 2.2.1.1.At the output of the sampler, binary intermediate code words are available at delta rate.

The *comparator* and the *gain control circuit* and the *digital integrator* realize the conversion from intermediate to delta codes. At each delta sampling time, the intermediate code word is compared to the binary word generated by the feedback loop gain control and integrator. A delta bit one or zero is produced depending on the result of the comparison (positive or negative result). This delta bit is available for transmission and is also fed into the feedback loop. With this information, the gain control circuit and the digital integrator determine the value of the reconstructed signal. The gain control and the integrator were described in section 2.2.1.1.

2.2.2. SYSTEM APPROACH

Performances of PCM and delta codecs are evaluated by computing the amount of quantizing noise they add to the transmitted signal. The same criterion has to be used for the DDMC, but it is impossible to consider it alone. The converter receives a binary code and produces another code which cannot be used directly to compute the signal-to-noise ratios. Therefore, the DDMC must be simulated when inserted in the complete codec-converter-codec system.

The objective is to have a quality better (or equal) than the quality obtained by going back to an analog signal to make the conversion. Thus, the complete systems shown in Figure 2.10 have to be simulated and their per-

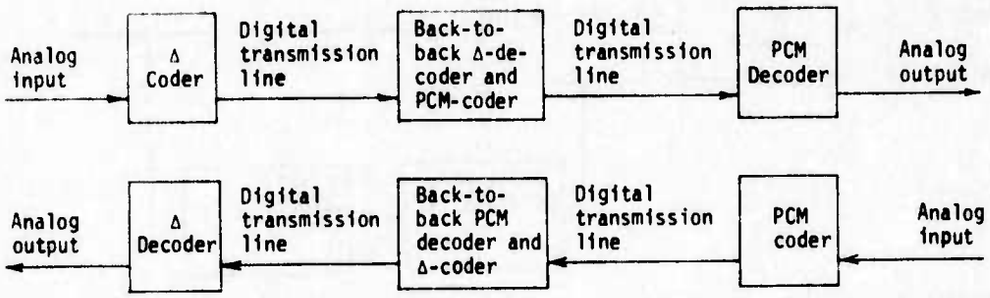


Figure 2.10A.- Reference System

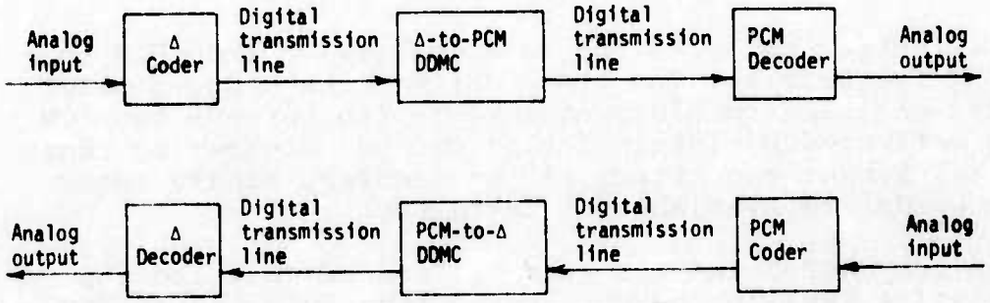


FIGURE 2.10B.- System with DDMC's.

formances compared, the signal-to-noise ratio of the analog system being used as a reference. It must be noted that the DDMC, being digital, can be exactly simulated on a general purpose computer. This is not true for the delta and PCM codecs which are partly analog circuits which have to be digitized in order to be simulated. Because of analog hardware inperfections, the real codecs introduce more degradation than the simulated ones and therefore the DDMC could be designed to give a S/N lower (probably by 2 or 3db) than the reference but would still offer the same quality as the analog system. However, it was decided to design it to obtain the same S/N as the reference for the following reasons:

1. to have as good a quality as possible,
2. since no practical tests had yet been made, the difference between computed and real performances of the analog system could not be properly evaluated.

2.2.2.1. 16kHz DELTA TO PCM (FIGURE 2.11)

In Figure 2.11 and in all the following figures the digital filters are defined by their Z-transfer functions. Each filter is represented by a box which contains the function with the proper coefficient values.

As explained in Section 2.2.1.1 the first block is the gain control circuit which receives the delta sequence and which generates, once per sampling period, a binary number representing the delta step size. In the case of CVSD the gain control circuit is made of a logic block followed by an analog syllabic filter (see section 2.1.2). Therefore, the DDMC gain control circuit contains the same logic block followed by a digital syllabic filter.

The digital integrator is a digital first-order low-pass filter with a very low cut-off frequency. It digitally ingegrates all the binary numbers received from the gain control circuit and produces, once per delta sampling period, a binary number which represents the sum of all the delta steps. This binary number is the intermediate code word.

The intermediate code word is then processed by a 4th-order digital low-pass filter in order to attenuate high frequencies of the quantizing noise before the rate conversion. Once per delta sampling period the filter produces a linear PCM word (binary number) which represents the transmitted voice signal from which the delta noise has been filtered.

The rate conversion form delta to PCM sampling frequency is made by a zero-order holder (see section 2.2.1.1) followed by a sampler at 8kHz (PCM rate). The output of the sampler is a linear PCM word (intermediate code) which is digitally compressed (see section 2.2.1.1) to produce the PCM word.

2.2.2.2. PCM TO 16kHz DELTA (FIGURE 2.12)

The intermediate code (linear PCM) at PCM rate is produced by the PCM expandor (see section 2.2.1.2).

The rate converter must increase the sampling frequency from 8 to 16 kHz. It is made of a linear interpolator (section 2.2.1.1) and of a first-order low-pass digital filter. The low-pass filter (cut-off frequency 3.2 kHz) smoothes the staircase type signal given by the linear interpolation. The output of the filter is thus the intermediate code at 16kHz.

The intermediate code to delta conversion is made by comparing the value of the intermediate word to the value of the digital number produced by the feedback loop. As explained in Section 2.2.1.2 delta bit 1 or 0 is transmitted depending on the

result of the comparison and the feedback loop is composed of a gain control circuit and an integrator similar to those of Section 2.2.2.1.

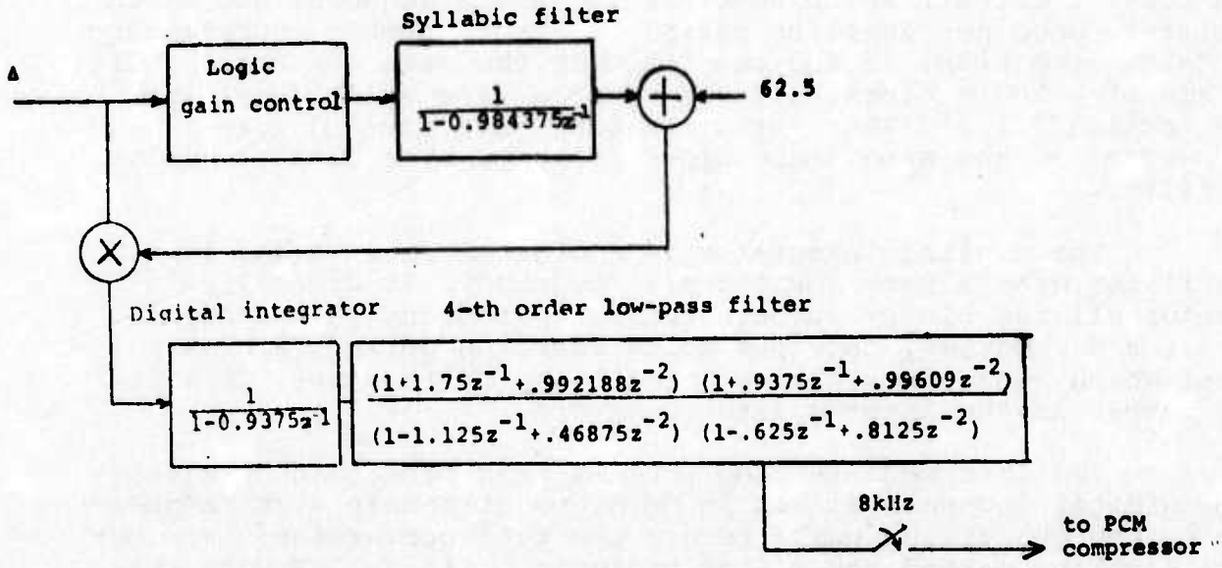


FIGURE 2.11.- 16kHz CVSD to PCM DDMC

2.2.2.3. 32kHz DELTA TO PCM (FIGURE 2.13)

Except for the sampling frequency this converter is similar to the one of Section 2.2.2.1. Again a 4th- order low-pass filter is used to attenuate delta noise high frequencies. Its cut-off frequency is 3.2kHz. As indicated in Section 2.2.1 the holder and smoothing filters are not necessary when the sampling rate is reduced from 32kHz to 8kHz. As sampling times are coincident it suffices to use one sample out of four and to disregard the three others.

It must be noted that the coefficient values of a digital filter depend on the sampling frequency. Therefore the coefficients of the 32kHz filter (integrator and low-pass filter) are different from the coefficients of the 16 kHz filters of Section 2.2.2.1 even though the frequency responses are similar.

2.2.2.4. PCM TO 32kHz DELTA (FIGURE 2.14)

Except for the sampling frequency, this circuit is the same as the one of Section 2.2.2.2.

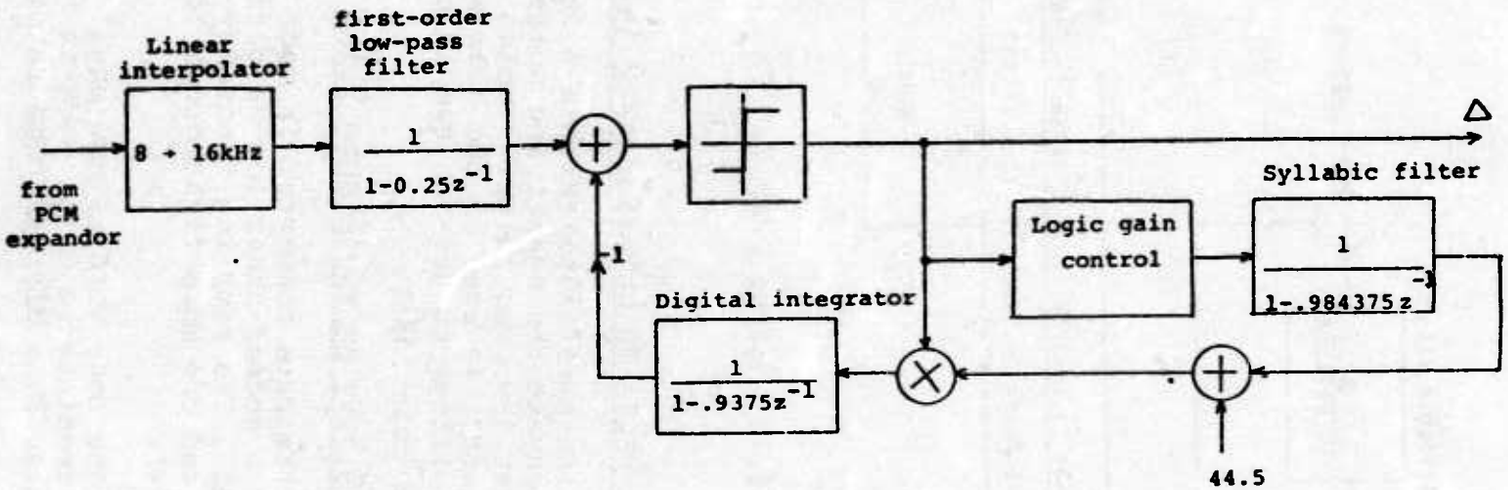


FIGURE 2.12.- PCM to 16kHz CVSD.

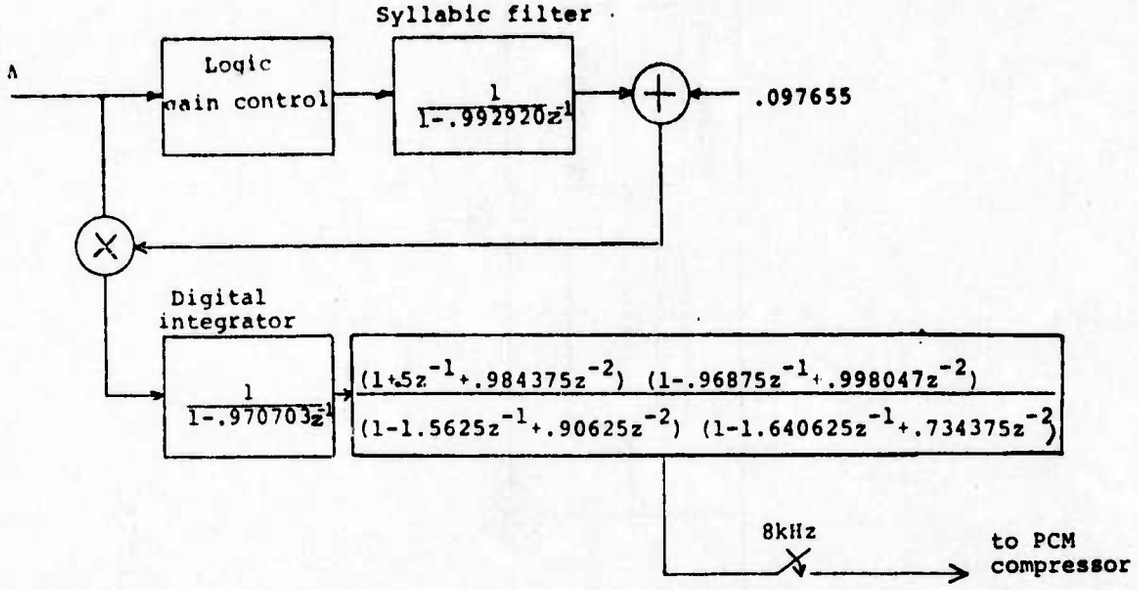


FIGURE 2.13.- 32kHz CVSD to PCM

2.2.2.5. 19.2kHz Delta to PCM (Figure 2.15)

A 4th- order low-pass filter with a 3.2kHz cut-off frequency is used to attenuate the quantizing noise. A zero-order holder with a second-order low-pass filter sampled at 64kHz and with a 5kHz cut-off frequency is used in the sampler. To reduce from 64kHz to 8kHz, it suffices to use one sample out of eight, the sampling times being coincident.

2.2.2.6 PCM to 19.2kHz delta (Figure 2.16)

The PCM to delta rate converter is made of a linear interpolator followed by a second-order low-pass filter at 64kHz (cut-off frequency: 5 kHz). The sampling frequency is then reduced to 19.2 kHz by a holder and one more first-order low-pass filter (cut-off frequency: 3 kHz).

The intermediate code word is now available at Δ rate. The conversion from intermediate to delta code is made, as explained in Section 2.2.2.2, by a digital comparator and a feedback loop.

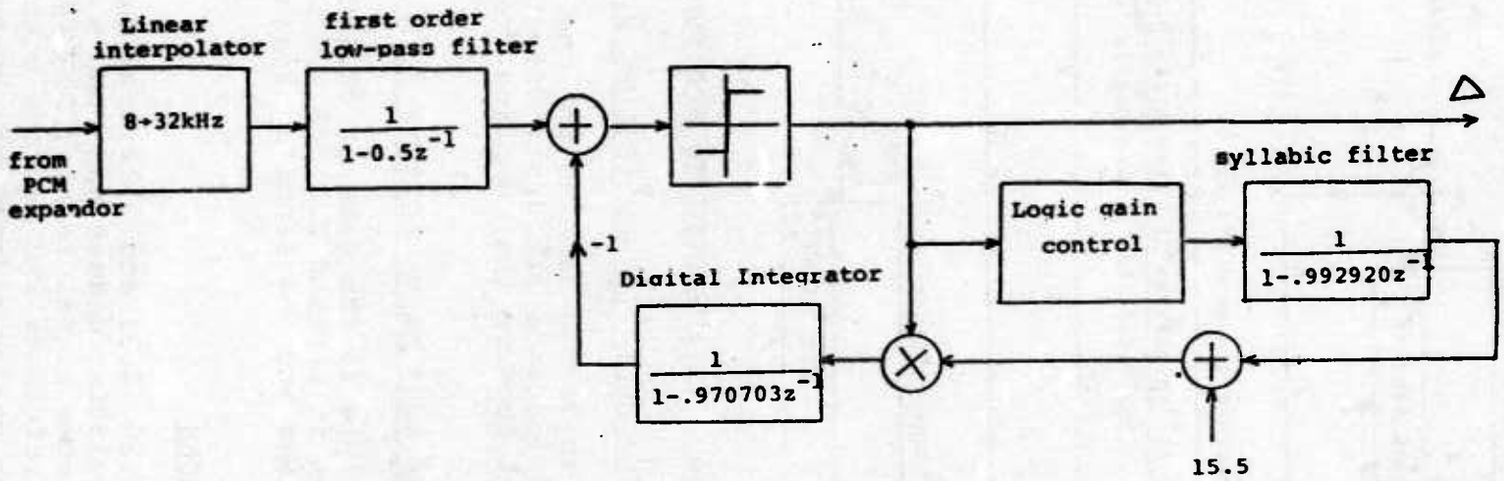


FIGURE 2.14.- PCM to 32kHz CVSD

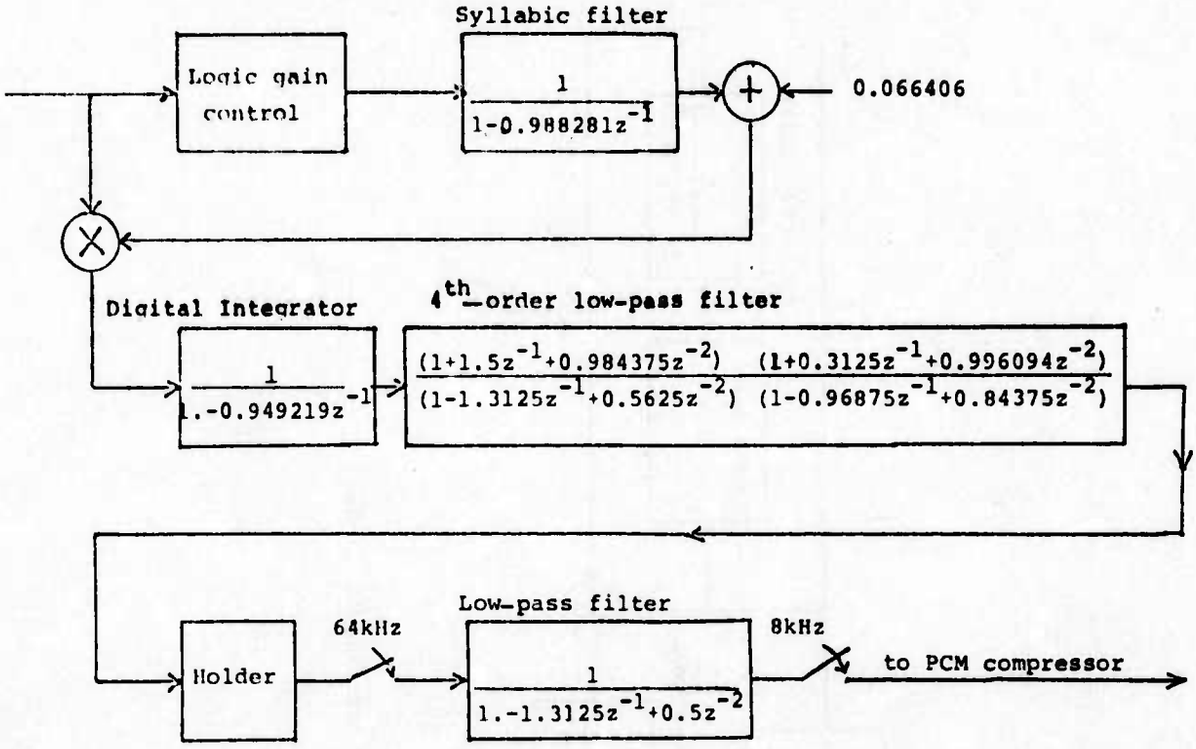


FIGURE 2.15- 19.2kHz CVSD to PCM DDMC.

2.2.2.7. 38.4 kHz DELTA TO PCM (FIGURE 2.17)

The block diagram is the same as the one shown for the 19.2kHz Delta to PCM DDMC (Section 2.2.2.5). Only the filter coefficients are different because the sampling frequency is different.

2.2.2.8. PCM TO 38.4kHz DELTA (FIGURE 2.18)

Again the principle is the same at 38.4kHz as at 19.2kHz and the explanations given in section 2.2.2.6 are still valid. Only the coefficient values and the sampling frequency are different.

2.2.2.9 PERFORMANCES

Figures 2.19, 2.20, 2.21 and 2.22 show the signal-to-noise ratios computed by simulating codecs and DDMC's at the four sampling frequencies. At some signal levels, DDMC's perform slightly better than the reference and at some others slightly worse. This is because the analog filters of the reference and the digital filters of the converters do not have exactly the same cut-off frequencies. As we used a single input frequency in the simulation, the quantizing noise spectrum was peaky and the

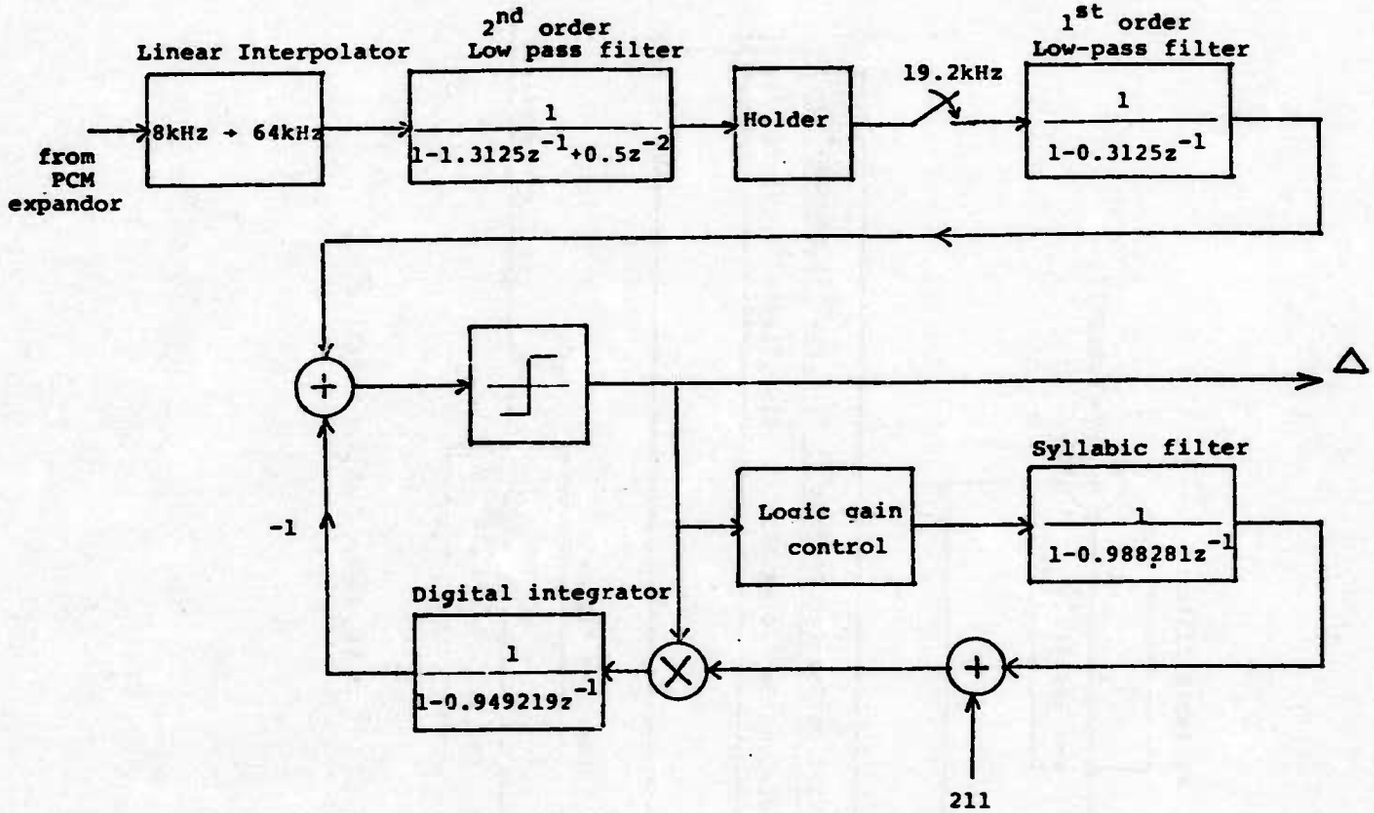


FIGURE 2.16.- PCM to CVSD, 19.2kHz.

S/N was therefore quite sensitive to cut-off frequency. Results are judged good since average S/N ratios are similar over the complete dynamic range.

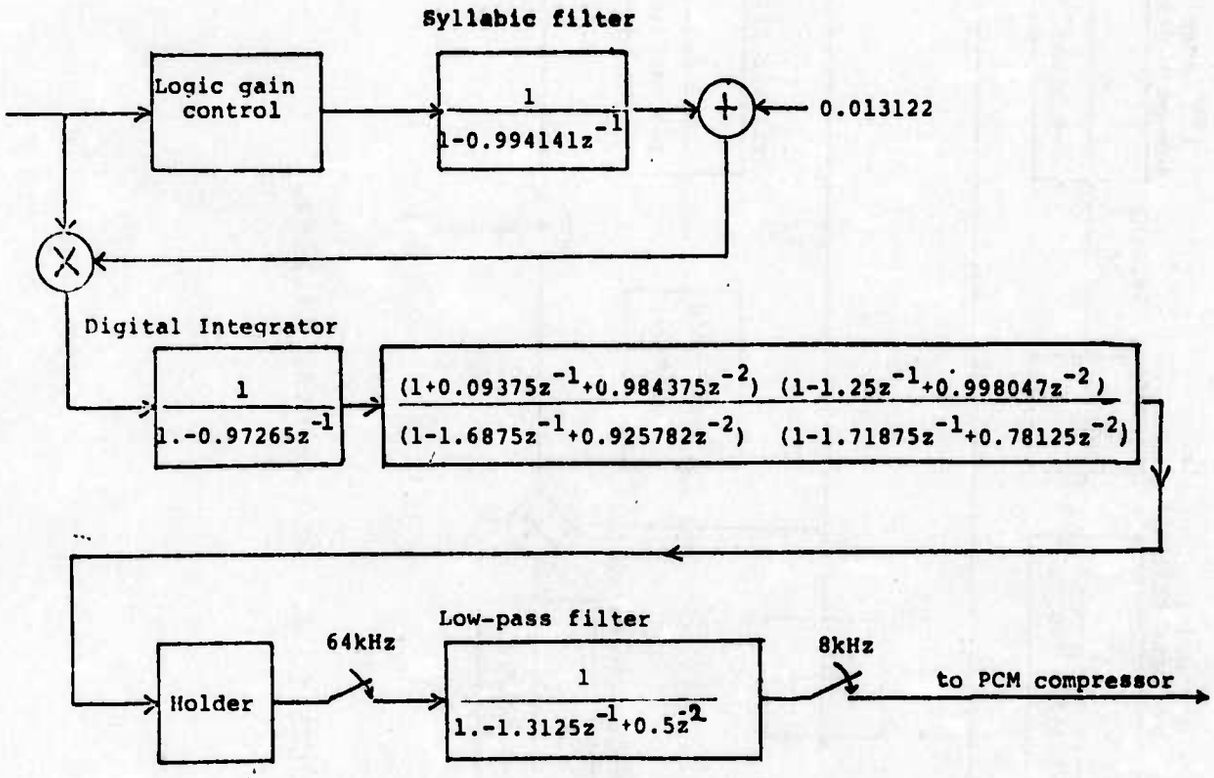


FIGURE 2.17.- 38.4kHz CVSD to PCM DDMC

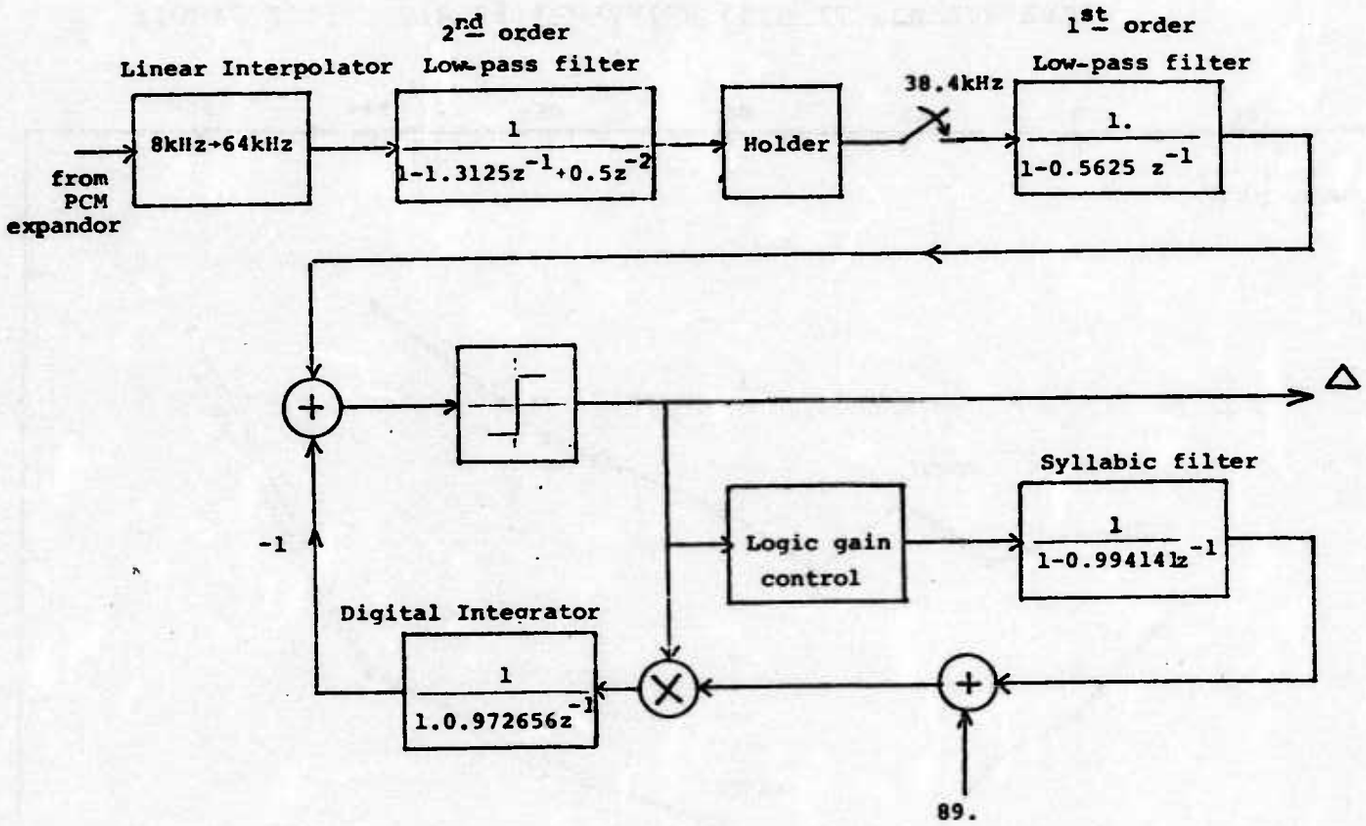


FIGURE 2.18.- DCM to CVSD, 38.4kHz

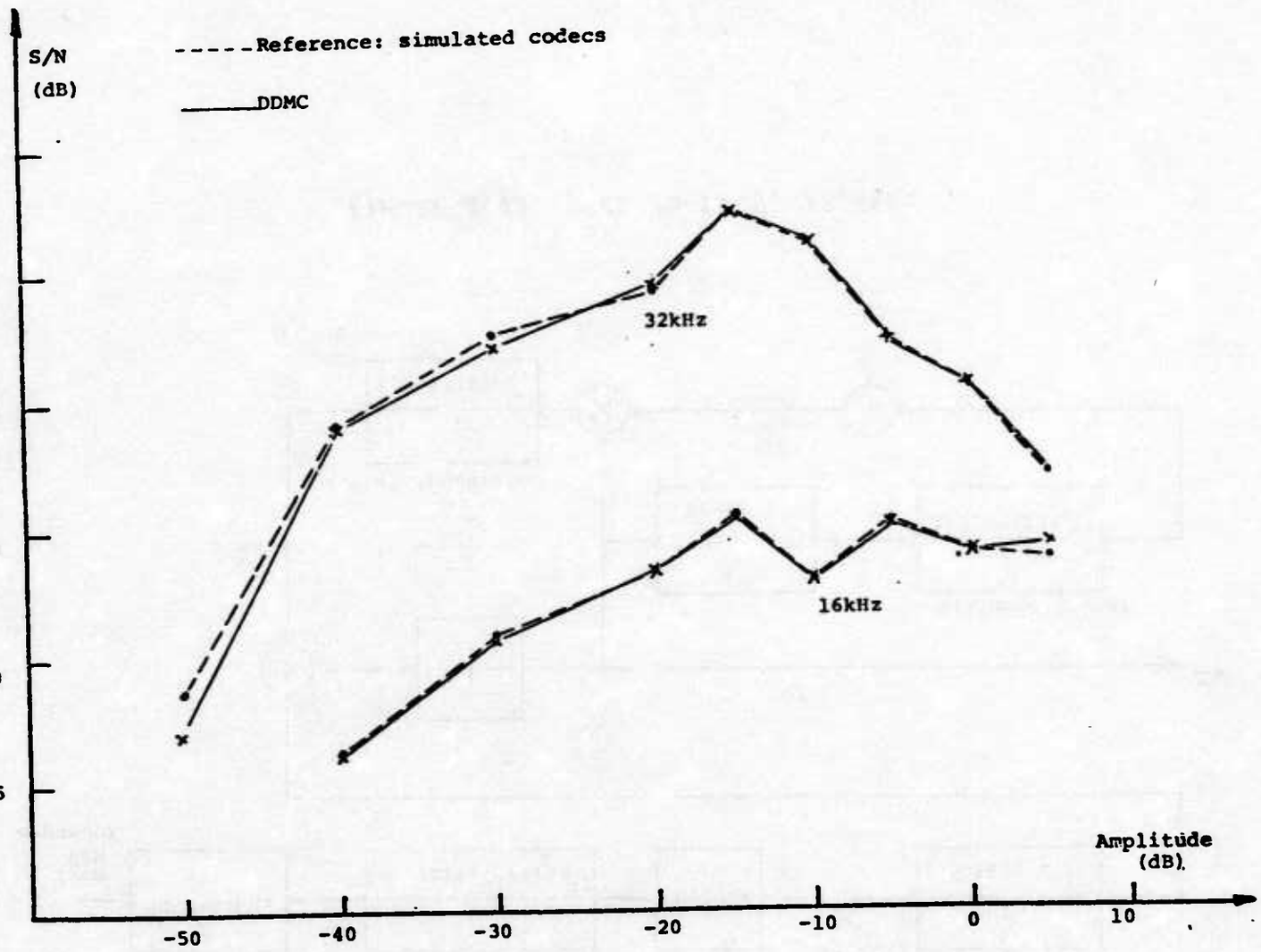


FIGURE 2.19.- S/N of simulated CVSD to PCM converter.

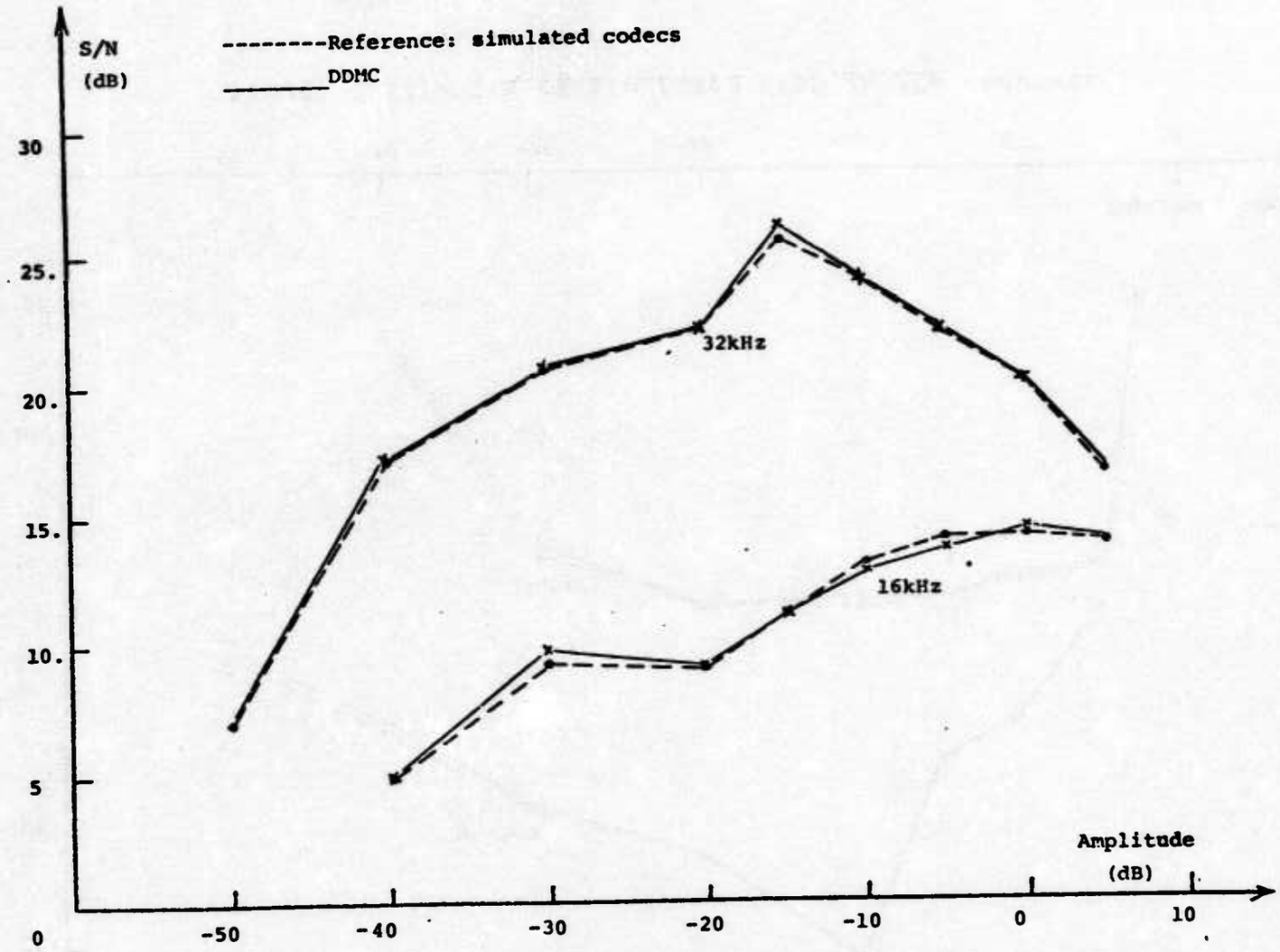


FIGURE 2.20.- S/N of simulated PCM to CVSD converter

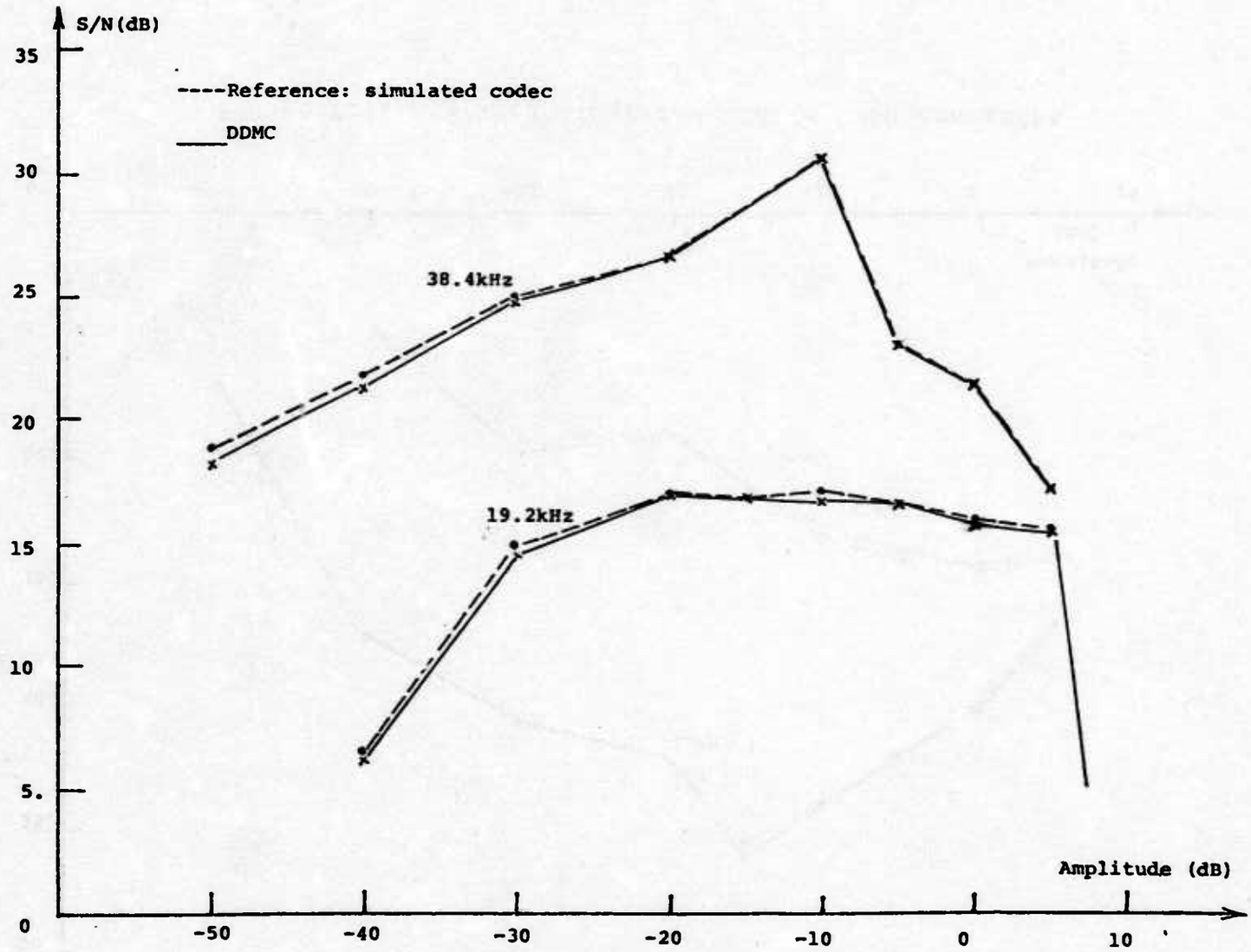


FIGURE 2.21.- S/N of simulated CVSD to PCM converter.

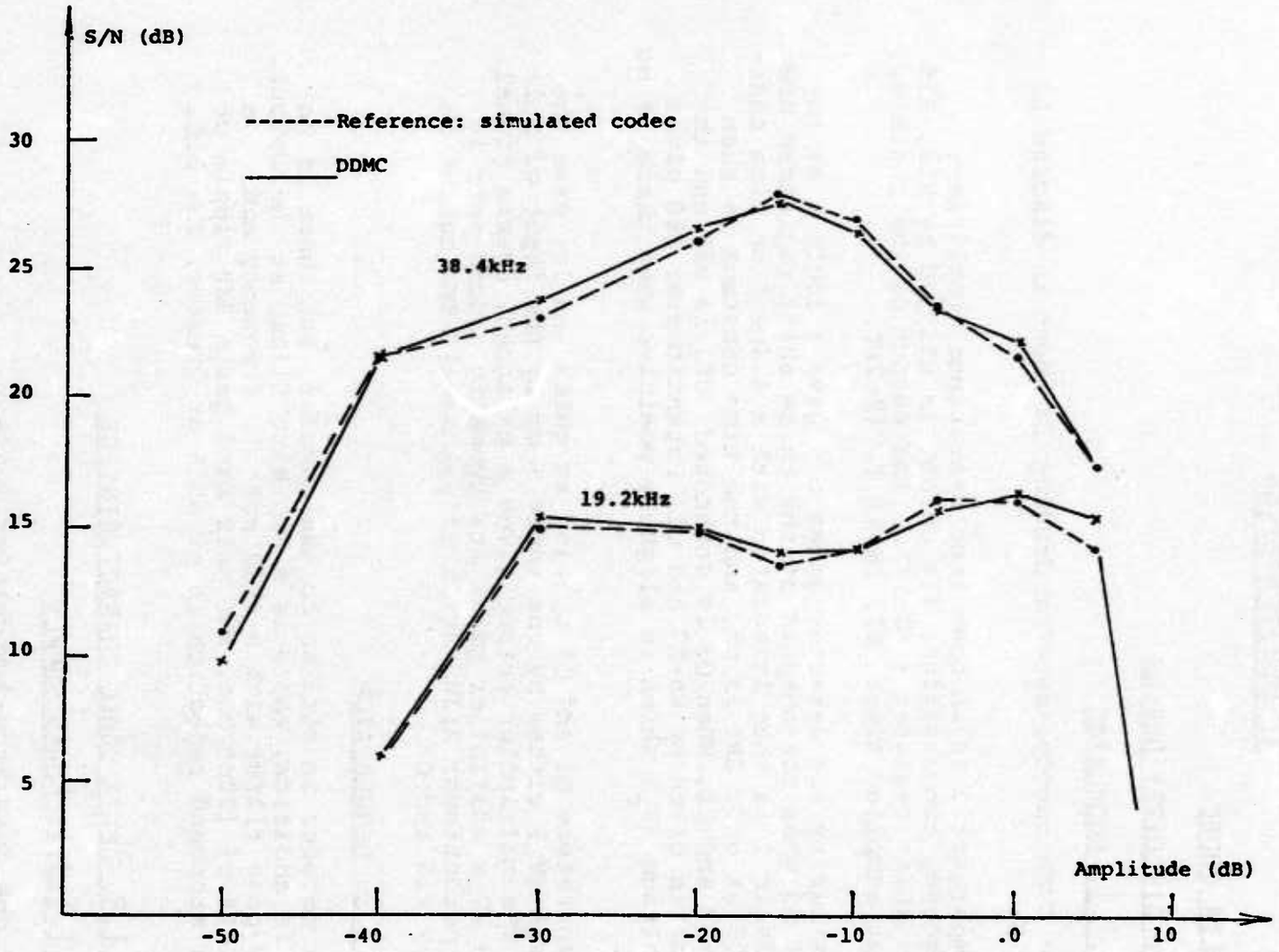


FIGURE 2.22.- S/N of simulated PCM to CVSD converter.

3. IMPLEMENTATION

3.1. DELTA CODEC

3.1.1. CIRCUITRY DESIGN

3.1.1.1. MODULATOR

The CVSD encoder-decoder drawing is shown in diagram B2 of Appendix B.

Comparator 2 is an open loop operational amplifier, without frequency compensation. Its output is clipped by R18, R19 CR2 to drive shift register 4 (0-5V). The output of the register gives bits at sampling times NT, (N-1) T, (N-2)T.

Similarity bit detector gates 5,6 give a logic 1 at the collector of Q3 when the outputs of the three shift registers are equal.This logic 1 is then integrated with a 4.4ms fine time constant. When Q3 is off, CR1 is on, and the time constant is then given by R4+R7 and C1, When Q3 is saturated, CR1 is off and the time constant is given by R5+R7 and C1. Potentiometer R60 gives a control voltage (V_c) which is slightly positive when there is no audio input.

Transistors Q1 and Q2 operate as gates and let pass the control signal (V_c) either by the input + or by the input of multiplier 11. The multiplier output gives a balanced, square signal of amplitude $2V_c$ x multiplier gain. Its symmetry around zero is adjusted by potentiomer R130 (drift adjustement). The output is integrated by R15 and C2.

3.1.1.2. DEMODULATOR

The decoder is similar to the encoder, but there is no comparator. In addition, there is a smothing filter at the output. It is a low-pass filter with a 4kHz cut-off frequency and a minimum rolloff of 130dB/Oct. The pass band has a 3dB ripple or less and the stopband rejection is at 45dB or greater. The D.C. gain is ½.

3.1.1.3. DELTA CODEC CHARACTERISTICS

3.1.1.3.1. POWER SUPPLY

For one modulator-demodulator (codec)

Voltage	Current	Power
+15V	25mA	0.375mW
-15V	8mA	0.120mW
+ 5V	110mA	0.550mW
Total power: 1W		

Power Supplies: Harrison 5201B-Hewlett-Packard

3.1.1.3.2. CLOCKING RATE

The codec is optimized to operate from 16kbits/s to 38.4kbits/s. The clock controls a TTL circuit (levels 0,5V).

3.1.1.3.3 IMPEDANCE OF CODEC

Input Impedance: 2.2kΩ

Output impendance: 68Ω (R23 is a loading resistor). It is not used if the output is connected to an adapted line (680Ω).

3.1.1.4 ALIGNMENT

3.1.1.4.1 MODULATOR

The input being grounded, modulator R60 is adjusted for triangles of 40mV p-p at 19.2kbits/s and 20mV p-p at 38.4 kbits/s.

The input being a 800Hz test tone, the symmetry of the multiplier output is adjusted by potentiometer R130. The multiplier not being linear over the total dynamic range, the 800Hz test tone amplitude must be chosen at middle range (from low levels to saturation ≈-15db).

3.1.1.4.2 DEMODULATOR

The modulator input being grounded, demodulator R60 is adjusted for triangles of 20mV p-p at 19.2 and 38.4 kbits/s.

Demodulator R-130must be adjusted exactly as modulator R-130 (see 3.1.1.4.1).

3.1.1.5 COMPONENTS

The components required are described in detail in Appendix C.

3.2. CONVERTERS

3.2.1. STRUCTURE OF THE DDMC

The aim of the present work is to prove the feasibility of direct digital conversion between delta and PCM and it is only required to build a single channel system.

For a single channel converter, serial operations require less hardware than parallel ones. Therefore, the DDMC prototype will be implemented with a serial structure.

3.2.2. DESIGN

3.2.2.1. DIGITAL FILTERS

Digital filtering is the process of spectrum shaping using digital hardware. The aims of digital filtering are the same as those of continuous filtering but the processed signals are discrete instead of being continuous.

In a digital filter, the input and output signals are not represented by a continuous waveform but by samples. Usually the sample values are given by binary numbers. Once per sampling period, the filter receives a signal sample and produces by means of digital logic operations an output sample.

The output sample $y(nT)$ of a digital filter at time nT (sampling period T seconds) is computed from the input sample ($x(nT)$) and a linear combination of past inputs and outputs

$$y(nT) = \sum_{i=0}^{N} a_i x((n-i)T) - \sum_{i=1}^{M} b_i y((n-i)T) \qquad (3.1)$$

where the a_is and b_is are constant coefficients. Equation 3.1 is called a finite difference equation.

The logic circuit which implements the operations of Equation 3.1 is schematically represented in Figure 3.3.

The input sample $x(nT)$ is fed into a one period delay block. $x((n-1)T)$ is available at the output of this block. There are N such delay blocks connected in tandem which provide the values of $x((n-1)T)$, $x((n-2)T)$,..., $x((n-N)T)$. Each of these $x((n-i)T)$, $i=0$ to N, is multiplied by its weighting factor a_i. Similarly, M delay blocks provide the values of $y((n-i)T)$, $i=1$ to M, which are multiplied by the coefficients b_i. An adder gives the output value $y(nT)$ by computing the sum of all these terms.

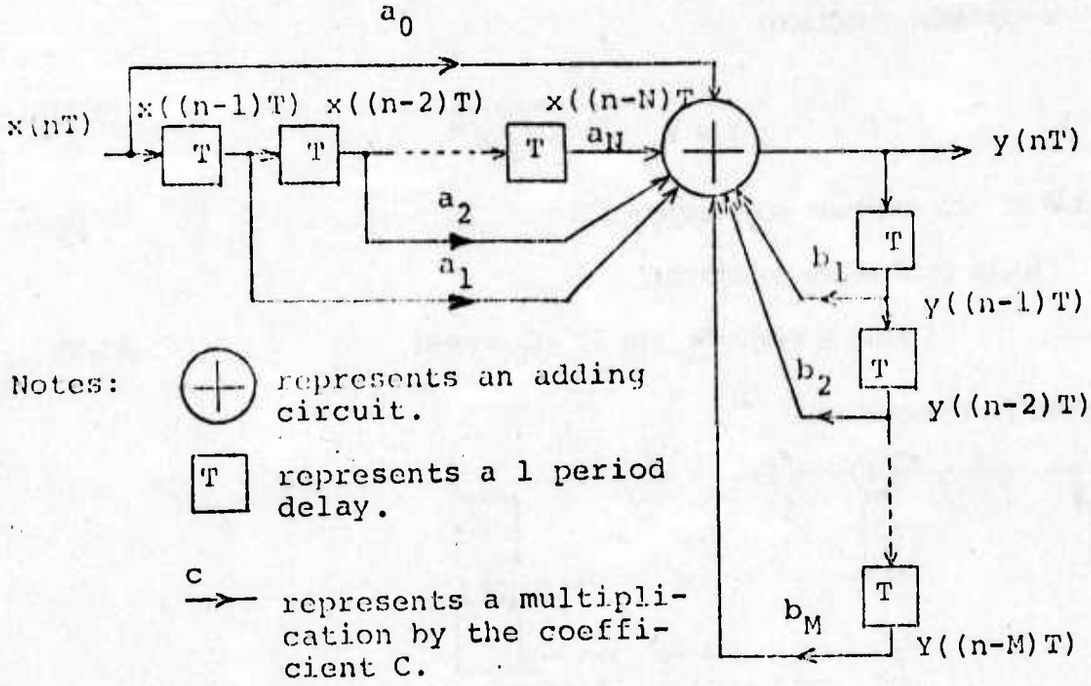


FIGURE 3.3.- Digital Filter

In the following, the filters that are used in the DDMC are described. For each filter, the z-transfer function, the finite difference equation and a block diagram representation are given. The finite difference equation is a particular case of the general equation 3.1 and the block diagram is a simplification of Figure 3.3 in which all the paths where the coefficients equal zero have been removed.

First-order low-pass filter

z-transfer function:

$$\frac{y(z)}{x(z)} = H(z) = \frac{1}{1+K_1 z^{-1}} \qquad (3.2)$$

where K_1 is a constant coefficient similar to the a_i's and b_i's.

Finite difference equation:

$$y(n) = x(n) - K_1\, y(n-1) \qquad (3.3)$$

Block diagram representation:

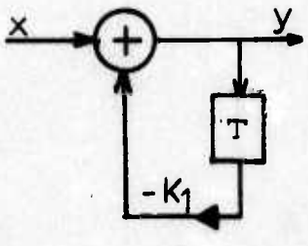


FIGURE 3.4.- 1st Order Digital Filter

Second-order low-pass filter

z-transfer function:

$$H(z) = \frac{1}{1 + K_1 z^{-1} + K_2 z^{-2}} \tag{3.4}$$

where K_1 and K_2 are constant coefficients.

Finite difference equation:

$$y(n) = x(n) - K_1 y(n-1) - K_2 y(n-2) \tag{3.5}$$

Block diagram representation:

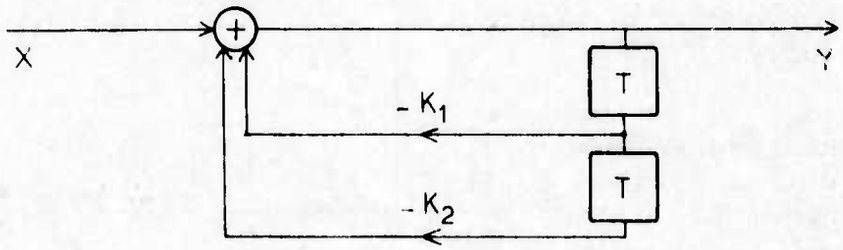


FIGURE 3.5.- 2nd-order digital filter.

Second-order filter with prediction

z-transfer function:

$$H(z) = \frac{1 + K_1 z^{-1}}{(1 + K_2 z^{-1})(1 + K_3 z^{-1})} \tag{3.6}$$

where K_1 and K_2 and K_3 are constant coefficients.

Finite difference equation:

$$y(n) = x(n) + K_1 x(n-1) - (K_2 + K_3) y(n-1) - K_2 K_3 y(n-2) \tag{3.7}$$

Bloc diagram representation:

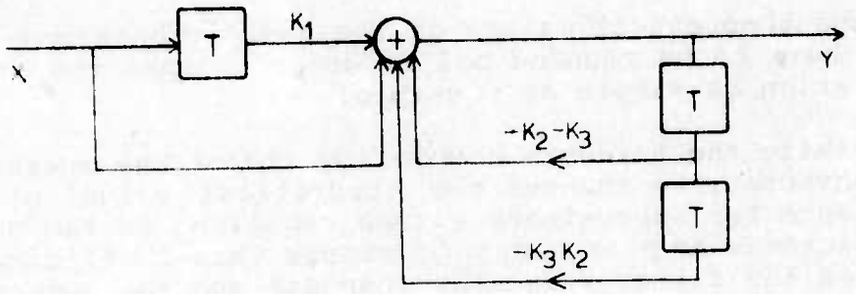


FIGURE 3.6.- 1-zero, 2-pole digital filter.

Two-pole & Two-zero filter

z-transfer function:

$$H(z) = \frac{1 + K_1 z^{-1} + K_2 z^{-2}}{1 + K_3 z^{-1} + K_4 z^{-2}} \qquad (3.8)$$

where K_1, K_2, K_3 and K_4 are constant coefficients.

Finite difference equation:

$$z(n) = x(n) + K_1 x(n-1) + K_2 x(n-2) - K_3 y(n-1) - K_4 y(n-2) \qquad (3.9)$$

Block diagram representation:

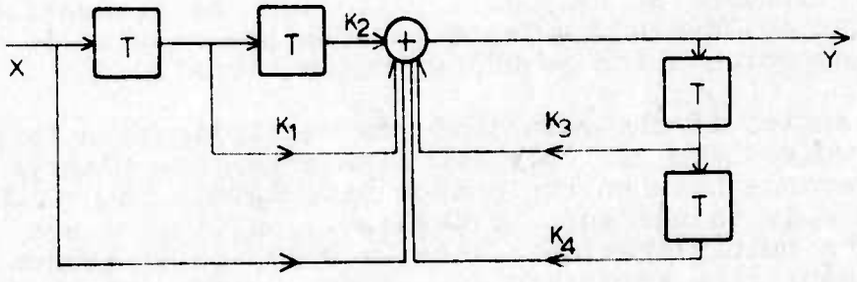


FIGURE 3.7.- 2-pole,2-zero digital filter.

3.2.2.2. FILTER COEFFICIENT ROUNDING.

Once the theoretical values of the coefficients have been computed, they have to be rounded off in order to make the practical implementation as simple as possible.

To minimize the hardware complexity and/or the operating times in the converter, we changed the theoretical values of the filter coefficients for approximate values requiring as few additions and subtractions as possible. Of course this coefficient rounding modifies the filter frequency response and the amount of simplification was limited by the desired filter performance. It must be noted that the filter characteristic is more sensitive to coefficient rounding when the sampling frequency is high. For this reason, coefficients are generally simpler at 19.2kHz than at 32 or 38.4kHz.

3.2.2.3. SELECTION OF SUITABLE WORD LENGTH

The system was, as described in Section 2.2, simulated on a general purpose computer. Samples were represented by floating-point binary words with all the precision of the computer.

Floating-point arithmetic is difficult to implement with serial circuits and thus, fixed-point operations are made in the DDMC. The word length must be as short as possible to keep the amount of hardware minimal. Limiting the number of bits per word introduces noise in the filters and we must determine the smallest word length which does not noticeably degrade the system performances.

In general, the results of the multiplication of a sample by a filter coefficient needs an infinite number of bits to be exactly represented. Of course, the result must be truncated and thus noise is introduced at each multiplication. As truncation limits the number of levels available to code the result, it is really quantizing noise which is added to the signal.

For example, if the result of the multiplication is represented by a word which has only two bits after the binary point, the difference between two consecutive levels is $\frac{1}{4} = 0.25$ This means that only values such as 0.25, 0.5, 0.75 are available. If the multiplication result is 0.62, it is truncated down to 0.50 (quantizing error = 0.62 - 0.50 = 0.12). The difference between two consecutive levels is the quantization step.

Let us assume that there are M filters in tandem in the DDMC. Each filter requires one or more multiplications. In a given filter (filter number i; i=1,..M) the multiplication results are truncated with a quantizing step S_i.

It is possible to evaluate approximately the noise contribution of the truncations if we assume that the quantizing error is uniformly distributed and that noise samples are uncorrelated. The total truncation noise power (P_T) of a converter as a function of the quantization steps is found to be:

$$P_T = C_1 S_1^2 + C_2 S_2^2 + \ldots C_M S_M^2 \qquad (4.1)$$

where C_1, C_2,... C_M are numerical coefficients, and S_1, S_2,... S_M are the quantization steps of the M filters.

To be practically unnoticeable, it is assumed that the truncating noise (P_T) must be 6db below the system noise as computed without truncation in Section 2.2. It was also decided that the contribution of all filter noises should be equal

i.e. $C_1 S_1^2 = C_2 S_2^2 = \ldots C_M S_M^2 = P_T/M$.

Thus, we were able to compute approximate values for S_1, $S_2 \ldots S_M$ and to determine how many bits were necessary after the binary point. For instance, if we compute:

$S_i = \sqrt{\frac{P_T}{Mc_i}} = 0.34$, we need two bits after the binary point to represent results of multiplications in the ith filter. This gives:

$$S_i = 2^{-2} = 0.25 < 0.34$$

As several assumptions had been made to obtain these values, simulations, where all the truncations were made, were run to check the results. In some cases, the number of bits had to be modified but theoretical and simulated values were very close.

The maximum values of the samples were also computed to determine the number of bits on the left of the binary point. This was straightforward as the gains and the input signals of the filters were known.

Figures 3.8 to 3.17 give the complete schematics of the CVSD DDMC's (explained in Sections 2.2.2) at 16, 19.2 32 and 38.4kHz sampling rates. Word lengths are indicated for each filter by numbers in brackets. The following conventions are used:

(a,b.c)

a : indicates if a sign bit is needed (it is not needed for the syllabic filter which is always positive).
a = 1 requests a sign bit
a = 0 means that a sign bit is not necessary.

b : indicates the number of bits on the left side of the binary point.

c : indicates the number of bits on the right side of the binary point.
c can be negative. This means that there is no bit on the right side of the binary point and that the truncation is made on the left side up to the bit of weight $2^{-|c|}$.

EXAMPLES:

(1,4.2) indicates a word which is either positive or negative, whose maximum value is:

$$2^3 + 2^2 + 2^1 + 2^0 + 2^{-1} + 2^{-2} = 15.75$$

and whose smallest non-zero value is:

$$2^{-2} = 0.25.$$

Total number of bits: 1 + 4 + 2 = 7

(0,5.3): always positive; maximum value:

$$2^4 + 2^3 + 2^2 + 2^1 + 2^0 + 2^{-1} + 2^{-2} + 2^{-3} = 31.875$$

minimum value:

$$2^{-3} = 0.125$$

Total number of bits: 0 + 5 + 3 = 8

(1,7,-3): positive or negative; maximum value:

$$2^6 + 2^5 + 2^4 = 102$$

minimum value:

$$2^4 = 16$$

Total number of bits: 1 + 7 - 3 = 5

S/N ratios obtained with truncation paramaters were given in Section 2.2.2.

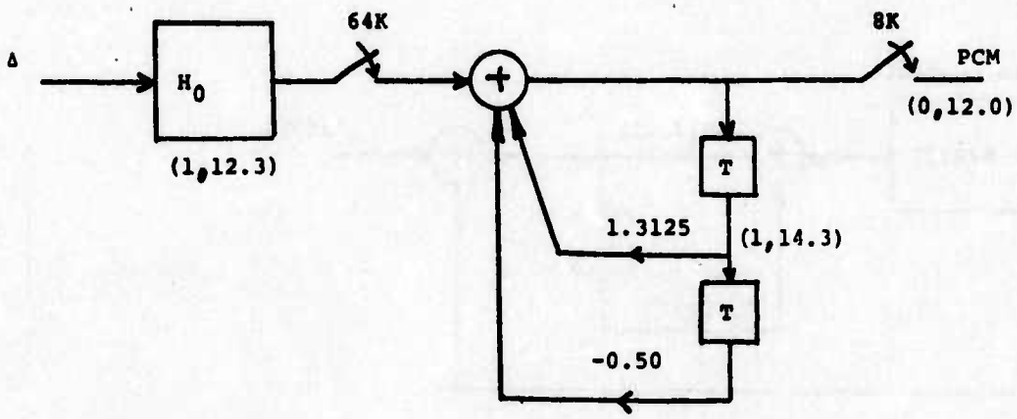


FIGURE 3.8.- Δ frequency to PCM frequency conversion circuit.

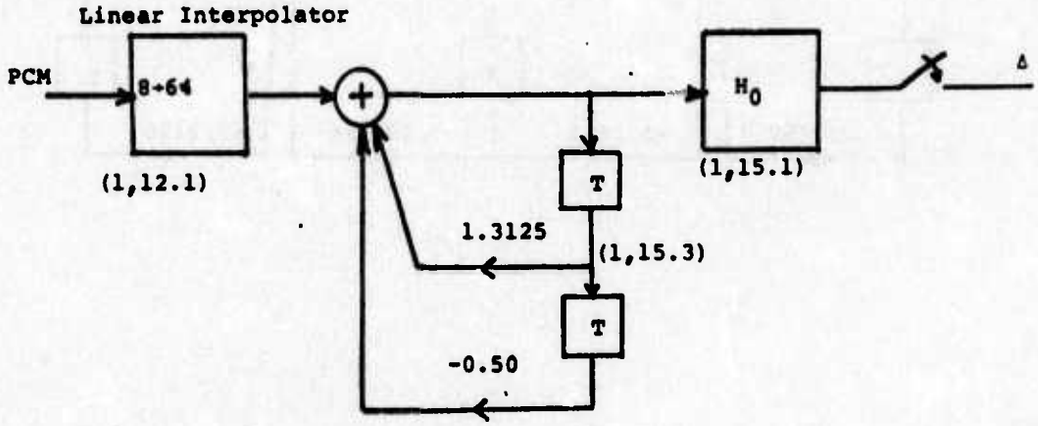


FIGURE 3.9.- PCM frequency to Δ frequency conversion circuit.

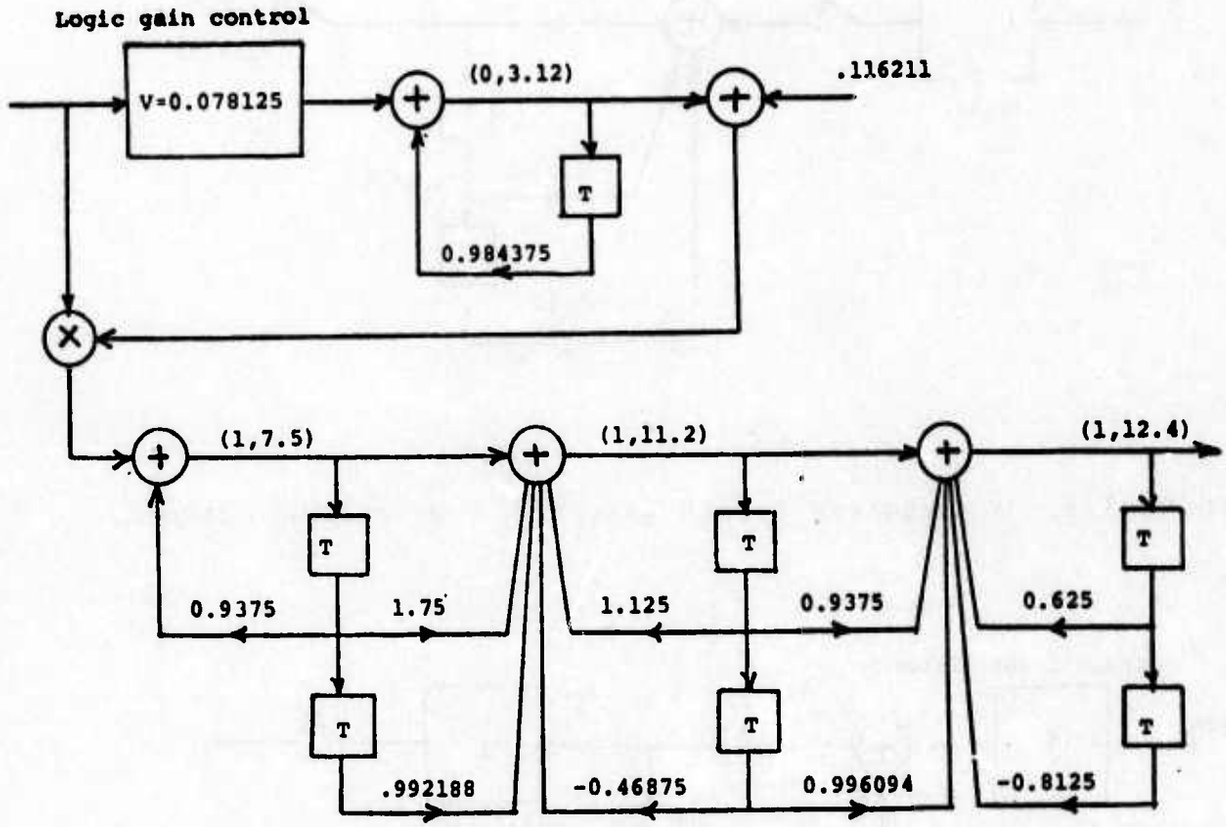


FIGURE 3.10.- Δ→PCM 16K.

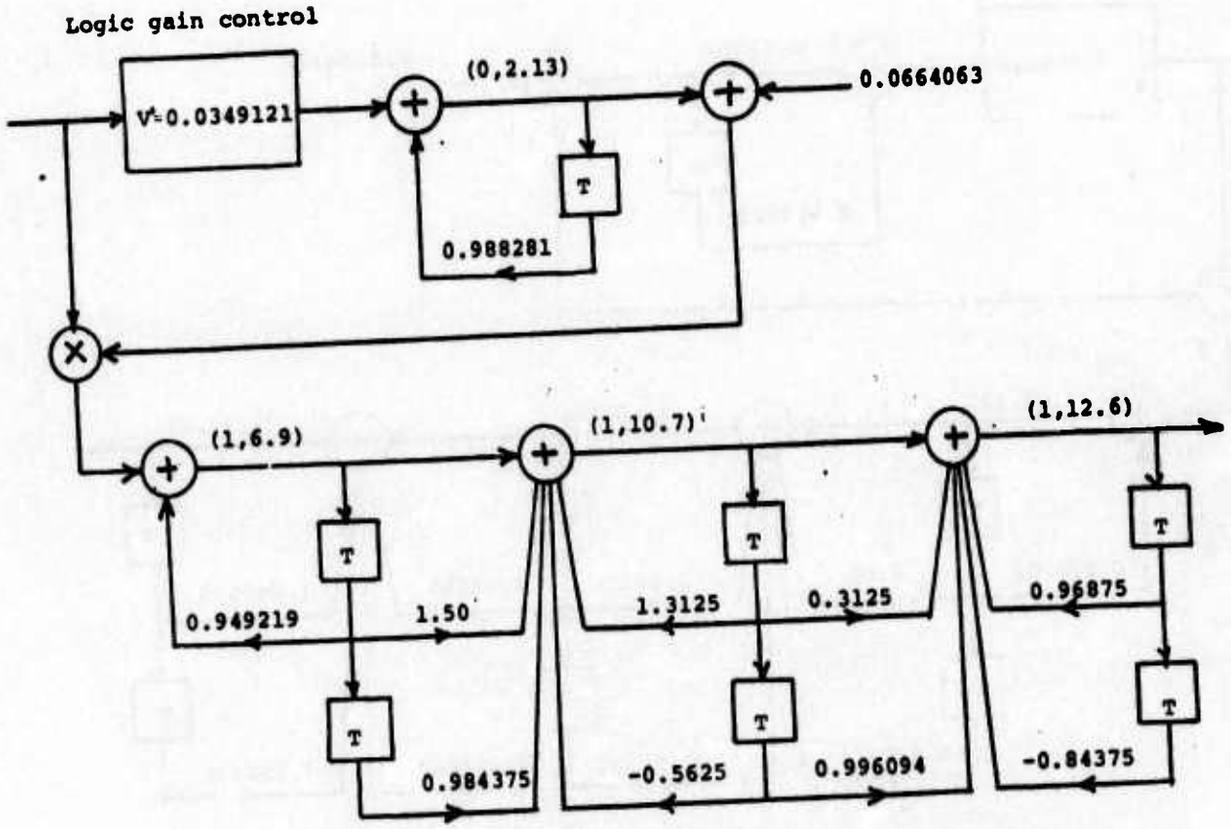


FIGURE 3.11.- 19.2kHz Δ-PCM.

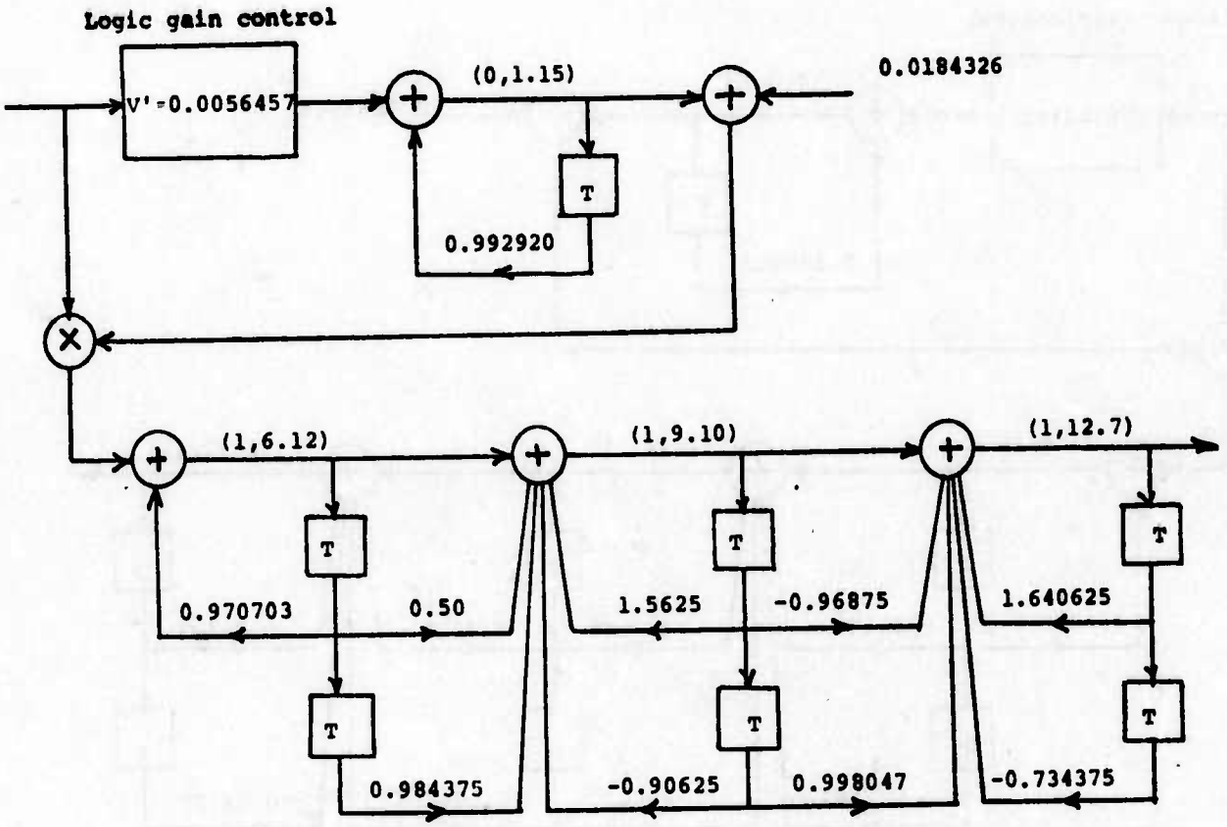


FIGURE 3.12.- 32K Δ→PCM.

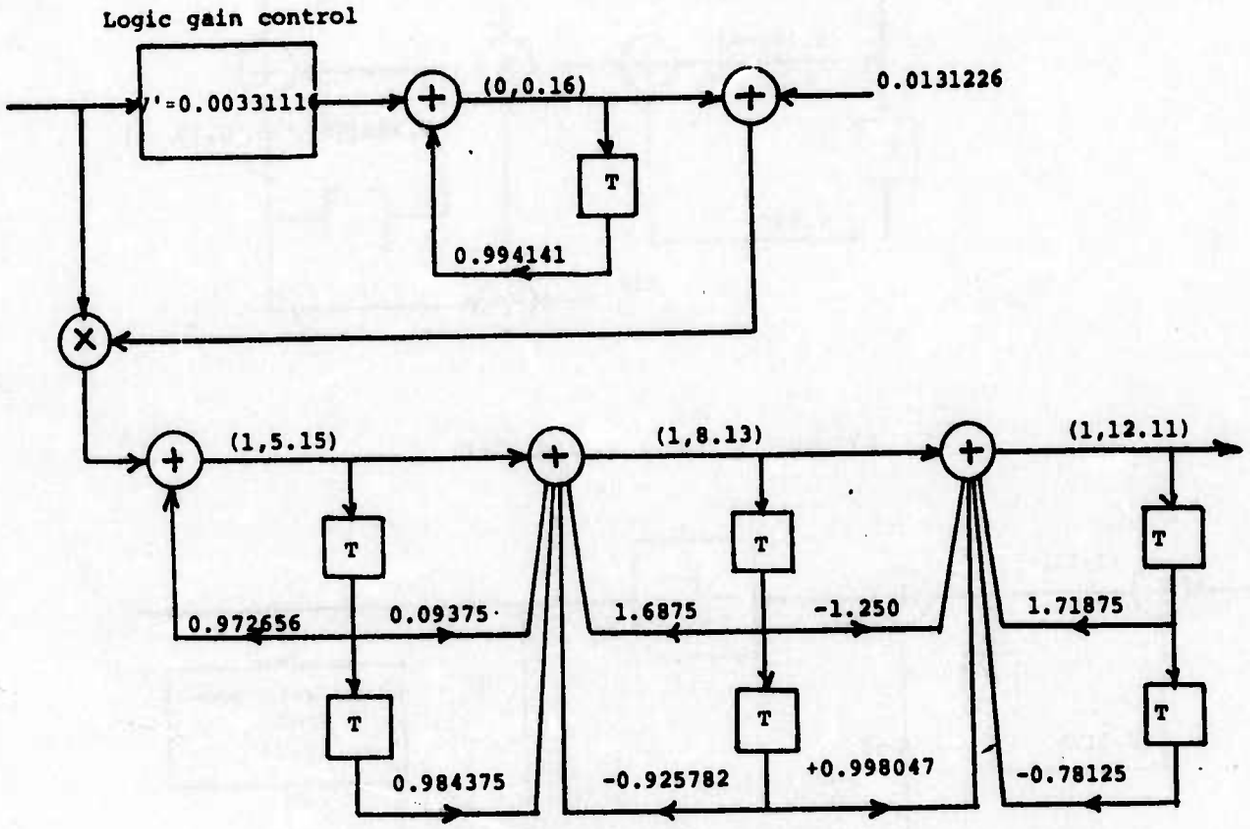


FIGURE 3.13.- 38.4K Δ→PCM.

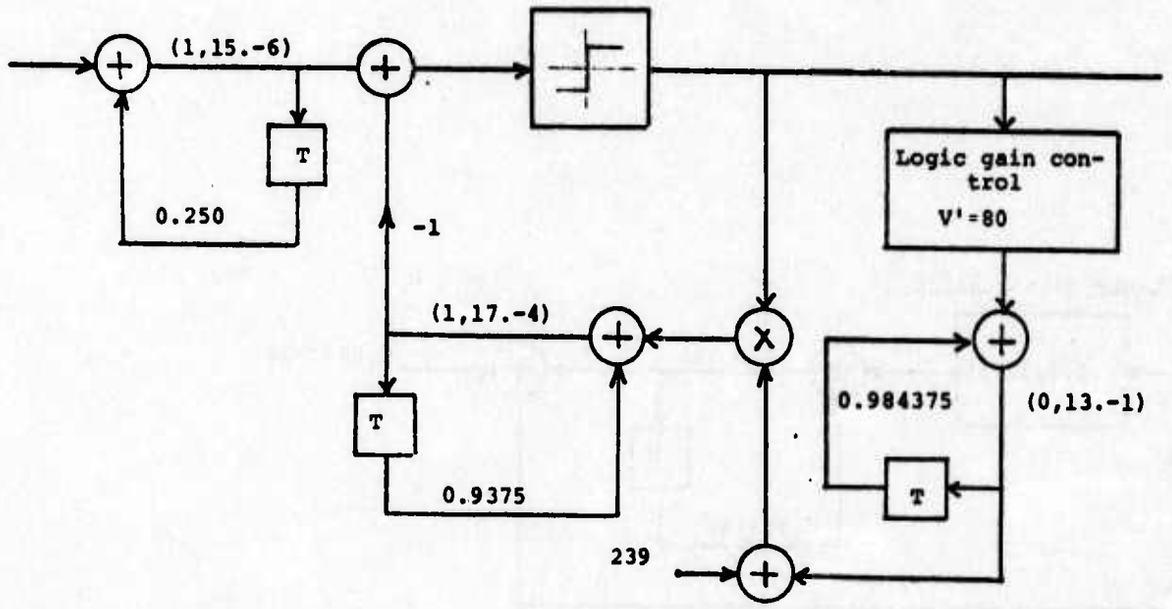


FIGURE 3.14.- PCM→Δ 16K

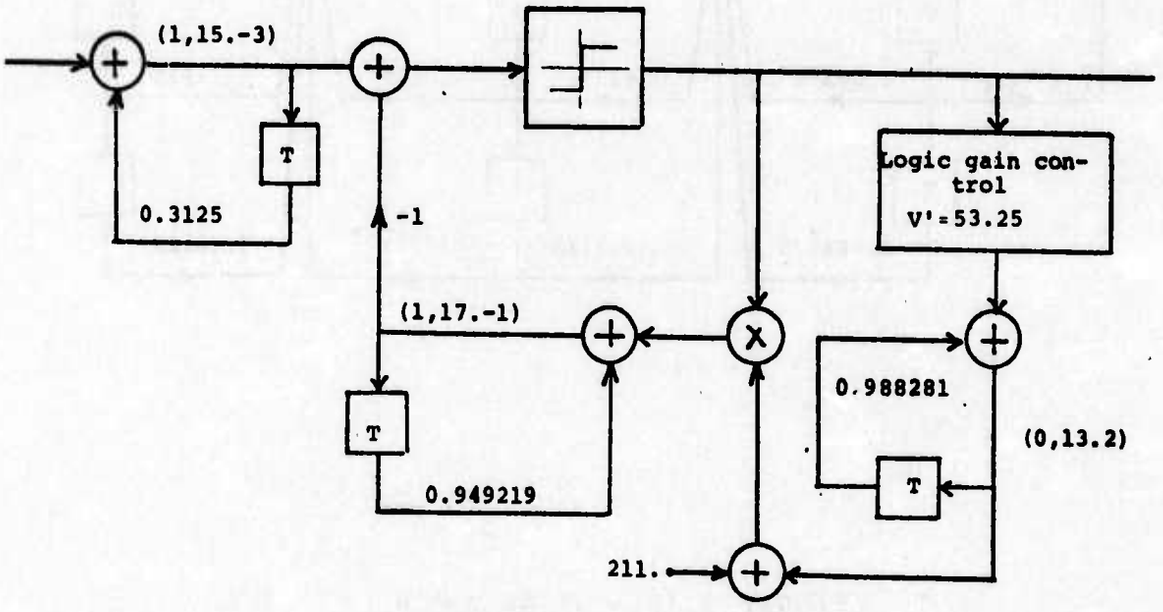


FIGURE 3.15.- 19.2kHz PCM→Δ

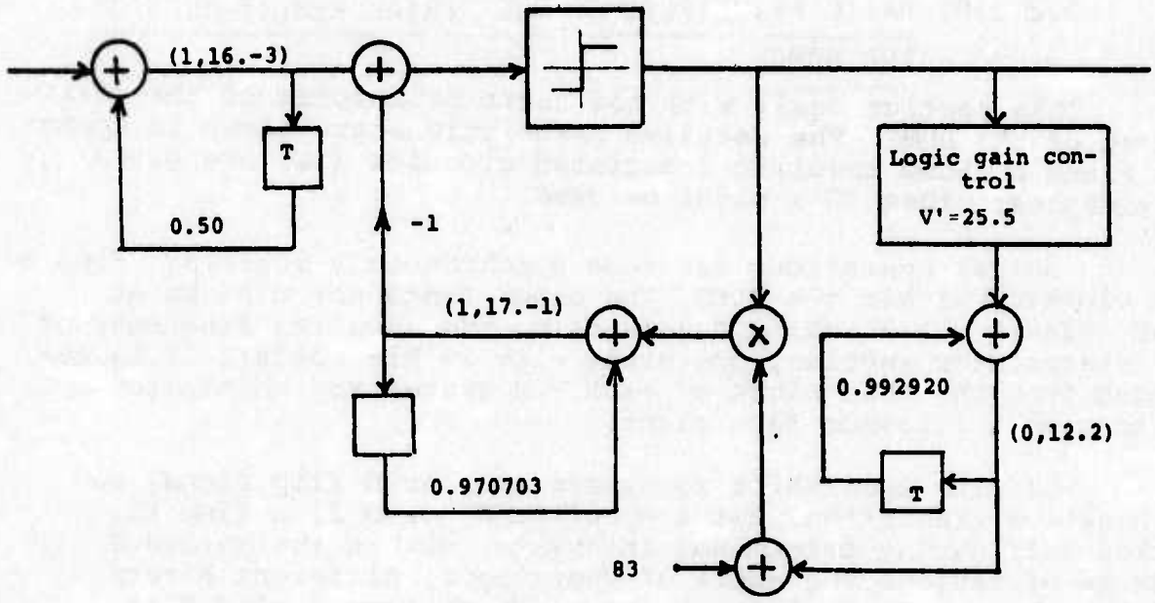


FIGURE 3.16.-PCM→Δ 32K

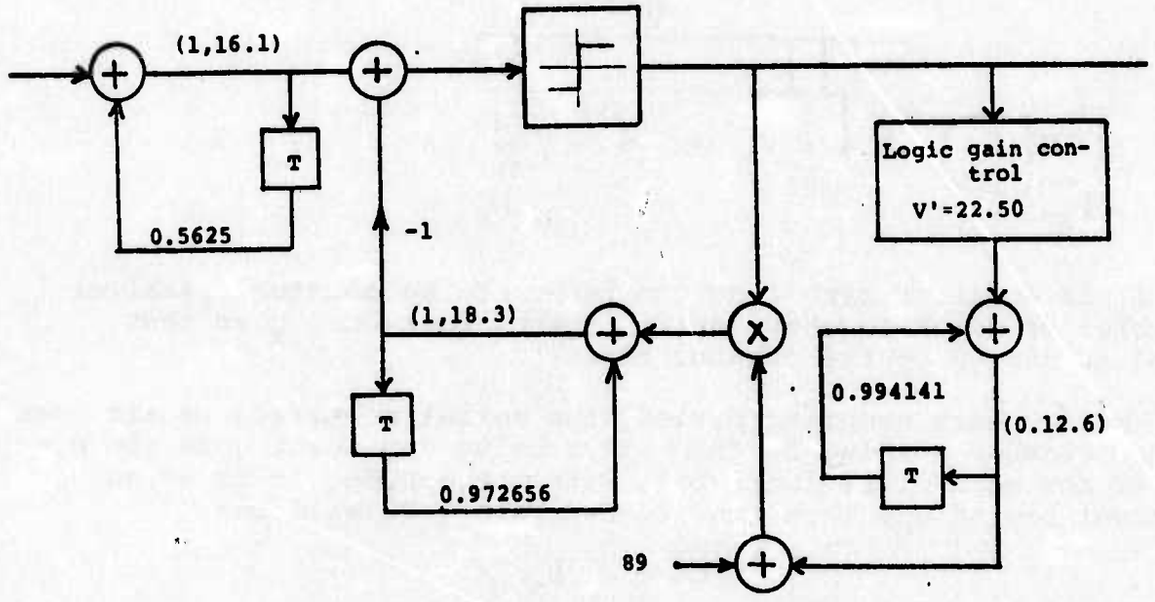


FIGURE 3.17.- PCM→Δ 38.4K

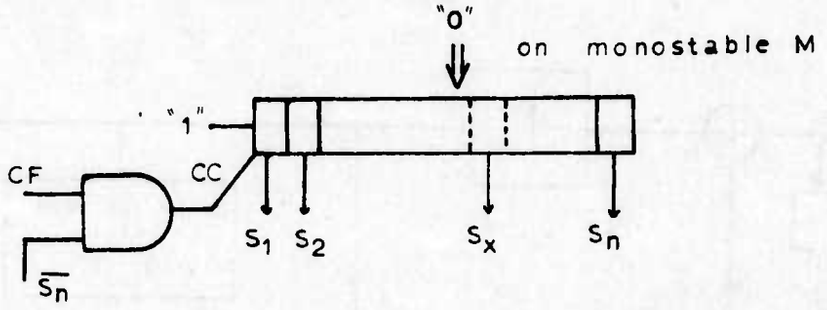
3.2.2.4. BASIC PRINCIPLES OF THE SERIAL REALIZATION OF THE DDMC

This section deals with the basic principles of the realization of the DDMC. The detailed descriptions are given in Appendix A and B. Some specific integrated circuits (IC) are given as examples; other IC's might be used.

Serial operations are made synchronously starting from a fast clock (CF) within the DDMC. The clock frequency must be at least .064x19 = 1.216MHz (.064MHz being the sampling frequency of the interpolator section, operating with 19 bit words). CF is generated from the 8kHz clock of each PCM system and multiplied by 192 to give a 1.536MHz fast clock.

CF acts upon shift registers (SR) or D flip flops, on the negative transition. But a specific SR or D flip flop is clocked only during determined intervals, within the period T (because of various sequences of operations, different binary word lengths..). So an information on chronology during T is needed. This will be performed by counting the transitions by means of a binary counter.

The binary counters used in the DDMC are made of shift registers: each transition of the shift register clock (CC) shifts a logical one through the register.



So, S_x is equal to zero from the reset of the counter (parallel transfer of zero) to the x shift of the clock CC. S_x is then equal to one up to the counter reset.

During each sampling period, the serial computations are over when S reaches a value S_n this value being dependent upon the order of the most significant bit, within the DDMC. It is of no use to count beyond S_n. Then, the counter clock CC will be:

$$CC = CF\ \overline{S}_n.$$

As desired, this stops the counting. At the beginning of the next sampling period, forcing each S to 0 will make the counter run again. Such a reset of the counter is performed by a monostable M, triggered at the beginning of each sampling period.

A phase diagram of the events between Z sampling times (given by the negative transition of monstable M) is shown in Figure 3.18.

M and CF are independent signals. Successive values of S_x determine whether or not CF must be sent on a specific SR or D^x flip flop. In order to prevent critical races, the clock input on SR and D flip flop is always inhibited by S_1. Thus a transition on CF cannot shift any register without being counted (S_1 is tne result of the first transition of CF on the counter).

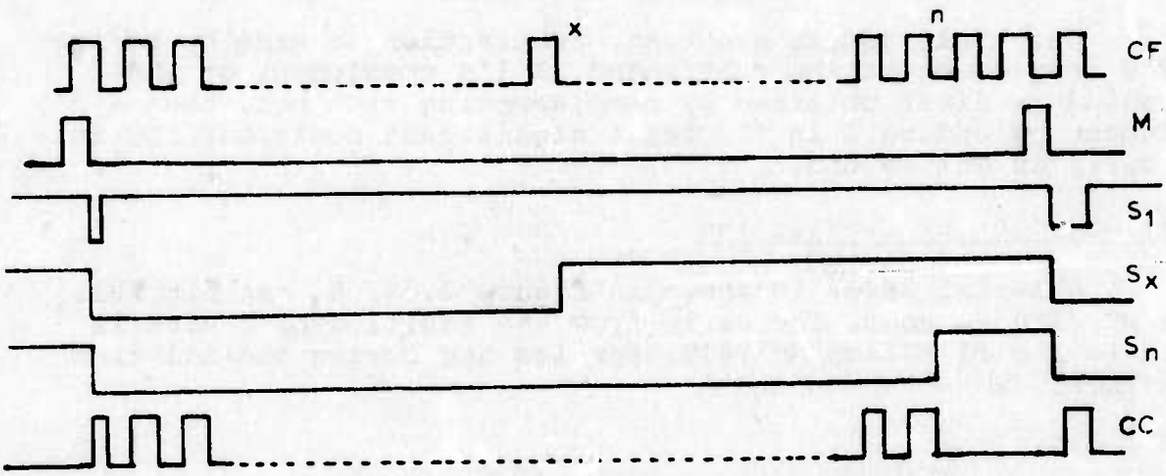


FIGURE 3.18.- Timing conditions

These are the timing conditions during the basic operations which are:

-right shift of parallel storage in a shift register.

-parallel or serial, addition or subtraction.

-multiplication of a binary word by a constant.

-conversion from Δ to PCM sampling frequencies (or vice versa).

3.2.2.4.1 SHIFT - REGISTER (SR)

They are of the MC 7495 type. They come in four position chips, and several of them are connected in series,so as to get the desired number of positions. When the number of positions is one more than a multiple of 4, a clocked J-K flip-flop can be used for the additional positions.

MC 7495 performs parallel in / parallel out, right and left shift depending upon the logic level present at the mode control input MC. In fact only right shifts and parallel in will be performed.

Serial transfer (shift) is made on the negative transition of a clock CS while MC=0; parallel in is related to a clock CP and MC=1.

3.2.2.4.2. ADDITION AND SUBTRACTION

Only full adders are used. Subtraction is made by adding the 2's complement of the subtrahend. A 1's complement of the subtrahend is first obtained by complementing each bit, then a 2's complement by adding 1 in the least significant position: the initial carry is set to one.

Serial addition or subtraction

A serial adder is shown in Figure 3.19. A one bit full adder MC 7480 is used. The carry from the addition of 2 bits is stored in a D flip-flop MC 7479, for its use during the addition of the next higher order bits.

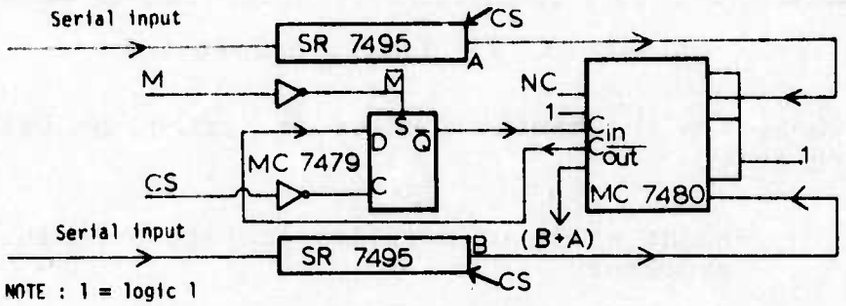


FIGURE 3.19.- Serial adder (A+B)

The initial value of the carry is set to 0, by the same monostable M that resets the binary counter. Thus, the carry is set prior to the shift of bits. A serial subtractor is shown in Figure 3.20.

Complementation of the bits of the subtrahend is done by using the inverting input of the full adder. Monostable M sets the initial carry at one.

As a conclusion, serial adders or subtractors are composed of one full adder MC 7480, one D flip-flop and 2 inverters (that can be shared with other adders or subtractors). In the following they will be called Full Adder (FA), and symbolized as in Figure 3.21.

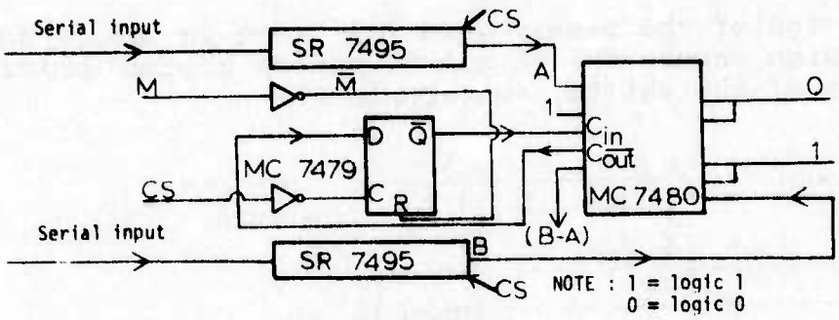


FIGURE 3.20.- Serial subtractor (B-A)

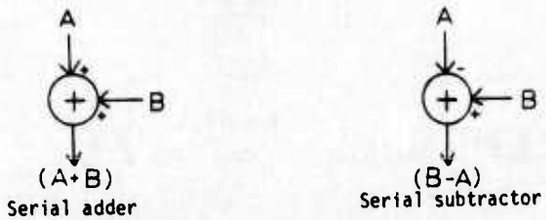


FIGURE 3.21.- Symbols

Carry must be stored whenever at least one bit changes at the input of the FA. So the clock on the D flip-flop must be the union of both serial clocks of the 2 SR containing the terms of the addition.

3.2.2.4.3. MULTIPLICATION OF A BINARY WORD X BY A CONSTANT.

This operation is found in all digital filters. The problem of multiplication by a constant is a problem of multiplication by powers of 2 (shifts) and additions.

If so, only right shifts are performed, since all coefficients are of the form 2^{-n}, with $n \geq 0$. For a right shift, the least significant bits are ignored, whereas the sign bit is entered at the left of the binary word.

The multiplication by 2^{-n} can be performed while shifting the binary word through its SR. The output of the n^{th} position of the SR is used (least significant bit position being numbered 0^{th}). If p is the length of the binary word, the sign bit must be sent after the $(p-n)^{th}$ shift.

The three NAND gates in Figure 3.22 perform the previous operations and deliver, in series, an output y=x/8.

The sign of the binary word x is kept in memory during the shifts (sign memory SM) in a D flip-flop clocked prior to the beginning of the shifts (monostable M).

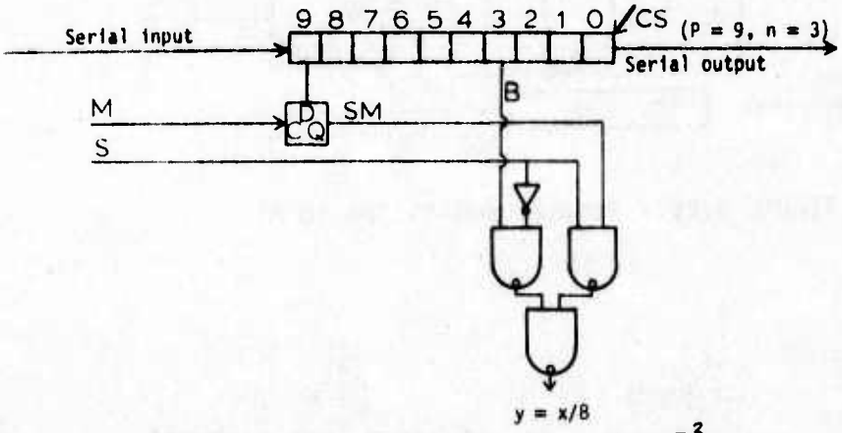


FIGURE 3.22.- Multiplication by 2^{-3}

The value of y is then added algebraically to other values of $(x)(2^{-n})$ in order to perform the multiplication by a constant. This is done with 2-input serial adders or subtractors (FA), connected in such a way as to minimize the delay of propagation of partial results, and to avoid overflow on partial results.

3.2.2.4.4. CONVERSION FROM Δ TO PCM SAMPLING FREQUENCIES (OR VICE VERSA)

The Δ and PCM clocks not being synchronous, a buffer register (B) is to be introduced between the Δ and the PCM shift register (Figure 3.23). The Δ sample is found in the SR1 register, after computation during a time smaller than the sampling period. The Δ sample is entered in parallel in the buffer B (write order with clock CW). The output of this buffer is sent, also in parallel, in the input register SR0 of the PCM section (Read order with clock CR). The write and read orders are found during conversion from PCM to Δ.

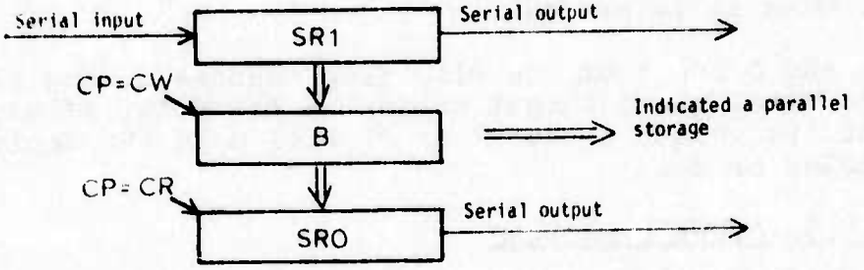


FIGURE 3.23.- *Introduction of the buffer B when shifting from one sampling frequency to another*

The READ order must not follow the WRITE order by less than T_p+T_s where T_p is the maximum propagation delay time of the buffer and T_s the set-up time in SRO (the hold time is zero in the worst case). If this condition is not respected, the binary word might be altered during the frequency conversion.

A solution to this problem is to delay the READ order by maintaining CR high if it was so on the negative transition of CW.

The circuit in Figure 3.24 generates the clocks CW and CR, departing from CRA and CWA, which will be the sampling clocks (either FΔ or CPCM). The two delay blocks are needed to compensate for delay propagation times in the shift registers and D flip-flop, and critical races.

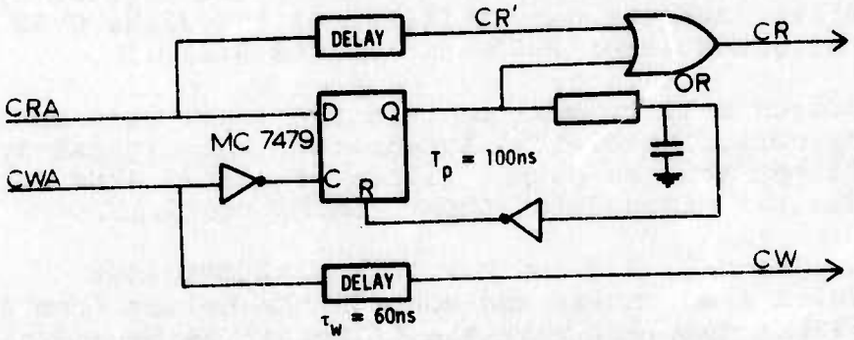


FIGURE 3.24.- *Generator of CR and CW for a frequency conversion*

A D flip flop MC 7479 makes the decision whether to delay or not, by generating a pulse T_p at the Q output if CRA=1 on the negative transition of CWA. This pulse is added to CR' with an OR gate; so the negative transition of CR is delayed with respect to CR', when it is needed.

If the D input of the flip flop changes during the set-up or holding time, the Q output cannot be predicted after clocking. But its value, either 1 or 0, will make the decision whether to delay or not.

3.2.2.5. OVERALL PICTURE

The DDMC converts CVSD delta signals at 16, 19.2, 32 and 38.4kbps into one channel of the D.1, TD968, TD660 and A law PCM channel bank multiplexers and vice versa.

3.2.2.5.1. Δ→PCM DDMC

The delta to PCM part of the DDMC prototype is built with 21 boards as represented in Figure 3.25.

-Board B-22 is the CVSD coder-decoder.

-Boards B-10 to B-12 contain the logic gain control circuit, the digital integrator, the digital syllabic filter and the output filter of the 16kHz digital demodulator shown in Figure 3.10.

-Boards B-13 to 15 contain the logic gain control circuit, the digital integrator, the digital syllabic filter and the output filter of the 19.2kHz CVSD digital demodulator shown in Figure 3.11.

-Boards B-16 to B-18 contain the logic gain control circuit, the digital integrator, the digital syllabic filter and the output filter of the 32kHz CVSD digital demodulator shown in Figure 3.12.

-Boards B-19 to B-21 contain the logic gain control circuit, the digital integrator, the digital syllabic filter and the output filter of the 38.4kHz CVSD digital demodulator shown in Figure 3.13.

-Boards B-7, B-8 and B-9 work with the four delta frequencies and contain the holder from Δ to 64 kHz sampling rate,the filter at 64kHz and the delta timing circuit shown in Figure 3.8.

-Board B-5 contains the digital PCM compressor for the four PCM systems.

-Boards B-1, B-3 and B-4 are the interface boards.

3.2.2.5.2. PCM→Δ DDMC

The PCM to delta part of the DDMC prototype is composed of 14 boards as represented in Figure 3.26.

-Boards T-1, T-3 and T4 are the interface boards. The first one contains the analog circuit, the clock rating, the pulse shaping and the phase-lock loop. The second one has the channel words and counters to extract the channel information to be converted. The last one contains the framing detector.

-Board T-5 (non existant) would have contained the interface between the A-law multiplexer and the DDMC.

-Board T-6 contains the four expanding laws.

-Boards T-7, T-8 and T-9 work with the four different delta frequencies and contain:

- -the sign adjustment (T-7),
- -the liner interpolator from 8 to 65kHz (T-8)
- -the delta timing filter
- -the low-pass filter from 64kHz to the delta sampling rate (Figure 3.9).

-Board T-10 contains the 16kHz digital modulator CVSD circuit shown in Figure 3.14.

-Boards T-11 and T-12 contain the 19.2kHz digital modulator CVSD circuit as shown in Figure 3.15.

-Boards T-13 and T-14 contain the 32kHz digital modulator CVSD circuit as shown in Figure 3.16.

-Boards T-15 and T-16 contain the 38.4kHz digital modulator CVSD circuit as shown in Figure 3.17.

The detailed circuit descriptions and drawings of each of the previously mentioned boards are presented in Appendices A and B.

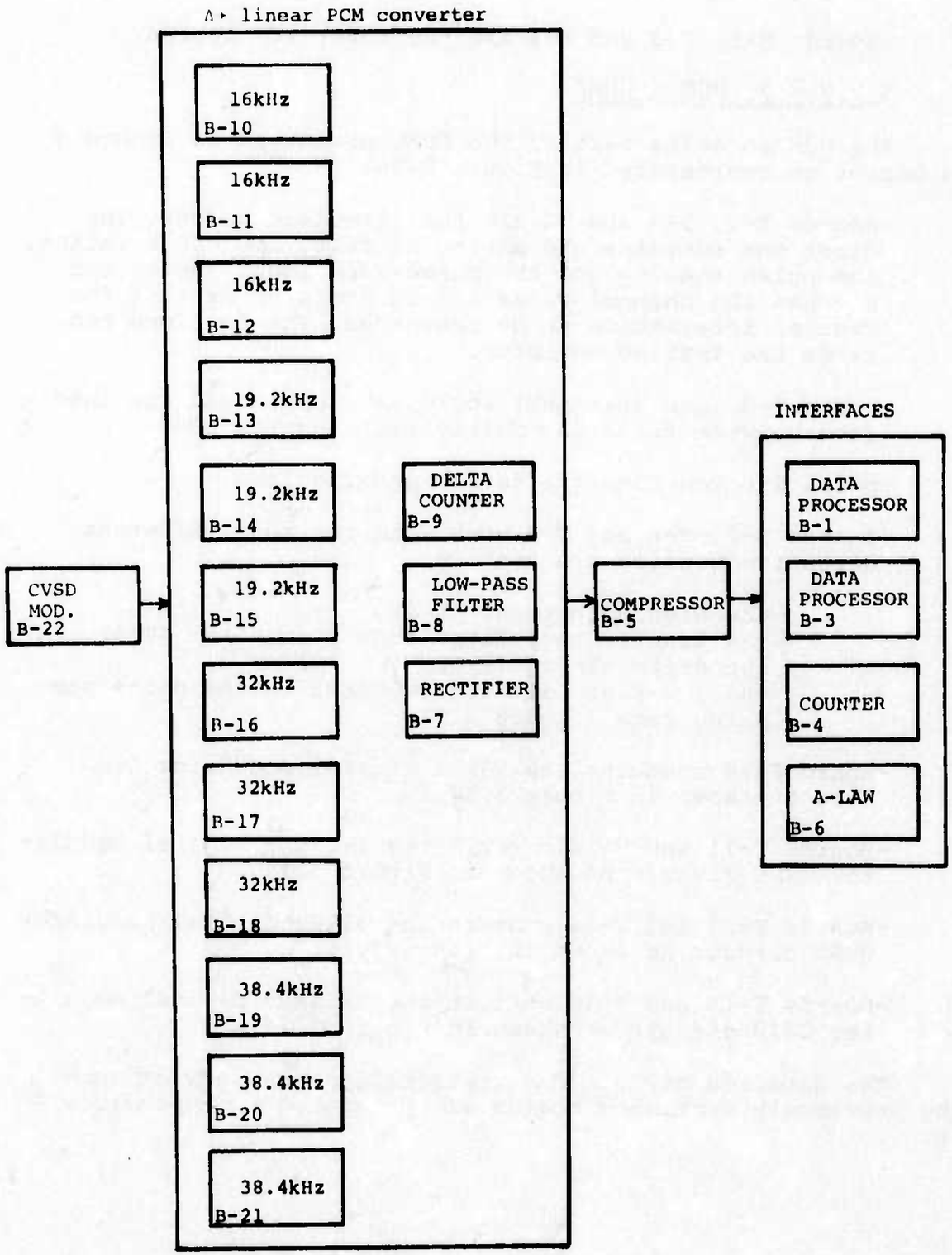


FIGURE 3.25.- Δ→ PCM DDMC.

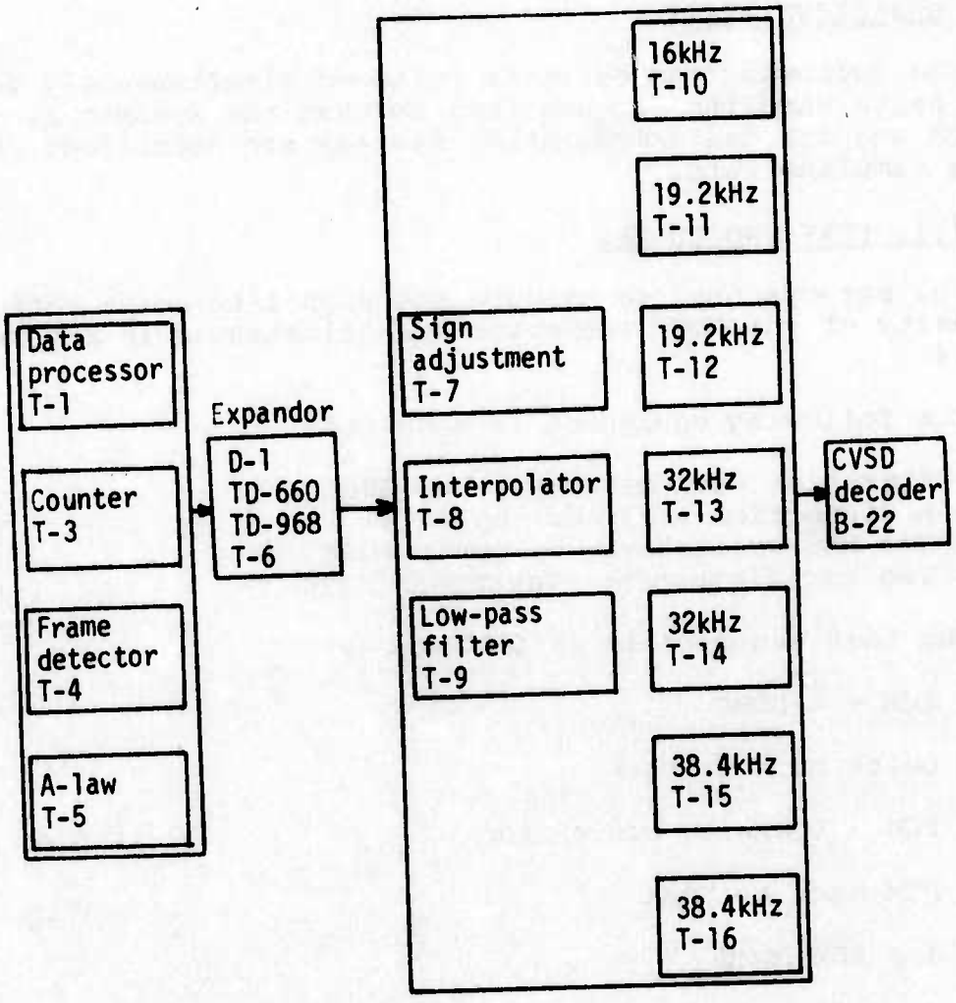


FIGURE 3.26.- PCM→Δ DDMC

4. TESTS

In the following section the objective and subjective test results obtained with the DDMC prototype are presented.

4.1. OBJECTIVE TESTS

The following procedure is followed simultaneously for the four delta sampling frequencies, so that the dynamic range of the PCM and the delta modulation systems are coincident for any delta sampling rate.

4.1.1. TEST PROCEDURES

The set-ups used to measure the signal-to-noise ratio and linearity of the DDMC converter are illustrated in Figures 4.1 to 4.4.

The following equipment is required:

- A precise wave generator: hp 200CD.
- A distortion analyser: hp332 A
- Two RMS voltmeters: hp model 403B
- Two oscilloscopes: Tektronix 543B

The test sequence is as follows:

-1 PCM → Δ DDMC

-2 Delta back to back

-3 PCM → Δ analog conversion

-4 PCM back to back

-5 Δ → PCM DDMC

-6 Δ → PCM analog conversion.

4.1.1.1. PCM → Δ DDMC SET-UP

Figure 4.1 illustrates the PCM → Δ DDMC measurement set-up.

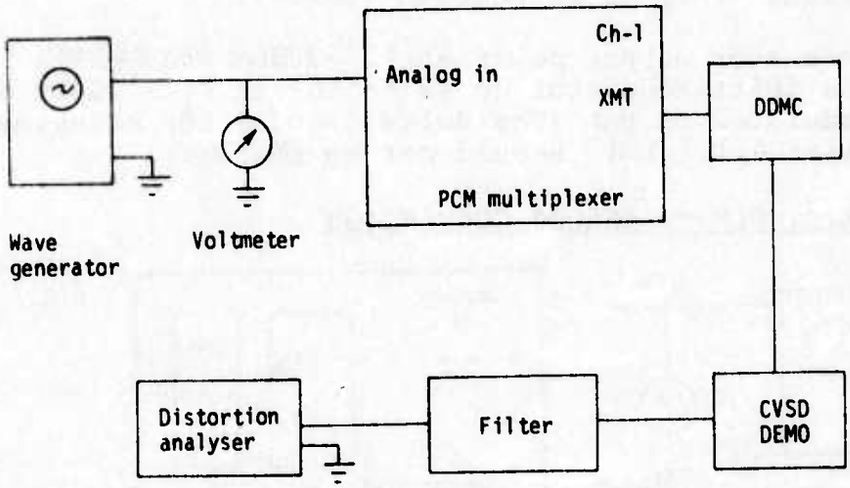


FIGURE 4.1.- CVSD - DEMOD conversion measurement set-up

A. Adjust the wave generator output power (Pin) to -5dbm with a 800Hz test tone and measure P_1.

B. With the PCM input power (Pin) at -35dbm, adjust the demodulator syllabic filter potentiometer so that the output is at P_1 -30dbm.

4.1.1.2. DELTA CODEC MEASUREMENT SET-UP

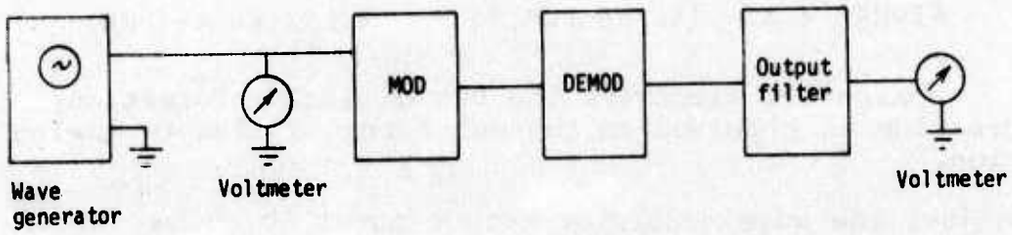


FIGURE 4.2.- Δ codec adjustment set-up

A. Adjust the wave generator output P_3 (Figure 4.2) so as to obtain the same value of P_1 as in Section 4.1.1.1.

B. Put the generator output power at P_3 -30dbm and adjust the gain of the delta modulator so as to obtain P_1 - 30dbm at the delta demodulator output (The delta demodulator adjustment made in Section 4.1.1.1.B should not be changed).

4.1.1.3. PCM →Δ ANALOG CONVERSION

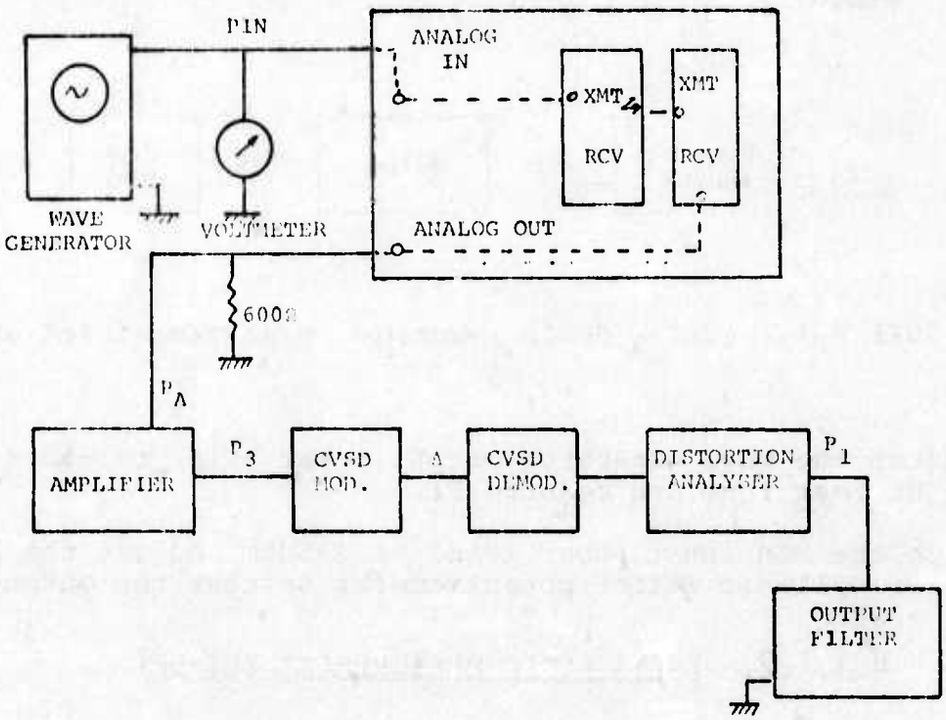


FIGURE 4.3.- Analog PCM to Δ conversion set-up.

Channel 1 transmits the PCM digital information; this information is received on channel 5 for digital to analog conversion.

A. Adjust the wave generator output power to -5dbm.

B. Adjust the amplifier gain so that the output reconstituted waveform is at P_1

C. Measure the powers P_A and P_3

4.1.1.4. Δ→ PCM DDMC CONVERSION

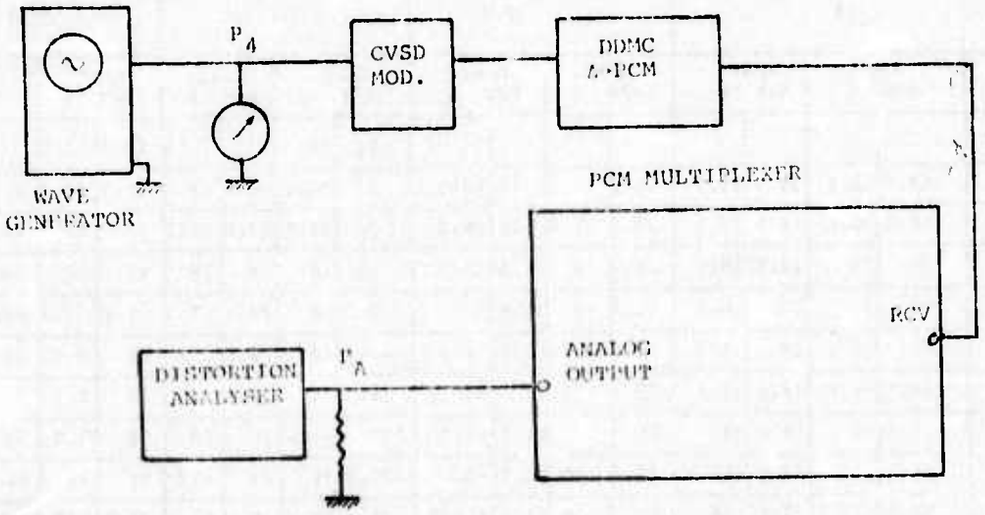


FIGURE 4.4.- Δ→ PCM DDMC conversion set-up.

A. Adjust the wave generator output to P_4 (P_4 is approximately equal to P_3).

B. Adjust the wave generator output to P_4 -30dbm. The analog PCM output should read P_4 -30dbm.

4.1.1.5 Δ→ PCM ANALOG CONVERSION

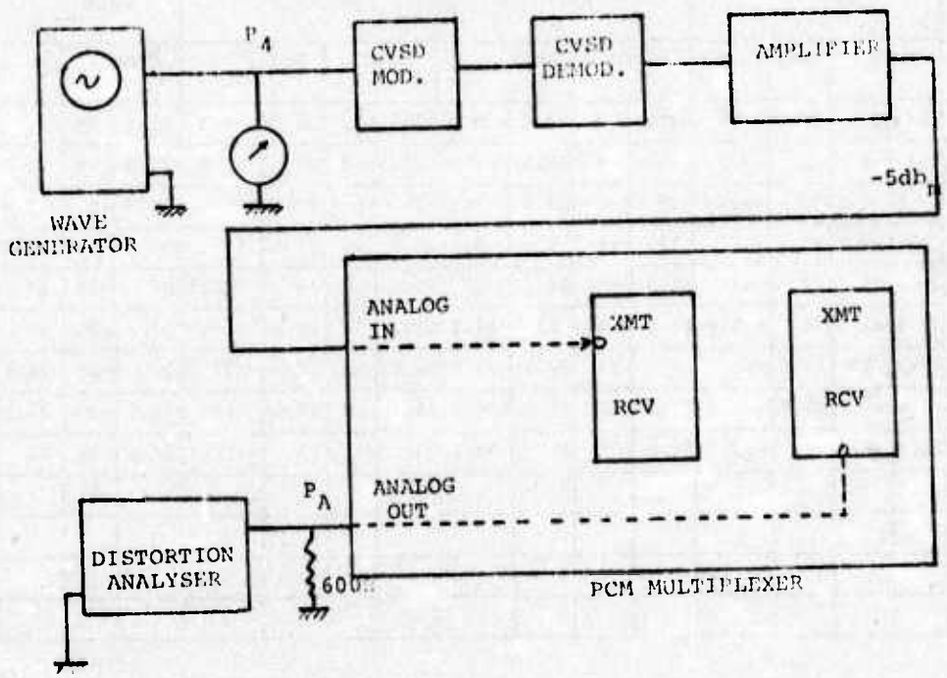


FIGURE 4.5.- Δ→ PCM analog conversion.

	Δ sampling frequency															
	16				19.2				32				38.4			
Power in db	DDMC S/N	L	Anal. S/N	L	DDMC S/N	L	Anal. S/N	L	DDMC S/N	L	Anal. S/N	L	DDMC S/N	L	Anal. S/N	L
+10									22	10.5			22.5	10.5		
+5	19.5	10.5	19.5	10.5	19.5	10.5	21	10.5	22	10.5	23.5	10.5	22.5	10.5	22.5	10.5
+3	19.5	10.5	19.5	10.5	19.5	10.5	21	10.5	22	10.5	23.5	10.5	23	10.5	23.5	10.5
0	19	10	18.5	10.5	20	10	21.5	10.5	24	10	24	10.5	23	10	22.5	10.5
-5	20	7	21	6.5	20.5	+7	21.5	7	25.5	+8	26.5	7.7	26.5	7.5	26.5	+8
-10	20	+2.3	19	1.2	21	+2.5	21.5	1.6	25.5	+3	28.5	+2	29	2.25	29	2.4
-15	19.5	-1.5	18.5	-3.4	22	-1.5	22	-3	26.5	0	28.5	-2.5	29	-1.25	30	-2.4
-20	18.5	-6	18.5	-8	21	-6	21.5	-8.2	27	-4.5	28	-8	29	-5.7	30	-7.5
-25	18.5	-10	17.5	-12.5	21.5	-10	21.5	-12	26.5	-9	27	-12	28	-10	29	-11.7
-30	16.5	-15.5	17.5	-16.5	20	-16	19.5	-16.5	25	14.5	26	-16.5	26.5	-15	28.5	-15.7
-35	15	-23.5	16	-20.5	16	-23	19	-21	-22	-22	25	-21	24.5	-21.5	27	-20
-40																
-45																

TABLE 4.1.- PCM → Δ conversion (D1).

	Δ sampling frequency															
	16				19.2				32				38.4			
Power in db	DDMC		Anal.		DDMC		Anal.		DDMC		Anal.		DDMC		Anal.	
+10	17	2.5	20.5	-.5	19.5	4	23.5	0	21	+3	24.5	-0.5	21.5	+4	26	-1
+5	17	-5	22	-2.5	21	-4	22.5	-2.5	21.5	-3	27	-3.5	22.5	-4	27	-3.5
+3	17.5	-6.5	23	-4.2	24	-6	23.5	-4.2	24	-5.4	27.5	-5	24.5	-5.4	27.5	-5
0	18	-9.5	23	-7.7	19	-9	24	-8	24.5	-10	28.5	-9	26	-8.7	27.5	-9
-5	17.5	-15.7	23	-12	19.5	-14	24	-12	24	-16	28	-13.5	26	-12	27	-14
-10	17.5	-21.5	22	-16.5	18.5	-19.5	23	-17.4	22.5	-22	27.5	-18.5	25.	-20	27	-18.5
-15	17	-25	22.5	-20	18	-24	22.5	-22	21.5	-26	26	-23	24	-25	26.5	-23
-20	14.5	-29.5	20.5	-23.5	18.5	-28	21.5	-26.5	20.5	-30	24.5	-28	21.5	-30	23.5	-27.5
-25	11.5	-32	19	-25.7	14.5	-31	19	-30.5	20	-32.5	23	-32.5	19.5	-35	23	31.5
-30																
-35																
-40																
-45																

TABLE 4.2.- Δ → PCM conversion (D1).

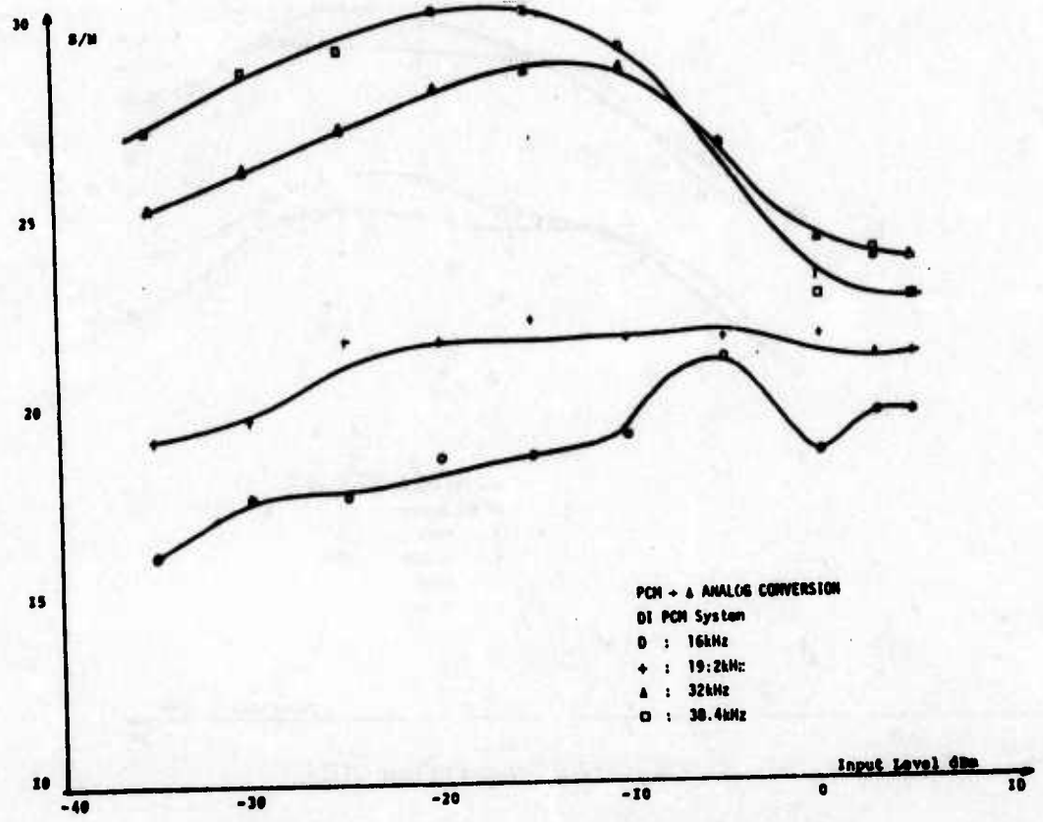


FIGURE 4.6A.- PCM→Δ analog conversion (D1).

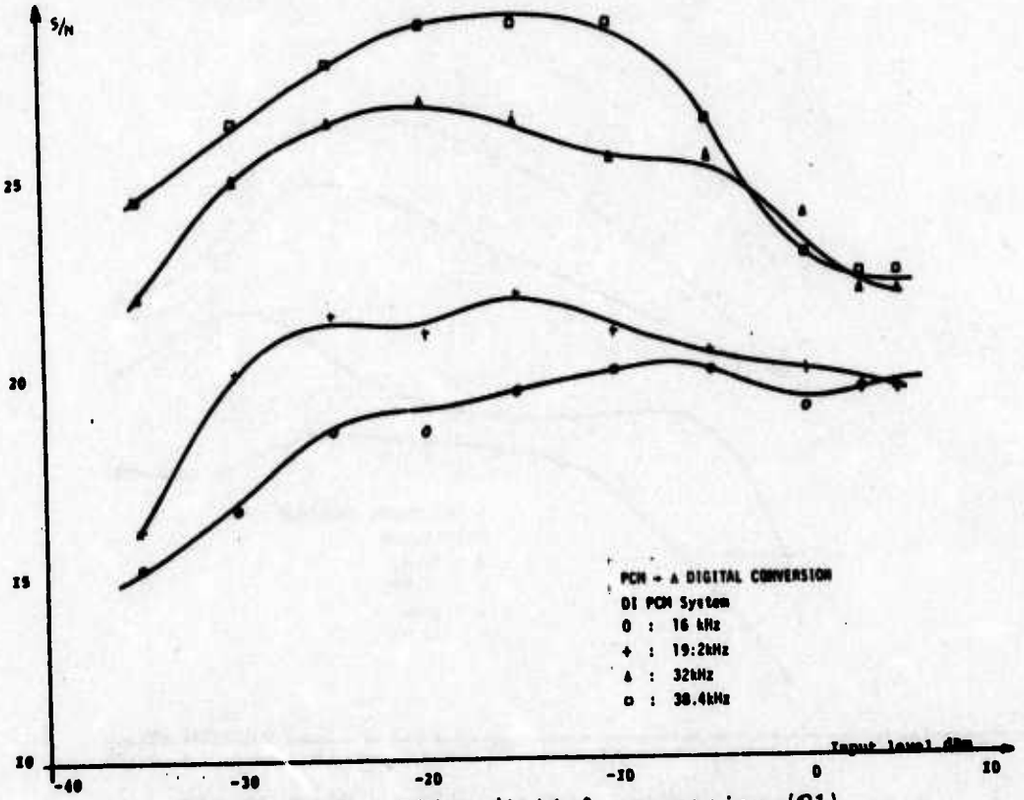


FIGURE 4.6B.- PCM→Δ digital conversion (D1).

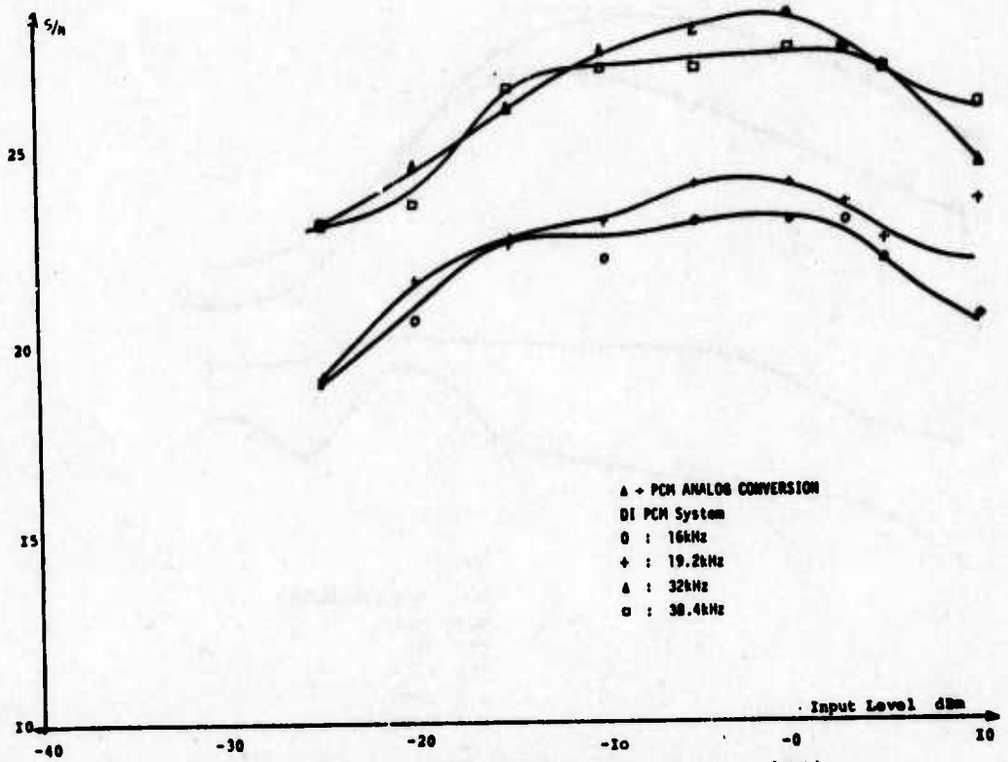


FIGURE 4.7A.- Δ→PCM analog conversion (D1).

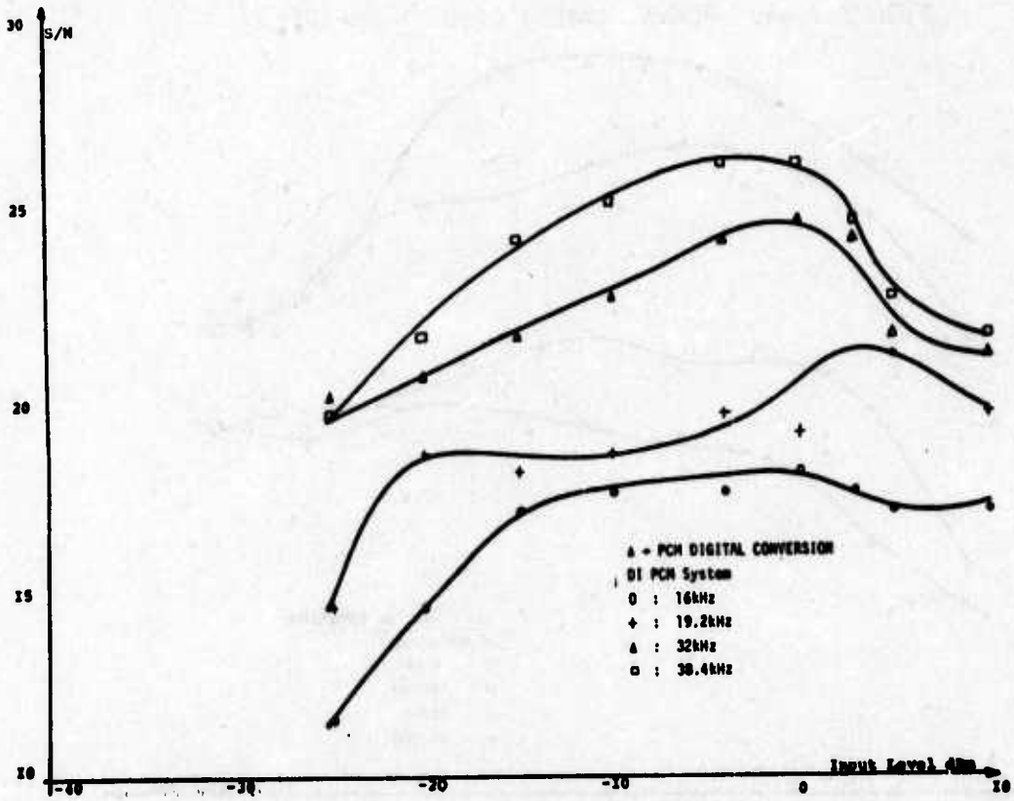


FIGURE 4.7B.- Δ→PCM digital conversion (D1).

Power in db	Δ sampling frequency							
	16		19.2		32		38.4	
	S/N	Lin	S/N	Lin	S/N	Lin	S/N	Lin
+10	20	+9	20	+9	20	9	20	9
+5	+16	+4	+19	+4	23.5	4.5	24.5	+4.5
+3	15	+2	+18.5	+2	24.	+2	25.5	+2
0	+14.5	-0.5	+18	-1	25.5	-1	28	-1
-5	+15	-6	+19	-6	27	-6	29	-6
-10	+16	-12	+20	-11	25.5	-11.5	28.0	-11.5
-15	+14.5	-14	+20.5	-14	23	-17	24.5	-17
-20	+13.5	-21	+16.5	-20	20	-22	22	-21
-25	+11.5	-24.5	+14	-24	15	-25	16	-25
-30								
-35								
-40								
-45								

TABLE 4.3.- CVSD modulator - demodulator back-to-back.

Power in db	S/N	Lin.
+10		
+5	18	+5
+3	28	+4
0	28	+2
-5	27	-5
-10	26	-10
-15	24.5	-14
-20	24	-18
-25	22.5	-24
-30	20	-27
-35	17.5	-32

TABLE 4.4.- D1 back-to-back

Power in db	Δ sampling frequency															
	16				19.2				32				38.4			
	DDMC S/N	L	Anal. S/N	L	DDMC S/N	L	Anal. S/N	L	DDMC S/N	L	Anal. S/N	L	DDMC S/N	l	Anal. S/N	L
+10													SATURATION			
+5													SATURATION			
+3	+19	+9	+19	+9	+19	+9	+19	+9	20	+9.5	19.5	9.5	+20	+9	19.5	9.5
0	+20	+9	+20	+9	+20	+9	+20	+9	21	9.0	19.	9.5	+20	+9	19	9.5
-5	+18	+7	+18	+7	+19	+7	+18	+7	22.5	+7.5	20	7	+23	+7	20	7
-10	+15.5	+2	+15	+2	+17.5	+2	+18	+2	24	+2.5	23.5	+2	+26	+2	25	+2
-15	+16	-4.5	15.5	-4	+18	-4	18	-3.5	26	-2.5	25	-4	+26.5	-4	26	-4
-20	+15	-10	+14.5	-8	+18.5	-9	18	-8	25	-8	24	-9	+25	-10	25	-9
-25	+14	-16	+14	-14	+18.5	-15	18	-14	23	-14.5	23	-14.5	+24.5	-16	24.5	-14.5
-30	+12	-22.5	+12	-18	+16	-20	+17	-18	22	-19	22	-19	+23	-19	23	-19
-35	+8	-28	+10	-24	+13	-26	+12	-24	17	-25	18	-24	19	-24.5	19	-23
-40																
-45																

TABLE 4.5.- PCM → Δ conversion (TD968).

Power in db	Δ sampling frequency															
	16				19.2				32				38.4			
	DDMC S/N	L	Anal. S/N	L	DDMC S/N	L	Anal. S/N	L	DDMC S/N	L	Anal. S/N	L	DDMC S/N	L	Anal. S/N	L
+10	19	1.5	19	0	20	+2	20	0	20	+2	20	0	20	+3	20	0
+5	16.5	-7	16.5	-5.5	19	-6	19	-5.5	24	-6	24.5	-6	24.5	-6	25	-6
+3																
0	16	-12	16	-10	19	-11	19	-10	27	-11	27	-10.5	28	-10	28	-10.5
-5	16.5	-17	16.5	-15.5	20	-15.5	20.5	-15.5	26.5	-16	26	-16	29	-15	29	-16
-10	18.5	-22	18.5	-21	20.5	-20	+20	-20	26	-20.5	25.5	-21.5	28	-19	27	-21.5
-15	14	-27	14	-26	18	-24	18	-25.5	23	-25	22	-27	25	-23.5	23.5	-27
-20	11.5	-32	11.5	-31	16	-27	16	-33	20	-29	18	-33	22	-28	18	-33
-25	8	-35	9	-35	14	-31	13	-35	17	-32	13	-40	18.5	-31	13	-40
-30																
-40																
-45																

TABLE 4.6.- Δ → PCM conversion. (TD968).

Power in db	S/N	Lin.
+5	24	+6
+3	38	+4
0	38	+2
-5	38	-3.5
-10	37.5	-8
-15	36	-13.5
-20	32	-18
-25	28	-23.5
-30	23	-28
-35	18	-33.5

Table 4.7.- PCM modulator-demodulator back-to-back (TD968).

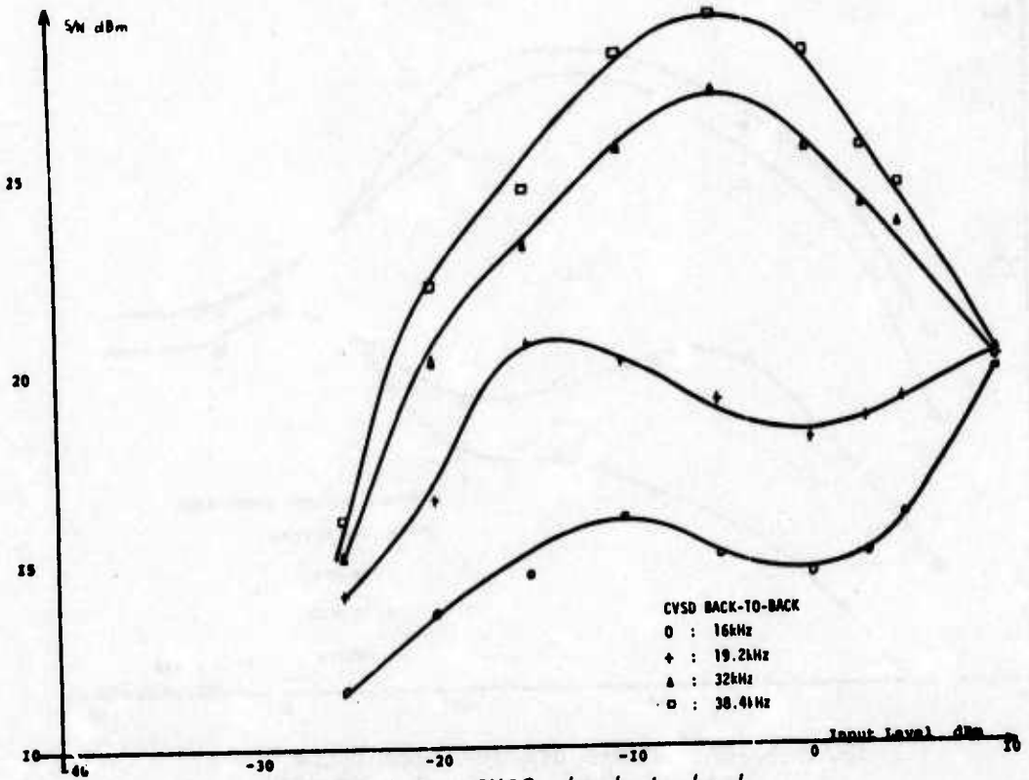


FIGURE 4.8.- CVSD back-to-back.

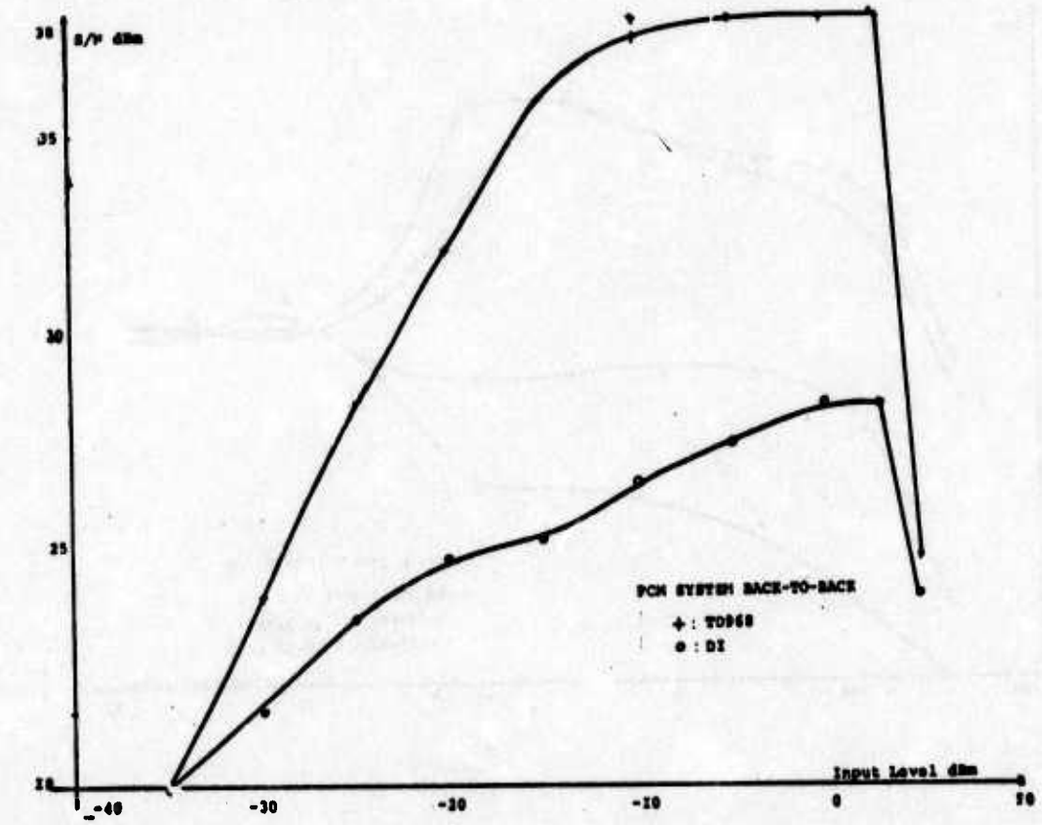


FIGURE 4.9.- PCM system back-to-back.

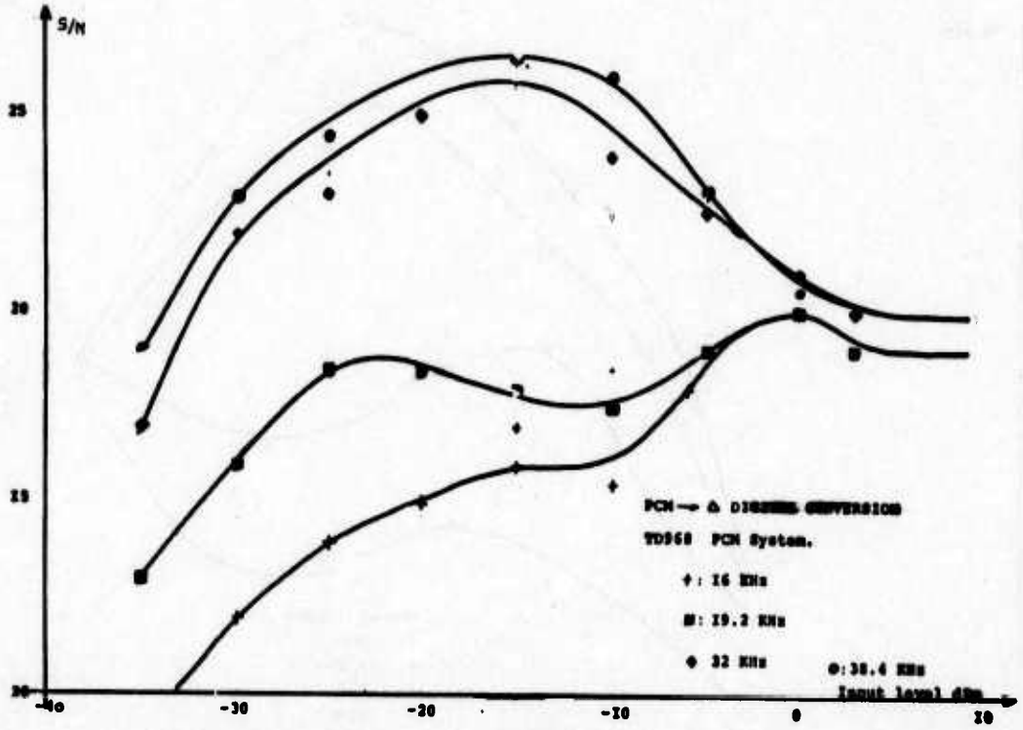


FIGURE 4.10A.- PCM→Δ digital conversion.

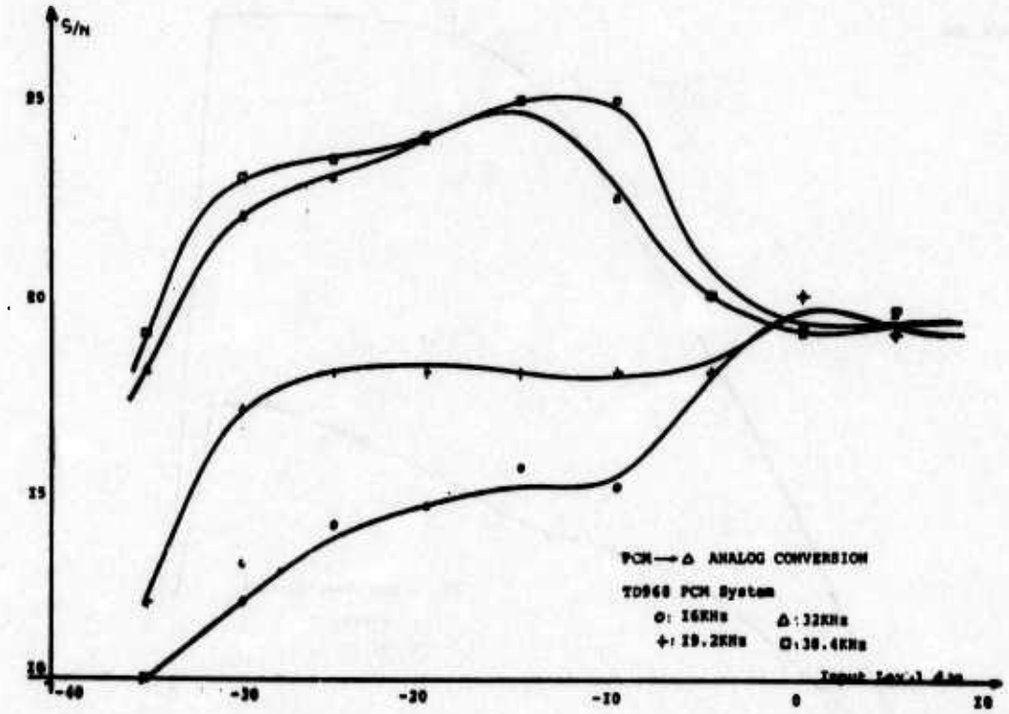


FIGURE 4.10B.- PCM→Δ analog conversion.

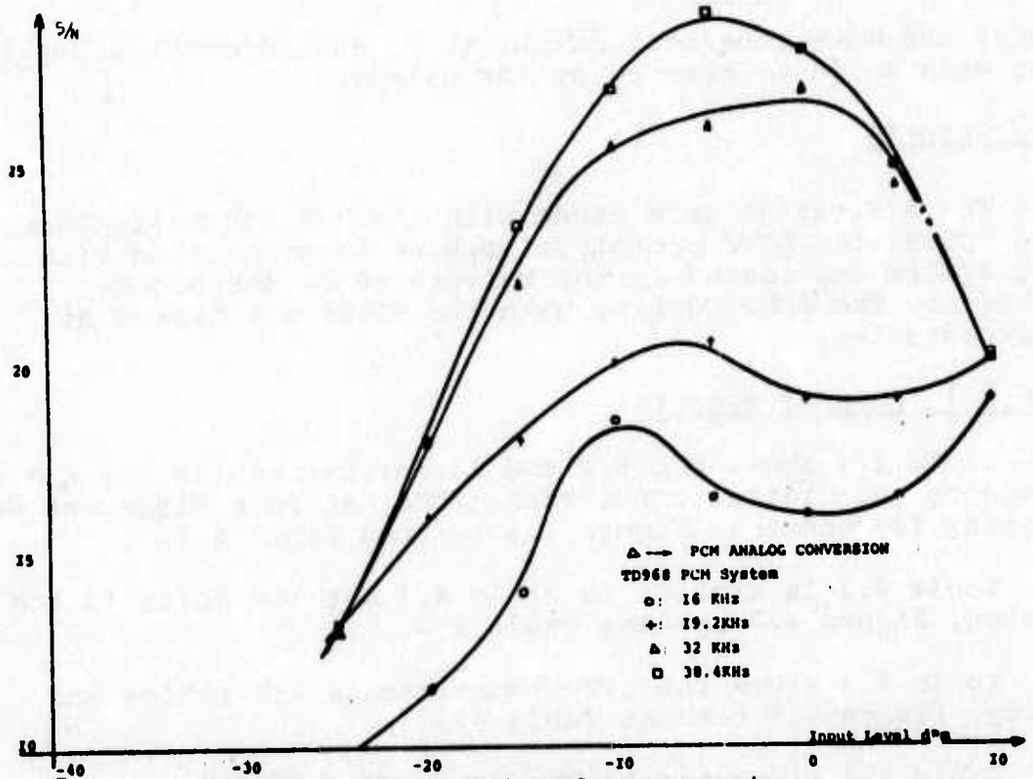


FIGURE 4.11A.- Δ→PCM analog conversion.

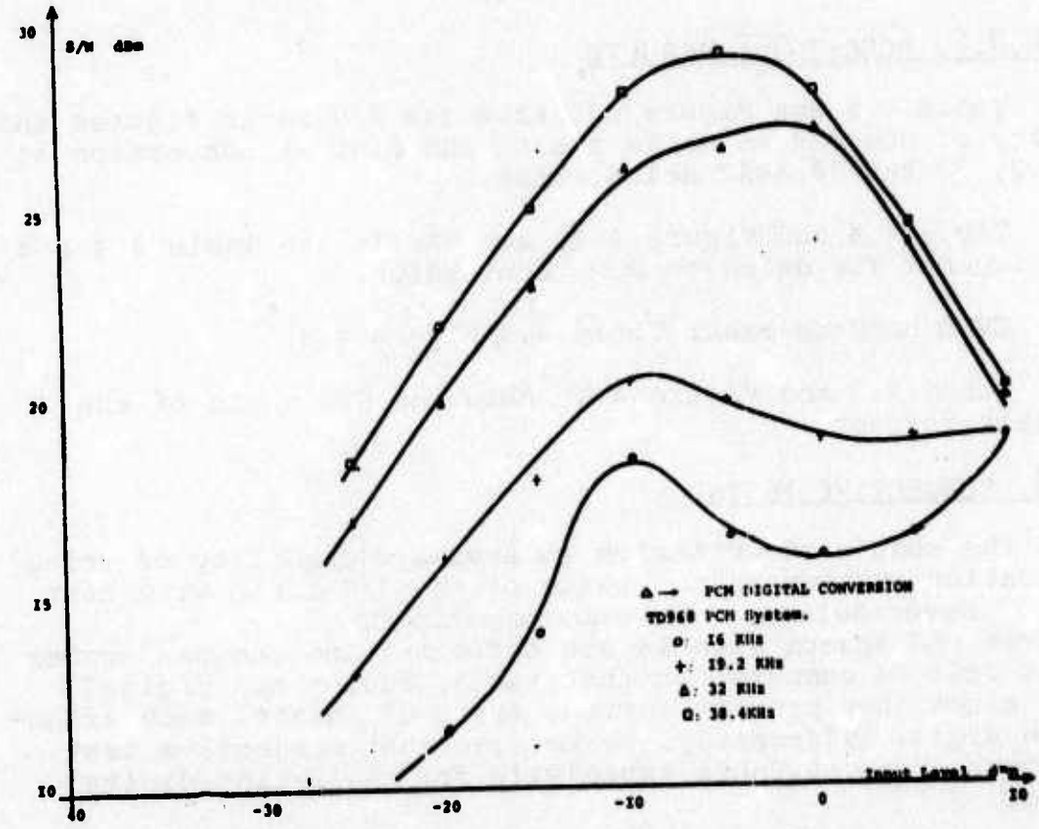


FIGURE 4.11B.- Δ→PCM digital conversion.

A. Adjust the wave generator output to P_4 and adjust the amplifier gain so as to have P_A at the output.

4.2 RESULTS

The S/N ratios were taken with the D-1 PCM multiplexer and the TD968. The DDMC prototype working in connection with the D-1 system was tested in the Université de Sherbrooke laboratories. The DDMC working with the TD968 was tested at RADC Laboratories.

4.2.1. DDMC-D1 RESULTS

Table 4.1 shows the S/N and linearity results for PCM to delta analog and digital conversion (DDMC) at four different delta sampling frequencies. Figure 4.6 resumes Table 4.1.

Table 4.2 is similar to Table 4.1 but for delta to PCM conversion. Figure 4.7 resumes Table 4.2.

Table 4.3 gives the CVSD back-to-back S/N ratios and linearity. Figure 4.8 resumes Table 4.3.

Table 4.4 gives the D1 back-to-back S/N ratios and linearity. Figure 4.9 resumes Table 4.4.

4.2.2. DDMC-TD968 RESULTS

Table 4.5 and Figure 4.10 show the S/N ratio figures and linearity of the PCM to delta analog and digital conversion at 16, 19.2, 32 and 38.4kHz delta rates.

Table 4.6 and Figure 4.11 are similar to Table 4.5 and Figure 4.10 but for delta to PCM conversion.

CVSD back-to-back: Table 4.3, Figure 4.8.

Table 4.7 and Figure 4.9 show the S/N ratio of the TD968 back-to-back.

4.3. SUBJECTIVE TESTS

The most used criterion to assess the quality of voice communication systems is the value of the S/N ratio with test tones. Nevertheless, the characteristics of sine waves and speech signals are different and one can wonder if it is fair to compare, on that basis, analog and digital systems since they present various types of noises, each affecting the signal differently. We believe that subjective tests appear to be more suitable especially for evaluating digital equipment.

Among the main concepts-intelligibility, preference, articulation index-used to subjectively rank-order communication systems, we have chosen intelligibility.

4.3.1. INTELLIGIBILITY TEST

The most discriminative intelligibility tests have monosyllabic words or nonsense syllables as stimuli. The best known—Harvard P.B. Word Test, Modified Rhyme Test, Consonant Recognition Test- were conceived for the English language. The material of our test consists of 660 French sound monosyllables with or without significance, divided into ten equally difficult lists. This basic material is presented in Figure 4.13. The test is based on the identification of either the initial or final consonant phoneme. 24 different test sheets similar to the one shown in Figure 4.14 are used for the test. A long training period for the listeners is not needed. Each list is read by eight different speakers, which increases the sensitivity of the test. The set-up used to run the test experiment is shown in Figure 4.12.

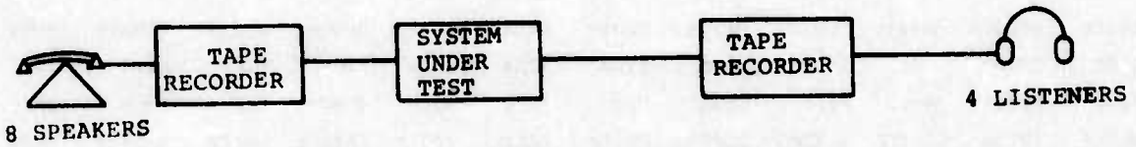


FIGURE 4.25.- Subjective test set-up.

4.3.2. RESULTS

The reference is a direct voice recording and the intelligibility score of this material is 93%.

Tables 4.8 and 4.9 show the intelligibility scores for each system tested. The TD-968 PCM multiplexer is used for testing.

	PCM to delta conversion			
	delta sampling rate			
	16 K	19.2K	32	38.4
DDMC	82%	84%	89%	89%
Analog	77%	80%	85%	85%

TABLE 4.8.- Intelligibility score.

pire	mire	zire	chire	nire	fire	cire	jire	lire	rire	lire	pire
telle	delle	nelle	quelle	velle	selle	zelle	relle	pelle	belle	velle	relle
nage	gage	fage	sage	chage	lage	rage	page	cage	tage	nage	gage
gute	fute	zute	chute	lute	rute	bute	mute	vute	tute	bute	vute
vante	sante	jante	gante	chante	zante	gnante	tante	dante	kante	kante	jante
chonde	londe	ronde	bonde	monde	ponde	donde	konde	fonde	sonde	fonde	donde
lore	pore	bore	gore	tore	dore	core	fore	sore	jore	fore	bore
poule	boule	moule	toule	doule	goule	voule	zoule	choule	roule	moule	boule
mien	tien	dien	rien	sien	gien	lien	zien	pien	bien	sien	lien
bieux	kieux	vieux	cieux	gieux	lieux	rieux	pieux	mieux	dieux	lieux	vieux
chui	lui	rui	pui	mui	tui	dui	cui	fui	zui	rui	tui
rose	pose	mose	tose	dose	fose	nose	chose	jose	lose	dose	pose
beur	neur	teur	gneur	veur	zeur	cheur	leur	jeur	peur	teur	gueur
sère	chère	gère	lère	père	mère	tère	nère	guère	vère	zère	mère
jal	ral	bal	mal	gal	nal	cal	gnal	tal	sal	tal	mal
gnure	gure	lure	bure	cure	vure	fure	chure	dure	nure	cure	gnure
nol	tol	gnol	col	fol	vol	gol	sol	rol	mol	nol	sol
dance	mance	gance	vance	zance	chance	lance	sance	rance	pance	zance	chance
keuse	gneuse	gneuse	veuse	teuse	ceuse	meuse	geuse	neuse	cheuse	cheuse	teuse
zine	chine	pine	fine	bine	dine	vine	line	cine	nine	cine	dine
fade	zade	pade	rade	sade	kade	jade	nade	gnade	gade	rade	nade
dette	jette	quette	zette	guette	nette	cette	bette	chette	lette	guette	lette
fic	zic	chic	jic	lic	ric	pic	mic	tic	nic	chic	zic
site	vite	nite	pite	fite	bite	gite	rite	zite	dite	gite	site
voi	soi	loi	joi	roi	moi	toi	doi	quoi	foi	moi	roi
cour	dour	sour	zour	pour	nour	gour	bour	four	pour	nour	jour
rac	vac	tac	nac	pac	bac	mac	fac	lac	gnac	bac	fac
mène	fène	vène	nène	kène	guène	bène	dène	zène	chène	dène	fène
jote	note	chote	dote	gnote	cote	zote	gote	bote	vote	gote	zote
toc	koc	doc	loc	roc	choc	foc	boc	voc	poc	voc	choc
gane	jane	cane	dane	bane	tane	pane	vane	mane	zane	jane	cane
lise	rise	fise	mise	pise	gise	chise	vise	guise	kise	pise	kise
zare	bare	sare	fare	mare	gnare	gare	tare	nare	jare	gnare	jare

Figure 4.13A.- First category: basic half list

lipe	lime	lite	libe	ligne	line	life	ligue	lige	lile	lipe	lime
jute	jude	juche	juse	juge	jule	jure	jupe	jube	jule	jure	jugue
lane	lague	lave	lace	lare	lape	lade	lame	late	labe	lave	labe
tigne	tife	tile	tisse	tise	tiche	tige	tire	tipe	tine	tiche	tisse
rore	roche	rosse	rope	robe	rome	rote	rone	rogue	rogne	rome	rope
couche	coule	coure	coupe	coute	coude	doune	couve	cousse	couse	coune	coule
brige	bribe	brime	brite	bride	brique	brigue	brive	brisse	brise	bride	brigue
tule	ture	tube	tuse	tune	tume	tuque	tugue	tuve	tude	tube	tude
dame	date	dade	daque	dague	dace	dave	dage	dache	dale	dace	dade
pèque	pègne	pèbe	pèse	pèche	pège	père	pède	pète	pène	pède	pèse
rafe	rave	race	rare	rape	rabe	rame	rate	raque	rague	rate	rame
touse	touche	toupe	toure	toube	toute	toude	toufe	toune	tougue	toure	toufe
vire	vide	vine	vigne	vique	vife	vice	vile	vive	vime	vigne	vive
lambe	lante	lanque	langue	lanfe	lanre	lanche	lampe	lande	lange	langue	lanche
brète	brègue	brèche	brège	brème	brèle	brèse	brèbe	brèfe	brève	brèche	brèfe
frime	frique	frire	frife	frile	frite	frive	frige	frise	friche	frite	frique
mugue	muque	muge	mune	mule	mugne	muse	mude	mure	muce	mugue	mugne
conve	conce	confe	conde	conge	combe	compe	conque	congue	conte	confe	conce
rude	rupe	rune	rule	ruche	ruse	rugue	russe	rume	rure	russe	rune
sèche	sèfe	sèze	sèque	sène	sève	sème	sèche	sègne	sèpe	sèque	sène
singe	simbe	sinde	sinve	sinre	simpe	sinte	sinfe	sinque	sinse	simbe	sinre
saule	saune	saute	sauge	sauve	sause	sauce	saume	saure	saufe	sauge	sauve
trache	trape	traque	trave	trace	trane	trafe	trale	trage	trame	trape	trache
rève	rèce	rèle	rème	rèfe	rèche	règne	rèse	rène	rèque	rèfe	rèle
douce	douve	douche	doube	doume	doure	doupe	douze	doule	doute	doume	doute
nague	nase	nape	nate	nave	nafe	nane	nasse	nabe	nache	nase	nate
cique	cise	cife	cide	cipe	cisse	cile	cigne	sime	cive	cive	cise
lofe	loge	lome	lone	loce	logue	lobe	lote	loche	loque	lone	loge
rampe	range	rangue	ranfe	rante	ranque	ranre	ranche	rambe	rande	ranre	rangue
vabe	vane	vase	vague	vage	vale	vache	vaque	vade	vare	vaque	vage
crène	crème	crègne	crèche	crède	crève	crèbe	crèpe	crèle	crège	crèle	crèpe
dise	dire	dige	dile	digue	dide	dique	dibe	dife	dipe	dise	dibe
lèce	lèle	lève	lème	lèque	lège	lène	lèse	lèfe	lège	lègue	lèque

FIGURE 4.13B.- Second category: basic nulf list

TEST D'INTELLIGIBILITE

NOM:_____ SYSTEME:_____

___ère	___ien	lan___e	da___e
___ure	___our	fri___e	na___e
___oule	___ade	tu___e	sin___e
___oi	___ieux	dou___e	pè___e
___ine	___age	sè___e	la___e
___ante	___ac	ro___e	ci___e
___ire	___onde	li___e	cou___e
___ène	___elle	lo___e	ju___e
___ic	___ance	tra___e	con___e
___eur	___ote	vi___e	ran___e
___ette	___euse	sau___e	ru___e
___ite	___ore	rè___e	bri___e
___ute	___are	ti___e	lè___e
___ise	___al	di___e	brè___e
___ose	___ol	tou___e	mu___e
___oc	___ui	va___e	ra___e
___ane		crè___e	

Scores :

Pourcentages :

FIGURE 4.14 - Test sheet

	Delta to PCM conversion			
	delta sampling rate			
	16K	19.2K	32K	38.4K
DDMC	84%	87%	88%	89%
Analog	88%	88%	90%	90%

TABLE 4.9.- Intelligibility score.

4.4. CONCLUSION

From the S/N ratio tests the DDMC -D1- PCM to delta conversion is equal to the analog conversion, but the DDMC-D1-delta to PCM conversion is not as good as the analog conversion.

The objective (S/N) tests on the DDMC-TD968 show that the digital conversion is equal to or better than analog conversion in both directions.

This difference can be explained by the difference which exists between the theoretical compression-expansion law of the D-1 (M-100) and the approximate law found in the D-1 multiplex equipment (see section 5.3.2.).

The subjective tests made on the systems connected to the TD968 do not correlate with the objective tests results. Intelligibility scores indicate that the digital PCM to delta conversion is preffered over the analog PCM to delta conversion. From delta to PCM the preference is reversed.

The intelligibility scores obtained indicate that we have high quality systems and in such a case it is difficult to conclude that one system is better than the other when there is only a difference of a few percentage points. We then conclude that the digital conversions give the same voice quality as the analog conversion.

5. DIVERSE CONSIDERATIONS

This section deals with, on one hand, the utilization of the conversion principle for the realization of a multiplexed 24-channel converter and on the other, with the possibilities and limitations discovered during the research for the present contract.

5.1 MULTIPLEX CONVERTER

Several digital filter design techniques are possible in the realization of a converter: serial or parallel arithmetic, microprocessor. The serial technology was used in the realization of the uni-channel converter. Because of the circuit operating speed it would be possible to convert five(5) channels instead of one by changing only the clocks and the memory size of the prototype. Thus, five uni-channel converters could be used as a multiplex 24-channel converter. Considering the fact that the cost of a uni-channel converter is approximately $2500 (components only), the cost of a multiplex converter would be $12,500, a cost which is considerably lower than that of a 24-channel PCM-D-1 multiplexer. In regard to bulk and weight, five uni-channel converters are the equivalent of a D-1 multiplexer.

With parallel arithmetic or a microprocessor (ROM) the operation time is reduced and, inversely, more operations can be done in a given amount of time. However, the lower the operation time, the higher is the cost. It follows that the advantages of parallel arithmetic or of a microprocessor over series arithmetic are more on the level of bulk, weight, size and of maintenance than that of cost. In general, the DDMC will cost less than an analog conversion since the cost of a numerical conversion must be compared to that of two conversions in the analog case, that is: PCM $\rightleftarrows$ analog, analog $\rightleftarrows$ Δ.

5.2 FUTURE APPLICATIONS

In addition to the PCM $\rightarrow\Delta$ conversion done for reasons of network compatibility, the conversion technique can be used for compression. In this sense, PCM information sent at a 64 kbit/sec rate can be sent at a 32kbit/sec rate in Δ, using the PCM $\rightarrow\Delta$ conversion. Moreover, use of a TASI system could further reduce the information rate from 32kbit/sec to 16kbit/sec. The inverse process would permit to reobtain the PCM signal at a 64kbit/sec rate. Thus, a 64kbit/sec PCM signal could be transmitted at a 16kbit/sec rate without significantly deteriorating its subjective quality.

5.3 Possible Improvements

5.3.1 Multipliers

In the prototype all the digital multipliers found in the digital filters are constructed using a pyramid structure of adders which requires in the worst case, N - 1 adders by coefficient (figure 5.1).

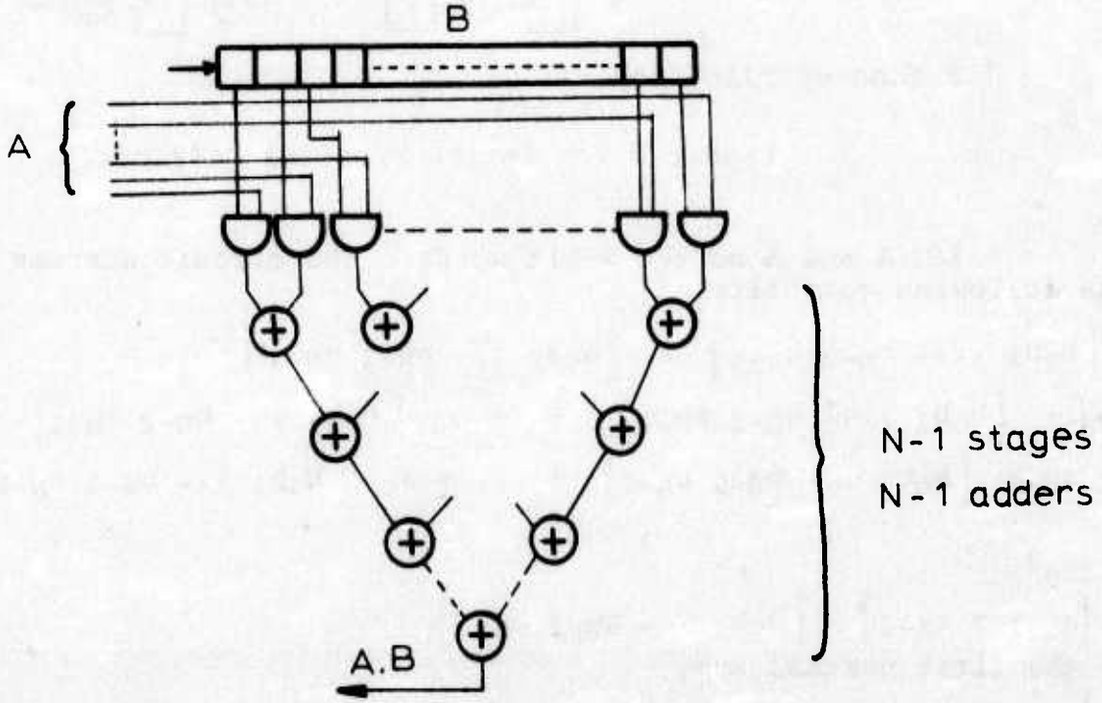
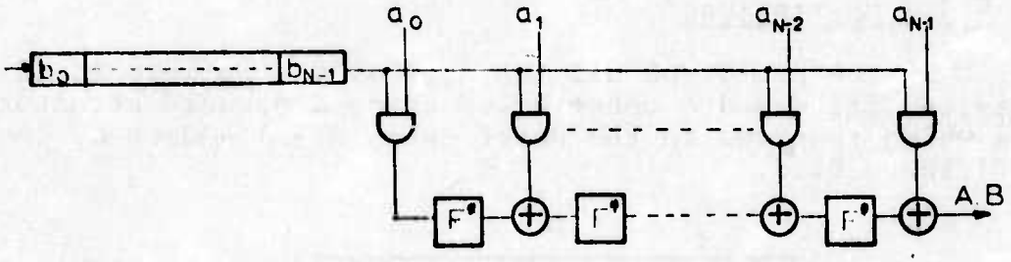


Figure 5.1.- Multiplication using pyramid structure of adders.

In this method there is a truncation error at the output of each adder. The total error is not necessarily negligible.

The pipeline multiplication method illustrated in figure 5.2 does not have the disadvantages of the preceding technique.



* F denotes Flip flop.

Figure 5.2.- Serial Pipeline Multiplier.

Let A and B be two N-bit words. The circuit carries out the following computation:

$$\left[b_0 b_1 \ldots b_{N-2}\ b_{N-1}\right] \times \left[a_0 a_1 \ldots a_{N-2}\ a_{N-1}\right] =$$

$$a_{N-1}\left[b_0 b_1 \ldots b_{N-2}\ b_{N-1}\right] + a_{N-2}\left[b_0 b_1 \ldots b_{N-2}\ b_{N-1}\right]$$

$$+ a_{N-3}\left[b_0 b_1 \ldots b_{N-2}\ b_{N-1}\right] + \ldots + a_0\left[b_0 b_1 \ldots b_{N-2}\ b_{N-1}\right]$$

where

$\left[a_{N-1} + a_{N-2}\right]\ \left[b_0 b_1 \ldots b_{N-2}\ b_{N-1}\right]$
is the first partial sum,

$\left[a_{N-1} + a_{N-2} + a_{N-3}\right]\ \left[b_0 b_1 \ldots b_{N-2}\ b_{N-1}\right]$
is the second partial sum,

$\left[a_{N-1} + a_{N-2} + \ldots a_0\right]\ \left[b_0 b_1 \ldots b_{N-2}\ b_{N-1}\right]$
is the (N-1)-th partial sum.

The N most significant bits of each partial sum above are obtained at the outputs of the N adders and stored in the flip-flops at the shift times of the register which contains A.

The N first output bits are neglected if the desired result is truncated to N bits. A zero reset of the flip-flops precedes each multiplication.

5.3.2 D-1 COMPANDING SCHEME

The M-100 law is approximated in the D-1 by an analog circuit (diode and resistance). In the DDMC prototype, the M-100 law is digitized to be as close to the analog characteristic as possible. Nevertheless there is a difference between the two realizations and the two operations (D-1 compression, DDMC expansion) are not, strictly speaking inverses of each other. This difference degrades the signal-to-noise ratio.

In order to minimize this degradation the DDMC law must be designed to be not a M-100 law but the approximate M-100 law found in the D-1 system.

6. GENERAL CONCLUSION

The objectives aimed at in this second phase of this R & D contract on a direct digital modulation converter were twofold:

1. Design a one channel converter which converts a CVSD code at 16, 19.2, 32 and 38.4kHz into D-1, TD968 or D-2, TD660 and European A law PCM multiplexers and vice-versa.

2. Build a prototype of such a converter, that will give at least as good a quality as the existing means (analog) of conversion between these two digital formats.

The reader can notice that these objectives were met: this is a breakthrough in this field since this is the first totally digital device of its type completely designed and built.

It is to be noted that, since the prototype is limited to a single channel, serial operation was used. If multiplexing is studied, some subsystems might be shared by several channels. We believe that the approach then taken should be parallel instead of serial. This would result in an increased sharing of components and a corresponding decrease in the cost per channel.

The first section of this report deals with the theoretical aspect of the problem and in this respect is an extension of the phase I report. The computer simulation of the CVSD code, the optimization of the parameters of the DDMC (gain adaptation, filters, etc...) are presented in detail in this section.

The overall implementation structure is presented in chapter 3 in order to allow the reader to follow through the main subsystem operations of the DDMC.

The detailed circuit description presented in Appendix A gives the entire analysis of the implementation strategy and technology.

The circuit drawings associated with the circuit description are presented in Appendix B. Appendix C gives a complete component list.

The objective and subjective evaluations show that the DDMC performs as well as the analog conversion. However the DDMC-D1-delta to PCM conversion is not as good as the analog conversion. This is due to the discrepancy between the theoretical M-100 law built in the DDMC and the analog approximate M-100 law existing in the D1-channel bank.

The actual DDMC prototype built for a single channel could be modified to take care of five(5) channels by changing the clock circuits and by lengthening the digital filter memories.

A better signal-to-noise ratio could be obtained by using "pipeline" multiplier technology instead of the pyramidal multiplier technology.

The DDMC could be used as a rate compressor if combined with a TASI system. That would permit to obtain a compression factor of four(4) without serious degradation of the subjective quality.

APPENDIX A

DETAILED CIRCUIT DESCRIPTIONS

This appendix treats two main topics: first the circuit descriptions of the delta to PCM converter, second the circuit descriptions of the PCM to delta converter.

In each case the circuit board will be described as part of a function (interfaces, expandor etc...).

To understand each board description it is necessary to refer to the corresponding drawing of Appendix B. Signal notations employed in the following description are the ones used on the drawings. Symbols "Nx" (N30 for example) are the integrated circuit numbers on boards and drawings. This notation makes easier the maintenance and the fault location. Those symbols are often in brakets.

Symbol "BRx", associated with the circuit number of a full adder represents its flip flop (BR) and x is the flip flop circuit number.

A.1 DELTA TO PCM CONVERTER

The delta to PCM part of the DDMC prototype is built with 21 boards which can be divided into five different parts:

-the CVSD coder
-the digital delta decoder function
-the common delta to linear PCM functions
-the compressor function
-the interfaces.

A.1.1. THE CVSD CODER

The CVSD coder is built with the CVSD decoder on board labeled B-22.

The CVSD coder-decoder circuitry design was described in section 3.1.1.

A.1.1.1. BOARD B-22 DESCRIPTION

The four delta frequencies are generated on this board. Gates N42, C15 and potentiometer R27 provide a 32kHz frequency which is divided by 2 through flip flop N27 to give the 16kHz frequency. Gates N28, C16 and potentiometer R28 provide a 38.4kHz frequency which is divided by 2 through flip flop N27 to give the 19.2kHz frequency. Gates N20 allow the chosen Δ frequency (front panel) to operate the CVSD and the DDMC by FΔ1 and FΔ2.

Gate N18 allows the correct digital delta bit stream to enter the CVSD decoder. Gates N19 and N21 allow the analog delta bit stream used for the analog CVSD coder to enter in the CVSD decoder (CoΔ is located on the front board and permits to commute CVSD back-to-back).

Potentiometer R30 adjusts the attenuated (R29) level of the decoder output before feeding the headphone through the top jack of the telephone set (front panel).

Amplifier N24 adjusts (R33) the voice amplitude coming from the microphone through the bottom jack (front panel) before entering the audio input of the CVSD coder. The microphone is supplied by -15V and R31, C18.

A.1.2. THE DIGITAL DELTA DECODER FUNCTION

A.1.2.1. GENERAL DESCRIPTION

The digital CVSD decoder is made of:

-an open loop delta circuit identical in its principle to the one presented in the PCM to delta converter section (A.2.4.1). The only difference lies in the logic gains. The integrator and the syllabic filter being identical in both directions.

-a 6th order elliptic filter.

The implementation of the various coefficients requires adders, control gates, shift registers and flip flops (as mentioned in Section 3.2.2.4).

For each delta frequency a digital CVSD was built. Each one of these is composed of three boards:

-The first board contains the open loop delta plus the signal wires from the integrator to the 6th-order filter.

-The second board contains the first part of the digital filter which is the shift registers, the control gates and the adders needed to build up the filter coefficients of this part of the filter plus the other filter coefficients.

-The third board contains the second part of the digital filter or two shift registers, adders and gates, the clocks needed to operate these functions.

In order to simplify the second and third board description, we will use the following notations for the 6th-order filter presented in Figure A.1.

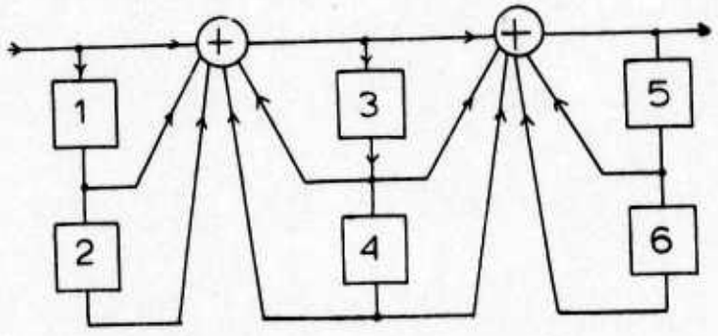


FIGURE A.1.- *Filter contained in boards, B-11, B-12, B-15, B-16, B-18, B-19, B-20, B-21.*

A122 1 BOARDS B10, B13, B16, B19 These boards are the A-boards for the Δ→PCM transition respectively at 16, 19.2, 32 and 38.4kHz bit rate.	16 kHz B10	19.2kHz B13	32kHz B16	38.4 kHz B19
Delta shift register	9	2	8	1
with detection circuit	2,10,11	9,15,16	9,10,15	8,9
Adder register at syllabic filter input	3	1,8	2,3	2,3
Syllabic filter	5,6,7,14	4,5,6,7	4,5,6,7	4,5,6,7
secondary adder receives the outputs	21 BR4 Q_2 (14), Q_0(7)	14 BR13 Q_2(7), Q_0(16)	14 BR21 Q_3(7), Q_0(6)	14 BR20 Q_3(7), Q_0(6)
secondary adder receives the outputs		12 BR13 Q_2(5), S(14)	12 BR12 Q_0(5), Q_2(4)	13 BR20 S(14, Q_2(5)
and adder receives			13 BR11 S(14), S(12)	
to the main adder	12 BR4	3 BR11	11, BR19	10 BR11
Adder register at syllabic filter output	29	10	16, 17	17, 18
with the adder	13 BR34	17, BR23	18 BR24	19 BR11
Multiplier by -1	24, 30	16, 18, 22 and gates in adder 24	23, 29	12,22,29
Integrator shift register 1	37,38,39,40	25,26,20,21	31,32,33,34,35	31,24,25,26,27,28
with the sign memory	31	32	24	31
the secondary adder	25 BR34	35 BR42	41 BR40	35 BR41
receives	Q_0(39) Q_0(40	Q_3(21) Q_3(20)	Q_2(35), Q_1(34)	Q_3(28), Q_2(27)
and the adder		33, BR40	39, BR40	32, BR16
receives		Q_1(20), Q_3(26)	Q_1(33), S(41)	S(35), Q_3(26)
and		31BR 32		
Receiving		S(35), S(33)		
to the main adder	22, BR31	24 BR23	25 BR26	23 BR16,
Connection from the integrator toward the filter				
Shift register 2	40,41,42, 35			
The adder	26 BR28	41, BR42	3 of B board	34 BR41
receives	Q_2(41), Q (35)	Q_2(21 Q_3(2)	Q_1(35)	Q_2(27), Q_3(27)
And		39, BR40		
receives		S(41) and integrator register input		
Toward the main adder	12 of B Board	5 of B board		2 of B board
Clocks	2,8,23,33		15, 29, 30	29,30

A122 1 Boards B10, B13, B16, B19.

A122 2 Boards B11, B14, B17, B20 These boards are the B -board for the A→ PCM transition respectively at 16, 19.2, 32, 38.4kHz bit rates	16kHz B11	19.2kHz B14	32kHz B17	38.4kHz B20
Shift register 2 ----------		1,2,3,4	4,5,6,7,8	13,3,4,5,6,7
with the secondary adder-----	11, BR10	11, BR9	23, BR28	12, BR11
which receives the outputs---	$Q_0(40)$, $Q_2(39)$	$Q_3(4)$ Q_1 (3)	$Q_0(7)$, $Q_2(8)$	$Q_1(16)$, $Q_3(7)$
The bound adders----------	12 BR13, 14 BR13	5, BR6	3, BR1, 2, BR1	2, BR9, 1, BR9
the secondary adder----------	9 BR10			
receives----------	$Q_0(40)$ D_s (37) of the A° board			
with the bound adder---------	14, BR13			
Shift register 3 and 4----------	1,2,3,4,5,6,7	33,24,35,42,14, 29,30,31,32,25	9,10,11,12,13, 14,15,16,17,18	15,16,17,18,19, 20,21,23,24,25,26-
with the secondary adder-----	25, BR32	21, BR28	25, BR29	35, BR27, 38,BR31
which receives the outputs---	$Q_2(3)$, $Q_2(6)$	$Q_1(32)$, Q(25)	$Q_2(13)$ $Q_2(17)$	$Q_2(19)$ $Q_1(19)$, S(39), $Q_0(20)$
toward the main adder-------	33, BR32, 30, BR23	7, BR6	21, BR27, 20, BR19	36, BR22, 37, BR31, 10, BR11
The secondary adder---------	24, BR38	22, BR23		39, BR32
receive----------	$Q_1(3)$ $D_s(1)$	$Q_1(3)$, Q(25)		$Q_3(25)$, $Q_3(24)$
to the adder----------	39, BR38, 40, BR41	1 of C-board		38, BR31, 36, BR22 37, BR31, 10, BR11
The secondary adder---------	28, BR34	29, BR40	24, BR29	40, BR32
receives----------	$Q_2(7)$, $Q_1(4)$	$Q_1(42)$, $Q_3(42)$	$Q_3(12)$, $Q_0(18)$	$Q_0(26)$, $Q_1(25)$
and the adder----------		38, BR37	26, BR28	41, BR33
which receives----------		Q(39), Q(14)	$Q_3(13)$, $Q_3(18)$	$Q_1(20)$, $Q_0(26)$
toward the main adder-------	33,BR32, 30, BR23	27, BR28	22, BR27, 21, BR27, 20, BR19	34, BR33, 37, BR31 10, BR11
The input of shift register 3 and the output----------		of 39	of 26	$Q_3(19)$
go to the bound adder-------		36, BR37	2 of C board	8*of C-board 3,22,36
The secondary adder---------	42, BR41			3 and 9 of C board
receives----------	$Q_3(7)$, $Q_3(5)$			S(8*),$Q_2(24)$, $Q_3(26)$ $Q_1(20)$
toward the bound adder------	40, BR41			22 and 36 of C board
Clocks----------	37,31			

A122 2 Boards B11, B14, B17, B20.

A122 3 Boards B12, B15, B18, B21. These boards are the C-board for the Δ→ PCM transition respectively at 16, 19.2, 32, 38.4kHz bit rates.	16kHz B12	19.2kHz B-15	32kHz B18	38.4kHz B21
Shift register 5 and 6----------	1,2,3,4,5,6,7, 14,21	31,32,33,34,35 3,4,5,6,7	8,9,10,11,12 13,14,19,20,21	5,6,7,14,21,28 35,42,41,40,39
The secondary adder----------	32, BR18	13, BR12	28 BR41	30 BR38
receives the output----------	$Q_3(4)$, $Q_1(4)$	$Q_0(7)$, $Q_2(7)$	$Q_2(21)$ and input of register 6	$Q_2(40)$, $Q_2(14)$
And the adder----------		19 BR12	27 BR41	32 BR33
which receives----------		$Q_2(6)$, $Q_1(6)$	S(28), Q_2 (12)	Q_2 (21), Q_1 (21)
towards the main adder-------	17, BR18,16, BR15	23 BR16, 9 BR15	25 BR39, 7 BR6	31 BR38, 12 BR13, 36 BR29
The secondary adder----------	33, BR34	25 BR24	36, BR37	27, BR34
receives----------	$Q_1(14)$, $Q_3(14)$	$Q_2(35)$ $Q_1(34)$	$Q_1(11)$ $Q_1(20)$	$Q_3(39)$ $Q_3(21)$
And the adder----------			38, BR37	26, BR33
which receives----------			$Q_0(12)$, $Q_1(21)$	S(27) $Q_1(39)$
towards the main adder--------	35 BR34, 17, BR18, 16 BR15	37, BR30	24 BR39, 25 BR39, 7 BR6	12 BR13, 36 BR29.
Clocks----------	29,30	8,15,22,29,36	22,26	24

A122 3 Boards B12, B15, B18, B21.

A.1.2.2. BOARDS B-10 TO B-21 DESCRIPTION

A.1.2.2.1. BOARDS B-10, B-13, B-16 AND B-19

A.1.3. THE COMMON DELTA TO LINEAR PCM FUNCTION

This part is composed of three boards: B-7, B-8 and B-9; its main function is to provide a 8kHz linear PCM information at the compressor input.

It contains:

- 64K and 8K timing, counter and gate control circuits.
- Holder circuit and a 64kHz filter.
- Delta counter.

A.1.3.1. BOARD B-7: 64K AND 8K TIMING AND COUNTER AND GATE CONTROL TOWARDS THE COMPRESSOR

This board is composed of timing and gate controls. The shift register (N31, N32, N33, N34, N35) is the 64kHz counter, reset on impulse M_2, created on each negative edge of the 64kHz frequency, by flip flop N.18 and R_2, C_2. It is filled with ones up to the value 19 of the counter by means of the serial clock of the shift register (N.30).

This counter creates the signals 64Sx (singal Sx defined in 3224 relative to the frequency 64kHz) necessary to the 2nd-order filter, as its serial clock CS121 (N.127) and the serial clock CS (N28, N30) necessary to the input register of the compressor board B-5.

The 8kHz is synchronous and in phase with the 64kHz frequency. The inpulse M_1 is created on the 8kHz by flip flop N26, R_1, C_1, anc variable V which detects the first period of the 64kHz (relatively to the 8kHz) is created by flip flop N18 (see timing diagram A.2). MΔ, the impulse relative to the delta frequency, FΔ, is created by flip flop N22, R_4 and C_4.

The two clocks CW and CR necessary to the holder (B-8) are created by flip flop N26, R_3, C_3, C_5 inverters N24 and N25 and gates N27.

The second part of this board deals with the operations necessary before entering the compressor according to the different PCM laws. When, in A or M100 laws, the binary word output from the 2nd-order filter has to be rectified through flip flop N7 and gates N13, N15 by means of the sign S, memorized in flip flop N10. In M255 law, the value 16.5, transferred on each M_1 in registers N19, N20, is added in N21 (BR12) to the rectified word.

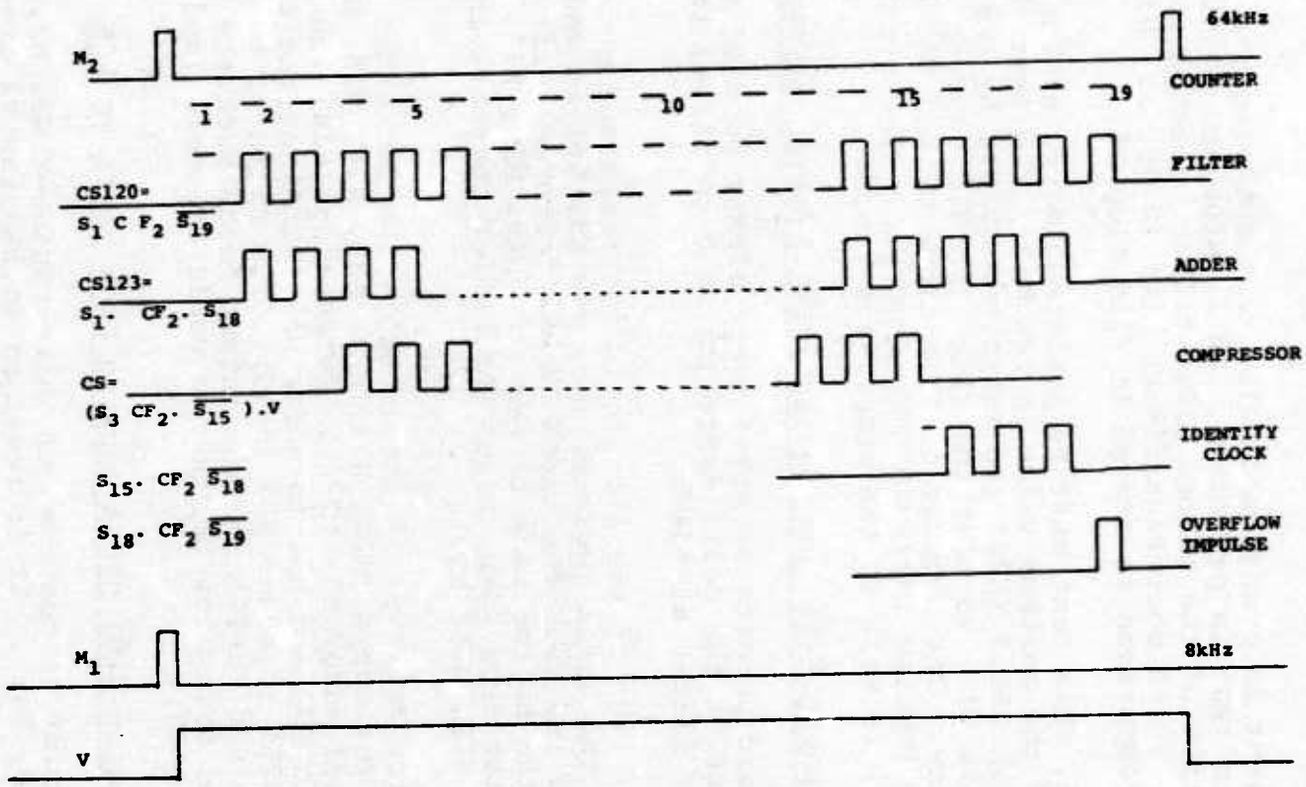


FIGURE A-2.- B-7 timing diagram.

When in TD660, the binary output of the filter has to be multiplied by 1/12.185 (0.000.10101) by means of adders N5 (BR19), N6 (BR6), gates N3, N4 and then rectified through flip flop N7 and gates N14, N15 before entering the compressor. (See Appendix F).

To prevent an overflowed value from entering the compressor, an overflow test is performed. In A, M100 and TD660 it is done at the output of the second order filter by comparing the identity of the three most significant bits (N.30, N2, N3). The result of the comparison is stored in flip flop N9.

In M255, this test must be performed after having added 16.5, to see if the maximum value is reached. The last three impulses of clock CS123 (N29) are inhibited or not by the adder's output (N27, gate N11) so that the flip flop N12 does or does not count an overflow. The outputs of flip flops N9 and N12 do or do not allow an impulse (N29) through gates N11. The overflow result, called DE, is sent to the compressor board.

A.1.3.2. BOARD B-8: HOLDER AND 64kHz DIGITAL FILTER

This board permits to enter every binary word of each delta demodulator at the delta frequency, and to filter them in the second order filter at 64kHz.

The selection of the incoming bit stream and associated serial clock of the shift register (N3, N4, N5, N6) is made through gates N2 and N9. The clock CW built from $F\Delta$ writes this binary word in the buffer made of register N10, N11, N12, N13 and the clock CR built from 64kHz reads the buffer content, in shift registers (N17, N18, N19, N20).

This shift register is the input of the 2nd order filter composed of two registers (N22, N23, N24, N25, N26, N15, N16, N21, N14) and principal adder N7 (BR34). Outputs Q_2 (N14) and Q_1(N26) are gated through N32 and N31 to adder N35 (BR34) as the outputs Q_3(N25) and Q_1(N25) to adder N33 (BR30). The filtered words are added in circuit N28 (BR27) and the output feeds back the principal adder. The sign bits of the two words are memorized in D flip flops (N30, N27).

A.1.3.3. BOARD B-9: DELTA COUNTER FROM DELTA TO PCM

This counter is composed of shift register N2, N3, N5, N6, N37, N38, N40, N41 . It is reset on an impulse $M\Delta$ created on each negative edge of the delta frequency F_Δ (N25, 27) and it is filled with logic ones with the serial clock of the shift register stopping on the value 30 of the counter (N27).

F_Δ and fast clock CF_2, are independent. Every S_x has the value 0, up to the value x of the counter and 1 up to its reset. The timing diagram is presented in Figure A-3.

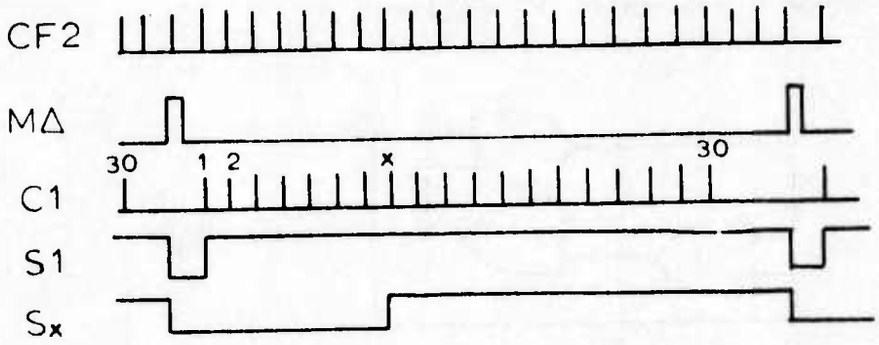


FIGURE A-3.- *Timing diagram of delta counter, delta to PCM.*

A.1.4. THE COMPRESSION FUNCTION

This compression function from linear to different compressed PCM characteristics is done by one board (B-5). It contains four compression laws the M100, M255 or TD968, A, and TD660.

A.1.4.1 INPUT GATES (N1)

The PCM bit train can come from four different sources according to the compression law (M255, A, M100, or TD660). A four-position switch (1,2,3,4) enters a "1" in one gate and "0" in the three others.

A.1.4.2 INPUT REGISTER (N4, N5, N6, 1, N10)

It is a 12 bit register usually controlled by a serial clock which gives 12 impulses per frame. If there is overflow after loading (tested on another board), the registers pass to parallel control (the overflow information appears on DE) and "1"'s are loaded in the 12 register positions.

A.1.4.3. CLOCKS

A.1.4.3.1. 8kHz CLOCKS (N2, N9)

Four 8kHz clock signals are needed:

A) Parallel clock of the work register -C2.
B) Mode control of the work register. MC.
C) Counter zero reset impulse -R0 (except for law TD660)
D) Impulse for the work register serial shift and for the the incrementation of the counter for laws A and M100 only.

These signals are obtained with two set-ups similar to the one in Figure A.4 mounted in series

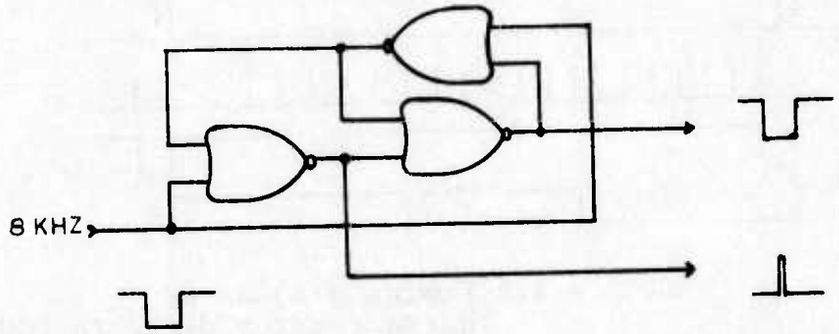


FIGURE A.4.- *Impulse generator*

The signals are of the form indicated in Figure A.5

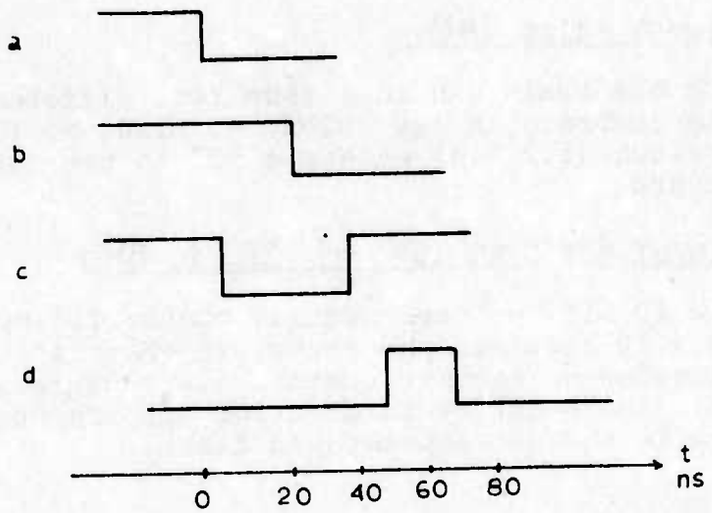


FIGURE A.5.- *Timing diagram.*

CF and the 8kHz are synchronous but their phase is ill-defined. Therefore, the case where a CF trailing edge occurs too soon after (or at the same time as) an identical 8kHz edge must be avoided.

For this reason, at each 8kHz trailing edge, the Δ flip-flop is reset to zero. The first CF impulse cannot therefore be gated to the work unit since Q=1. Q will however become equal to "1", opening the gate and blocking it in this position until the next 8kHz trailing edge.

In law TD660 (4), the flip-flop is constantly blocked at zero by its reset in order to prevent sending the fast clock into the work unit.

A.1.4.4. WORK REGISTER (N11, N12, N13)

It is initially charged in parallel by the input register. Its contents can be shifted by impulses acting on the serial clock (C1), coming from the central unit.

A.1.4.5. WORK UNIT (N28, N10, N19, N20)

In law M255 (1=1), the 7 most significant work register bits are tested. If at least two of them equal "1", two impulses are emitted. The first one HC will increment the counter, the second one HS shifts the register contents toward the less significant bits.

In laws A and M100 (2 or 3 =1), the operations are identical except at the beginning of each frame. First, the contents of the register are shifted (impulse d) in the clock section. A unit counter is also incremented if at least 1 of the 7 most significant bits equals "1".

In law TD660 (4=1), impulse HS is blocked (it is unnecessary to block HC since the counter is blocked at 0).

A.1.4.6. COUNTER (N28, N35)

It is reset to zero at the beginning of each frame by a reset impulse (impulse c) in the clock section) for laws M255, A and M100. In law TD660, it is blocked permanently at zero again by its reset.

A.1.4.7. MEMORY GATES (N26, N27, N34, N33, N41, N40)

Depending on the law, M100 or TD660, the memory does not receive the same information coming from the same points which makes it necessary to gate each memory input.

A.1.4.8 THE MEMORY (N31)

It is supplied by +5v and -9v. The latter is created from the -15v by a zener diode (CR2). CR1, which has a higher power rating, conducts only when CR2 is short-circuited, thus protecting the memory until breakdown of CR2 (open circuit).

Addresses 0 to 127 are used for law M100, those from 132 to 211 (A7=1 for law TD660). Addresses 212 to 255 contain the same information as address 211 (namely 31) in order to avoid overflow.

It must be noted that memory fan-out is 1.

A.1.4.9 OUTPUT GATES (N8, N23,N23, N24, N30, N37

They permit to output with 7 wires regardless of the law by always taking the least significant bit (B8) as reference.

A.1.5. THE Δ→ PCM INTERFACES

The interface circuits permit the connection of the converter output with real PCM channel banks. Those circuits provided the interfacing of the D-1, D-2 or TD968 with the TD660 multiplexers. Three boards are used for interfaces:B-4, B-3 and B-1.

The selection of the PCM channel is done on board B4 by strapping one CHN, $1 \leq N \leq 24$ with the CHN wire (see Section A.1.5.1.4) this board also generates all the clocks needed for boards B-1 and B-3 as well as the DDMC master clock.

Board B-3 transforms the parallel PCM into serial PCM information. Board B-1 permits the various PCM channel bank operations.

A.1.5.1. BOARD B-4

This board generates all the clocks for boards B-1 and B-3 and the master clocks for the DDMC.

The selections are made with a switch located on the front panel, to obtain the function D1, TD660, TD968 or A.

-Position 1 is the TD968 command
-Position 2 is the A law command
-Position 3 is the D1 command
-Position 4 is the TD660 command.

A.1.5.1.1 MASTER CLOCKS

The square wave clocks are needed to correspond to each PCM system: Dϕ1, Dϕ2, and Dϕ3 (Figure A.6 p. 96).

For the D 1 multiplexer, Dϕ1 is created by an oscillator composed of gate 29 and the crystal X1 (Frequency 1.544MHz).

For the TD660, Dϕ2 is created by gate 30 and is adjustable by the potentiometer P2 (frequency 576KHz).

For the TD968, Dϕ3 is created by gate 37 and is adjustable by the potentiometer P3(frequency 768KHz).

The result of the selection by gate N1 gives one of the three clocks (Dϕ which is either Dϕ1, 2 or 3).

External clocks (Dϕ2T or Dϕ3T) could be connected (by a strap on the board) instead of Dϕ2 or Dϕ3.

A.1.5.1.2. DIGIT COUNTER

It is a sign counter composed of shift registers N2 and N3 and flip-flop N5.

The trailing edge of Dϕ shifts a "1" in the counter. The return loop (circuit N4 and N12) permits a count by 8 or 9 for the D1, 8 for the TD968 and 6 for the TD660 system.

A parallel loading order is sent to the digit and channel counter if a wrong load is detected by gates N9, N10, N29 and N39.

The digit counter generates all the signal D1, D2, D3, D4, D5, D6, D7, D8, D9, DF and CS2 (1.4) (Figures A.8, A.13 p.97 and p. 102) D1 through D9 are the time positions of the code bits and of the frame bits (Figures A8, A.13 p. 97, and p. 102).

A.1.5.1.3. CHANNEL COUNTER

It is a ring counter composed of registers N16, N17, N18, N19, N20, N21.

A count by 12 (TD968, TD660) or by 24 (D1) can be done by the return loop (circuit N15).

The counter is operated by a serial clock CS2 (see Section A.1.5.1.3.).

As for the digit counter, circuits N38 and N40 check the loading of the channel counter and order a parallel operation in the case of wrong loading.

Signals CH1 through CH24 are high during the time interval 1 to 24 corresponding to the PCM channel (see Figures A.8, A.13;p. 97 and p. 102).

These signals are at a 8kHz rate.

A.1.5.1.4. FRAME COUNTER

DF is the frame bit position, this position being variable with each PCM multiplexer.

D1 OPERATION.

When the channel counter is in the 24th position and when the digit counter is in the 8th a frame signal FR1 is generated by gate N33.

This signal FR1 is high during the frame digit duration.

TD660 OPERATION.

As above FR2=(CH12).(DF), where DF is the 6th position of the digit counter and CH12 is in the 12th position of the channel counter.

TD968 OPERATION.

The framing pattern is set every 12 frames (on frame 1). Thus a divide by 12 counter (circuits 32, 35, 41) generates a signal F3 at logic level "1" when it is the frame 1. The signalling bit is set on frame 6. Thus the framing counter generates SIG3 for frame 6 in the same way as F3 was generated for frame 1.

A.1.5.1.5.PHASE LOCK LOOP OSCILLATOR

This oscillator (circuits N14, N5, N13, N6) generates CF1, CF2, 8K and 64K synchronous with the loading signal(CH5+CH6) of the channel counter. (CH5+CH6) is chosen to have a pulse larger than 10µs in every case and to provide a delay for the compression board B5.

Since as the 8KHz clock of B5 is CH2, the delay between 8K and CH2 is 8 channel durations (at least 100 µs).

A.1.5.1.6. A LAW OPERATION

In the A law position all the counters work as for the D1 with the master clock Dϕ1.

This permits to get all the signals needed for writing and reading PCM data.

A.1.5.2. BOARD B-3

This board transforms the parallel PCM (Leads called PDA0 to PDAG) into serial PCM, DQ1, DQ2, DQ3 according to the table below:

	D1	TD968	TD660
Serial Output	DQ2	DQ3	DQ1

the DQ signals are in the DDMC code (See Figure A.7 P.97).

A.1.5.2.1 BUFFER 1

This board receives the parallel PCM data, PDA0, PDA1, PDA2, PDA3, PDA4, PDA5, PDA6 from compression board B5 which represents the amplitude of the signal in the DDMC code.

Those data are stored (clock CH9Da) in shift registers N12 and N13 through gates N9, N10, N11 according to the following table:

CIRCUIT N°	OUTPUT	D1	TD660	TD968
N 12	Q_0	PDA0	PDA0	PDA0
N 12	Q_1	PDA1	PDA1	PDA1
N 12	Q_2	PDA2	PDA2	PDA2
N 12	Q_3	PDA3	PDA3	PDA3
N 13	Q_0	PDA4	PDA4	PDA4
N 13	Q_1	PDA5	PDA5	PDA5
N 13	Q_2	PDA5	1	PDA6
N 13	Q_3	1	1	PDA5

PDAS is the sign of the signal after the buffer 30.

A.1.5.2.2. ZERO CODE SUPRESSOR

-Not used for TD660 operation.

-When the code 11111111 is detected a zero is subsituted for the least significant bit through gate N40.

In TD968 operation, only the precedent operation is done on the digit D7 if the channel is in a framing or a signalling frame (signal F3 or SIG3 at logic level 1) by means of gate 39.

The zero code detector is composed of gates N21,N28,N35.

A.1.5.2.3 BUFFER 2

The data are entered into buffer 2 (circuits N26, N27). The parallel clock is inhibited by CHN to prevent writing during the channel N chosen for transmission.

The serial clock is a 5,6, or 7 period square clock created by gates N1, N16, N31, N37, N38. (see length of the words, Figure A.6 p. 96).

A.1.5.3. BOARD B-1

A.1.5.3.1. D1 OPERATION

DQ2, by means of gate N30 is transformed into D1 code (Table 2). It was previously in DDMC code.

The sign SQ4 is substituted into the most significant bit (MSB) of the pattern through the gates 28 and 23.

The RBC (reference binary counter) creates the framing code 0101... This code is transformed into the frame patterns and is mixed with the sigalling pattern through gate 32.

Gates N36 and N39 mix the incoming PCM, the framing and the signalling pattern (coming out of gate 32) into a complete frame (see Figure A.9, p. 98).

The signal is stored in the flip flop 40 to prevent transition chances.

This unipolar PCM is transformed into a bipolar output (see Figure A.6, p. 96) by means of circuits N33, N19 and transformer T1.

PCM IOUT is the bipolar PCM output and is sent on the transmission line.

A.1.5.3.2. TD660 OPERATION

DATA TRANSMISSION

This circuit works like that of the D1 through gates N2, N9, N34, N36, N37, N38 and N39 with signal DQ1.

The output of flip flop N38 is transformed into the TD660 output level by transistors Q_1 and Q_2 (see Figures A.6 and A.8, pp. 96-97, for level and configuration). PCM2OUT is the PCM output and is sent on the transmission line.

CLOCK OPERATION

Dϕ is stretched through flip flop N33 to be a 100ns pulse. This pulse is transmitted to the line by means of circuits Q_3 and Q_4.

A.1.5.3.3. TD968 OPERATION

Signal Dϕ3 is sent to gate N10 to be multiplexed with the frame pattern.

The reference binary counter (registers N3, N4 and N5) provides the framing pattern 000001101101 which is multiplexed with the incoming data and the signalling bits by gates N24, N25, and N26.

The output of gate N25 is sent to the flip flop N40 used to prevent transition chances.

Circuits Q_7, Q_8, Q_9 and Q_{10} provide a unipolar NRZ (non-return to zero) PCM signal: PCM 3 OUT, which is sent to the transmission line.

CLOCK

Dϕ is converted by Q_{11}, Q_{12}, Q_{15} and Q_{14}, to be transmitted through the transmission line. After conversion Dϕ becomes Dϕ 3TOUT.

A.2 PCM TO DELTA CONVERTER

The PCM to delta part of the DDMC prototype is composed of 14 boards which can be subdivided into different parts:

- the interfaces
- the expandor
- the common linear PCM to digital delta function
- the CVSD decoder.

A.2.1. THE PCM →Δ INTERFACES

The interface circuits permit the connection of the DDMC input to the real PCM channel banks: The D-1, D-2, TD660. Three boards are needed to do the interfacing: T-1, T-3 and T-4.

A.2.1.1. BOARD T1

A.2.1.1.1. D1 OPERATION (SEE FIGURE 7 FOR LEVEL)

The PCM data, (leads PCMIR and PCMIT) are sent into a circuit composed of T1, Q1, CR2 and comparator 4.

Diode D1 gives a DC voltage equal to half the real value of the bipolar PCM. Diodes D2 and D3 rectify the bipolar signals to obtain a unipolar PCM compared, by means of comparator N4, to the DC voltage. The output of gate N11 is a unipolar PCM.

This output is sent into resonant amplifier Q_2, Q_3 and Q_6 tuned to 1.544mHz with inductances L1 and L2; a Schmit trigger squares the signal of this amplifier and gives Dϕ1, the master clock.

Flip flop N18 creates a unipolar PCM. The PCM transition coincides with the trailing edge of master clock Dϕ1.

The PCM signal and clock are sent to boards T3 and T4 to provide the frame synchronization.

A.2.1.1.2. TD660 OPERATION (SEE FIGURE 1 FOR LEVEL)

The PCM data (Lead PCM2R) are sent into equalizer Q_4 and circuits N16 and N17.

Amplifier N16 gives a DC voltage equal to half the peak value of the PCM and comparator N17 compares the PCM2 and DC signals.

Clock Dϕ2 is regenerated in the same way by circuits Q_5, N23 and N24.

The PCM bits and clock are sent to boards T3 and T4 to provide the frame synchronization.

A.2.1.1.3. TD968

The NRZ (no return to zero) unipolar (Lead PCM3R) is regenerated by circuit N33.

Clock Dϕ3R is regenerated by circuit N32 (see Figure 1 for levels). The output of flip flop N26 is a regenerated PCM.

The transition of the PCM coincides with the trailing edge of clock Dϕ3. The framing synchronization is done by boards T3 and T4.

A.2.1.1.4 COMMON PARTS

The 3 PCM signals are sent into gate N20 to be selected. The output PCM of gate N20 is rectified by gates N27 and N34. The common clock Dϕ (Dϕ1, Dϕ2 or Dϕ3) is stretched by circuit N28. Gates N40, N41 and N21 create a 6, 7 or 8 pulse clock during the CHN duration ($1 \leq N \leq 24$ for D1 and $1 \leq N \leq 12$ for TD968 or TD600.)

These pulses shift the PCM data for channel N into buffers N30 and N31. The data are held 125µs for the expandor (E_0 to E_6). The sign is stored in flip flop N35.

Signal 078 contains information for the TD968 only. A "1" value means the PCM is only 7 bits during a framing or a signalling frame.

A.2.1.2. FRAME SYNCHRONIZATION

A.2.1.2.1. PRINCIPLE

The counter board generates a frame signal (FR1, FR2, FR3) (Fig.A.8,9,10). When this frame signal is high, the PCM bit is checked and compared to the value of a Reference Binary Counter (RBC). The comparison result (CR) is stored (See Section A.2.1.2.3) in the correlator.

If CR is high ("1" level) and there are at least 3 "1" CR's among the last 5 CR's the counters (digit, channel and frame) are stopped by the off signal CO one period of Dϕ and reset in the frame position (A.2.1.2.2). New clocks are made until CR becomes low ("0" level).

If result CR is "0", nothing is done, the counter is not stopped and continues running.

Low CR result "0" is called a good CR.

High CR result "1" is called a wrong CR.

A.2.1.2.2. BOARD T3

This board is composed of a digit counter, a channel counter and a frame counter.

Circuits N7, N6, N30, N13, N26 and N39 give CF1, CF2, 8K and 64K the signal clocks for all the boards except T1, T3, and T4. This is a phase lock loop system used to obtain CF1, CF2, 8K and 64K synchronous with the PCM signal CHN-9 (A.2.1.2.2.2).

Signal CH -9 could be selected by strapping on board T3 when N value is changed (A.2.1.1.4). CH -5 (A.2.1.2.2.2) is a 8kHz signal for the expanding board delayed 5 channel durations from the chosen CHN (A.2.1.1.4).

A.2.1.2.2.1. DIGIT COUNTER (DC)

Master clocks Dϕ1, Dϕ2, Dϕ3 are selected by gate N1. The result Dϕ is sent to boards T1 and T4 and is also streched to be a pulse by circuit N8.

The digit counter is a ring counter composed of register N2, N3, N4 and gates N12, N5. Gates N12 and N5 provide a count by N6, N8, or N9 if in position D1, TD968 or TD660. The D1 function is command lead 2.

Th TD968 function is command lead 1.

The TD660 function is command lead 4.

Gates N9,N10,N11 and N29 are a zero detector,if the digit counter is not loaded properly. They create a signal order for parallel loading through gates N38 and N30.

In D1 operation the digit counter counts by 8 for each channel except channel 24. A count by 9 is provided for channel 24 (Figure 6).

In TD660 operation the digit counter counts by 6 (Figure 7).

In TD968 operation the digit counter counts by 8 (Figure 8).

This counter creates D1, D2,... D9, DF and CS2 (Figures 6,7,8 and Figures 3,4,5).

Signal CO (board T3) can inhibit Dϕ for one period to provide the frame detection (A.2.1.2.1.).

A.2.1.2.2.2 CHANNEL COUNTER (CC)

This counter is a ring counter, composed of shift registers N16, N14, N18, N19, N20, N21 and gate 40.

In D1 operation, the CC counts by 24 and in TD968 or TD660 operation by 12 by means of gate N40.

This counter is implemented by CS2 (A.2.1.2.2.1, Figures 6,7, 8). Signal CH- 5 is a 8kHz pulse needed for the expandor board. Signal CH- 9 is a 8kHz pulse needed for the phase lock loop oscillator. Signal CHN is needed to pick up the PCM data of channel N. N, can be selected between 1 and 24 for D1 operation

and between 1 and 12 for TD968 and TD660 operation.

This is done by a strap on the board itself.

The delay between CH-5, CHN and CH-9 should be respected to prevent transition chances (see section A.1.5.1.6. for explanation).

A.2.1.2.2.3 FRAME COUNTER

A.2.1.2.2.3.1. D1 AND TD660 OPERATION

Gate N28 creates FR1 when DC is in position 8 (signal DF) and CC in position 24 (CH24) (Figures 4 and 6).

Gate 28 creates FR2 when DC is in position 6 (DF) and CC in position 12 (CH12) (Figures 3 and 7).

A.2.1.2.2.3.2. TD968 OPERATION

It is a divide by 12 counter implemented by the signal CH1 (A.2.1.2.2.3) (circuits N35, N42 and N38).

The signal called IN78 is a signal which is high when the frame is a framing or a signalling frame.

F3 is a signal which is high during a framing frame.

SIG3 is a signal which is high during a signalling frame. (see Figures 5 and 8).

A.2.1.2.3. BOARD T4

A.2.1.2.3.1.COMMON SYSTEMS

Gate N2 creates FR3 from F3 and DF, FB3 is a 12 pulse signal which represents the position of the frame bits for the TD968.

Gate N9 selects FR1, FR2.or FR3 for D1, TD660 or TD968 operation. (see section A.2.1.2.2.4). The result FR is used to select the PCM frame bits from board T1.

The framing patterns for the D1 and TD660 are the same (Figure 1). The RBC1 is common (circuits N15, N23, N26, N29, N30, N31, N37). For the TD968, the RBC2 is composed of shift registers N38, N39, N40 and gate N13 (Figure 1 for frame pattern).

Gate N10 selects RBC1 or RBC2.

The principle of operation was developed in Section A.2.1.2.1.

A.2.1.2.3.2 CORRELATOR (COR) (SEE SECTION A.2.1.2.1 FOR PRINCIPLE).

A.2.1.2.3.2.1 GENERAL

The correlator (circuits N24, N31, N32, N33, N34, N25) counts the number of wrong CR's (see Section A.2.1.2.1) in 5 CR's.

The incoming PCM (lead PCM) is compared with BRC1 or BRC2 by means of gate N3; gate N21 selects the result CR during frame time (see sections A.2.1.2.3.2.2., A.2.1.2.3.2.3.).

CR is entered into COR by means of circuit N42, the clock is a pulse validated when FR is high (circuit N9).

Signal CO is high when there are at least 3 wrong CR's in the correlator and the last CR being entered is wrong.

This CO signal (high lead) is able to stop the digit counter for one period of $D\phi$ when in the "out of frame" condition.

"Out of frame" condition is declared when 3 CR's out of 5 are wrong.

When the frame has been lost and if the CR is not good, the frame is considered being lost. To be in the frame condition, at least one good CR is needed (see Table A.2).

N° of wrong CR's in the COR	Last CR entered into COR: $\hat{CR}$	CO	Frame condition
0	good	low	in
1	good	low	in
1	wrong	low	in
2	good	low	in
2	wrong	low	in
3	good	low	in
3	wrong	high	out of
4	good	low	in
4	wrong	high	out of

TABLE A.2.

When CO is high the digit counter (Section A.2.1.2.2.1) is stopped and signals FR stay high and permit a check of the following PCM bits as if they were frame bits.

A.2.1.2.3.2.2 TD660 AND D1 RBC1 (REFERENCE BINARY COUNTER)

The reference binary counter is a counter which contains the frame reference pattern (0101...).

Flip flop N31 changes state every frame to provide the framing pattern.

When an "out of frame" condition is determined, CO opens gates N37, N30, N23 and N26 and the value of the PCM digit is entered by means of these gates, into flip flop N31.

If the RBC value and the PCM bit in check are the same, CR is necessarily good. Thus CO goes low (see Table A.2) and the digit counter runs again. This reset of the RBC1 is needed to prevent the RBC1 from being at the opposite value of the frame pattern.

Gate N10 selects RBC1 or RBC2 output.

A.2.1.2.3.2.3. TD968 RBC2

Since the frame pattern occurs every 12 frames and is 000001101101, the RBC2 is a shift register (N38, N39, N40) clocked by FR3 (see Section A.2.1.2.3.1).

Gate N10 selects RBC1 or RBC2 output.

When an "out of frame" condition occurs, CO goes high and the digit counter is stopped, the digit counter can run again only when a CR is good.

A.2.1.2.3.2.4 SPECIAL FEATURES

Circuits N35,N36,N24,N42 are needed when the COR is filled with 5 wrong CR's and when FR is low (this could happen when the DDMC is switched "on") to prevent the counter board T3 from being stopped and to prevent frame synchronization.

A.2.1.2.3.2.5 ALARM FEATURE

A red light, on the front panel, provides a visual alarm for the "out of frame" condition. When CO goes high, flip flop N35 changes state and transitors Q1 and Q2 are satured: the light goes on. An incorporated push button is provided with the light. This buttom resets flip flop N35 in the off condition. If pushing this button makes the light go off, frame has been found.

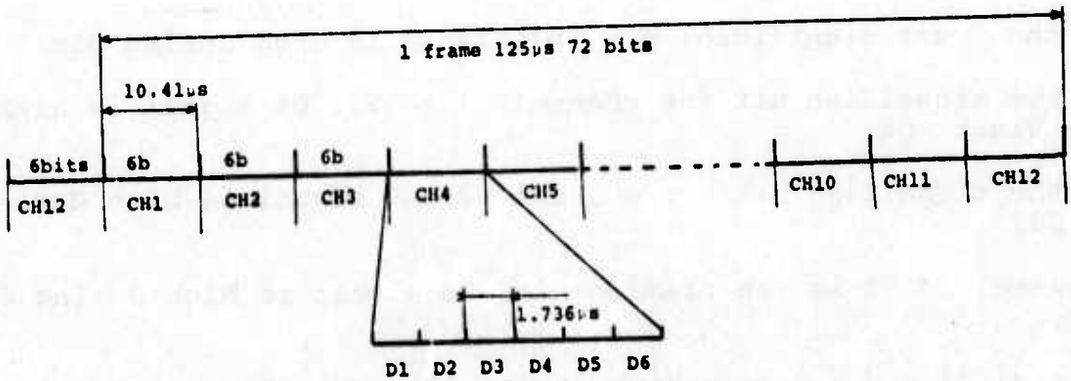
	D1	TD968	TD660
SAMPLING FREQUENCY	8kHz	8kHz	8kHz
COMPANDING LAW	μ100	μ255	2 segments law
OUTPUT LEVELS	bipolar logic "1" ±6V±1V logic 0 0V bipolar	NR2 unipolar logic 1 +6V ±1V 0 -6V ±1V open line	unipolar logic 1 0V± 0.4V 0 -2V ± 0.4V
LINES	balanced 100Ω±10%	unbalanced 78Ω±10%	unbalanced 91Ω±10%
BIT RATE	1.544 kb/s	768Kb/s	576kb/s
PULSE WIDTH	0.65μs	1.302μs tr ≤ 162μs tf ≤ 162μs	1.736μs tr = 20μs tf = 120μs
BITS/WORD	7	8,7 on framing and signalling	6,5 for channel 12
BITS/FRAME	193	96	72
NUMBER OF CHANNELS	24	12	12
TIMING	1.544kHz not transmitted	768kHz transmitted square wave 50% ±6V ± 1V trailing edge coincides with center of data output interval	576kHz transmitted base -2 ± 0.4V peak 0 ± 0.4V pulse wicth 80 to 150μs leading edge leads the PCM transition by 0 to 80μs
FRAMING	one bit between LSB and signalling on the last channel of each frame pattern:0101...	one bit substituted to the least significant bit of each channel every 12 frames pattern: 000001101101	one bit substituted as the least significant bit of the last channel of each frame pattern:0101....
SIGNALLING	Last digit of each channel	one bit substituted as the least significant bit of each channel every 12 frames with a shift of 6 frames with a with framing	

FIGURE A.6.- PCM channels banks requirements.

		D1	TD968	TD660
PCM CODE	POSITIVE	MSB LSB level 1 111111	MSB LSB 1 0000000	MSB LSB 1 1 1 1 1 1
		1 000000	1 1111111	1 0 0 0 0 0
		0 111111	0 1111110	0 1 1 1 1 1
	NEGATIVE	0 00001	0 0000001	0 0 0 0 0 0
		STRAIGHT BINARY	STRAIGHT BINARY	STRAIGHT BINARY

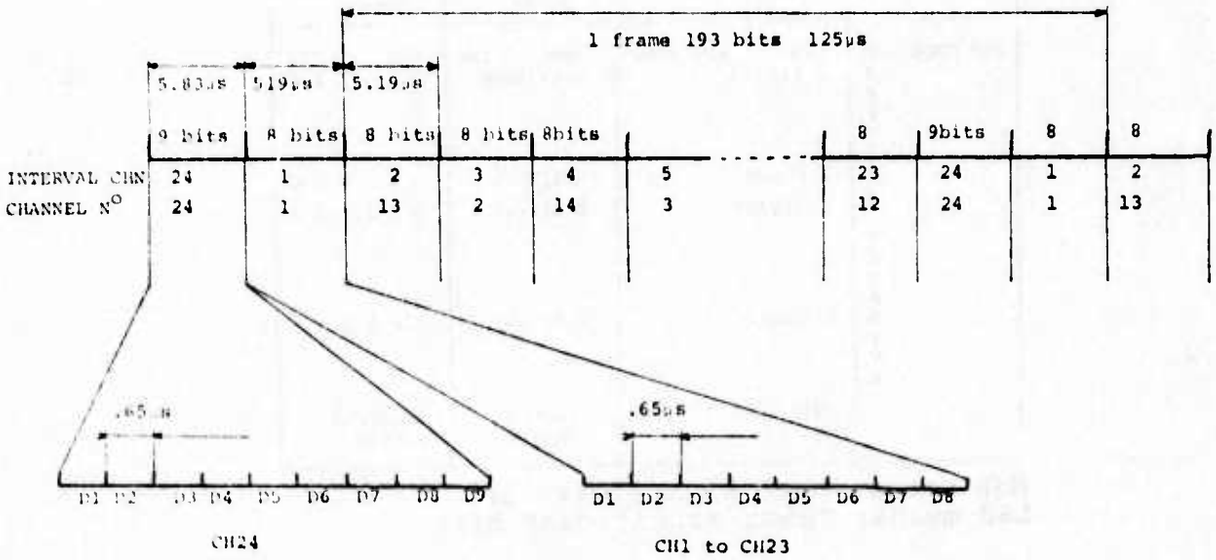
MSB means: most significant bit.
LSB means: least significant bit.

FIGURE A.7.- PCM codes.



D1 through D6: coding bits
D1 is the most significant bit
D6 is the least significant bit except on channel 12
On channel 12 D6 is the framing bit while 05 is the least significant bit
FR2 is high during the framing bits (CH12 digit DF)
DF=D6
base frequency 576kHz

FIGURE A.8.- TD 660's: frame configuration.



D1 is the most significant bit (sign bit).D1 signal is high during digit D1.

D7 is the least significant bit. D7 signal is high during digit D7.

D8 is the signalling bit for channels 1 to 23. D8 signal is high during digit D8.

D9 is the signalling bit for channel 24. D9 signal is high during digit D9.

For channel 24 DS is the framing bit. D8 signal is high during digit D8.

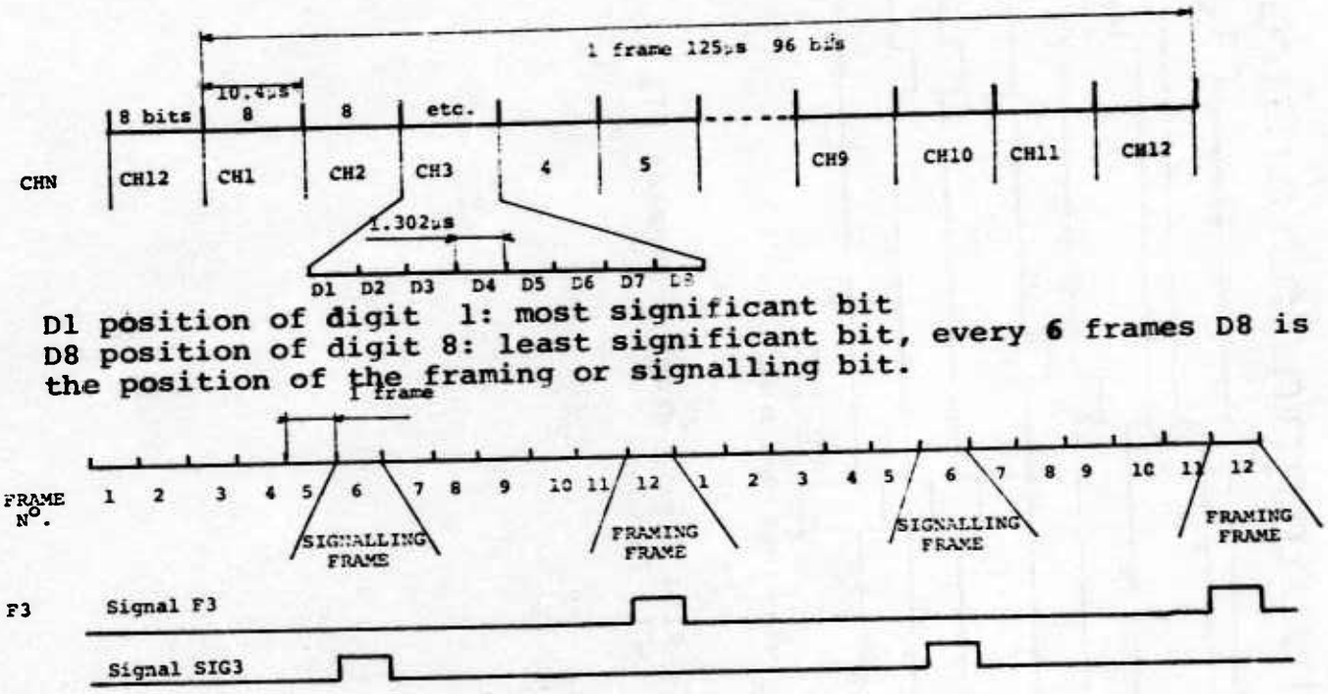
CHN signal ($1 \leq N \leq 24$) is high during interval CHN ($1 \leq N \leq 24$).

FR1 is high during the frame bit (channel 24 dig. DF).

DF=D8

Basic frequency 1.544 mHz

FIGURE A.9. - D1's frame configuration.



D1 position of digit 1: most significant bit
D8 position of digit 8: least significant bit, every 6 frames D8 is the position of the framing or signalling bit.

Framing pattern 12 bits 000001101101 at DF instant when F3 is high.
Signalling bits at DF instants when S163 is high.
FR3 is a 12 pulse signal corresponding to the 12 framing bits.

FIGURE A.10.- TD 968's frame configuration.

TIMING DIAGRAM BOARD B1, B3, B4, T1, T3, T4 FOR EXAMPLE CHN=CH1 MEANS THAT CHANNEL ONE IS CHOSEN AS TRANSMITTING AND RECEIVING CHANNEL.FRONT SWITCH IS IN D1 POSITION.

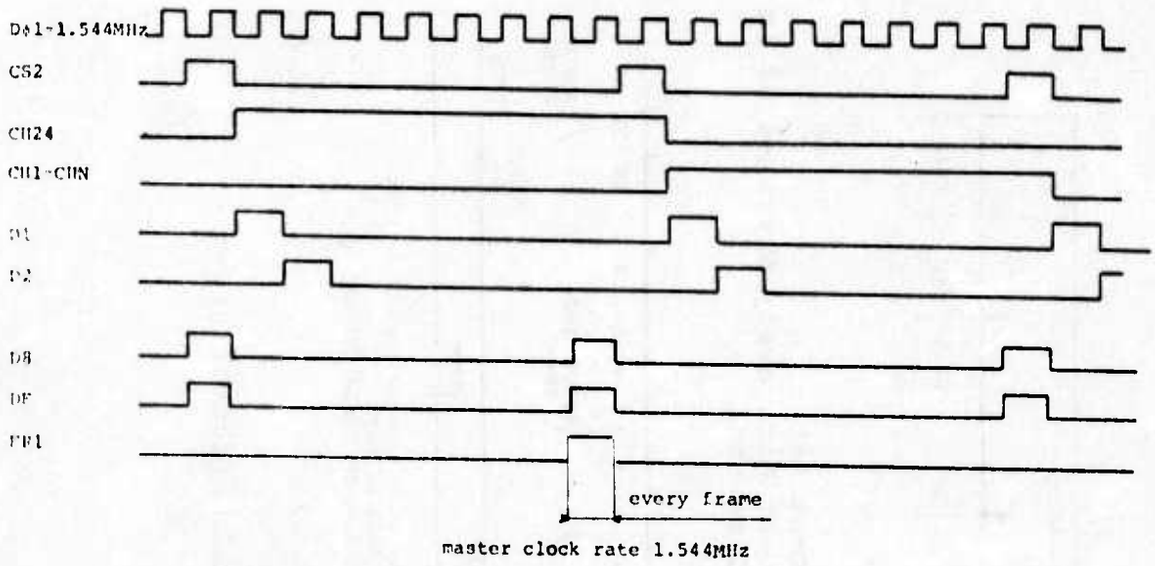
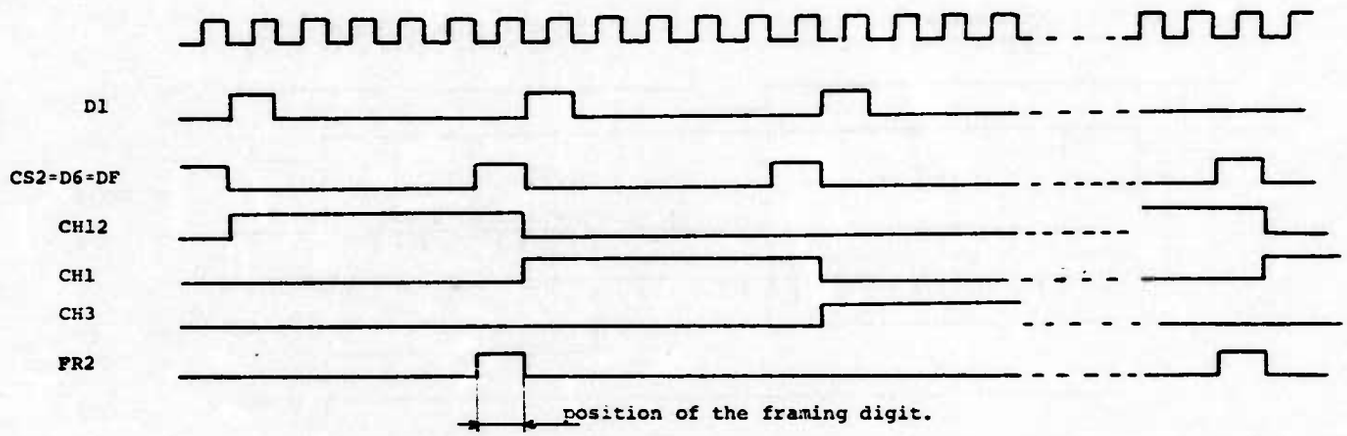


FIGURE A11.- DI's Timing diagram (boards B1, B3, B4, T1, T3, T4).

TIMING DIAGRAM BOARD B1, B3, B4, T1, T3, T4, TD660.



FR2 is high during DF for channel 12

FIGURE A.12.- TD 660's timing diagram (Boards B1, B3, B4, T1, T3, T4).

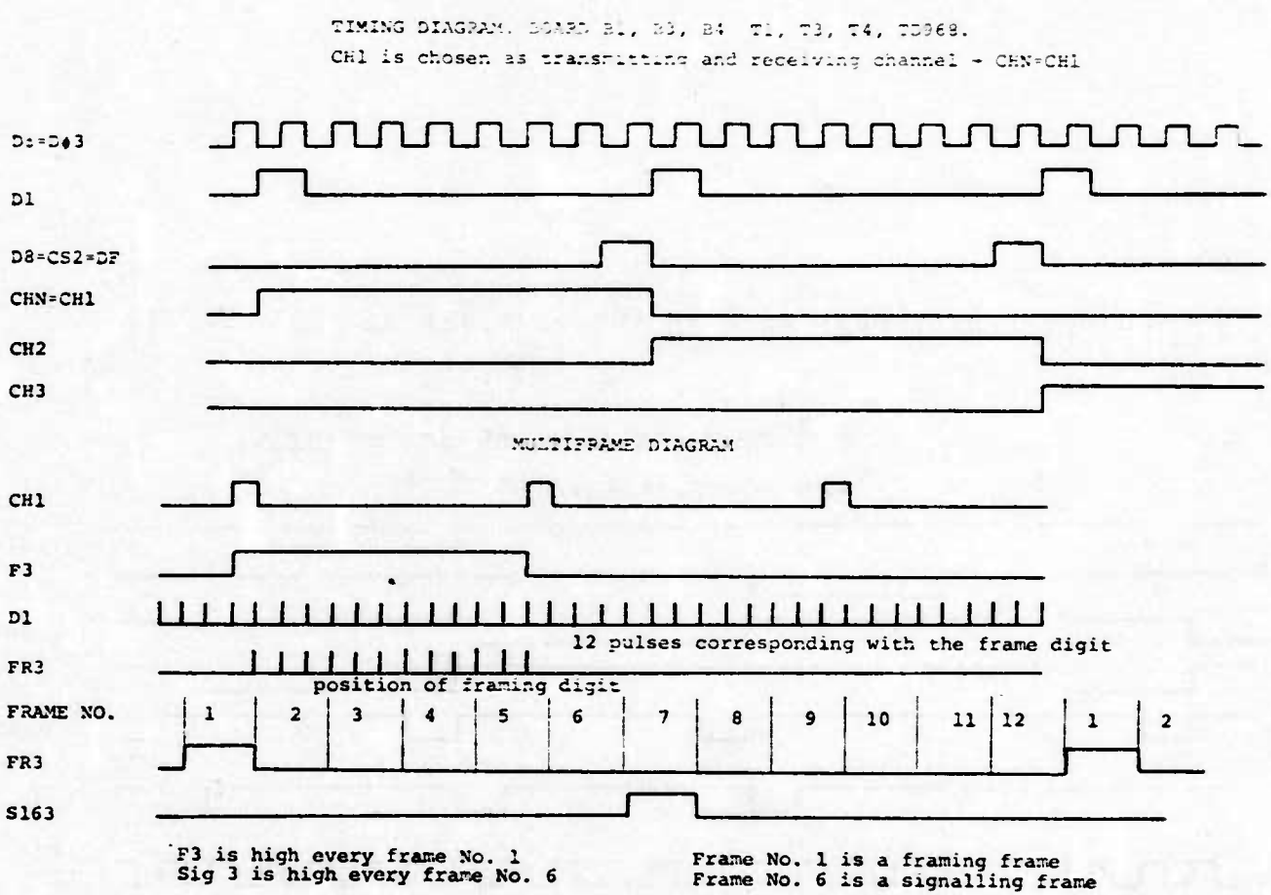


FIGURE A.13,- TD 968's timing diagram (Boards B1, B3, B4, T1, T3, T4

A.2.2. THE EXPANDOR FUNCTION

This expansion from compressed to linear PCM is done by one board T-6 and contains the four expansion laws: the μ-100, μ-255 or TD968, A and TD660.

A.2.2.1.1. CLOCKS

The board contains four different clocks which vary according to the expansion laws.

-8kHz work clock. One of the two signals according to the expansion law.

-8kHz, output register

-14 impulses at 1.5MHz

-Repetition at 8kHz

-Fast clock at 1.5MHz

8kHz work clock (N30)

This clock is used to create two other signals, one identical but delayed, the other an impulse on the trailing edge generated by the set-up (Figure A4, A5): these three signals exist for all the laws except for the impulse which is blocked in law TD660 (4).

Fast clock (N22 - N23) -CF

CF and the 8kHz are synchronous but their phase is ill defined. The situation where a CF trailing edge occurs too soon after (or at the same time as) an identical 8kHz edge must be avoided.

For this reason, the D flip-flop is reset to zero (preceding "c" impulse on its reset) at each trailing edge of the 8kHz. The first CF impulse cannot therefore be switched to the work register since $\overline{Q}=1$. Q will however become equal to 1, operating the switch and blocking it in this position for the rest of the 8kHz period.

In law TD660 (4), the flip-flop is constantly blocked at zero by its reset in order to avoid sending the fast clock into the work register.

Output clock -M1 and CSI

M1 serves to load the output register in parallel and CS1 (14 impulses) to unload it in series.

A.2.2.1.2 MEMORY (N2)

It is supplied by + 5V and - 9V sources. The latter is created from the - 15V by a Zener diode (CR1). CR2 which has a larger power capacity conducts only when CR1 is short circuited, thus protecting the memory until the breakdown of CR1 (open circuit). A voltage higher than - 9V would not damage the memory but could change its contents.

Law M100 uses addresses 0 to 63, law TD660 addresses 80 to 95. The remaining memory fan-out is 1.

A.2.2.1.3. DECOUNTER GATES (N8 - N15)

In laws M255 and A the signal comes directly from inputs E4-E5 and E6. In law M100, 3, it comes from outputs D4-D3-D2 of memory (N2).

A.2.2.1.4. DECOUNTER (N11, N12, N16, N27, N18, N23, N23)

Loading

At the time of the trailing edge of the 8kHz, the impulse "C" discussed in A.2.2.1.1. lets the signal pass on the "set" and "reset" of the flip flop. The signal must be available before the impulse. Two cases are possible: the signal is 1 or 0. Thus Q = 0; Thus Q = 1.

In the case where the signal is 1, so must be preponderant. For this, the impulse "C" must be longer than the transition time Δ of a gate.

Decounting

It is performed as long as one of the 3 most significant bits is 1 in law M255 (1), or as long as one of the 2 most significant bits is 1 in laws A (2) and M100 (3).

Each decounting impulse is sent to the work register serial clock. In laws A and M100, a supplementary shift impulse is sent into the work register before the decounter begins to function.

A.2.2.1.5. WORK REGISTER GATES (N13,N14,N15,N19,N20,N21,N26,N27,N28)

For each work register position it is necessary that:

CASE; M255: 1 for 8 bits, 0 for 7 bits $\overline{(M7)}$
A : 0
M100: 0
TD660: E4

CASE 2

M255: $\overline{E0}$ for 8 bits, 10 for 7 bits.
A: $\overline{E0}$
M100: D8
TD660: 1st segment (E4=1): $\overline{E0}$
2nd segment (E4=0): 0

CASE 3

M255: $\overline{E1}$
A: $\overline{E1}$
M100: D7
TD660: 1st segment (E4=1): $\overline{E1}$
2nd segment (E4=0): 1

CASES 4 and 5

A and M255: $\overline{E2}$ for position 4, $\overline{E3}$ for position 5
M100: D6 for position 4, D5 for position 5
TD660: E2 for position 4, E3 for position 5 1st segment
D8 for position 4, D7 for position 5 2nd segment

CASE 6

A: $\overline{E4}+\overline{E5}+\overline{E6}$
M255: 1
M100: D2+D3+D4
TD660: 0 for 1st segment
D6 for 2nd segment

CASES 7,8,9,10

M255: 0
A: 0
M100: 0

TD660: 0 1st segment
D5, D4, D3, D2, 2nd segment.

A.2.2.1.6 WORK REGISTER (N32.N32.N33.N34).

It is loaded in parallel by the 8kHz. The data must be input into the set-up at least 1.5µs before this loading because of the memory response time.

A.2.2.1.7 OUTPUT REGISTER (N38.N39.N40.N41.N42).

Its in-parallel loading clock must lay by at least 10µs that of the preceding register. The 14 serial unloading impulses (CS1) must not occur less than 50ns after the M1 trailing edge.

A.2.3. THE COMMON LINEAR PCM TO DIGITAL DELTA FUNCTION

This part is composed of three boards T-7, T-8 and T-9; its main function is to provide the linear PCM information at the correct delta rate at the digital delta input part. It is a rate converter from 8kHz to delta rate 16, 19.2, 32 or 38.4kHz.

It contains:

- a 64kHz counter, a digital sign adjuster,
- a linear interpolator and a delta counter,
- a second order digital filter at 64kHz.

A.2.3.1. BOARD T_7: THE 64 kHz COUNTER AND DIGITAL SIGN ADJUSTER

This board is composed of the interpolator input gates control and of the 64kHz counter.

The expanded word coming out of the expandor board by means of CS1 (N32, N26) passes directly through gate N10 in case of the A and M100 laws. For the M255 law, 16.5 is substracted from it, by means of registers N3 and N4 and adder N1, and in case of TD660, it is be multiplied by 12.1875. In fact it is multiplied by 12.1875/16 (i.e.2^4) (adders N2, N15, N15, BR8, N9) and then multiplied by 16, four shifts (N24) being eliminated from CS1 (N24, N25).

Then the sign of the binary word, SI, permits to recover the full sine wave (2's complement: circuits N13, N27, N5) before entering the linear interpolator I.

The clocks and timing signals necessary for the interpolator and 2nd order filter are generated on this board by the 64kHz counter. This serial counter (N17, N18, N19, N20, N21) is reset by the M_2 impulse created on each negative edge of the 64kHz clock. It is filled with one ("1") by means of a fast clock CF_1 which stops (N23) on the value 20 of the counter (N11).

The two frequencies 8kHz and 64kHz are perfectly in phase. M_1 is the impulse created on the negative edge of the 8kHz frequency (N5). V is a variable in the "1" state during the first period at 64kHz between two successive impulses M_1.

CS1, CS2, CS3, CS4 are serial clocks necessary for the interpolator; CS5 is the serial clock of the 2nd filter (N24, N25, N11, N27, N32). CS1 is a test point to visualize the interpolator output (N25, N34).

For more details, see the timing diagram Figure A.14.

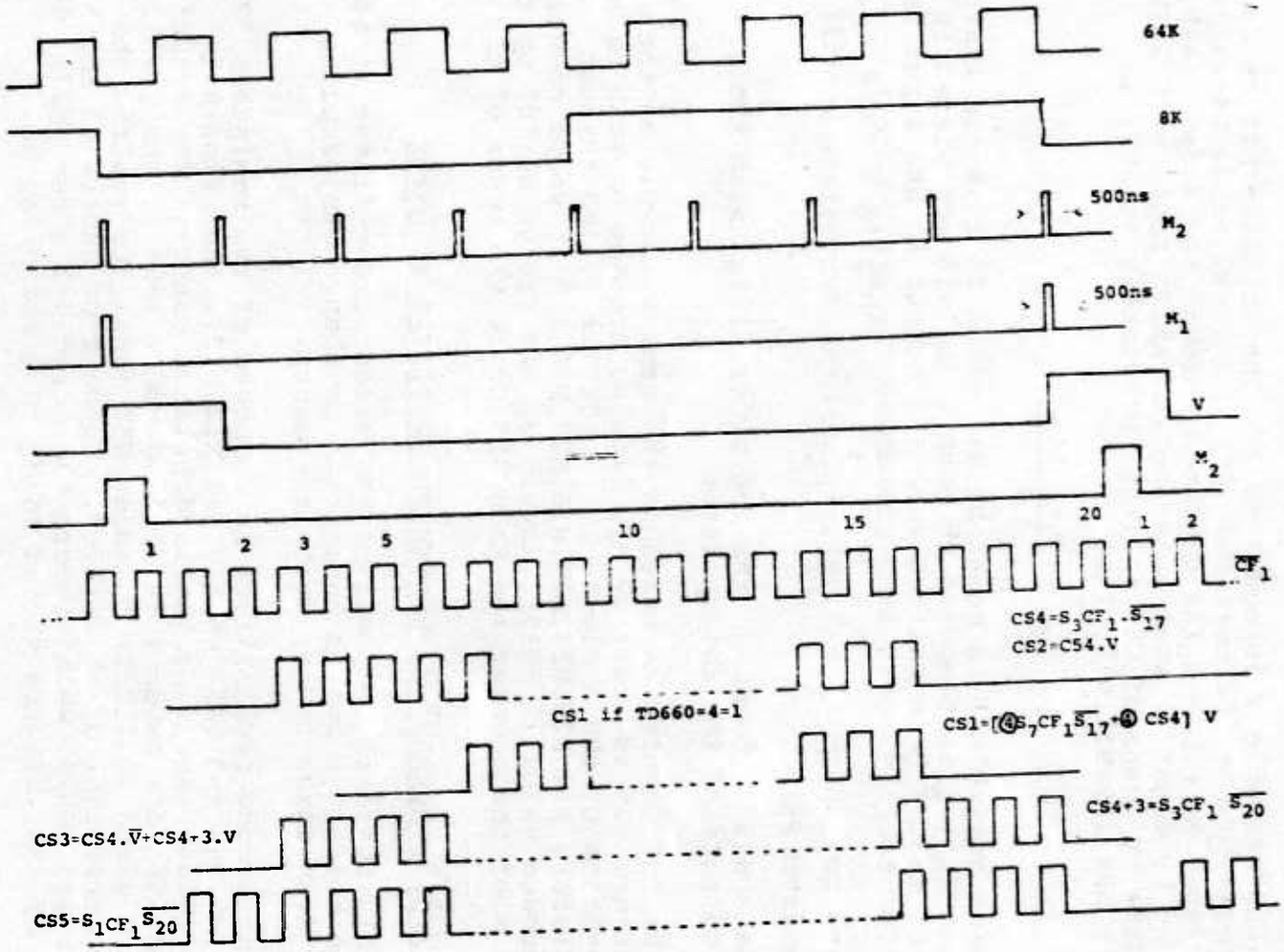


FIGURE A.14-T7 timing diagram.

A.2.3.2. BOARD T-8: LINEAR INTERPOLATOR AND DELTA COUNTER

This board is composed of the linear interpolator and of the delta counter. Two phases have to be considered for the interpolator computing.

When variable V is equal to 1: the incoming bit stream X_{n+1} is input into shift register SR2 (N2,N3,N4,N4)while the difference $X_{n+1} - X_n$ is computed through the adder N14(6,7) and divided by eight(8) when entering the shift register SR3 (N16, N17,N18,N19) by means of CS4 + 3. X_n, previously in SR2, is shifted in SR4 (N9,N10,N11,N12)

$$\frac{\Delta}{8} = \frac{X_{n+1} - X_n}{8}$$

When variable V is equal to 0: gates 21,20,6 are inhibited so that $X_n + \frac{\Delta}{8}$ is computed through adder N14 and placed in SR4 by means of CS4. $\frac{\Delta}{8}$ is shifted from SR3 output to SR3 input to be ready for the $\frac{\Delta}{8}$ next step computing $(X_n+\frac{\Delta}{8})+\frac{\Delta}{8} = X_n + 2 \cdot (\frac{\Delta}{8})$

And so, up to $X_n + 7\ (\frac{\Delta}{8})$, X_{n+1} the next step, is still in shift register SR2.

Gate N35 feeds the 2nd order filter with the sequential outputs of the interpolator.

The "∧" Counter is based on the same principle as the 64kHz counter. It is reset by M_Δ, impulse created on each negative transition of the ∧ clock. "1" is filled through shift registers N22,N23,N24,N25,N26,N27,N28 and it stops counting on the decoded value 25 (N15). Every S_x has the value "0" up to the value x of the counter and then "1" up to the reset of the counter.

A.2.3.3. BOARD T-9, SECOND-ORDER FILTER AT 64kHz

This board is composed of the second-order filter at 64kHz and of the holder, a buffer permitting to change the sampling frequency from 64kHz to any delta frequency.

The second-order filter is composed of two registers SR6 (N2,N3,N4,N5,N6) and SR5 (N9,N10,N11,N12,N13), the principal adder N27 (BR34) receiving the interpolator output. The outputs Q_2(N13), Q_1(N6) are gated (N14,N21) to adder (BR31), and Q_2(N12), Q_0(N13) are gated (N14,N21) to adder N32 (BR31) to realize the feedback coefficient of the filter. Outputs of adders N1 and N32 feed adder N33 (BR34) which enters the principal adder (N27). The sign bits of SR5, SR6 are stored on M_2 in D flip flop N8.

On each negative edge of the delta frequency F_Δ, a pulse M∧ is created (N29, R_1,C_1) and the binary word in the buffer (N28, N16,N17,N18,N19) must be transfered in parallel in the shift

register SR7 (N20, N23, N24, N25, N26). SR7 is the input of any digital delta CVSD: to enter the right length binary word at the right time, four serial clocks are gated (N22, N21).

On each negative edge of the 64kHz, the binary word computed in the second order filter must be transfered in the buffer. As there is no phase or frequency relation between 64K and F_Δ, a system creates 2 clocks, very near 64K and F_Δ, which prevents negative edges from being synchronous within 20 ns (N29, R_2, C_2, N35, N15, N14, C_4).

A.2.4.1. THE DIGITAL DELTA CODER FUNCTION

A241 The digital delta coder function General description	16kHz	19.2kHz	32kHz	38.4kHz
The digital CVSD system at------ is composed of	16kHz	19.2kHz	32kHz	38.4kHz
A low-pass first-order filter with a shift register of---	12bits	16bits	16bits	18bits
A feed back loop Δ composed of- an identity detector comparing three successive Δ bits and driving the input of a syllabic filter with a shift register of--- preceeded by an adding with a shift register of-------- and followed by an adding with a shift register of--- a multiplier by ± 1 giving the algebric increase which is then summed in an integrator with a shift register of----------	12bits 4bits 4bits 14bits	16bits 8bits 8bits 17bits	16bits 4bits 8bits 17bits	18bits 4bits 8bits 22bits
The low-pass filter, the syllabic filter and the integrator are three first-order filters the loop coefficients are realized respectively by---------	0,1,1,serial adders	1,2,3,serial adders	0,3,2 serial adders	1,2,2 serial adders
The different clocks driving the registers come from the same fast clock. For every register the sign is made in memory to be sent by a control gate so that the serial calculation is well defined until the last serial shift. In the case of the syllabic filter the sign memory does not exist, because the sign stays plus.				

The digital delta codec function

A.2.4.2. DIGITAL CVSD AT 16KHZ

A 24? Digital CVSD at 16kHz (realized on Board T10)	CIRCUIT NUMBERS
Low-pass filter	
main adder	1 BR2
shift registers	3,4,5
memory for sign	2
the output is sent toward main adder	$Q_1(5)$
	14, 20
Comparator of the integrator output with followed by memory for sign and A register with the identity detector	8 BR15
	9
	10
	24,17,11
Adding register at syllabic filter input	6
Syllabic filter	
main adder	18 BR25
shift register	19, 27, 28
the outputs are sent toward adders	$Q_3(28)$ $Q_1(27)$
	26 BR25, 18
Adding register at syllabic filter output	16
with adder	23, BR9
Multiplier by $\pm$ 1	29, 24 and BR15
Integrator	
main adder	22 BR15
shift register	32,33,34,35
memory for sign	30
outputs are sent towad adder	Q(35), $Q_1(34)$, 20,29 31, BR30
Clockn	12,13,20

Digital CVSD at 16KHz.

A.2.4.3. DIGITAL CVSD AT 16 KHZ

A243 Digital CVSD at 19.2kHz, 32kHz, 38.4kHz For these three frequencies the realization is made on two boards called boards A and B. Boards A respectively T11, T13, T15. Boards called boards A and B.	19.2kHz T11	32kHz T13	38.4kHz T15
A2431 Low pass filter			
main adder	1 BR2	2 BR1	1 BR2
shift register	3, 4, 5, 6	3, 4, 5, 6	3, 4, 5, 6,
sign memory	2	1	2
the outputs	Q_2 (5) Q_3 (6)	Q_1 (6)	Q_2 (7) and Q_3(6)
are sent towards the adder	11 BR18	2 BR1	12 BR11
Comparator	8 BR9	23 BR22	8 BR15
between outputs of the low pass filter and the integrator	9	19	16
with the memory flip flop	10	24	12
Δ register	16, 17, 20, 23	20, 21	17, 18
with the identity detector	13, 14	7	10
Adding register at syllabic filter input			
Syllabic filter			
main adder	19 BR18	14 BR22	22 BR15
shift register	25, 26, 27, 28	15, 16, 17, 18	24, 25, 26, 28
the outputs	Q_0 (27) and Q_2 (28)	Q_1 (18) and Q_2 (16)	Q_2 (26) and Q_0 (26)
are sent toward the adder	35 BR34	13 BR19	32 BR30
in the same way the outputs	S (35) and Q_2 (26	Q_2 (15) and Q_1 (15)	Q (28) and S(32)
are sent toward the adder	33 BR34	12 BR10	32 BR11
and the outputs of these			
adders towards the adder		11 BR10	
Adding register at syllabic filter outpur	31, 32		34, 35
with the adder	30 BR29		33 BR11
The 20 inputs-outputs of this board A deal with the input signal, the Δ output signal, the "S_i" signals of the counter, the M_Δ and F_Δ signal, the test-points FE12 and FS12 as well as the connections with board B, that is to say the clock signals, and the two connections: IC (integrator-comparator) and SL (syllabic filter and logic)			

Digital CVSD at 16 kHz

Boards T12,T14,T16

A 2432 Boards T12, T14, T16	19.2kHz T12	12kHz T14	38.4kHz T16
Adding register at syllable filter output---------- with the adder------		12,13 11 BR10	
Multiplier by $\frac{1}{4}$ ----------	37	8,9,14	8,20
Integrator main adder----------	25 BR39	14 BR5 set and reset	1 BR2 set and reset
shift register------	26,11,12,13,14	1,2,3,4	3,4,5,6,7,21,2
sign memory--------- the outputs--------- are sent toward the loop adder---------- in the same way the outputs---------- are sent toward the loop adder---------- and the outputs of these two adders toward the adder----------	26 $Q_3(14), Q_3(13)$ 27 BR41 $Q_1(13) Q_3(12)$ 40 BR41 38 BR39	6 $Q_3(4)$ $Q_2(3)$ 7 BR6 $Q_2(2)$, Q(7) 15 BR10	2 $Q_0(7)$, $Q_1(6)$ 19 BR18 Q(21), S(19) 10 BR18
Clocks ----------	9,10,23	16,17,18	23,24,9
The inputs-outputs of this board deal with these connections between boards A and B, the N_1 signal and the "S_1" signal of the counter the test-point 112 as well as the clocks for the first board.			

Boards T12,T14,T16.

A.2.5 THE CVSD DECODER

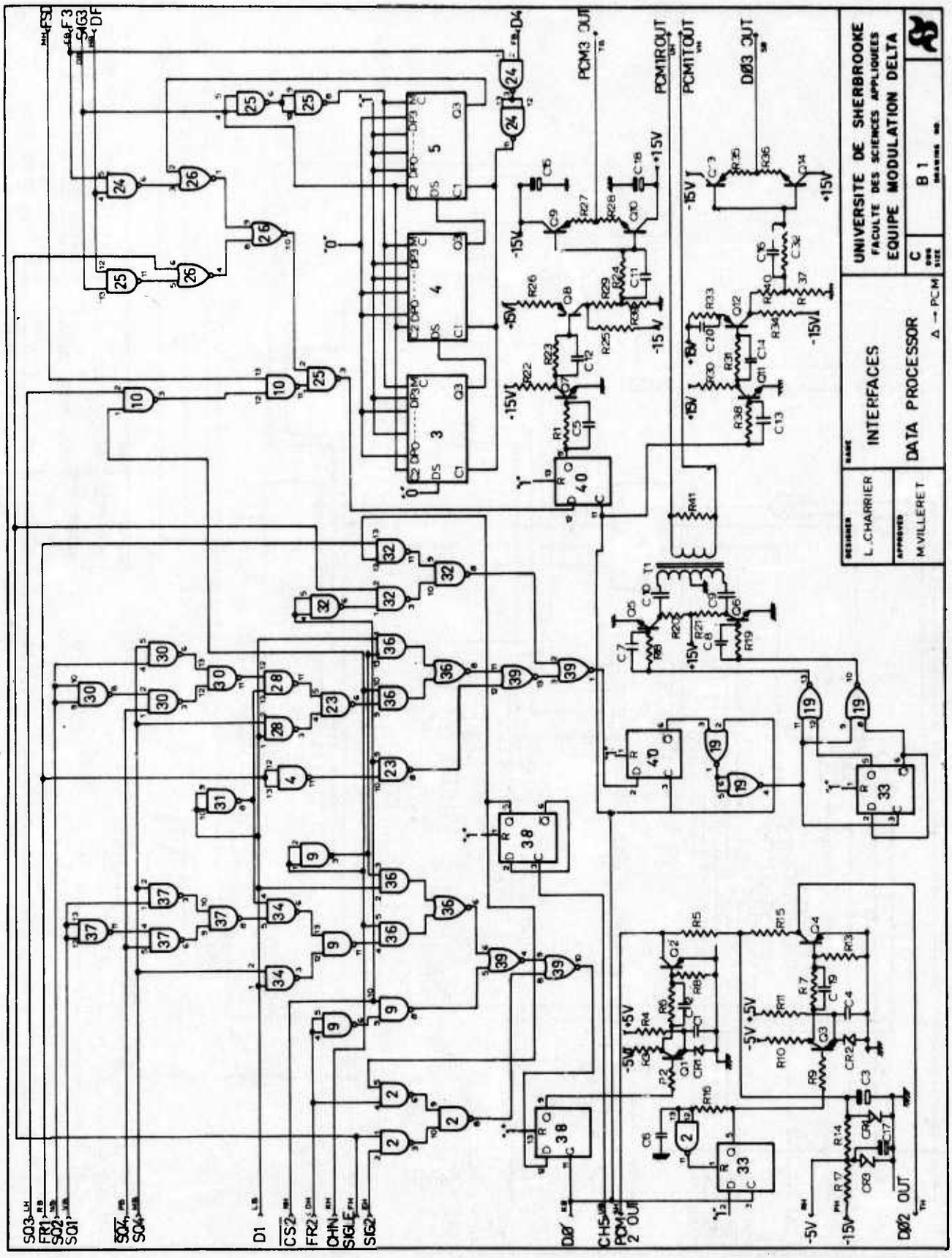
The CVSD decoder is built on the same board as the CVSD coder as it was mentioned in Section A.1.1.

APPENDICES B AND C

	B1	B3	B4	B5	B6	B7	B9	B8	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20	B21	B22
DH	FR2		4	3		2^{12}	S4	CO32	S16			Δ	$\overline{CS114}$			Q2	S20			DS	MOD
EH	SIG2	PAD4	5	AM100		2^{13}	S3	$\overline{CS32}$				FΔ2	P			CS133	A	Δ			SF1
FH	SIGLE	PAD3	1	1		2^{6}	S1	$\overline{CS38}$				CS111	A				Q'O			S107	AUDIO IN
HH		PAD2	DØ3T	2		2^{2}	S2	CO19		CS145			CS113	D	Q1	S	S26	FΔ2	$\overline{JS23}$	S23	-15V
JH	+15V	PAD1	DØ2T	M255		2^{4}	S5	CO38	MΔ			S8	S7	C	Q2		S16		J	O2	+15V
KH	CHN	PADO	D5	4		2^{-2}	S6	$\overline{CS16}$				S10	S14	S24	MΔA		$\overline{S135}$	S8	S	S16	
LH	DQ3	PAD5	DØ	TD		DE	S7	CO16	Δ	SF145	SF147	CS110	S20	S22	SF132		S134	S	CS105	O3	SFM
MH	$\overline{SFD}$	CH9	D1			S	S8	$\overline{DS16}$	S1		MΔ	S12	$\overline{MΔ}$			O1	Q"2	S10	S16	Q0	Δ
NH	$\overline{CS2}$	D4		CS		SG	S9	$\overline{DS19}$	S6	A	CS147	S14			Δ	DS	MΔB	$\overline{MΔ}$	$\overline{CS106}$	S26	
PH	-15V	3	$\overline{CF2}$	CH2		M1	S10	$\overline{DS32}$	FΔ2	S21						OO	MΔA	EQ3	S24	$\overline{S106}$	
RH	-5V		D4			M255	S11	$\overline{DS38}$		QO			S25	S1	FΔ2	S26	S22	S3	$\overline{MΔ}$	SF108	FΔ1
SH	PCM2 OUT	PAD6	DF			AM100	S12	CW		T				S2	S5	S16	CS136		EQ3	CS108	FΔ2
TH	DØ2OUT	1	64K			1	S13	S3120		B						S23	SF136		DS		
UH	PCM1R OUT	4	8K			M2	S14	M2		S18	$\overline{DS16}$	CS112		$\overline{DS19.2}$		MΔB	Q'2		CS106		BJI
VH	PCM1T OUT			-15V		4	S15	CR		S14?		$\overline{MΔ}$		$\overline{MΔ}$			DS'		SF106		TJC
AB							S16							CS111							
BB												S16		CS110							
CB			$\overline{CF1}$	$\overline{CF2}$		$\overline{CF2}$	$\overline{CF2}$		$\overline{CF1}$	$\overline{CF1}$	$\overline{CF1}$			$\overline{CF2}$	$\overline{CF2}$			$\overline{CF2}$			
DB	SIG3	D5	CHN	PDA4		CW	$\overline{MΔ}$	SF121	S10	MΔ	S11	S21	D	S16	CS134	S21	S25	J	O3	$\overline{CS38}$	TJI
EB	F3	DQ4	CH2	PDA6			$\overline{CF2S29}$	CS121	S21	S19	E			CS113	S26	S20	$\overline{CS136}$		Q0		TBJM
FB	D4	DQ5	CH5			MΔ	$\overline{CF2S30}$	2^{12}	S13	S23			S23	CS112	S6	DS'	S9	S14	Q2	$\overline{CF2S3}$	BJO
HB	DF	DQ1	CH9	PDA5		$\overline{MΔ}$	S25	2^{13}	A	Q2			S16	S13	S10	Q'O	$\overline{CF2S29}$	$\overline{JS23}$	$\overline{S106}$	Q'3	
JB		DQ2	-5V			FΔ2	S26	2^{6}	CS145	S16	S9			S21	S13		S13	CS105		S14	Δ16
KB	DØ	DQ3	F3				S27	2^{4}			$\overline{CS16}$			$\overline{CS114}$	CS133	$\overline{S135}$	$\overline{CS32}$	SF104		S6	Δ19
LB	D1	$\overline{CS2}$	$\overline{SFD}$			64K	S28	2^{2}	QO		S10	CS113	S24	S5	S17	O'2	S27	S1	S107	MΔ	Δ32
MB	DQ4	SG	SIG3			CR	S21	2^{-2}	S8	S20	S26	S5		S4	S1	S134	$\overline{MΔ}$	S17	S21	S27	Δ38
NB	DQ2	M1	FR2	PDA3		8K	S22		S3			A				$\overline{CS136}$	$\overline{DS32}$		S17	S24	CO16
PB	DQ5	FR1	FR1			64S17	S23	S	T			$\overline{CS114}$		S8	S	S24		S26	S24	$\overline{Q1}$	CO32
RB	FR1	SIG3	$\overline{CS2}$			CS	S24		B	S11	$\overline{CS147}$		CS115	S7	OO	SF134		S23	S19		CO19
SB	DØ3OUT	F3					S17	64S17	S143		S21	B		S25	S23	S22		S4	S22		CO38
TB	PCM3 OUT	DØ		PDA0		64S16	S18	$\overline{CS121}$	SF143	E	S24	S20	$\overline{CS116}$	CS115		A		$\overline{CS106}$	$\overline{Q1}$	S28	AUDIO OUT
UB	CH5	CHN		PDA1		$\overline{CS121}$	S19	64S16	Q2	$\overline{CS147}$	S22	S19	C	$\overline{CS116}$	S4	Q"2		S2	Q'3		SRDM
VB	DQ1			PDA2		64S14	S20	64S14	CS143	S25	S23		S22	S27	DS	CS134		S18		$\overline{DS38}$	COΔ

AH: GND for any boords
BH: No connected for any boords
CH: +5V for any baards

DESIGNER: L CHARRIER	NAME: WRAP CONNECTIONS "B" BOARDS	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M VILLERET		C (DWG SIZE) — W B (DRAWING NO)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FACULTE DES SCIENCES APPLIQUEES
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M.VILLERET
INTERFACES
DATA PROCESSOR
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PCM3 OUT
PCM1ROUT
PCM1TOUT
DØ3 OUT
DØ2 OUT
+15V
-15V
+5V
-5V
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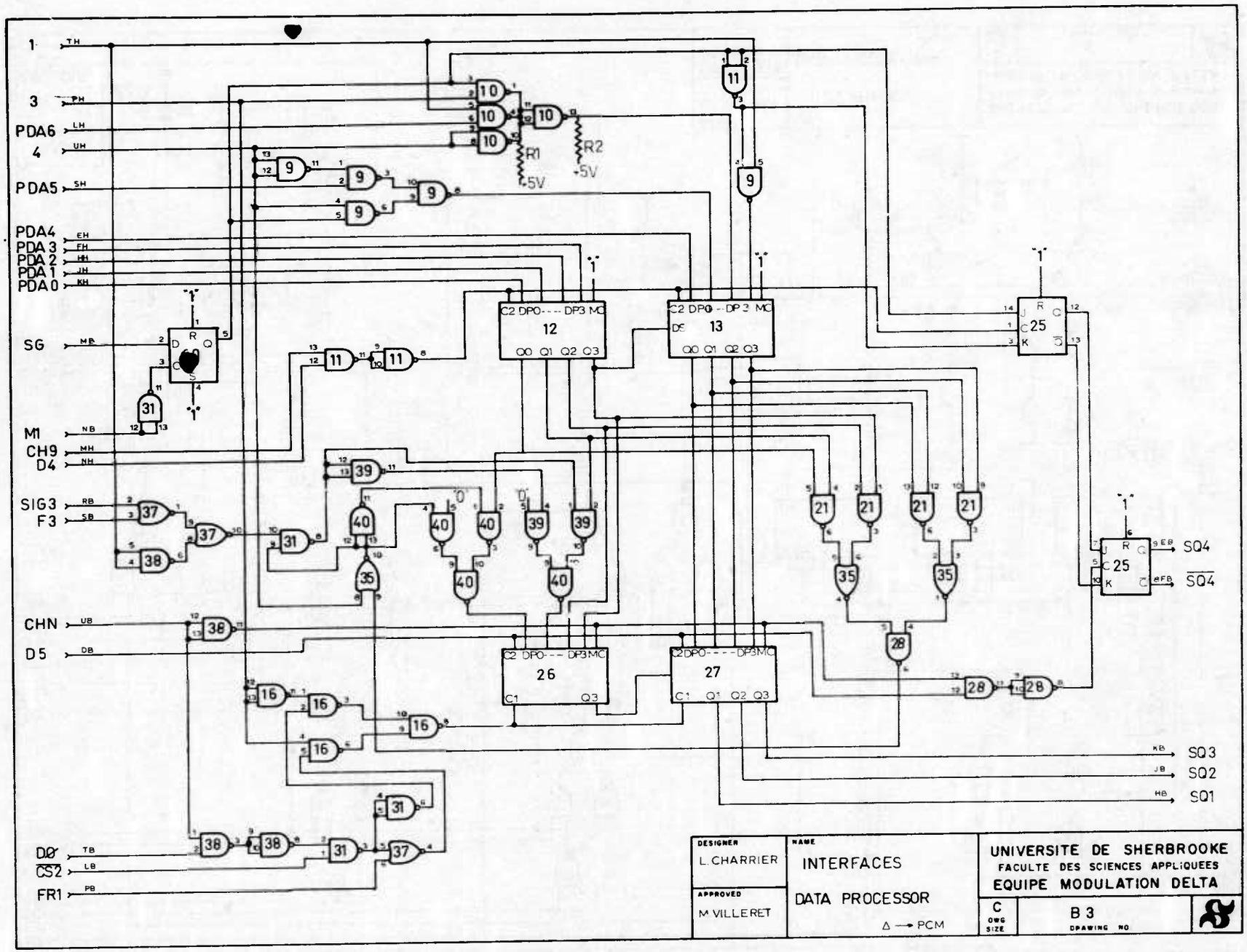
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D5
DØ
CS2
FR1
R1
R2
+5V
SQ4
SQ3
SQ2
SQ1
INTERFACES
DATA PROCESSOR
Δ → PCM
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M.VILLERET
UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
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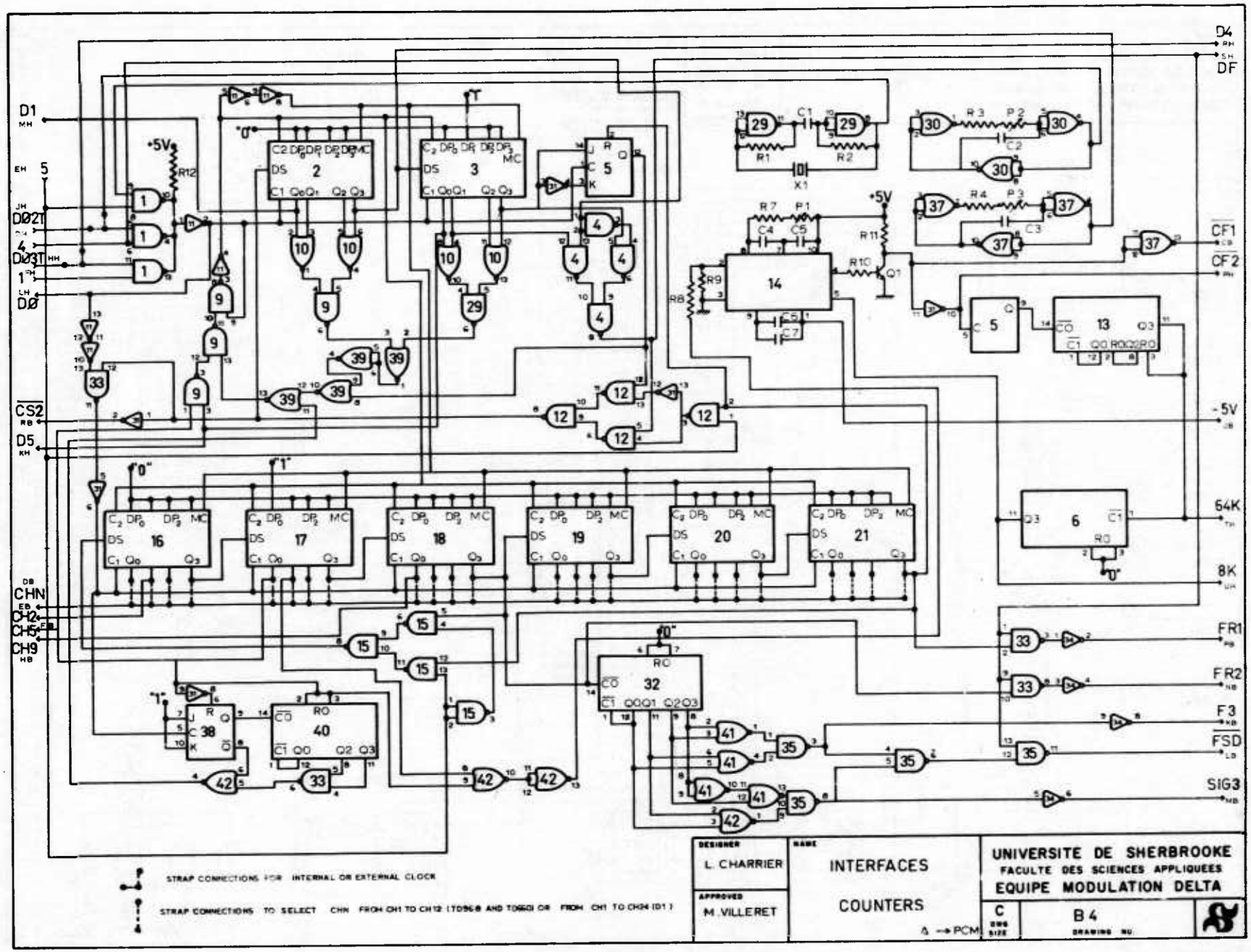
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8K
FR1
FR2
F3
FSD
SIG3
+5V
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"1"
STRAP CONNECTIONS FOR INTERNAL OR EXTERNAL CLOCK
STRAP CONNECTIONS TO SELECT CHN FROM CH1 TO CH12 (TD960 AND TD960I OR FROM CH1 TO CH24 (D1)
DESIGNER
L. CHARRIER
APPROVED
M. VILLERET
NAME
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UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
C
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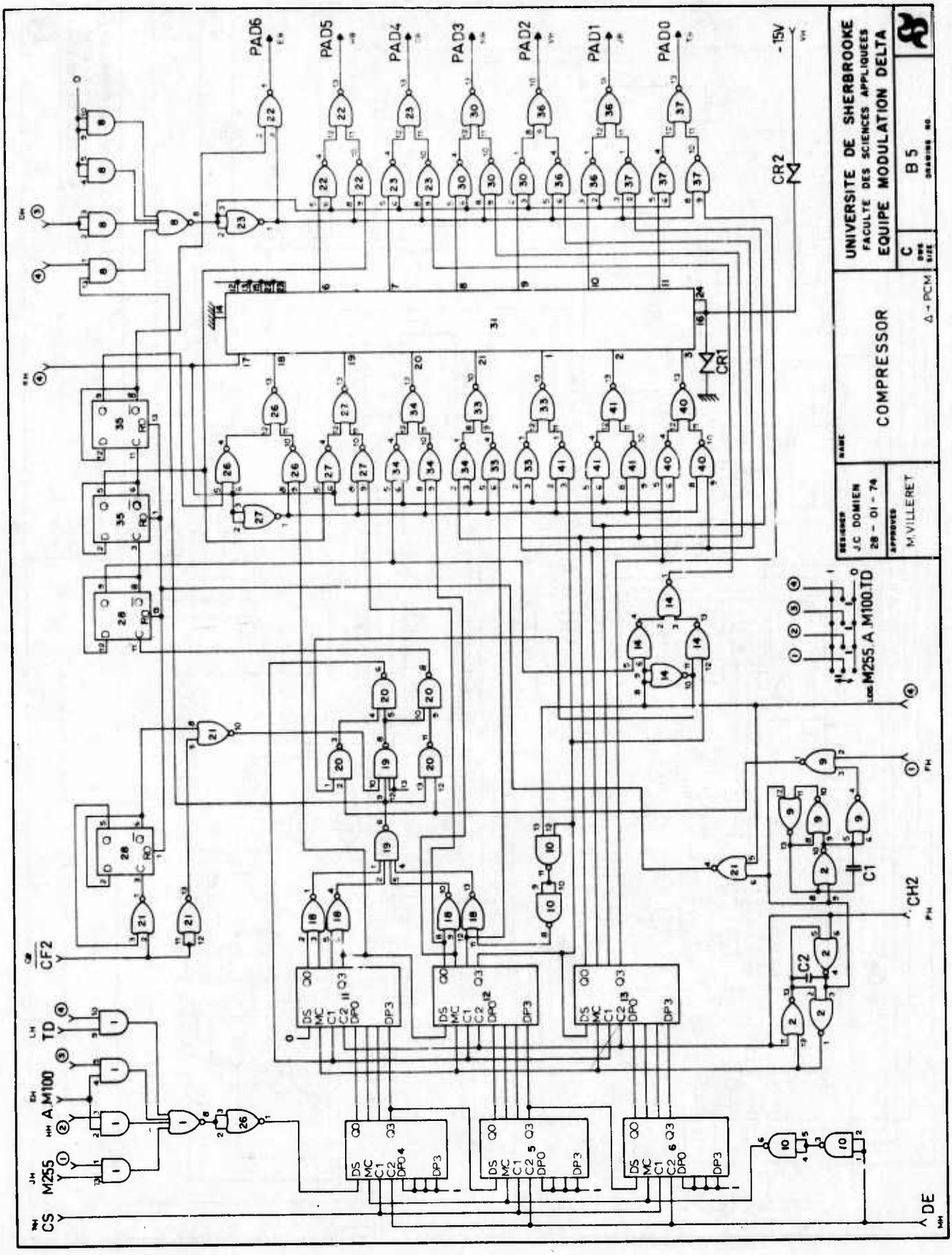
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28 - 01 - 74
M.VILLERET
PAD6
PAD5
PAD4
PAD3
PAD2
PAD1
PAD0
-15V
CR1
CR2
M255 A M100 TD
A M100
TD
M255
CS
CF2
CH2
C1
C2
DE

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EQUIPE MODULATION DELTA
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N. FORGET
M. VILLERET
Δ-PCM
CS
CF2
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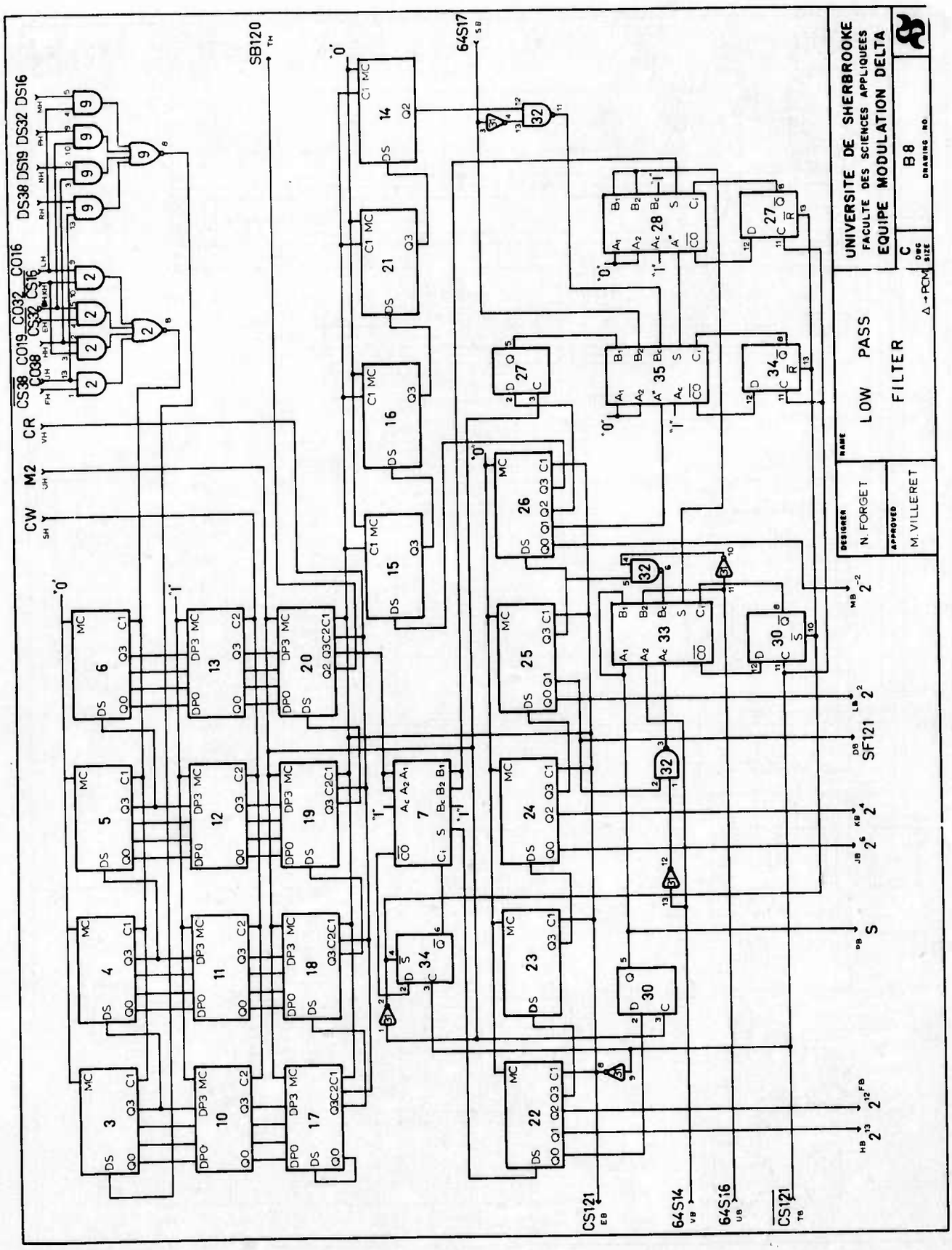
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SB120
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CW
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DS19
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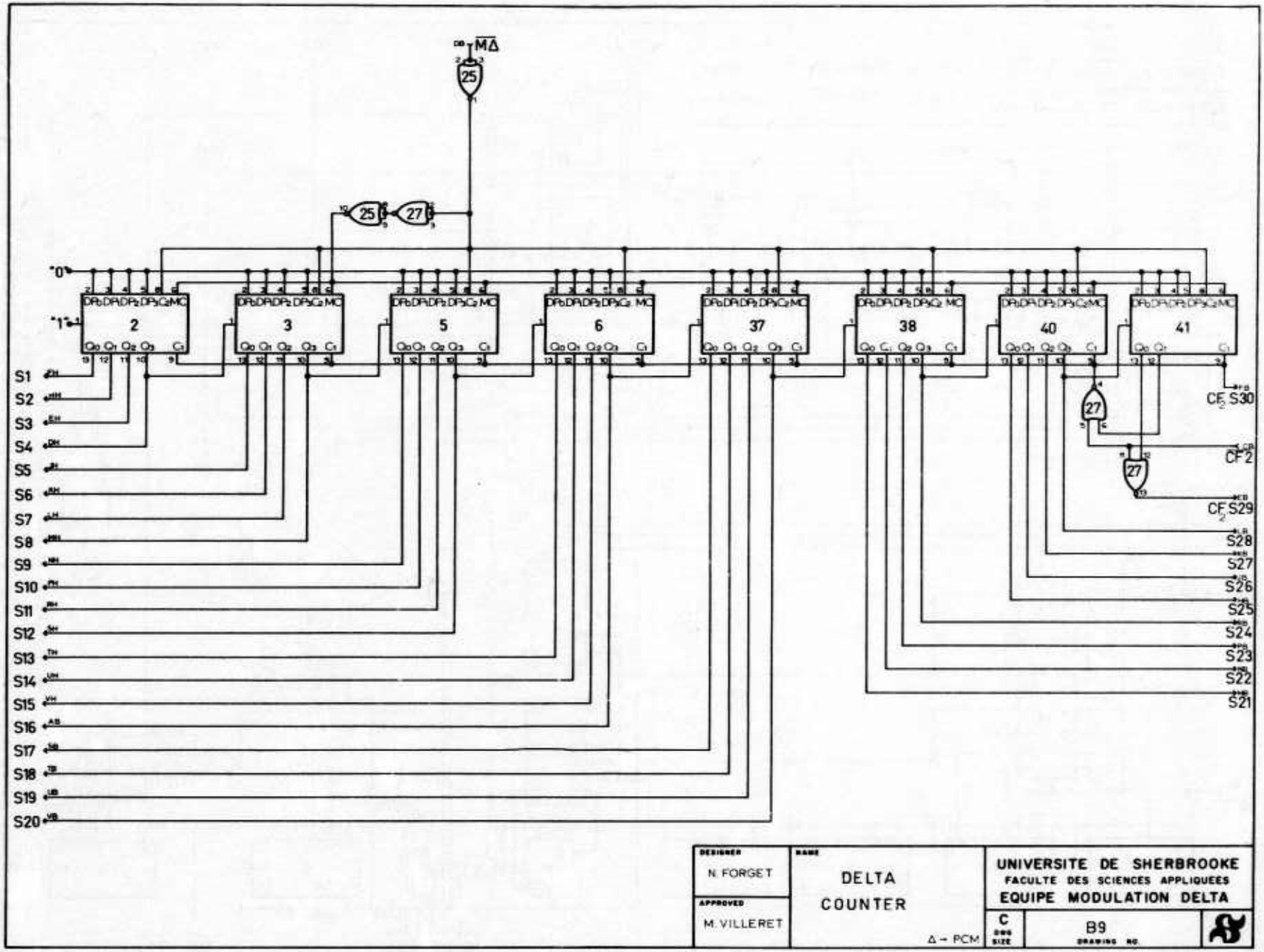
CS121
64S14
64S16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S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
27
27
CF2 S30
CF2
CF2 S29
S28
S27
S26
S25
S24
S23
S22
S21
DESIGNER
N. FORGET
APPROVED
M. VILLERET
NAME
DELTA
COUNTER
Δ → PCM
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EQUIPE MODULATION DELTA
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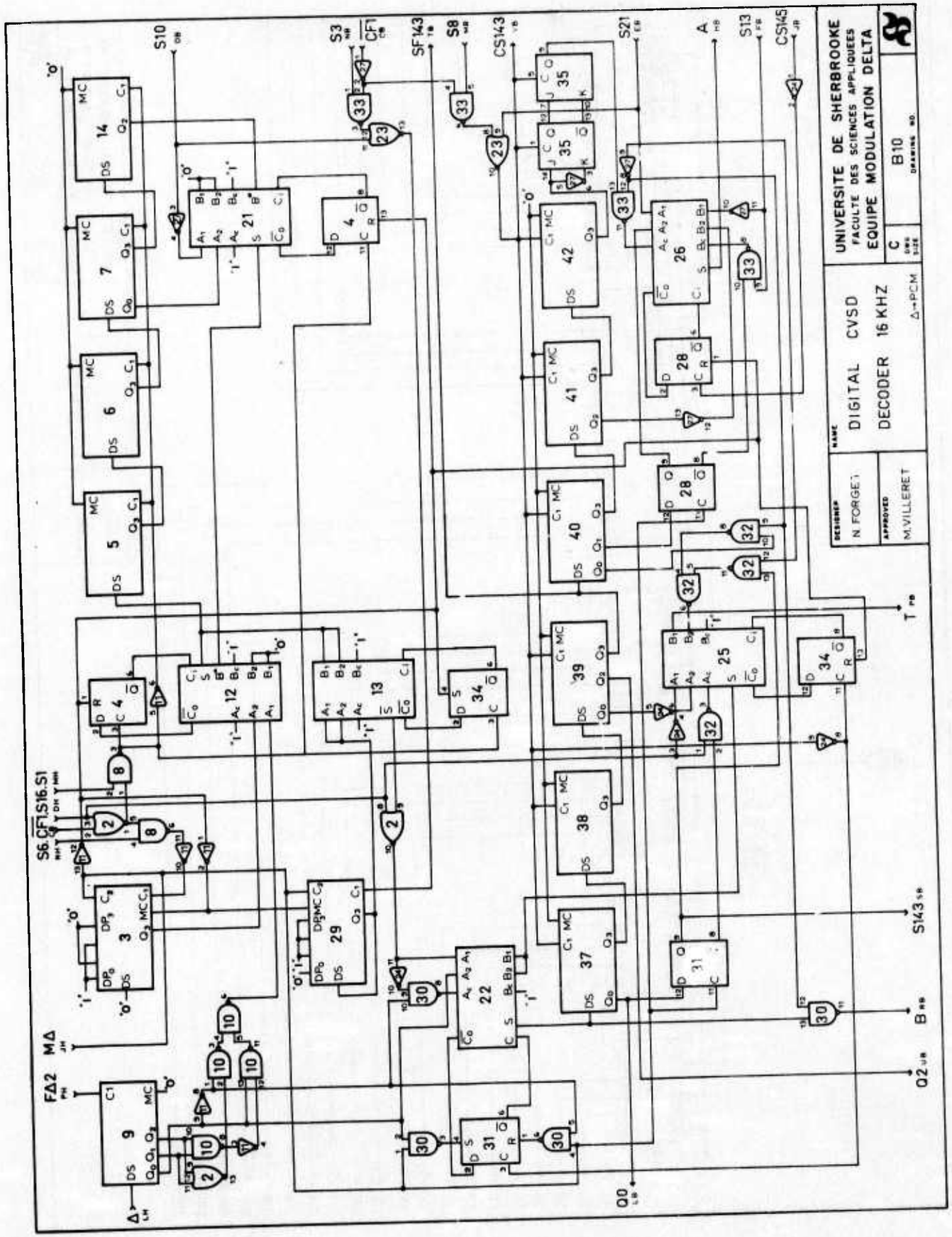
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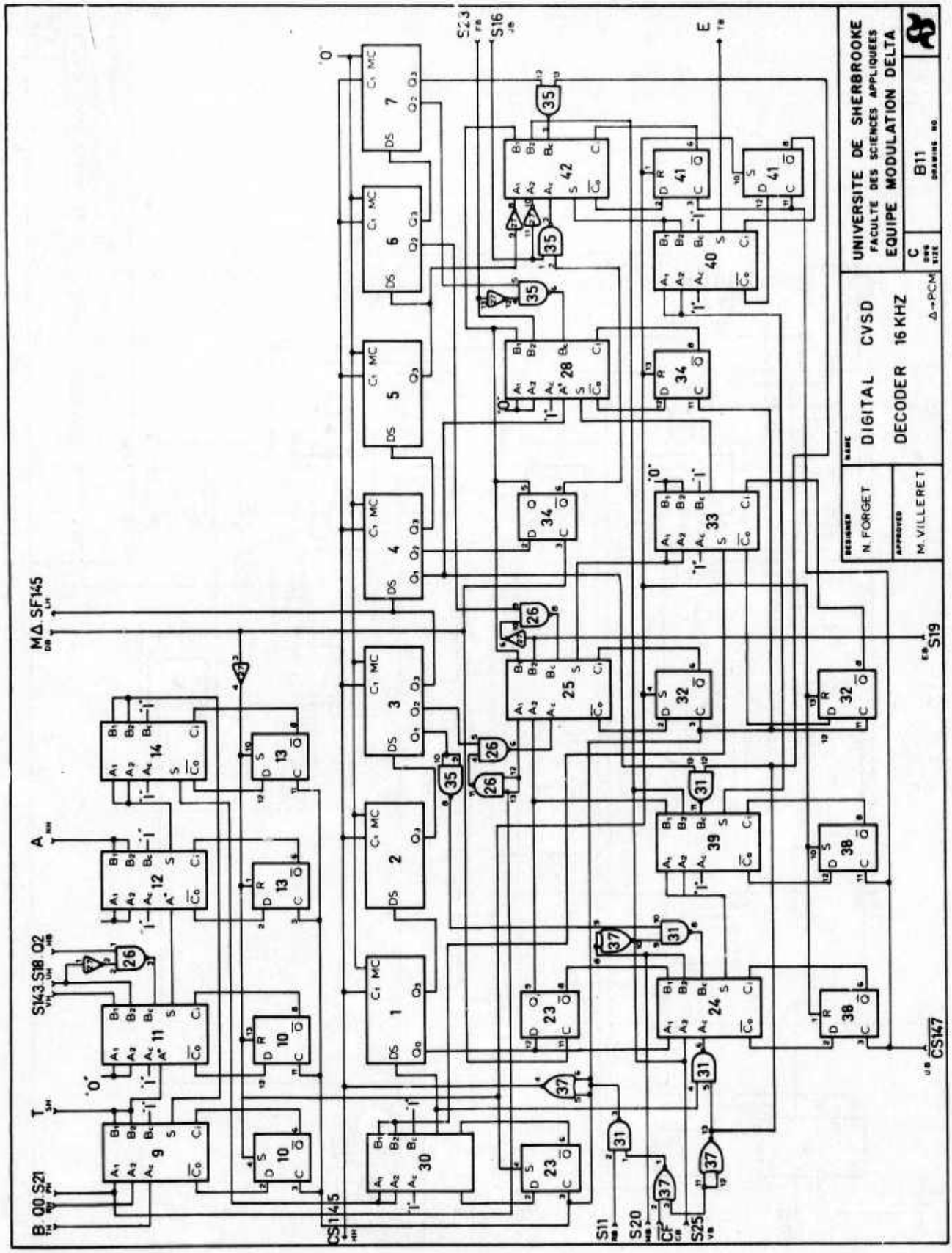
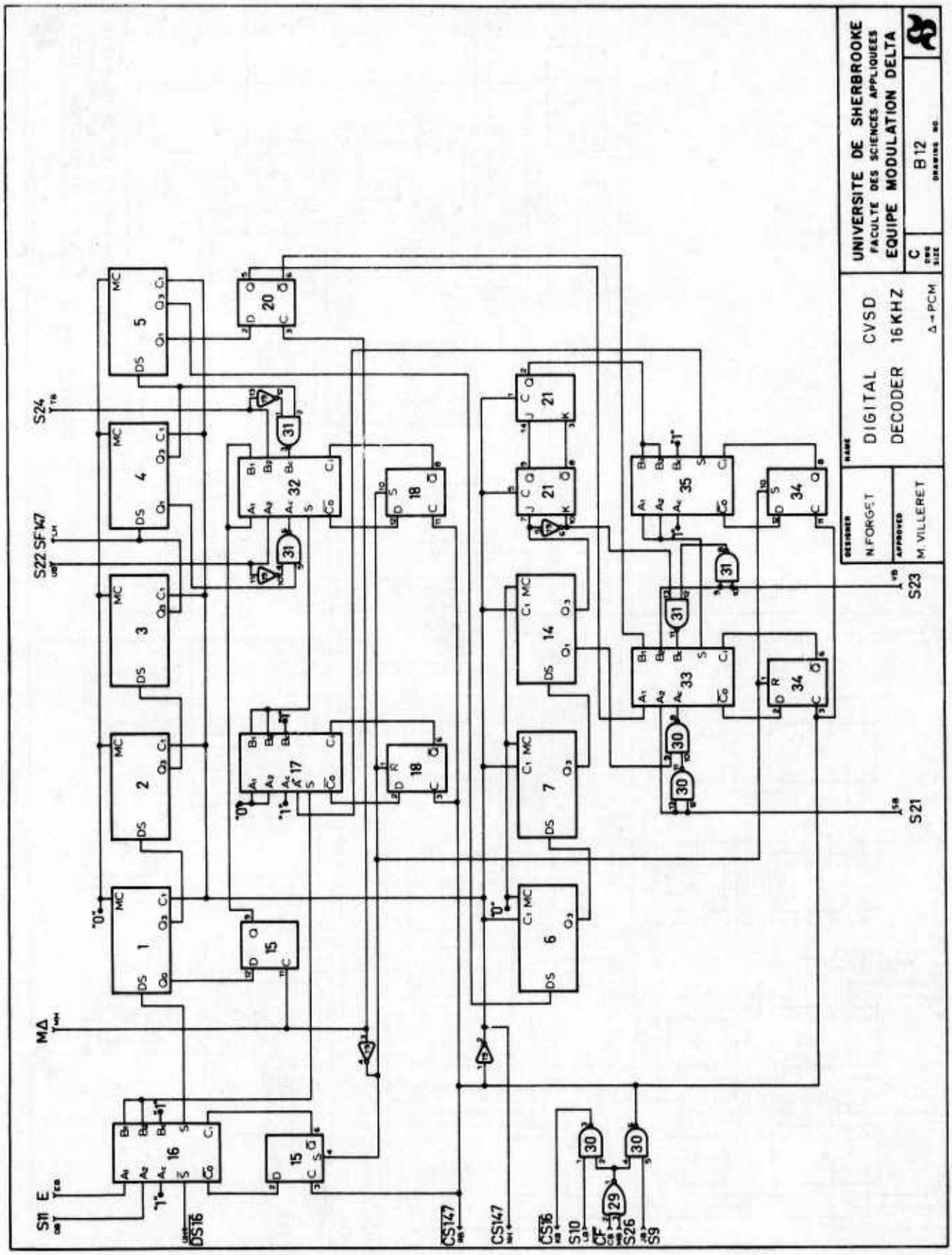
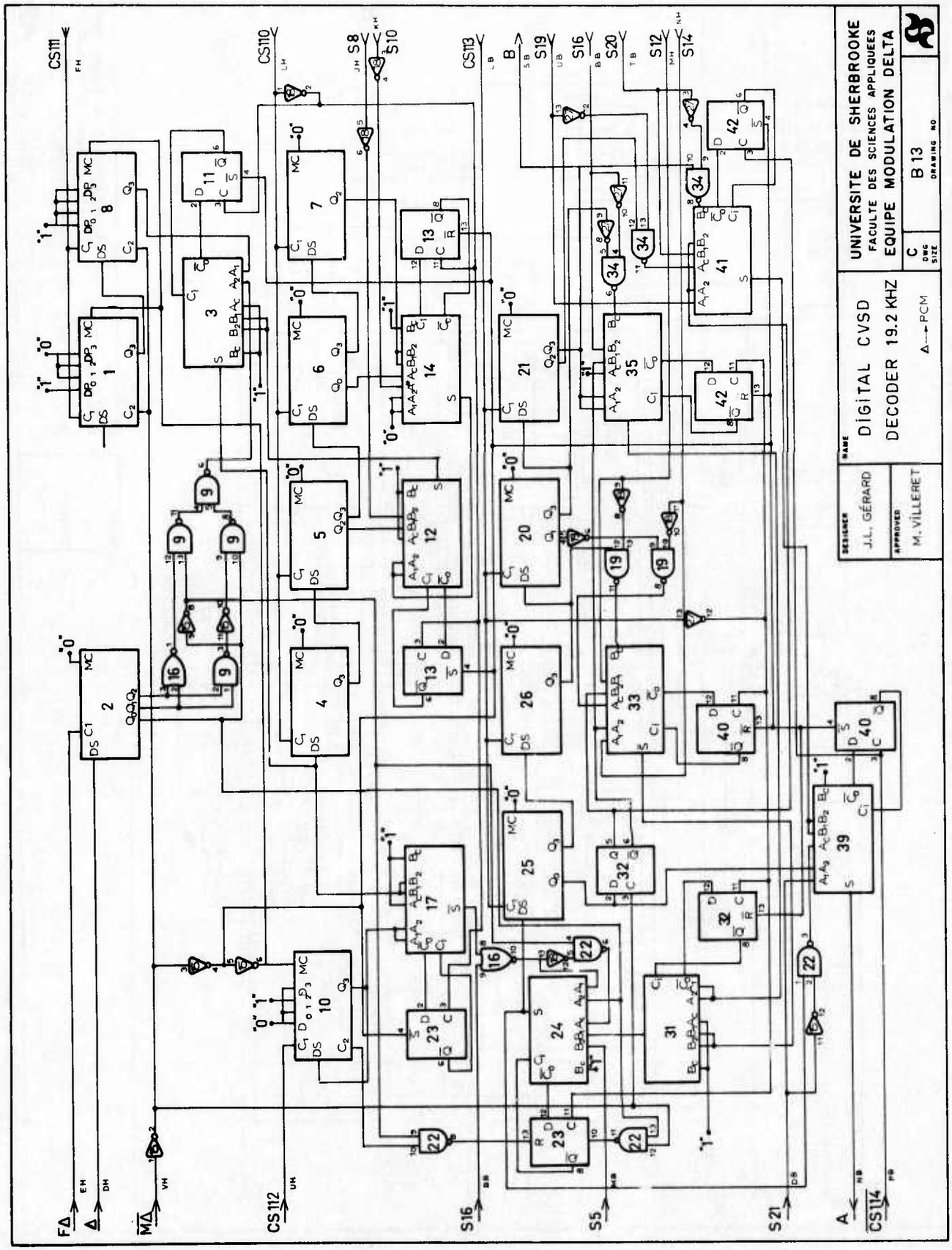
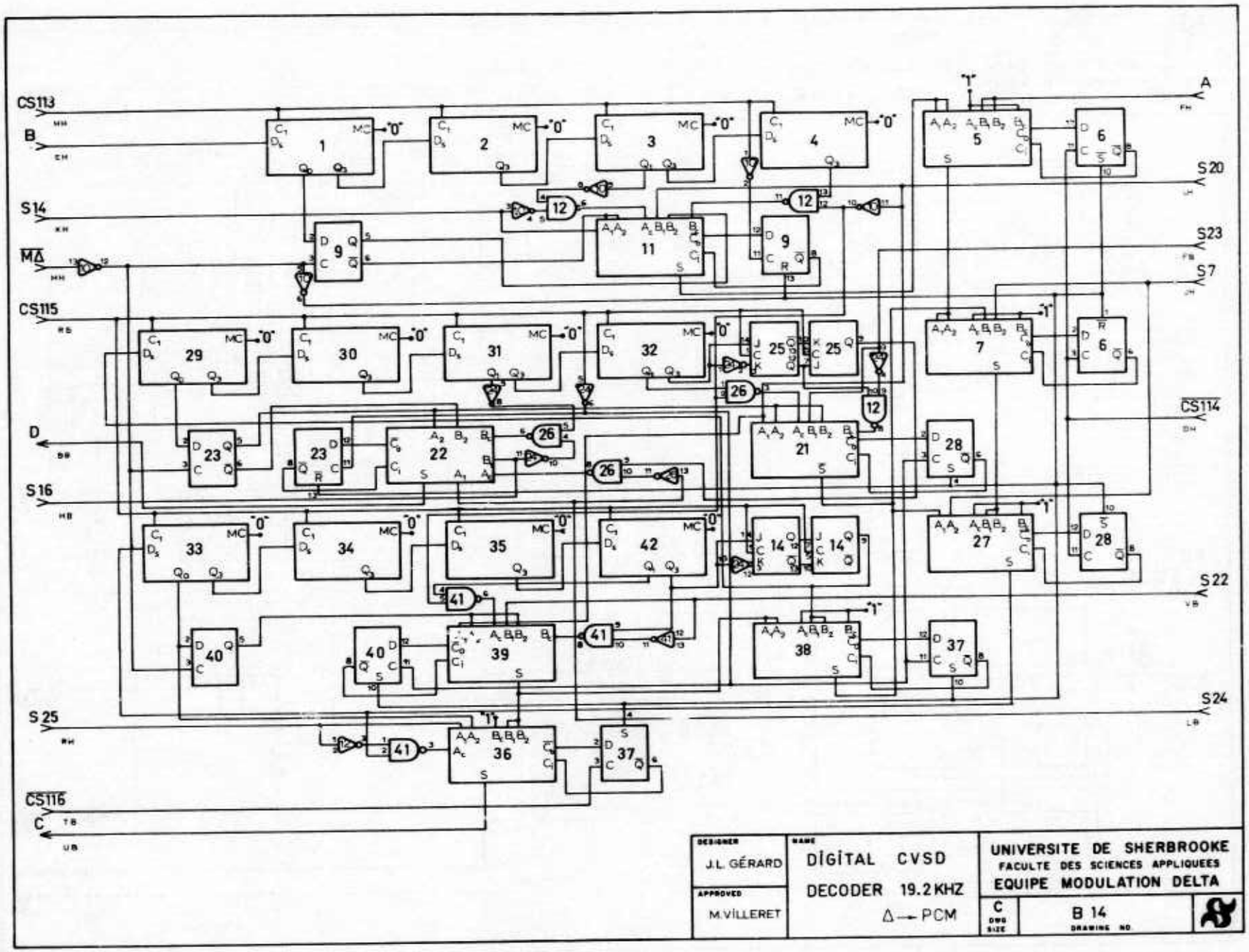
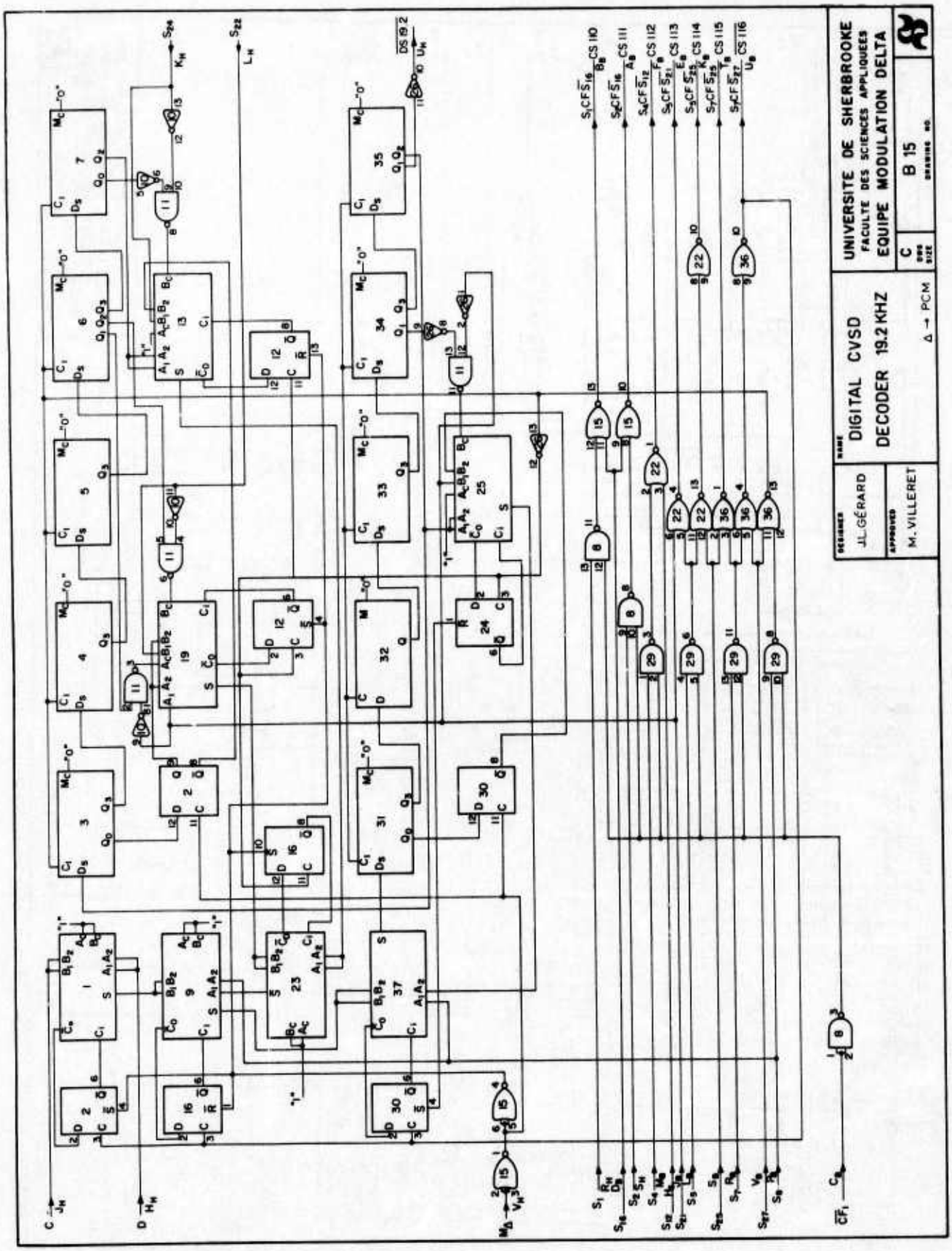
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DIGITAL CVSD
DECODER 16 KHZ
Δ→PCM
B10
N FORGET
M.VILLERET
S10
S3
CF1
SF143
S8
CS143
S21
A
S13
CS145
T
S143
B
Q2
Q0
FA2
MΔ
S6.CF1.S16.S1

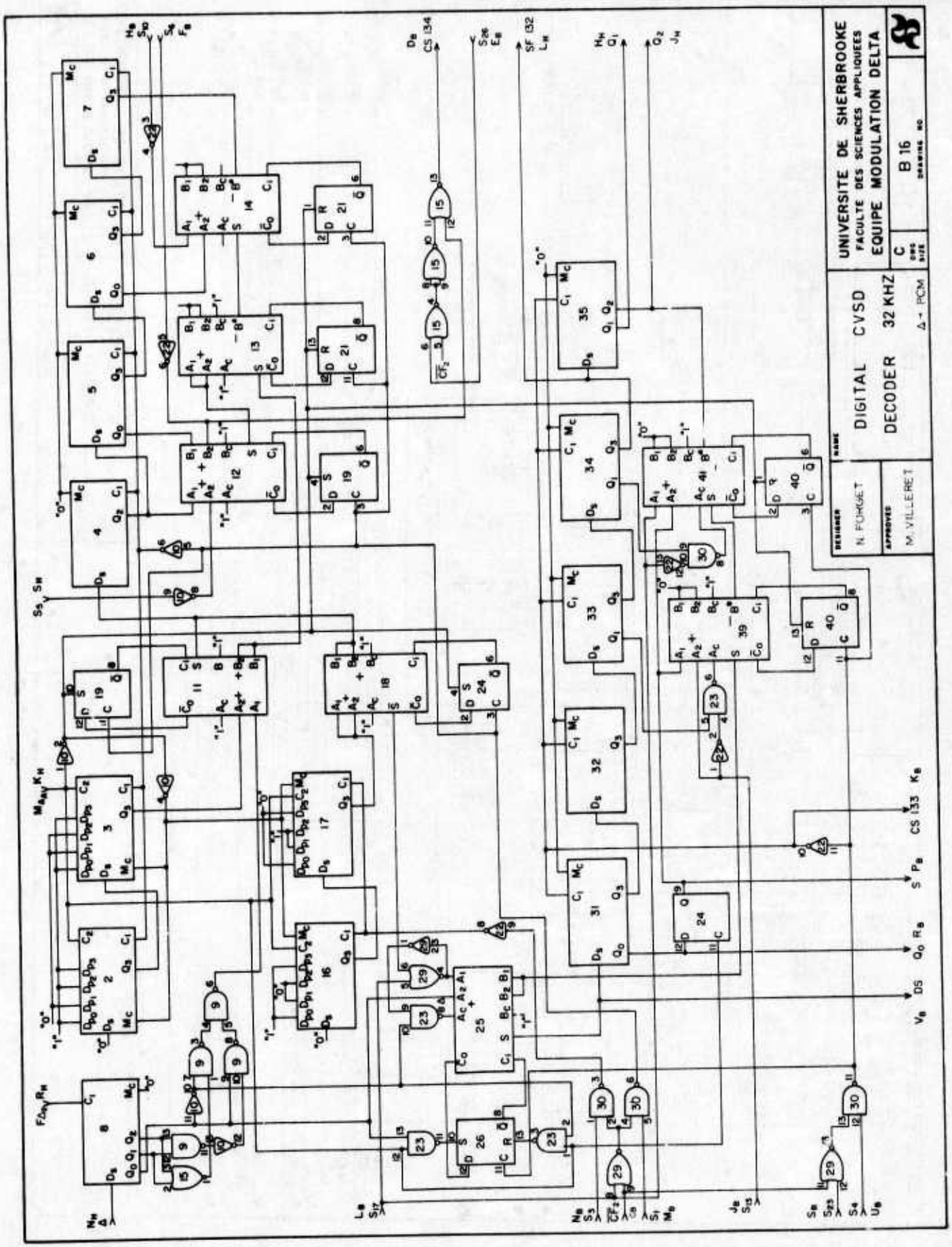

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DIGITAL CVSD
DECODER 16 KHZ
Δ→PCM
N. FORGET
M. VILLERET
B11
MΔ SF145
S19
CS145
CS147
S11
S20
S25
S16
E

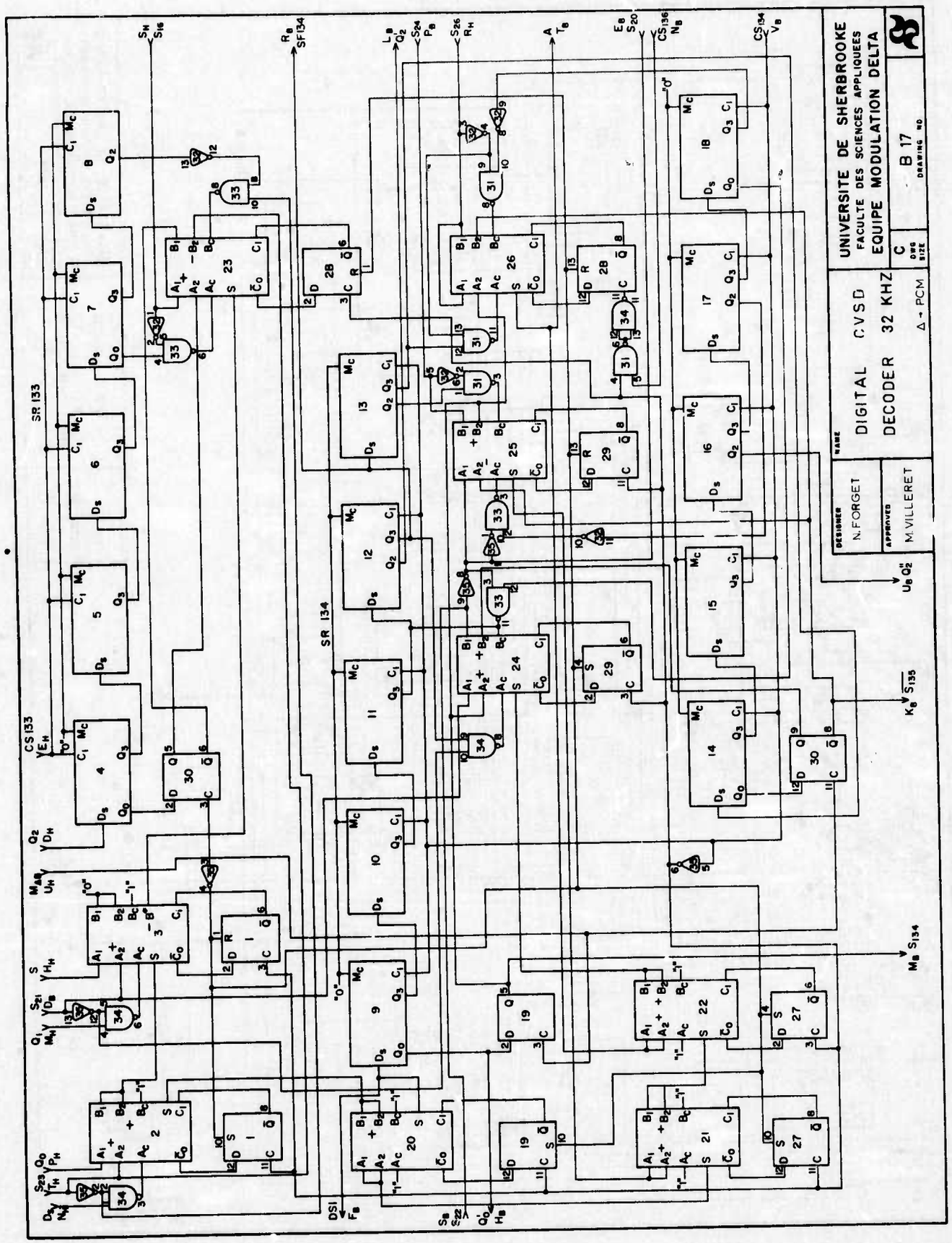

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DIGITAL CVSD
DECODER 16 KHZ
Δ→PCM
B12
N.FORGET
M.VILLERET
S24
S22 SF147
S23
S21
MΔ
S11 E
DS16
CS147
CS16
S10
CF
S26
S9

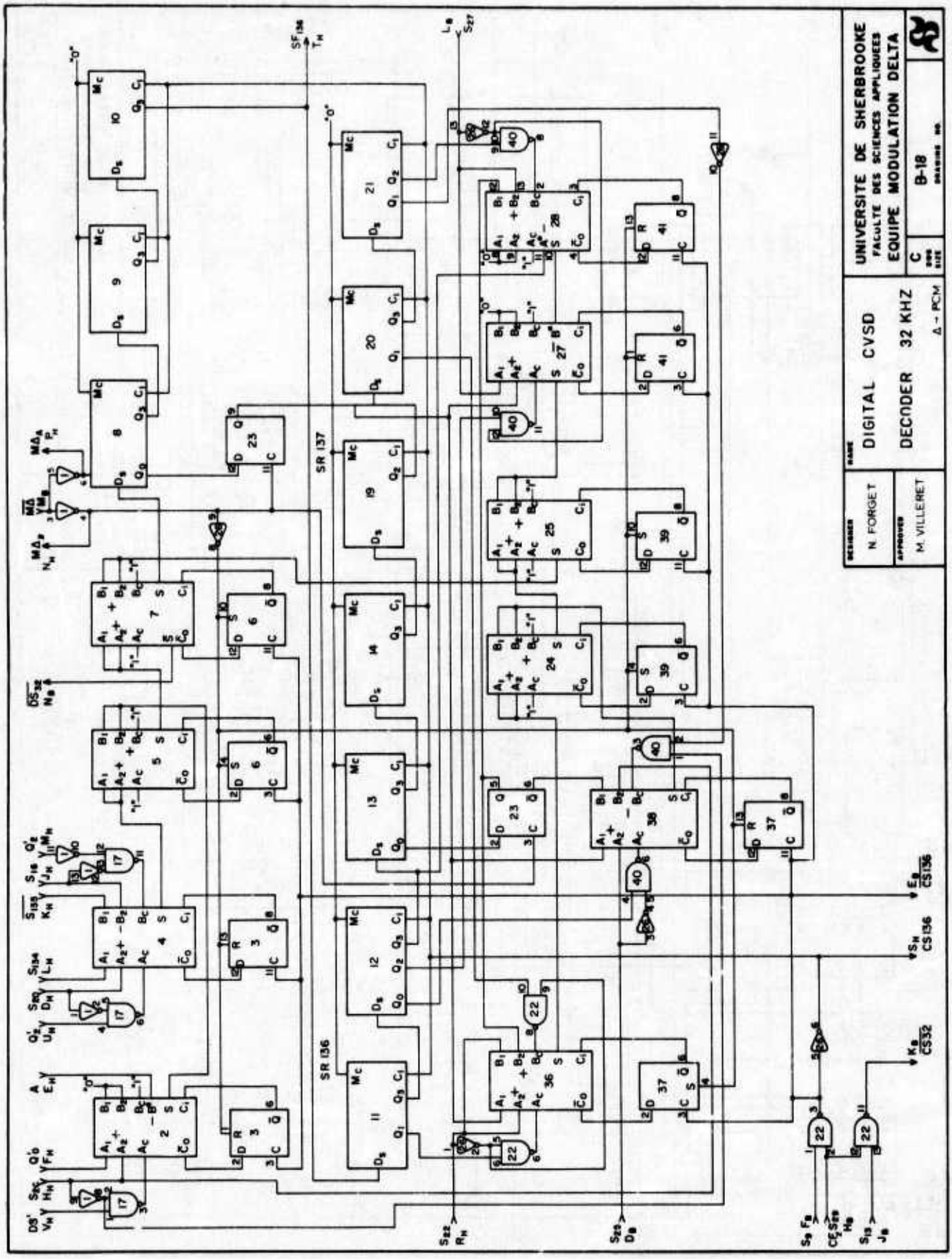

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DIGITAL CVSD
DECODER 19.2 KHZ
Δ → PCM
B 13
J.L. GÉRARD
M. VILLERET
CS111
CS110
CS113
CS112
CS114
S8
S10
S19
S16
S20
S12
S14
S5
S21
FΔ
MΔ

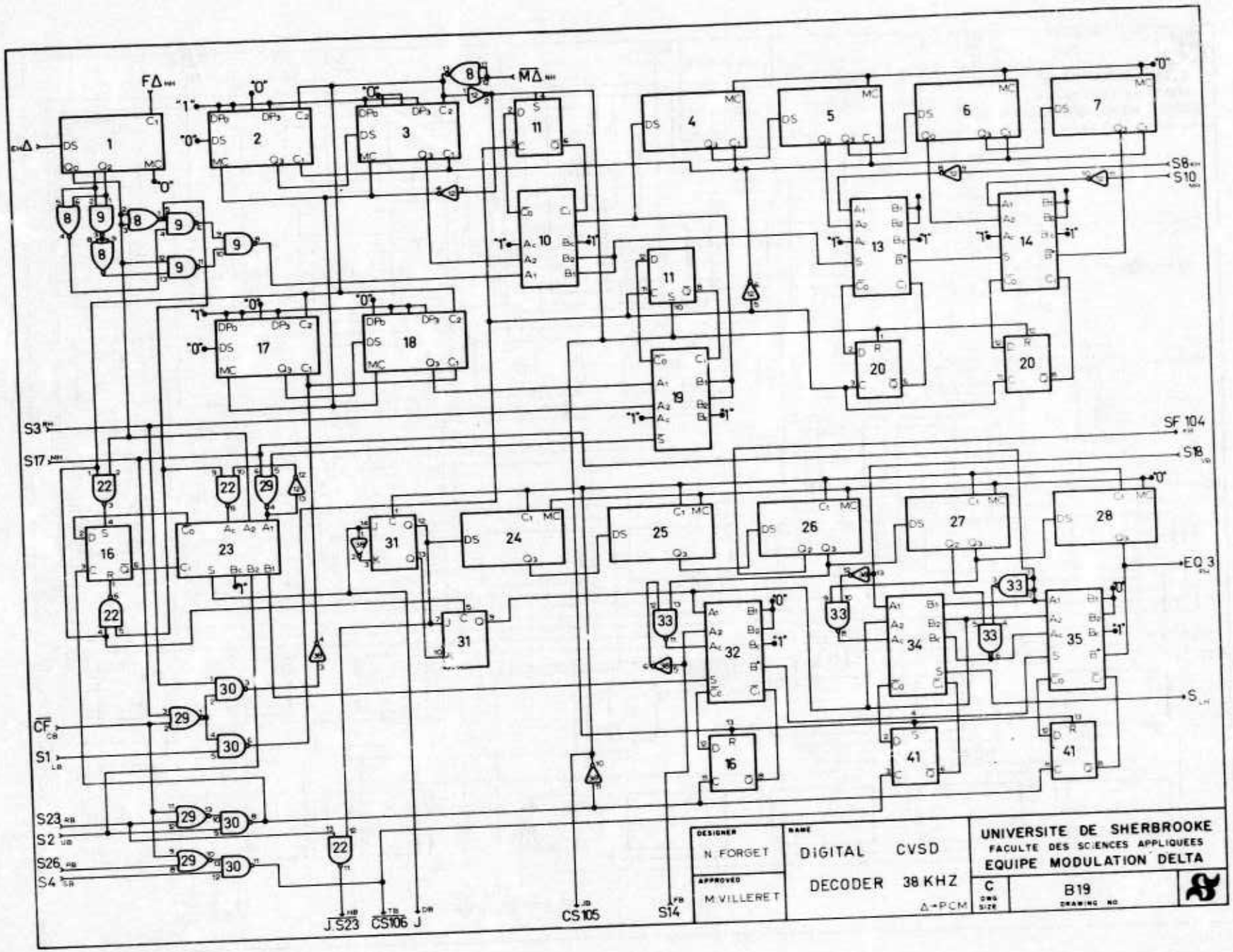

CS113
B
S14
MΔ
CS115
D
S16
S25
CS116
C
A
S20
S23
S7
CS114
S22
S24
DESIGNER
J.L. GÉRARD
APPROVED
M.VILLERET
NAME
DIGITAL CVSD
DECODER 19.2KHZ
Δ → PCM
UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
C
DWG SIZE
B 14
DRAWING NO

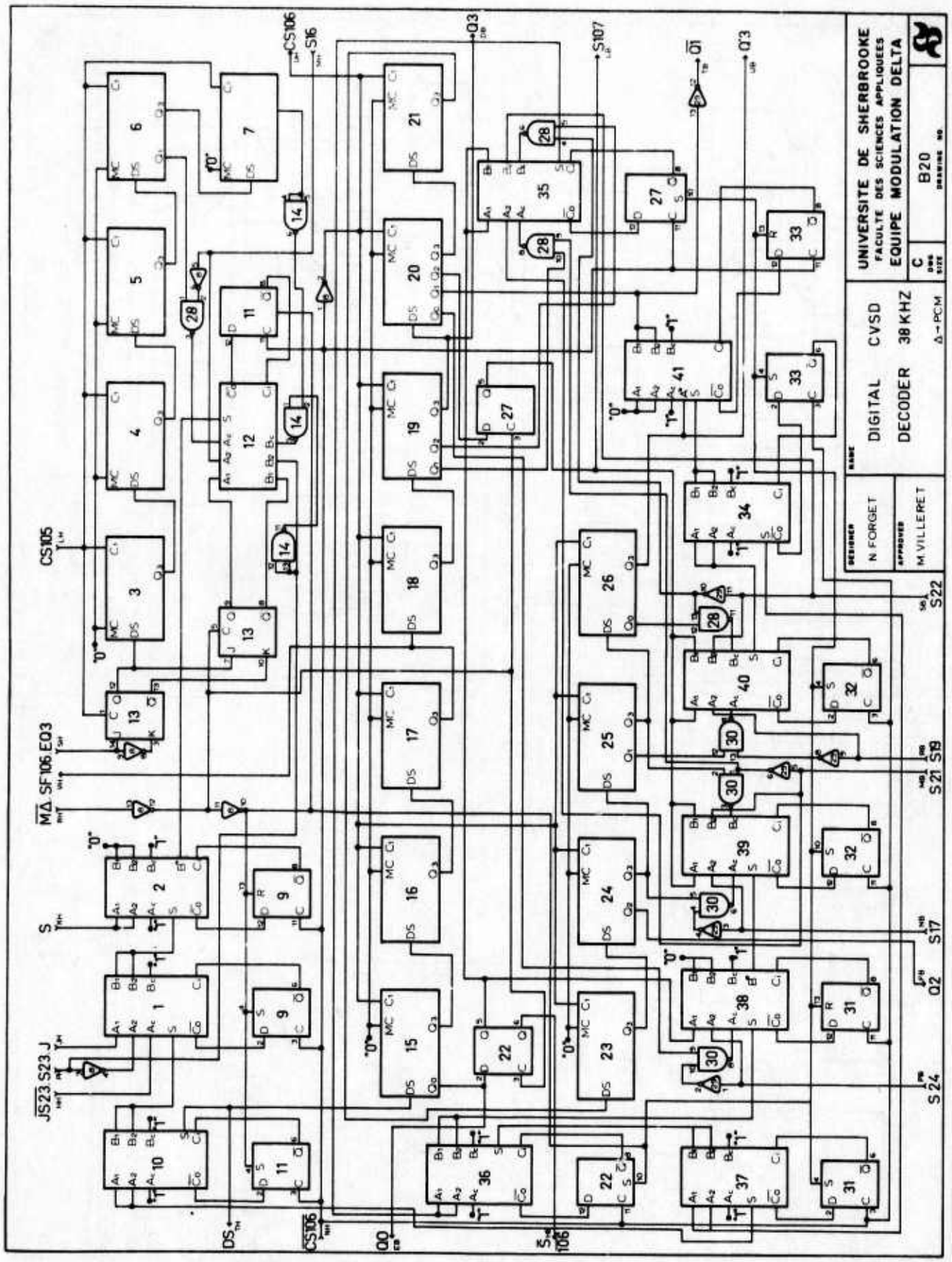

DIGITAL CVSD
DECODER 19.2 KHZ
Δ → PCM
UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
B 15
J.L. GÉRARD
M. VILLERET

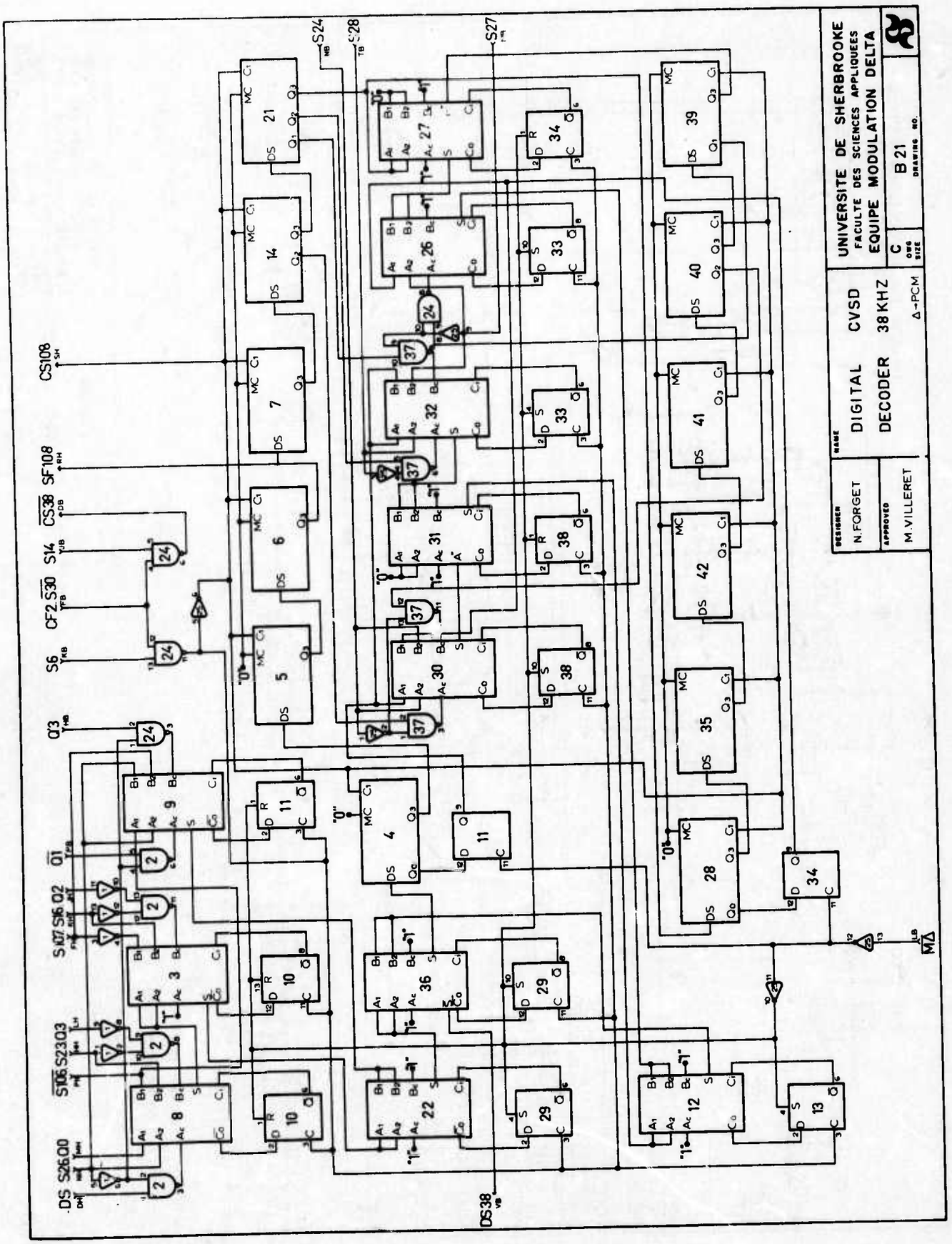

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DIGITAL CVSD
DECODER 32 KHZ
Δ→ PCM
B 16
N. FUHRET
M. VILLERET

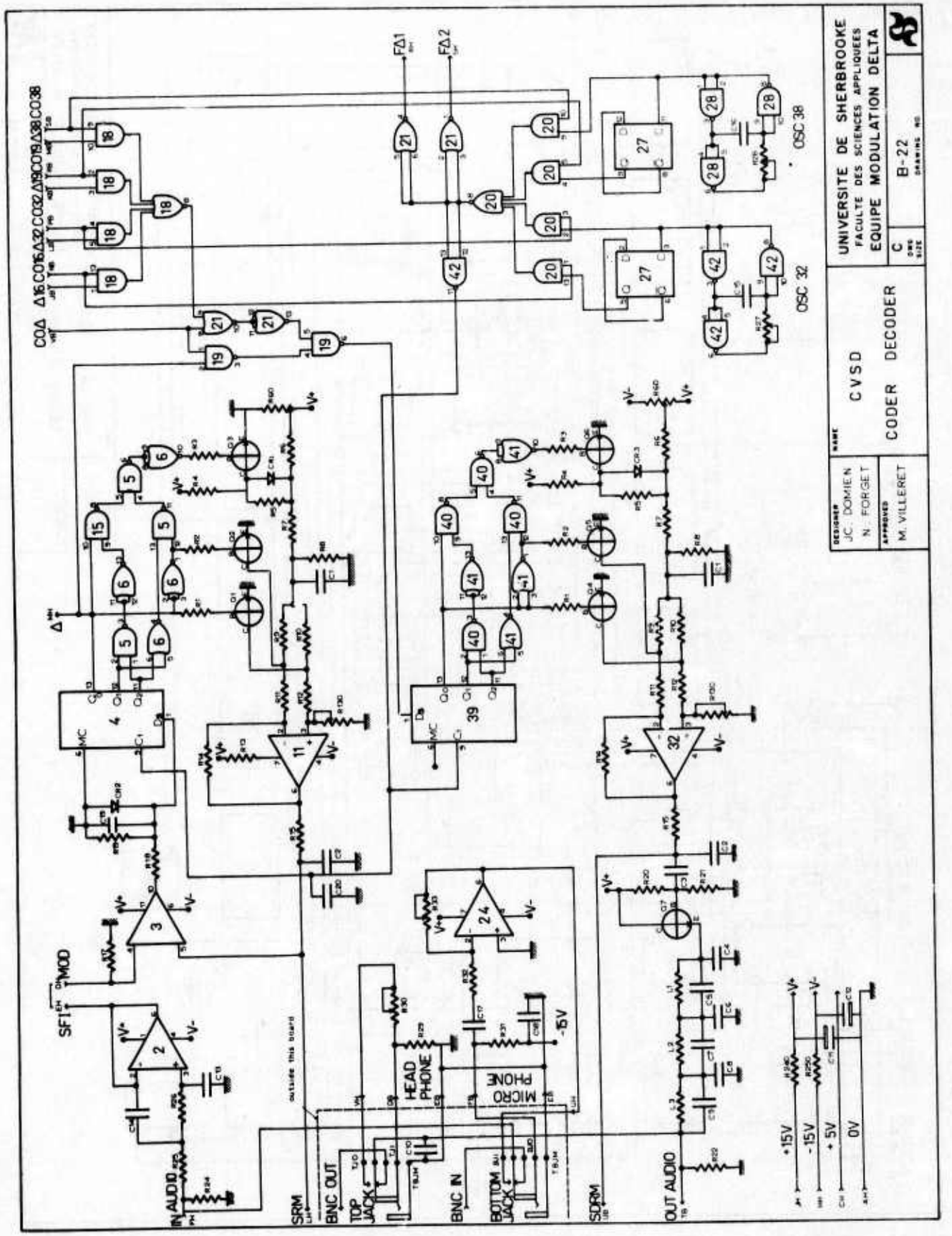

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DIGITAL CVSD
DECODER 32 KHZ
Δ → PCM
B 17
DESIGNED N.FORGET
APPROVED M.VILLERET
SR 133
SR 134
CS 133
SF 134
CS 135
CS 136


UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DESIGNED N. FORGET
APPROVED M. VILLERET
NAME DIGITAL CVSD
DECODER 32 KHZ
Δ - PCM
C
B-18
SR 137
SR 136


DESIGNER
N. FORGET
APPROVED
M. VILLERET
NAME
DIGITAL CVSD
DECODER 38 KHZ
Δ→PCM
UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
C
B19
DRAWING NO


UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
B20
DIGITAL CVSD
DECODER 38 KHZ
Δ→PCM
N FORGET
M VILLERET
CS106
S16
Q3
S107
Q1
Q'3
CS105
MΔ SF106 E03
S
JS23 S23 J
DS
CS106
Q0
S106
S22
S21 S18
S17
Q2
S24


UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DIGITAL CVSD
DECODER 38KHZ
Δ-PCM
B 21
N.FORGET
M.VILLERET
CS108
SF108
S14
S6
Q3
Q1
Q2
S24
S28
S27
DS38


UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
CVSD
CODER DECODER
B-22
DESIGNER
JC. DOMIEN
N. FORGET
APPROVED
M. VILLERET
OSC 38
OSC 32
HEAD PHONE
MICRO PHONE
BNC OUT
TOP JACK
BNC IN
BOTTOM JACK
IN AUDIO
OUT AUDIO
SRM
SDRM
MOD
-15V
+15V
+5V
0V

NUMBER (1)	TYPE (2)	OESCRIPTION
IC 1		
IC 2	MC7400P	4x2 INPUTS NAND GATE
IC 3	MC7495P	4 BITS SHIFT REGISTER
IC 4	MC7495P	" " " " "
IC 5	MC7495P	" " " " "
IC 6		
IC 7		
IC 8		
IC 9	MC7400P	4x2 INPUTS NAND GATE
IC 10	MC7400P	" " " "
IC 11		
IC 12		
IC 13		
IC 14		
IC 15		
IC 16		
IC 17		
IC 18		
IC 19	MC7402P	4x2 INPUTS NOR GATE
IC 20		
IC 21		
IC 22		
IC 23	MC7400P	4x2 INPUTS NAND GATE
IC 24	MC7400P	" " " " "
IC 25	MC7400P	" " " " "
IC 26	MC7402P	4x2 INPUTS NOR GATE
IC 27		
IC 28		
IC 29		
IC 30	MC7400P	4x2 INPUTS NAND GATE
IC 31	MC7400P	" " " " "
IC 32	MC7400P	" " " " "
IC 33	MC7479P	DUAL TYPE D FLIP FLOP
IC 34		
IC 35		
IC 36	MC7451P	2 AOI GATES
IC 37	MC7400P	4x2 INPUT NAND GATE
IC 38	MC7479P	DUAL TYPE D FLIP FLOP
IC 39	MC7402P	4x2 INPUT NOR GATE
IC 40	MC7479P	DUAL TYPE D FLIP FLOP
IC 41		
IC 42		

(1) FOR ADDED CLARITY, IC IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	OISSIP.	VOLTAGE	DESCRIPTION
C1	Metalized	100nF	±10%		250V	280 AEA 100K PHILIPS
C2	Ceramic	10nF	-20/+100%		40V	2222 62903103 " "
C3	Chimis	10 µF	-10+50%		25V	426 ARFIO " "
C4	Metalized	100nF	±10%		250V	280 AEA100K " "
C5	Ceramic	10nF	-20+100%		40V	222 629 03103 " "
C6	Ceramic	2.2nF	-20+100%		40V	2222 629 03222 " "
C7	" "	2.2nF	-20+100%		40V	2222 629 03222 " "
C8	" "	2.2nF	-20+100%		40V	2222 629 03222 " "
C9	" "	10nF	-20+100%		40V	2222 629 03103 " "
C10	" "	10nF	-20+100%		40V	2222 629 03103 " "
C11	" "	10nF	-20+100%		40V	2222 629 03103 " "
C12	" "	10nF	-20+100%		40V	2222 629 03103 " "
C13	" "	470pF	± 10%		100V	2222 630 03471 " "
C14	" "	470pF	± 10%		100V	2222 630 03471 " "
C15	Chimic	10nF	-10+50%		25V	426 ARFIO " "
C16	Chimic	10nF	-20±100%		40V	222 629 03103 " "
C17	" "	10µF	-10+50%		25V	426 ARFIO " "
C18	" "	10µF	-10+50%		25V	426 ARFIO " "
C19	Ceramic	10nF	-20+100%		40V	2222 629 03103 " "
C20	" "	10nF	-20+100%		40V	2222 629 03103 " "
CR1	IN5225	3.1V		1W	3.1V	Zener DIODE MOTOROLA
CR2	IN5225	3.1V		1W	3.1V	" " "
CR3	IN5233	5.1V		1W	5.1V	" " "
CR4	IN5225	3.1V		1W	3.1V	" " "
Q1	2N4126			300mW	VCB=30V	PNP TRANSISTOR
Q2	2N4126			300mW	VCB=30V	" " "
Q3	2N4126			" "	" " "	" " "
Q4	2N4126			" "	" " "	" " "
Q5	2N4124			" "	" " "	" " "
Q6	2N4124			" "	" " "	" " "
Q7	2N4124			" "	" " "	" " "
Q8	2N4126			" "	" " "	" " "
Q9	2N4126			" "	" " "	" " "
Q10	2N4124			" "	" " "	" " "
Q11	2N4124			" "	" " "	" " "

DESIRRER: L.CHARRIER	NAME: INTERFACES DATA PROCESSOR Δ→PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M.VILLERET		C (DOS SIZE) — NB1 (DRAWING NO) — 1/3

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2		
IC 3		
IC 4		
IC 5		
IC 6		
IC 7		
IC 8		
IC 9		
IC 10		
IC 11		
IC 12		
IC 13		
IC 14		
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22		
IC 23		
IC 24		
IC 25		
IC 26		
IC 27		
IC 28		
IC 29		
IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, IC* IS NOT DRAWN ON ELECTSICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION
Q12	2N4126			300mW	VCB=30V	PNP TRANSISTOR MOTOROLA
Q13	2N4126			" "	" "	" " " " "
Q14	2N4124			" "	" "	" " " " "
R1		1KΩ	± 5%	250mW	250V	STYLE 25 PHILIPS
R2		1KΩ	"	" "	" "	" "
R3		1KΩ	"	" "	" "	" "
R4		470Ω	"	" "	" "	" "
R5		100Ω	"	" "	" "	" "
R6		1KΩ	"	" "	" "	" "
R7		4.7KΩ	"	" "	" "	" "
R8		100Ω	"	" "	" "	" "
R9		1KΩ	"	" "	" "	" "
R10		1KΩ	"	" "	" "	" "
R11		470Ω	"	" "	" "	" "
R12		1KΩ	"	" "	" "	" "
R13		4.7KΩ	"	" "	" "	" "
R14		47Ω	"	" "	" "	" "
R15		100Ω	"	" "	" "	" "
R16		470Ω	"	" "	" "	" "
R17		100Ω	"	1W	500V	STYLE 52 " "
R18		2.2KΩ	"	250mW	250V	STYLE 25 " "
R19		2.2KΩ	"	" "	" "	" "
R20		470Ω	"	" "	" "	" "
R21		470Ω	"	" "	" "	" "
R22		1KΩ	"	" "	" "	" "
R23		1KΩ	"	" "	" "	" "
R24		1KΩ	"	" "	" "	" "
R25		1KΩ	"	" "	" "	" "
R26		100Ω	"	" "	" "	" "
R27		120Ω	"	" "	" "	" "
R28		120Ω	"	" "	" "	" "
R29		2.2KΩ	"	" "	" "	" "
R30		1KΩ	"	" "	" "	" "

DESIGNED: L.CHARRIER	NAME: INTERFACES DATA PROCESSOR Δ——PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M.VILLERET		C (DWG SIZE) — N B1 (DRAWING NO.) — 2/3

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2		
IC 3		
IC 4		
IC 5		
IC 6		
IC 7		
IC 8		
IC 9		
IC 10		
IC 11		
IC 12		
IC 13		
IC 14		
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22		
IC 23		
IC 24		
IC 25		
IC 26		
IC 27		
IC 28		
IC 29		
IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTNICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) ON EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	OISSIP.	VOLTAGE	DESCRIPTION
R31		1KΩ	±5%	250mW	250V	STYLE 25 PHILIPS
R32		1KΩ	"	" "	" "	" " " "
R33		100Ω	"	" "	" "	" " " "
R34		2.2KΩ	"	" "	" "	" " " "
R35		120Ω	"	" "	" "	" " " "
R36		120Ω	"	" "	" "	" " " "
R37		4.7KΩ	"	" "	" "	" " " "
R38		6.8KΩ	"	" "	" "	" " " "
R39		4.7KΩ	"	" "	" "	" " " "
R40		2.2KΩ	"	" "	" "	" " " "

DESIGNER: L. CHARRIER	NAME: INTERFACES DATA PROCESSOR Δ ⟶ PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) — N B1 (DRAWING NO.) 3/3

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2		
IC 3		
IC 4		
IC 5		
IC 6		
IC 7		
IC 8		
IC 9	MC7400P	4x2 INPUTS NAND GATE
IC 10	MC7401P	4x2 INPUTS NAND OPEN COLLECTOR GATE
IC 11	MC7400P	4x2 INPUTS NAND GATE
IC 12	MC7495P	4 BITS SHIFT REGISTER
IC 13	MC7495P	" " " "
IC 14		
IC 15	MC7400P	4x2 INPUTS NAND GATE
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21	MC7400P	4x2 INPUTS NAND GATE
IC 22		
IC 23		
IC 24		
IC 25	MC7473P	DUAL TYPE JK FLIP FLOP
IC 26	MC7495P	4 BITS SHIFT REGISTER
IC 27	MC7495P	" " " "
IC 28	MC7400P	4x2 INPUTS NAND GATE
IC 29		
IC 30	MC7479P	DUAL TYPE D FLIP FLOP
IC 31	MC7400P	4x2 INPUTS NAND GATE
IC 32		
IC 33		
IC 34		
IC 35	MC7402P	4x2 INPUTS NOR GATE
IC 36		
IC 37	MC7402P	4x2 INPUTS NOR GATE
IC 38	MC7400P	4x2 INPUTS NAND GATE
IC 39	MC7400P	4x2 INPUTS NAND GATE
IC 40	MC7400P	" " " "
IC 41		
IC 42		

(1) FOR ABOES CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS ARE PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION
R0	Carbonate	1K	± 5%	250mW	250V	STYLE 25 PHILIPS
R1	"	1K	± 5%	250mW	250V	" " " "

DESIGNER: L.CHARRIER	NAME: INTERFACES DATA PROCESSOR Δ→PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M.VILLERET		C SIZE — NB3 DRAWING NO. — 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC7401P	4x2 INPUTS NAND OPEN COLLECTOR GATE
IC 2	MC7495	4 BITS SHIFT REGISTER
IC 3	MC7495	" " " "
IC 4	MC7400P	4x2 INPUTS NAND GATE
IC 5	MC7473P	4 BITS COUNTER
IC 6	MC7493P	" " "
IC 7		
IC 8		
IC 9	MC7400P	4x2 INPUTS NAND GATE
IC 10	MC7402P	2x2 INPUTS NOR GATE
IC 11	MC7404P	HEX INVERTER
IC 12	MC7400P	4x2 INPUTS NAND GATE
IC 13	MC7493P	4 BITS COUNTER
IC 14	NE565A	PHASE LOCK LOOP
IC 15	MC7400P	4x2 INPUTS NAND GATE
IC 16	MC7495P	4 BITS SHIFT REGISTER
IC 17	MC7495P	" " " "
IC 18	MC7495P	" " " "
IC 19	MC7495P	" " " "
IC 20	MC7495P	" " " "
IC 21	MC7495P	" " " "
IC 22		
IC 23		
IC 24		
IC 25		
IC 26		
IC 27		
IC 28		
IC 29	MC7400P	4x2 INPUTS NAND GATE
IC 30	MC7402P	4x2 INPUTS NOR GATE
IC 31	MC7404P	HEX INVERTER
IC 32	MC7492P	DIVIDE BY TWELVE COUNTER
IC 33	MCA400P	4x2 INPUTS NAND GATE
IC 34	MC7404P	HEX INVERTER
IC 35	MC7400P	4x2 INPUTS NAND GATE
IC 36		
IC 37	MC7402P	4x2 INPUTS NOR GATE
IC 38	MC7473P	DUAL TYPE JK FLIP FLOP
IC 39	MC7402P	4x2 INPUTS NOR GATE
IC 40	MC7493P	4 BITS COUNTER
IC 41	MC7402P	4x2 INPUTS NOR GATE
IC 42	MC7402P	" " "

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION	
C1	Ceramic	2.2nF	-20+100%		40V	2222 624 0.3222	PHILIPS
C2	" "	4.9nF	-20+100%		40V	2222 624 03472	" "
C3	" "	10nF	-20+100%		40V	2222 629 03103	" "
C4	" "	1nF	-20+100%		40V	2222 629 03102	" "
C5	Metalized	100nF	±10%		250V	280 AEA 100K	" "
C6	Ceramic	10pF	± 2%		100V	2222 638 10109	" "
C7	" "	10pF	± 2%		100V	2222 638 10109	" "
P1	Carbon deposit	1KΩ	±10%	750mW		3006P	TRIMPOT
P2	" "	1000	"	" "		" "	" "
P3	" "	100Ω	"	" "		" "	" "
Q1	2N4124			300mW	VCB=30V	NPN TRANSISTOR	MOTOROLA
R1	Carbon deposit	4700	±5%	250mW	250V	STYLE 25	PHILIPS
R2	" "	4700	"	" "	" "	" "	" "
R3	" "	220	"	" "	" "	" "	" "
R4	" "	22Ω	"	" "	" "	" "	" "
R8	" "	10KΩ	"	" "	" "	" "	" "
R9	" "	1KΩ	"	" "	" "	" "	" "
R10	" "	10KΩ	"	" "	" "	" "	" "
R11	" "	4.7KΩ	"	" "	" "	" "	" "
R12	" "	470Ω	"	" "	" "	" "	" "
X1	MS14193	1.544000MHz	50Hz			63CCCN Northern electric	

DESSINER: L.CHARRIER	NAME: INTERFACES COUNTERS Δ → PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		DWG SIZE: C — DRAWING NO.: N B4 — 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC7454 P	4-W 2 INPUT AOI GATE
IC 2	MC7402 P	QUAD 2 INPUT NOR GATE
IC 3		
IC 4	MC7495 P	4 BIT UNIVERSAL SBIFT REGISTER
IC 5	MC7495 P	" " " "
IC 6	MC7495 P	" " " "
IC 7		
IC 8	MC7454 P	4-W 3 INPUT AOI GATE
IC 9	MC7402 P	QUAD 2 INPUT NOR GATE
IC 10	MC7400 P	QUAD 2 INPUT NAND GATE
IC 11	MC7495 P	4 BIT UNIVERSAL SHIFT REGISTER
IC 12	MC7495 P	" " " "
IC 13	MC7495 P	" " " "
IC 14	MC7402 P	QUAD 2 INPUT NOR GATE
IC 15		
IC 16		
IC 17		
IC 18	MC7402 P	QUAD 2 INPUT NOR GATE
IC 19	MC7420 P	DUAL 4 INPUT NAND GATE
IC 20	MC7400 P	QUAD 2 INPUT NAND GATE
IC 21	MC7402 P	QUAD 2-INPUT NOR GATE
IC 22	MC7402 P	" " "
IC 23	MC7402 P	" " "
IC 24		
IC 25		
IC 26	MC7402 P	QUAD 2 INPUT NOR GATE
IC 27	MC7402 P	" " "
IC 28	MC7479 P	DUAL TYPE D FLIP FLOP
IC 29		
IC 30	MC7402 P	QUAD 2 INPUT NOR GATE
IC 31	1702A	2048 BIT READ ONLY MEMORY INTEL
IC 32		
IC 33	MC7402 P	QUAD 2 INPUT NOR GATE
IC 34	MC7402 P	" " "
IC 35	MC7479 P	DUAL TYPE D FLIP-FLOP
IC 36	MC7402 P	QUAD 2 INPUT NOR GATE
IC 37	MC7402 P	" " "
IC 38		
IC 39		
IC 40	MC7402 P	QUAD 2 INPUT NOR GATE
IC 41	MC7402P	" " "
IC 42		

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION
C1		390pF	10%		100V	222 630 03391 PHILIPS
C1						NOT MARKED ON PRINTED CIRCUIT
CR1	IN4740		10%	1W	10V	ZENER DIODE MOTOROLA
CR2	IN5234		10%	.5W	6.2V	" " " "

DESIGNER: JC. DOMIEN	NAME: COMPRESSOR Δ→PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M VILLERET		DWG SIZE: C	DRAWING NO: NB5 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2.	MC 7400 P	4x2 INPUTS NAND GATES
IC 3	MC 7404 P	HEX INVERTERS
IC 4	MC 7400 P	4x2 INPUTS NAND GATES
IC 5	MC 7480 P	GATED FULL ADDER
IC 6	MC 7480 P	" " "
IC 7	MC 7473 P	DUAL J.K FLIP-FLOP
IC 8		
IC 9	MC 7479 P	DUAL D FLIP FLOP
IC 10	" "	" " "
IC 11	MC 7402 P	4x2 INPUTS NOR GATES
IC 12	MC 7479 P	DUAL D FLIP FLOP
IC 13	MC 7400 P	4x2 INPUTS NAND GATES
IC 14	" "	" " "
IC 15	" "	" " "
IC 16	MC 7404 P	HEX INVERTERS
IC 17		
IC 18	MC 7479 P	DUAL D FLIP FLOP
IC 19	MC 7495 P	4 BITS SHIFT REGISTER
IC 20	" "	" " "
IC 21	MC 7480 P	GATED FULL ADDER
IC 22	MC 7479 P	DUAL D FLIP FLOP
IC 23		
IC 24	MC 7404 P	HEX INVERTERS
IC 25	" "	" "
IC 26	MC 7479 P	DUAL D FLIP FLOP
IC 27	MC 7400 P	4x2 INPUTS NAND GATES
IC 28	MC 7402 P	4x2 INPUTS NOR GATES
IC 29	MC 7400 P	4x2 INPUTS NAND GATES
IC 30	MC 7402 P	4x2 INPUTS NOR GATES
IC 31	MC 7495 P	4 bits SHIFT REGISTER
IC 32	" "	" " "
IC 33	" "	" " "
IC 34	" "	" " "
IC 35	" "	" " "
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION
C_1		3.9nf	+2%		63V	279 AH C3 k9 PHILIPS
C_2		3.9nf	+2%		63V	" " " "
C_3		1nf	+2%		63V	279 AH C1 K " "
C_4		3.9nf	+2%		53V	279 AM C3 K_9 " "
C_5		470pf	±10%		100V	22630 03 471 " "
R_1		240Ω	5%	250mW	250V	CARBON DEPOSIT TYPE 25 PHILIPS
R_2		240Ω	"	"	"	" " " "
R_3		100Ω	"	"	"	" " " "
R_4		240Ω	"	"	"	" " " "

DESIGNER: N. FORGET	NAME: RECTIFIER Δ → PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M.VILLERET		DWG SIZE: C — N B7 1/1 — DRAWING NO

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NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2	MC 7454 P	4 WIDE 2 INPUT AND OR INVERT GATE
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	MC 7480 P	GATED FULL ADDER
IC 8		
IC 9	MC 7454 P	4 WIDE 2 INPUT AND OR INVERT GATE
IC 10	MC 7495 P	4 BITS SHIFT REGISTER
IC 11	" "	" " "
IC 12	" "	" " "
IC 13	" "	" " "
IC 14	" "	" " "
IC 15	" "	" " "
IC 16	" "	" " "
IC 17	" "	" " "
IC 18	" "	" " "
IC 19	" "	" " "
IC 20	" "	" " "
IC 21	" "	" " "
IC 22	" "	" " "
IC 23	" "	" " "
IC 24	" "	" " "
IC 25	" "	" " "
IC 26	" "	" " "
IC 27	MC 7479 P	DUAL D FLIP FLOP
IC 28	MC 7480 P	GATED FULL ADDER
IC 29		
IC 30	MC 7479 P	DUAL D FLIP FLOP
IC 31	MC 7404 P	HEX INVERTERS
IC 32	MC 7400 P	4x2 INPUT NAND GATE
IC 33	MC 7480 P	GATED FULL ADDER
IC 34	MC 7479 P	DUAL D FLIP FLOP
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N. FORGET	NAME: LOW PASS FILTER Δ—PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) — N B8 (DRAWING NO.) — 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2	MC 7495 P	4 BITS SHIFT REGISTER
IC 3	" "	" " "
IC 4		
IC 5	MC 7495 P	4 BITS SHIFT REGISTER
IC 6	" "	" " "
IC 7		
IC 8		
IC 9		
IC 10		
IC 11		
IC 12		
IC 13		
IC 14		
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22		
IC 23		
IC 24		
IC 25	MC 7402 P	4x2 INPUT NOR GATE
IC 26		
IC 27	MC 7402 P	4x2 INPUT NOR GATE
IC 28		
IC 29		
IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35		
IC 36		
IC 37	MC 7495 P	4 BITS SHIFT REGISTER
IC 38	" "	" " "
IC 39		
IC 40	MC 7495 P	4 BITS SHIFT REGISTER
IC 41	" "	" " "
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N FORGET	NAME: DELTA COUNTER Δ→PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M VILLERET		DWG SIZE: C DRAWING NO: NB9 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2	MC 7402 P	4x2 INPUT NOR GATE
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	MC 7479 P	DUAL D FLIP FLOP
IC 5	MC 7495 P	4 HITS SHIFT REGISTER
IC 6	" "	" " "
IC 7	" "	" "
IC 8	MC 7400 P	4x2 INPUT NAND GATE
IC 9	MC 7495 P	4 BITS SHIFT REGISTER
IC 10	MC 7400 P	4x2 INPUT NAND GATE
IC 11	MC 7404 P	HEX INVERTER
IC 12	MC 7480 P	GATED FULL ADDER
IC 13	" "	" " "
IC 14	MC 7495 P	4 BITS SHIFT REGISTER
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21	MC 7480 P	GATED FULL ADDER
IC 22	" "	" " "
IC 23	MC 7402 P	4x2 INPUT NOR GATE
IC 24	MC 7404 P	HEX INVERTER
IC 25	MC 7480 P	GATED FULL ADDER
IC 26	" "	" " "
IC 27	MC 7404 P	HEX INVERTER
IC 28	MC 7479 P	DUAL D FLIP FLOP
IC 29	MC 7495 P	4 BITS SHIFT REGISTER
IC 30	MC 7400 P	4x2 INPUT NAND GATE
IC 31	MC 7479 P	DUAL D FLIP FLOP
IC 32	MC 7400 P	4x2 INPUT NAND GATE
IC 33	" "	" " "
IC 34	MC 7479 P	DUAL D FLIP FLOP
IC 35	MC 7473 P	DUAL JK FLIP FLOP
IC 36		
IC 37	MC 7495 P	4 BITS SHIFT REGISTER
IC 38	" "	" " "
IC 39	" "	" " "
IC 40	" "	" " "
IC 41	" "	" " "
IC 42	" "	" " "

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N. FORGET	NAME: DIGITAL CVSD DECODER 16 KHZ Δ → PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M. VILLERET		DWG SIZE: C	DRAWING NO: N B10 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7495 P	4 BITS SHIFT REGISTER
IC 2	" "	" " "
IC 3	" "	" " "
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8		
IC 9	MC 7480 P	GATED FULL ADDER
IC 10	MC 7479 P	DUAL D FLIP FLOP
IC 11	MC 7480 P	GATED FULL ADDER
IC 12	" "	" " "
IC 13	MC 7479 P	DUAL D FLIP FLOP
IC 14	MC 7480 P	GATED FULL ADDER
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22		
IC 23	MC 7479 P	DUAL D FLIP FLOP
IC 24	MC 7480 P	GATED FULL ADDER
IC 25	MC 7480 P	GATED FULL ADDER
IC 26	MC 7400 P	4x2 INPUT NAND GATE
IC 27	MC 7404 P	HEX INVERTER
IC 28	MC 7480 P	GATED FULL ADDER
IC 29		
IC 30	MC 7480 P	GATED FULL ADDER
IC 31	MC 7400 P	4x2 INPUT NAND GATE
IC 32	MC 7479 P	DUAL D FLIP FLOP
IC 33	MC 7480 P	GATED FULL ADDER
IC 34	MC 7479 P	DUAL D FLIP FLOP
IC 35	MC 7400 P	4x2 INPUT NAND GATE
IC 36		
IC 37	MC 7402 P	4x2 INPUT NOR GATE
IC 38	MC 7479 P	DUAL D FLIP FLOP
IC 39	MC 7480 P	GATED FULL ADDER
IC 40	" "	" " "
IC 41	MC 7479 P	DUAL D FLIP FLOP
IC 42	MC 7480 P	GATED FULL ADDER

(1) FOR ADDED CLARITY, IC 8 IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N FORGET	NAME: DIGITAL CVSD DECODER 16 KHZ Δ→PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M VILLERET		DWG SIZE: C DRAWING NO: NB11 1/1

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NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7495 P	4 BITS SHIFT REGISTER
IC 2	" "	" " "
IC 3	" "	" " "
IC 4	" "	" " "
IC 5	MC 7480 P	GATED FULL ADDER
IC 6	MC 7479 P	DUAL D FLIP FLOP
IC 7	MC 7480 P	GATED FULL ADDER
IC 8		
IC 9	MC 7479 P	DUAL D FLIP FLOP
IC 10	MC 7404 P	HEX INVERTER
IC 11	MC 7480 P	GATED FULL ADDER
IC 12	MC 7400 P	4x2 INPUT NAND GATE
IC 13		
IC 14	MC 7473 P	DUAL TYPE JK FLIP FLOP
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21	MC 7480 P	GATED FULL ADDER
IC 22	" "	" " "
IC 23	MC 7479 P	DUAL D FLIP FLOP
IC 24	MC 7404 P	HEX INVERTER
IC 25	MC 7473 P	DUAL TYPE JK FLIP FLOP
IC 26	MC 7400 P	4x2 INPUT NAND GATE
IC 27	MC 7480 P	GATED FULL ADDER
IC 28	MC 7479 P	DUAL D FLIP FLOP
IC 29	MC 7495 P	4 BITS SHIFT REGISTER
IC 30	" "	" " "
IC 31	" "	" " "
IC 32	" "	" " "
IC 33	" "	" " "
IC 34	" "	" " "
IC 35	" "	" " "
IC 36	MC 7480 P	GATED FULL ADDER
IC 37	MC 7479 P	DUAL D FLIP FLOP
IC 38	MC 7480 P	GATED FULL ADDER
IC 39	" "	" " "
IC 40	MC 7479 P	DUAL D FLIP FLOP
IC 41	MC 7400 P	4x2 INPUT NAND GATE
IC 42	MC 7495 P	4 BITS SHIFT REGISTER

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: JL GERARD	NAME: DIGITAL CVSD DECODER 19.2KHZ Δ → PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M VILLERET		C (DWG SIZE) NB14 (DRAWING NO) 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7495 P	4 BITS SHIFT REGISTER
IC 2	" "	" " "
IC 3	MC 7480 P	GATED FULL ADDER
IC 4	MC 7495 P	4 BITS SHIFT REGISTER
IC 5	" "	" "
IC 6	" "	" "
IC 7	" "	" "
IC 8	" "	" "
IC 9	MC 7400 P	4x2 INPUT NAND GATE
IC 10	MC 7495 P	4 BITS SHIFT REGISTER
IC 11	MC 7479 P	DUAL D FLIP FLOP
IC 12	MC 7480 P	GATED FULL ADDER
IC 13	MC 7479 P	DUAL D FLIP FLOP
IC 14	MC 7480 P	GATED FULL ADDER
IC 15	MC 7404 P	HEX INVERTER
IC 16	MC 7402 P	4x2 INPUT NOR GATE
IC 17	MC 7480 P	GATED FULL ADDER
IC 18	MC 7404 P	HEX INVERTER
IC 19	MC 7400 P	4x2 INPUT NAND GATE
IC 20	MC 7495 P	4 BITS SHIFT REGISTER
IC 21	" "	" " "
IC 22	MC 7400 P	4x2 INPUT NAND GATE
IC 23	MC 7479 P	DUAL D FLIP FLOP
IC 24	MC 7480 P	GATED FULL ADDER
IC 25	MC 7495 P	4 BITS SHIFT REGISTER
IC 26	" "	" " "
IC 27	MC 7404 P	HEX INVERTER
IC 28		
IC 29		
IC 30		
IC 31	MC 7480 P	GATED FULL ADDER
IC 32	MC 7479 P	DUAL D FLIP FLOP
IC 33	MC 7480 P	GATED FULL ADDER
IC 34	MC 7400 P	4x2 INPUT NAND GATE
IC 35	MC 7480 P	GATED FULL ADDER
IC 36		
IC 37		
IC 38		
IC 39	MC 7480 P	GATED FULL ADDER
IC 40	MC 7479 P	DUAL D FLIP FLOP
IC 41	MC 7480 P	GATED FULL ADDER
IC 42	MC 7479 P	DUAL D FLIP FLOP

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: JL GERARD	NAME: DIGITAL CVSD DECODER 19.2 KHZ Δ → PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M VILLERET		C (DWG SIZE) NB13 (DRAWING NO) 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7495 P	4 BITS SHIFT REGISTER
IC 2	" "	" " "
IC 3	" "	" " "
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8		
IC 9		
IC 10		
IC 11		
IC 12		
IC 13		
IC 14	MC 7495 P	4 BITS SHIFT REGISTER
IC 15	MC 7479 P	DUAL D FLIP FLOP
IC 16	MC 7480 P	GATED FULL ADDER
IC 17	" "	" " "
IC 18	MC 7479 P	DUAL D FLIP FLOP
IC 19	MC 7404 P	HEX INVERTER
IC 20	MC 7479 P	DUAL D FLIP FLDP
IC 21	MC 7473 P	DUAL JK FLIP FLOP
IC 22		
IC 23		
IC 24		
IC 25		
IC 26		
IC 27		
IC 28		
IC 29	MC 7402 P	4x2 INPUT NOR GATE
IC 30	MC 7400 P	4x2 INPUT NAND GATE
IC 31	" "	" " "
IC 32	MC 7480 P	GATED FULL ADDER
IC 33	" "	" "
IC 34	MC 7479 P	DUAL D FLIP FLOP
IC 35	MC 7480 P	GATED FULL ADDER
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N FORGET	NAME: DIGITAL CVSD DECODER 16KHZ Δ→PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		DWG SIZE: C DRAWING NO: NB12 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7480 P	GATED FULL ADDER
IC 2	MC 7479 P	DUAL D FLIP FLOP
IC 3	MC 7495 P	4 BITS SRIFT REGISTER
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8	MC 7400 P	4x2 INPUT NAND GATE
IC 9	MC 7480 P	GATED FULL ADDER
IC 10	MC 7404 P	BEN INVERTER
IC 11	MC 7400 P	4x2 INPUT NAND GATE
IC 12	MC 7479 P	DUAL D FLIP FLOP
IC 13	MC 7480 P	GATED FULL ADDER
IC 14		
IC 15	MC 7402 P	4x2 INPUT NOR GATE
IC 16	MC 7479 P	DUAL D FLIP FLOP
IC 17		
IC 18		
IC 19	MC 7480 P	GATED FULL ADDER
IC 20		
IC 21		
IC 22	MC 7402 P	4x2 INPUT NOR GATE
IC 23	MC 7480 P	GATED FULL ADDER
IC 24	MC 7479 P	DUAL D FLIP FLOP
IC 25	MC 7480 P	GATED FULL ADDER
IC 26	MC 7404 P	HEX INVERTER
IC 27		
IC 28		
IC 29	MC 7400 P	4x2 INPUT NAND GATE
IC 30	MC 7479 P	DUAL D FLIP FLOP
IC 31	MC 7495 P	4 BIT SHIFT REGISTER
IC 32	" "	" " "
IC 33	" "	" " "
IC 34	" "	" " "
IC 35	" "	" " "
IC 36	MC 7402 P	4x2 INPUT NOR GATE
IC 37	MC 7480 P	GATED FULL ADDER
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: JL.GERARD

APPROVED: M.VILLERET

NAME: DIGITAL CVSD DECODER 19.2 KHZ Δ→PCM

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA

DWG SIZE: C

DRAWING NO: NB 15 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2	MC 7495 P	4 BITS SHIFT REGISTER
IC 3	" "	" " "
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8	" "	" " "
IC 9	MC 7400 P	4x2 INPUT NAND GATE
IC 10	MC 7404 P	HEX INVERTER
IC 11	MC 7480 P	GATED FULL ADDER
IC 12	" "	" " "
IC 13	" "	" " "
IC 14	" "	" " "
IC 15	MC 7402 P	4x2 INPUT NOR GATE
IC 16	MC 7495 P	4 BITS SHIFT REGISTER
IC 17	" "	" " "
IC 18	MC 7480 P	GATED FULL ADDER
IC 19	MC 7479 P	DUAL D FLIP FLOP
IC 20		
IC 21	MC 7479 P	DUAL D FLIP FLOP
IC 22	MC 7404 P	HEX INVERTER
IC 23	MC 7400 P	4x2 INPUT NAND GATE
IC 24	MC 7479 P	DUAL D FLIP FLOP
IC 25	MC 7480 P	GATED FULL ADDER
IC 26	MC 7479 P	DUAL D FLIP FLOP
IC 27		
IC 28		
IC 29	MC 7402 P	4x2 INPUT NOR GATE
IC 30	MC 7400 P	4x2 INPUT NAND GATE
IC 31	MC 7495 P	4 BITS SHIFT REGISTER
IC 32	" "	" " "
IC 33	" "	" " "
IC 34	" "	" " "
IC 35	" "	" " "
IC 36		
IC 37		
IC 38		
IC 39	MC 7480 P	GATED FULL ADDER
IC 40	MC 7479 P	DUAL D FLIP FLOP
IC 41	MC 7480 P	GATED FULL ADDER
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N. FORGET	NAME: DIGITAL CVSD DECODER 32 KHZ Δ → PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M. VILLERET		C (DWG SIZE)	N B16 (DRAWING NO.) 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7479 P	DUAL D FLIP FLOP
IC 2	MC 7480 P	GATED FULL ADDER
IC 3	" "	" " "
IC 4	MC 7495 P	4 HITS SHIFT REGISTER
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8	" "	" " "
IC 9	" "	" " "
IC 10	" "	" " "
IC 11	" "	" " "
IC 12	" "	" " "
IC 13	" "	" " "
IC 14	" "	" " "
IC 15	" "	" " "
IC 16	" "	" " "
IC 17	" "	" " "
IC 18	" "	" " "
IC 19	MC 7479 P	DUAL D FLIP FLOP
IC 20	MC 7480 P	GATED FULL ADDER
IC 21	" "	" " "
IC 22	" "	" " "
IC 23	" "	" " "
IC 24	" "	" " "
IC 25	" "	" " "
IC 26	" "	" " "
IC 27	MC 7479 P	DUAL D FLIP FLOP
IC 28	" "	" " "
IC 29	" "	" " "
IC 30	" "	" " "
IC 31	MC 7400 P	4x2 INPUT NAND GATE
IC 32	MC 7404 P	HEX INVERTER
IC 33	MC 7400 P	4x2 INPUT NAND GATE
IC 34	" "	" " "
IC 35	MC 7404 P	HEX INVERTER
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) RF EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N. FORGET	NAME: DIGITAL CVSD DECODER 32 KHZ Δ → PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) · N B17 1/1 (DRAWING NO.)

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7480 P	GATED FULL ADDER
IC 2	MC 7479 P	DUAL D FLIP FLOP
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8	MC 7404 P	HEX INVERTER
IC 9	MC 7402 P	4x2 INPUT NOR GATE
IC 10	MC 7480 P	GATED FULL ADDER
IC 11		
IC 12	MC 7400 P	4x2 INPUT NAND GATE
IC 13		
IC 14		
IC 15		
IC 16		
IC 17		
IC 18	MC 7479 P	DUAL D FLIP FLOP
IC 19	MC 7480 P	GATED FULL ADDER
IC 20	MC 7400 P	4x2 INPUT NAND GATE
IC 21	MC 7473 P	DUAL JK FLIP FLOP
IC 22		
IC 23	MC 7400 P	4x2 INPUT NAND GATE
IC 24	MC 7402 P	4x2 INPUT NOR GATE
IC 25		
IC 26		
IC 27		
IC 28		
IC 29		
IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: J.L.GÉRARD	NAME: DIGITAL CVSD CODER 38.4 KHZ PCM → Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) — N T16 (DRAWING NO) — 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7404 P	HEX INVERTER
IC 2	MC 7480 P	GATED FULL ADDER
IC 3	MC 7479 P	DUAL D FLIP FLOP
IC 4	MC 7480 P	GATED FULL ADDER
IC 5	" "	" " "
IC 6	MC 7479 P	DUAL D FLIP FLOP
IC 7	MC 7480 P	GATED FULL ADDER
IC 8	MC 7495 P	4 BITS SHIFT REGISTER
IC 9	" "	" " "
IC 10	" "	" " "
IC 11	" "	" " "
IC 12	" "	" " "
IC 13	" "	" " "
IC 14	" "	" " "
IC 15		
IC 16		
IC 17	MC 7400 P	4x2 INPUT NAND GATE
IC 18		
IC 19	MC 7495	4 BITS SHIFT REGISTER
IC 20	" "	" " "
IC 21	" "	" " "
IC 22	MC 7400 P	4x2 INPUT NAND GATE
IC 23	MC 7479 P	DUAL D FLIP PLOP
IC 24	MC 7480 P	GATED FULL ADDER
IC 25	" "	" " "
IC 26	MC 7404 P	HEX INVERTER
IC 27	MC 7480 P	GATED FULL ADDER
IC 28	" "	" " "
IC 29		
IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35		
IC 36	MC 7480 P	GATED FULL ADDER
IC 37	MC 7479 P	DUAL D FLIP FLOP
IC 38	MC 7480 P	GATED FULL ADDER
IC 39	MC 7479 P	DUAL D FLIP FLOP
IC 40	MC 7400 P	4x2 INPUT NAND GATE
IC 41	MC 7479 P	DUAL D FLIP FLOP
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N. FORGET	NAME: DIGITAL CVSD DECODER 32KHZ Δ → PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) — N B18 (DRAWING NO.) 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7495 P	4 BITS SHIFT REGISTER
IC 2	" "	" " "
IC 3	" "	" " "
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8	MC 7402 P	4x2 INPUT NOR GATE
IC 9	MC 7400 P	4x2 INPUT NAND GATE
IC 10	MC 7480 P	GATED FULL ADDER
IC 11	MC 7479 P	DUAL D FLIP FLOP
IC 12	MC 7404 P	HEX INVERTER
IC 13	MC 7480 P	GATED FULL ADDER
IC 14	" "	" " "
IC 15		
IC 16	MC 7479 P	DUAL D FLIP FLOP
IC 17	MC 7495 P	4 BITS SHIFT REGISTER
IC 18	" "	" " "
IC 19	MC 7480 P	GATED FULL ADDER
IC 20	MC 7479 P	DUAL D FLIP FLOP
IC 21		
IC 22	MC 7400 P	4x2 INPUT NAND GATE
IC 23	MC 7480 P	GATED FULL ADDER
IC 24	MC 7495 P	4 BITS SHIFT REGISTER
IC 25	" "	" " "
IC 26	" "	" " "
IC 27	" "	" " "
IC 28	" "	" " "
IC 29	MC 7402 P	4x2 INPUT NOR GATE
IC 30	MC 7400 P	4x2 INPUT NAND GATE
IC 31	MC 7473 P	DUAL JK FLIP FLOP
IC 32	MC 7480 P	GATED FULL ADDER
IC 33	MC 7400 P	4x2 INPUT NAND GATE
IC 34	MC 7480 P	GATED FULL ADDER
IC 35	" "	" " "
IC 36		
IC 37		
IC 38	MC 7404 P	HEX INVERTER
IC 39		
IC 40		
IC 41	MC 7479 P	DUAL D FLIP FLOP
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N.FORGET	NAME: DIGITAL CVSD DECODER 38.4 KHZ Δ → PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M.VILLERET		C (DWG SIZE)	N B19 1/1 (DRAWING NO.)

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7480 P	GATED FULL ADDER
IC 2	" "	" " "
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8	MC 7404 P	HEX INVERTER
IC 9	MC 7479 P	DUAL D FLIP FLOP
IC 10	MC 7480 P	GATED FULL ADDER
IC 11	MC 7479 P	DUAL D FLIP FLOP
IC 12	MC 7480 P	GATED FULL ADDER
IC 13	MC 7473 P	DUAL JK FLIP FLOP
IC 14	MC 7400 P	4x2 INPUT NAND GATE
IC 15	MC 7495 P	4 BITS SHIFT REGISTER
IC 16	" "	" " "
IC 17	" "	" " "
IC 18	" "	" " "
IC 19	" "	" " "
IC 20	" "	" " "
IC 21	" "	" " "
IC 22	MC 7479 P	DUAL D FLIP FLOP
IC 23	MC 7495 P	4 BITS SHIFT REGISTER
IC 24	" "	" " "
IC 25	" "	" " "
IC 26	" "	" " "
IC 27	MC 7479 P	DUAL D FLIP FLOP
IC 28	MC 7400 P	4x2 INPUT NAND GATE
IC 29	MC 7404 P	HEX INVERTER
IC 30	MC 7400 P	4x2 INPUT NAND GATE
IC 31	MC 7479 P	DUAL D FLIP FLOP
IC 32	" "	" " "
IC 33	" "	" " "
IC 34	MC 7480 P	GATED FULL ADDER
IC 35	" "	" " "
IC 36	" "	" " "
IC 37	" "	" " "
IC 38	" "	" " "
IC 39	" "	" " "
IC 40	" "	" " "
IC 41	" "	" " "
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N. FORGET	NAME: DIGITAL CVSD DECODER 38.4KHZ Δ ⟶ PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M VILLERET		C (DWG SIZE) — N B20 1/1 (DRAWING NO)

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7404 P	HEX INVERTER
IC 2	MC 7400 P	4x2 INPUT NAND GATES
IC 3	MC 7480 P	GATED FULL ADDER
IC 4	MC 7495 P	4 BITS SHIFT REGISTER
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8	MC 7480 P	GATED FULL ADDER
IC 9	" "	" " "
IC 10	MC 7479 P	DUAL D FLIP FLOP
IC 11	" "	" " "
IC 12	MC 7480 P	GATED FULL ADDER
IC 13	MC 7479 P	DUAL D FLIP FLOP
IC 14	MC 7495 P	4 BITS SHIFT REGISTER
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22	MC 7480 P	GATED FULL ADDER
IC 23		
IC 24	MC 7400 P	4x2 INPUT NAND GATE
IC 25	MC 7404 P	HEX INVERTER
IC 26	MC 7480 P	GATED FULL ADDER
IC 27	" "	" " "
IC 28	MC 7495 P	4 BITS SHIFT REGISTER
IC 29	MC 7479 P	DUAL D FLIP FLOP
IC 30	MC 7480 P	GATED FULL ADDER
IC 31	" "	" " "
IC 32	" "	" " "
IC 33	MC 7479 P	DUAL D FLIP FLOP
IC 34	" "	" " "
IC 35	MC 7495 P	4 BITS SRIFT REGISTER
IC 36	MC 7480 P	GATED FULL ADDER
IC 37	MC 7400 P	4x2 INPUT NAND GATE
IC 38	MC 7479 P	DUAL D FLIP FLOP
IC 39	MC 7495 P	4 BITS SRIFT REGISTER
IC 40	" "	" " "
IC 41	" "	" " "
IC 42	" "	" " "

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: N. FORGET	NAME: DIGITAL CVSD DECODER 38.4KHZ Δ→PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M. VILLERET		DWG SIZE: C	DRAWING NO: N B21 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2	MC 1741 CP1	OPERATIONAL AMPLIFIER
IC 3	MC 1709 CP	
IC 4	MC 7495 P	4 BITS SHIFT REGISTER
IC 5	MC 7400 P	4x2 INPUTS NAND GATE
IC 6	MC 7402 P	4x2 INPUTS NOR GATE
IC 7		
IC 8		
IC 9		
IC 10		
IC 11	MC1741 CP1	OPERATIONAL AMPLIFIER
IC 12		
IC 13		
IC 14		
IC 15		
IC 16		
IC 17		
IC 18	MC 7454 P	4 W 2 INPUTS AOI GATE
IC 19	MC 7400 P	4x2 INPUTS NAND GATE
IC 20	MC 7454 P	4 W 2 INPUTS AOI GATE
IC 21	MC 7402 P	4x2 INPUTS NOR GATE
IC 22		
IC 23		
IC 24	MC 1741CP1	OPERATIONAL AMPLIFIER
IC 25		
IC 26		
IC 27	MC 7479 P	DUAL TYPE D FLIP FLOP
IC 28	MC7404 P	HEX INVERTER
IC 29		
IC 30		
IC 31		
IC 32	MC 1741CP1	OPERATION AMPLIFIER
IC 33		
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39	MC 7495 P	4 BITS SRIFT REGISTER
IC 40	MC 7400 P	4x2 INPUTS NAND GATE
IC 41	MC 7402 P	4x2 INPUTS NOR GATE
IC 42	MC 7400 P	4x2 INPUTS NAND GATE

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION	
C1		1µF	10%		250V	280 AE A 10K	PHILIPS
C2		100nF	10%		100V	344 CHA 100K	" "
C3		100nF	10%		100V	344 CHA 100 K	" "
C4		68nF	2%		63V	295 AHC 68K	" "
C5		15nF	"		63V	295 AHC 15K	" "
C6		75nF	"		125V	295 AAC 75K	" "
C7		56nF	"		63V	295 AHC 56K	" "
C8		82nF	"		"	295 AHC 82K	" "
C9		39nF	"		"	295 AHC 39K	" "
C10		47nF	"		"	295 AHC 47K	" "
C11		68µF	±20%		15V	SPRAGUE 150 D	" "
C12		68µF	"		"	" "	" "
C13		4.7nF	10%		250V	280 AE A 4.7K	" "
C14		10nF	"		"	280 AE A10K	" "
C15		10nF	"		"	280 AE A 10K	" "
C16		10nF	"		"	280 AE A 10K	" "
C17		100nF	"		"	280AE A 100K	" "
C18		10µF	-10+50%		25V	426 ARRIO	" "
CR1	IN87A				23V	SIGNAL DIODE	MOTOROLA
CR2	IN87A				"	SIGNAL DIODE	" "
CR3	IN87A				"	SIGNAL DIODE	" "
L1		28mH	2%	13mA		UTCMS28	TAW
L2		17mH	"	15mA		UTC MS17	"
L3		19mH	"	15mA		UTC MS19	"
Q1	2N4124			300mW	VCB=30V	NPN TRANSISTOR	MOTOROLA
Q2	2N4124			"	"	" "	" "
Q3	2N4124			"	"	" "	" "
Q4	2N4124			"	"	" "	" "
Q5	2N4124			"	"	" "	" "
Q6	2N4124			"	"	" "	" "
Q7	2N4124			"	"	" "	" "
R1		4.7kΩ	5%	250mW	250V	CARBON DEPOSIT TYPE STYLE 25	PHILIPS
R2		4.7kΩ	"	"	"	" "	" "
R3		4.7kΩ	"	"	"	" "	" "
R4		4.7kΩ	"	"	"	" "	" "
C_{20}		100pf	±2%		100V	222263870101	PHILIPS
C_{19}		560pf	±10%		100V	222263003561	" "

DESIGNED: J.C. DOMIEN, N. FORGET	NAME: CVSD CODER DECODER	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) NB22 (DRAWING NO) 1/2

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2		
IC 3		
IC 4		
IC 5		
IC 6		
IC 7		
IC 8		
IC 9		
IC 10		
IC 11		
IC 12		
IC 13		
IC 14		
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22		
IC 23		
IC 24		
IC 25		
IC 26		
IC 27		
IC 28		
IC 29		
IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION
R5		4.7kΩ	5%	250mW	250V	CARBON DEPOSIT TYPE STYLE 25 PHILIPS
R6		36kΩ	"	"	"	" " " " "
R7		2.0kΩ	"	"	"	" " " " "
R8		20kΩ	"	"	"	" " " " "
R9		30kΩ	"	"	"	" " " " "
R10		30kΩ	"	"	"	" " " " "
R11		30kΩ	"	"	"	" " " " "
R12		30kΩ	"	"	"	" " " " "
R13		750Ω	"	"	"	" " " " "
R14		180kΩ	"	"	"	" " " " "
R15		10kΩ		"	"	" " " " "
R17		2.2kΩ	"	"	"	" " " " "
R18		22kΩ	"	"	"	" " " " "
R19		10kΩ	"	"	"	" " " " "
R20		100kΩ	"	"	"	" " " " "
R21		220kΩ	"	"	"	" " " " "
R22		680Ω	"	"	"	" " " " "
R24		2.2kΩ	"	"	"	" " " " "
R25		4.7kΩ	"	"	"	" " " " "
R26		4.7kΩ	"	"	"	" " " " "
R27		2kΩ ,	10%	750mW		TRIMMING POTENTIOMETERS-3006 BOURNS
R28		2kΩ	"	"		" " " " "
R29		680Ω	5%	250mW	250V	CARBON DEPOSIT TYPE STYLE 25 PHILIPS
R30		10kΩ	20%	100mW		TRIMMING POTENTIOMETERS 086BC10K ""
R31		220Ω	5%	1W	500V	CARBON DEPOSIT TYPE STYLE 52 ""
R32		680Ω	5%	250mW	250V	" " " " 25 ""
R33		10kΩ	20%	100mW		TRIMING POTENTIOMETERS 087BC 10K ""
R60		100kΩ	10%	750mW		" " " 3006 BOURNS
R130		50kΩ	"	"		" " " " ""
R240		10Ω	5%	250mW	250V	CARBON DEPOSIT TYPE STYLE 25 PHILIPS
R250		10Ω	"	"	"	" " " " ""

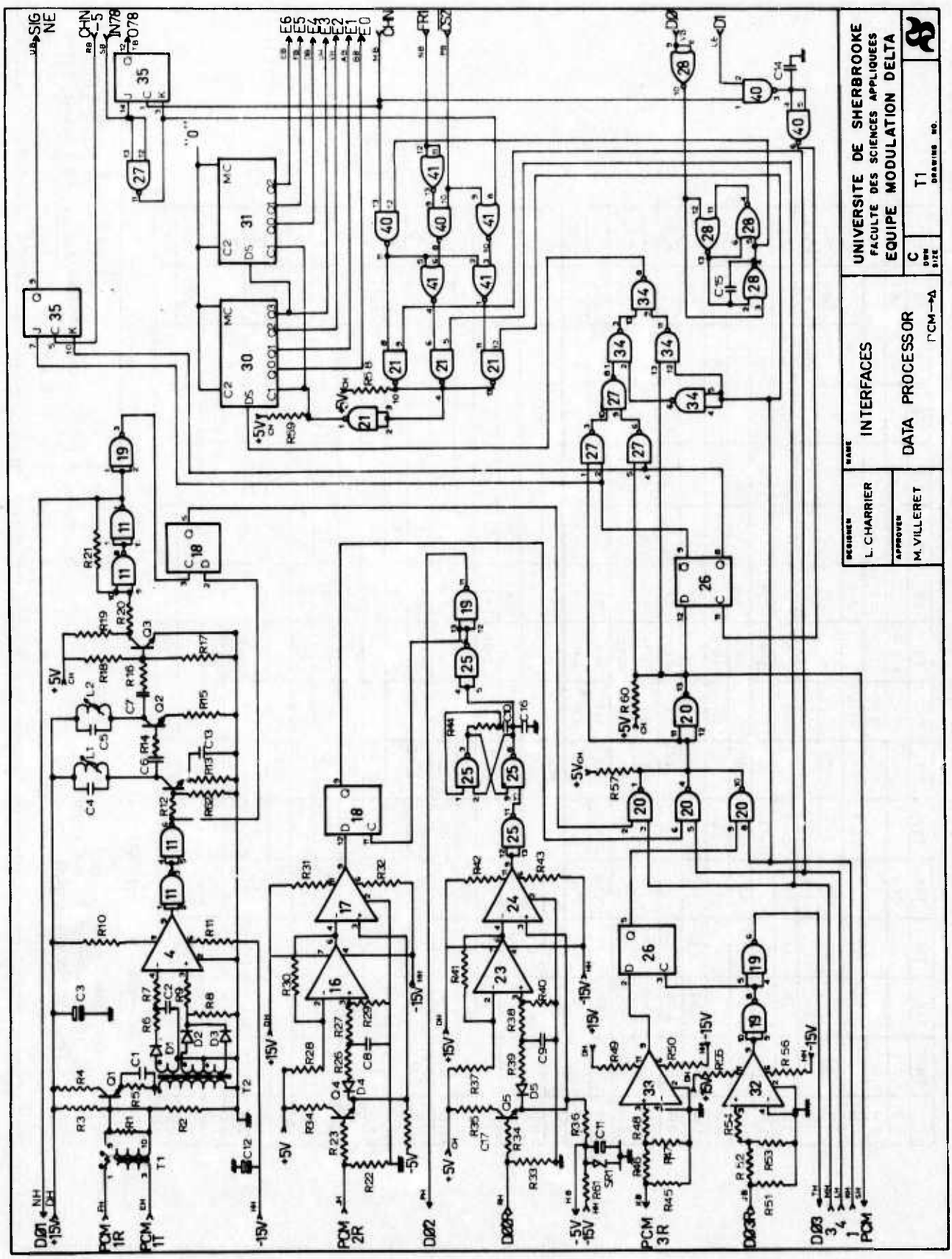
DESIGNER: JC. DOMIEN, N. FORGET	NAME: CVSD CODER DECODER	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M.VILLERET		C (DWG SIZE) NB22 (DRAWING NO) 2/2

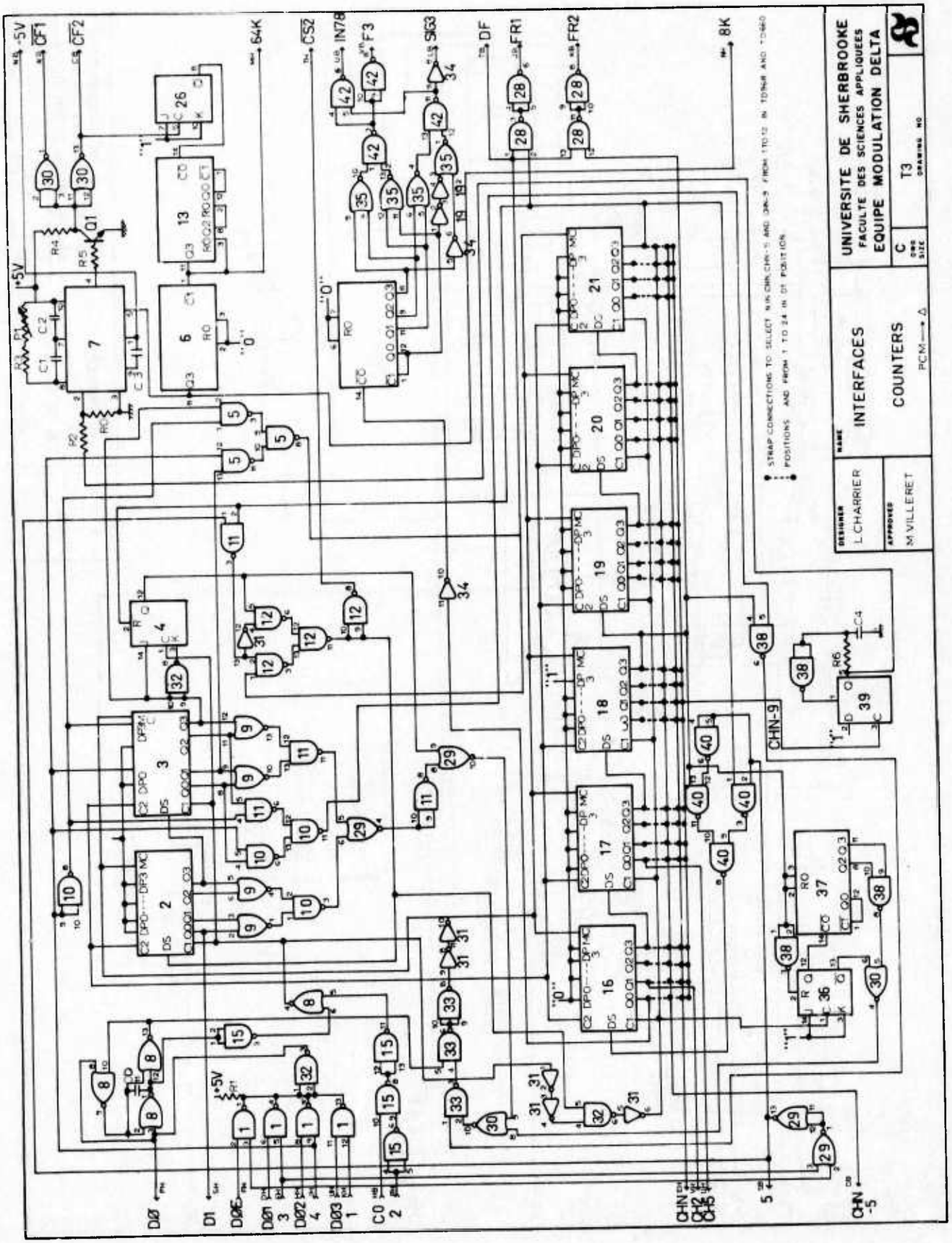
	T16	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T1
DH				CS9			CS27	64S18	I	8K	E2		DF	DØ1	+15V
EH	IC						S15		CS2	2	E1		F3	3	PCM1T
FH		SB38.4	$\overline{M\Delta}$		I12*		SB16		M2	2^{-1}	E0		PCM		PCM1R
HH	S4	MΔ	SL	SB32	S16	SB19.2			V	2^{1}			$\overline{CS2}$	DØ2	-15V
JH		S21		S19	CS20		S13		CS4				SIG3	4	PCM2R
KH		S24	MΔ	FE12*	CS18		S18	CS5	F				N	1	1
LH	LM	S6	$\overline{S}$		S3	FΔ1		SB19-32	CS3		-15V		FR1	DØ3	4
MH	S19	IC	$\overline{CS}$	Δ32	S1	$\overline{CS}$		SB38	$\overline{M\Delta}$				3	64K	3
NH	Δ38				S6		S6	SB16	S4				FR2	8K	DØ1
PH	MΔ	FΔ1 •	$\overline{M\Delta 2}$		S4			F	S6				4	DØ	DØ2
RH		Δ38 •	IC			CS22	S1	64S17	S5	64S17	E3		1	2	DØ2R
SH		CS14	S11	IC		CS21*	S3	SF5	S26	3	E5			D1	PCM
TH	S20		Δ32 •	S6	S21	IC	S8	64S2	S3	1	E4			$\overline{CS2}$	DØ3
UH		CS17		CS11	IC	S16	FΔ1 •	M2	S2	4				CH5	E3
VH			$\overline{M\Delta}$	FΔ1		$\overline{CS22}$	Δ16 •	64K	S1	SIGNE	2			CH2	E2
AB						$\overline{M\Delta}$									E1
BB						MΔ			64S17						E0
CB	$\overline{CF2}$		$\overline{CF2}$			$\overline{CF1}$	$\overline{CF1}$		$\overline{CF2}$	$\overline{CF2}$				$\overline{CF1}$	
DB		S12	CS9	$\overline{S}$		Δ19 •		CO32	S7	2^{5}	O78		AL	CHN-5	E4
EB	I12*	CS13	S1	$\overline{CS}$		S18		CS12	S8	2^{7}			CO	CHN	E6
FB	S1	CS16	S2	$\overline{M\Delta}$	$\overline{CS}$	$\overline{\Delta}$		CO16	S10	64S2	3		DØ		E5
HB	S26		S6	CS12		LM		CS17	S11	64K	E6			CO	-5V
JB	S6		S4	MΔ	S12			CO38	S12	CS3	1		CH5	FR1	DØ3R
KB	S5	S10		$\overline{M\Delta 2}$		CS18	S4	CS27	S13	M2	CHN-5		P	FR2	PCM3R
LB	CS17	LM	S10	SL		CS20	S7	CO19	S14	CS2	2^{5}			SIG3	D1
MB	CS15			CS8	S14	$\overline{M\Delta 2}$		CS22	S15	V	2^{7}			N	CHN
NB	S14		S8	S3				CS8	S16	64S15	2^{1}			-5V	FR*
PB	CS14		S21	S4		FS12*			S17	CS5	4				$\overline{CS2}$
RB	CS16*		CS11	$\overline{R}$	$\overline{\Delta}$			MΔ	S18	CS4	$\overline{CF1}$			$\overline{CF2}$	CHN-5
SB	S12		CS12		LM	S3		$\overline{M\Delta}$	S19	CS1				5	I78
TB	CS13	FS12*	CS8	S8	Δ19	S8		FΔ1	S20	I	8K			DF	O78
UB	S17	CS15	S15	FS12*	MΔ	S10	$\overline{MA}$		S21	64S18	CS1			I78	SIGNE
VB		FE12*	$\overline{R}$		$\overline{M\Delta 2}$	FE12*		64S15	S24	CSI	2^{-1}			F3	DØ

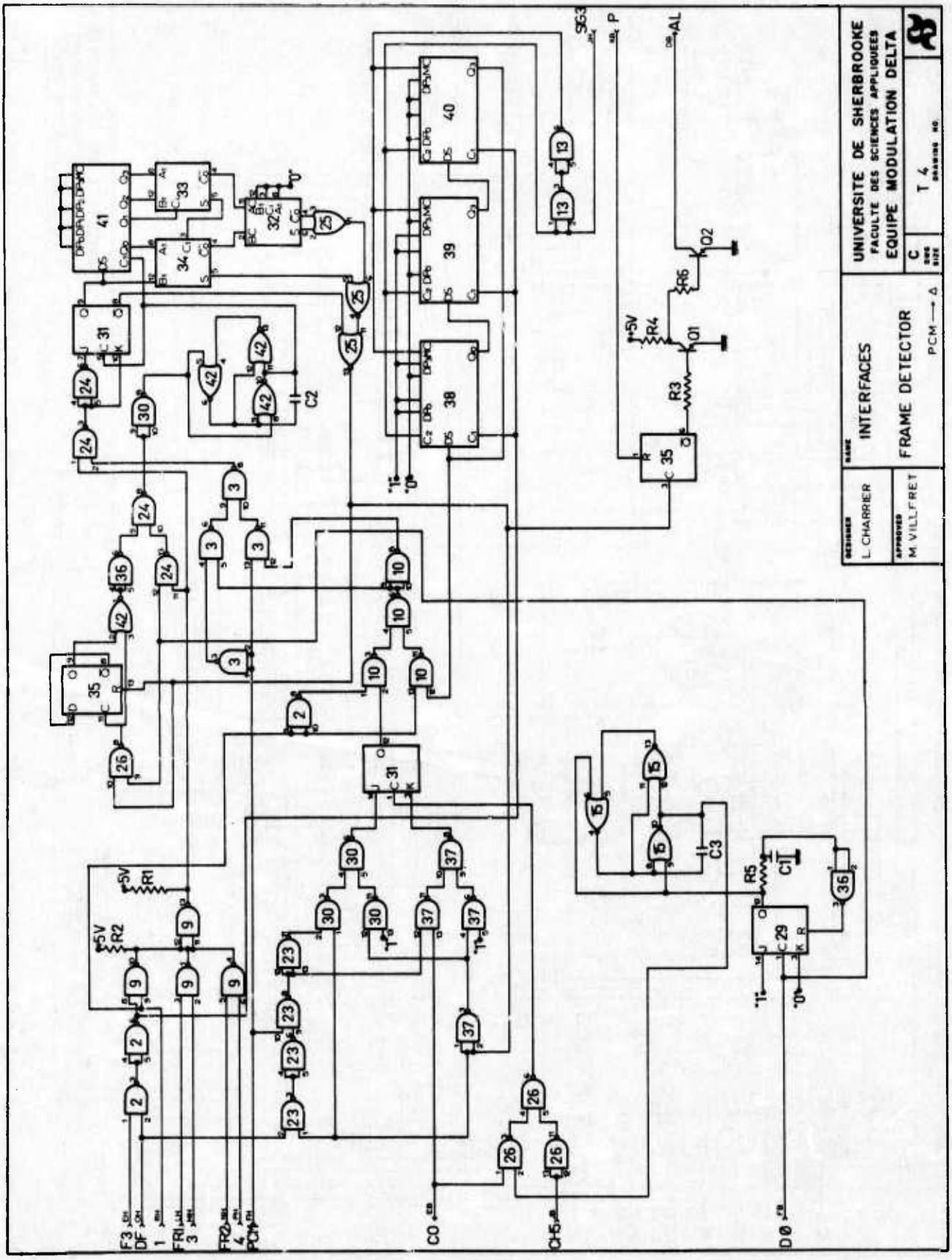
• Connected to board B22

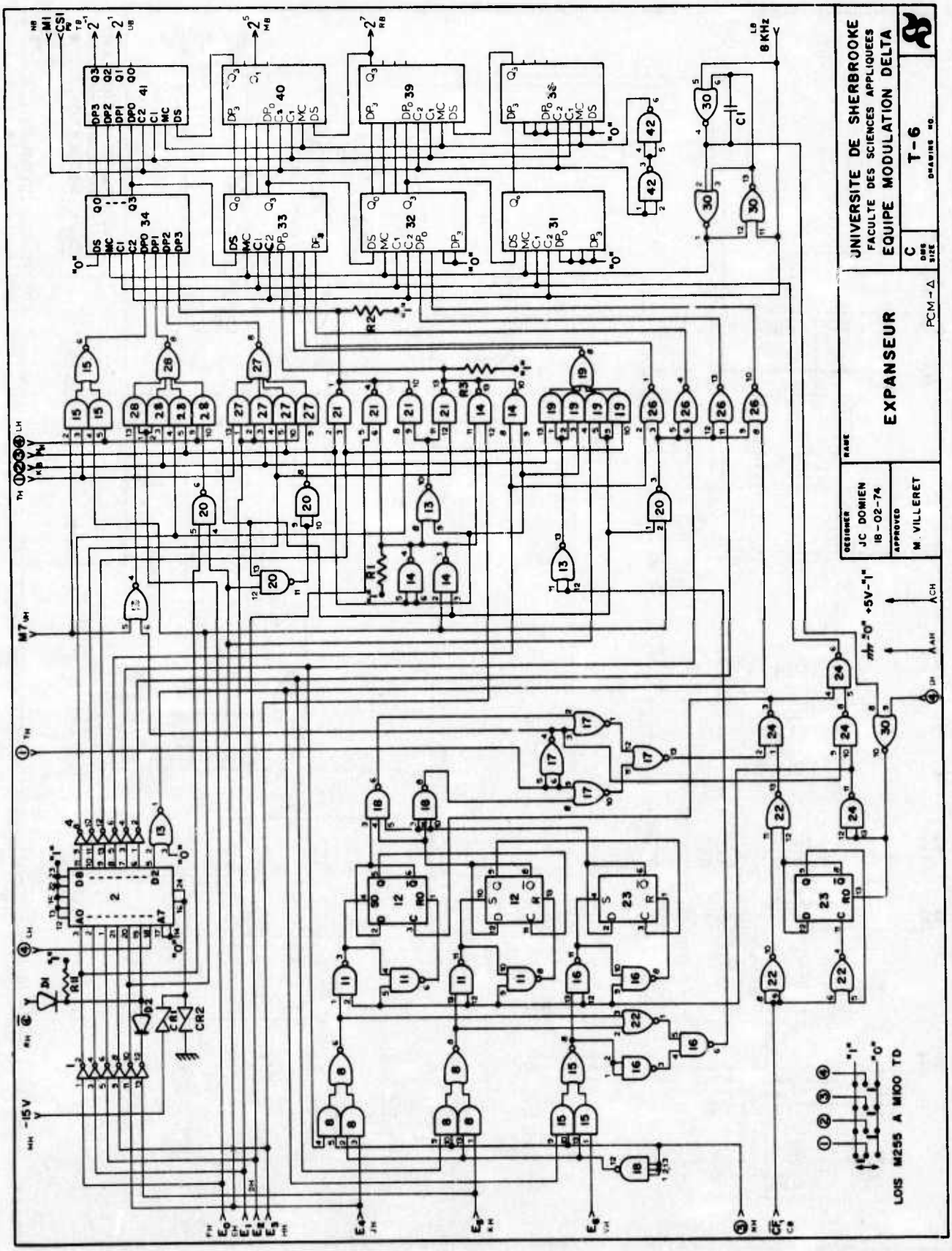
AH: GND for ony boords
BH: No connected for ony boords
CH: +5V for ony boards

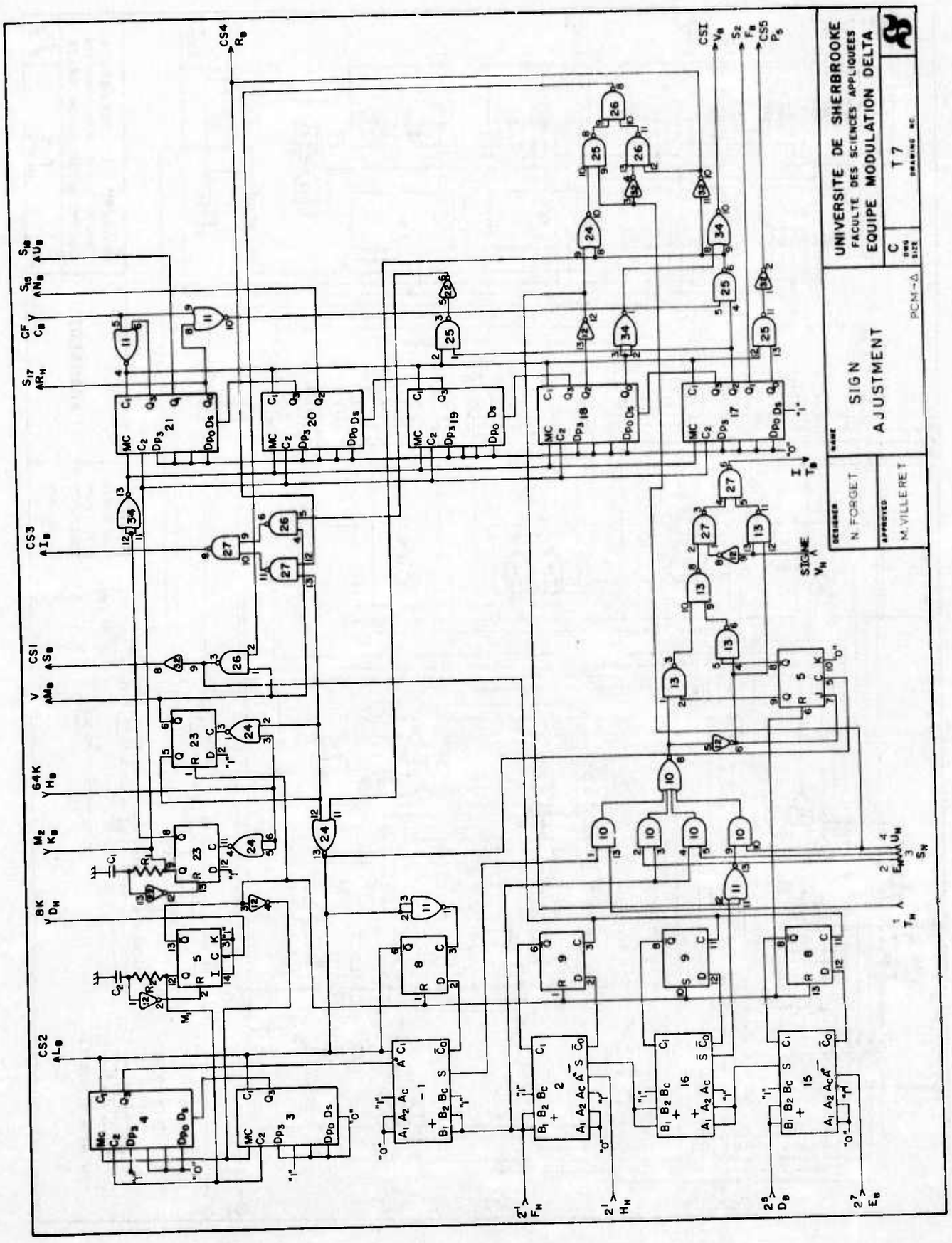
DESIGNER: L. CHARRIER	NAME: WRAP CONNECTIONS "T" BOARDS	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) — WT (DRAWING NO)

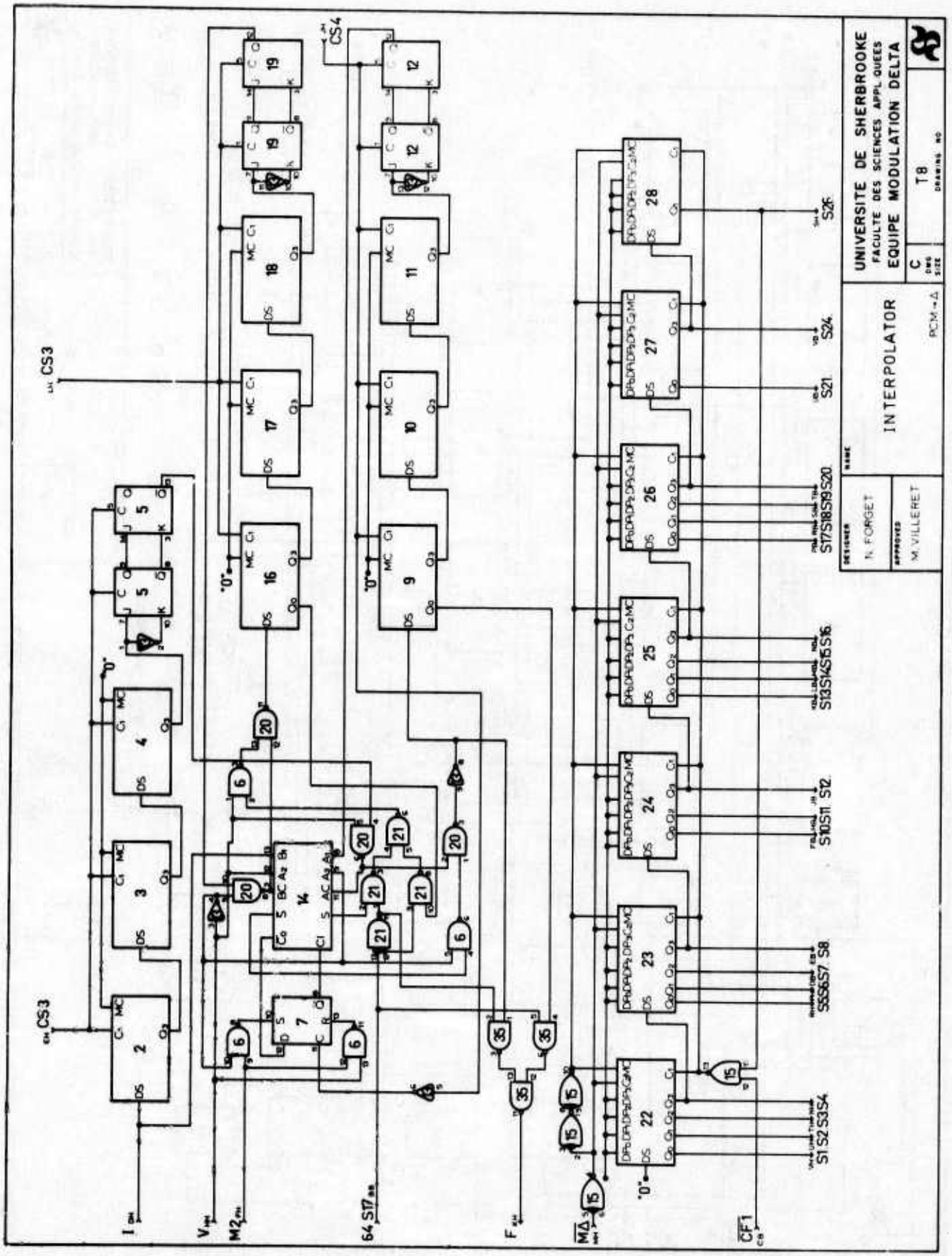

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DESIGNED L. CHARRIER
APPROVED M. VILLERET
NAME INTERFACES
DATA PROCESSOR
PCM→Δ
SIZE C
DRAWING NO. T1
SIGNE
CHN_5
IN78
OUT78
E6 E5 E4 E3 E2 E1 E0
CHN
FR1
FS2
D0
D1
PCM 1R
PCM 1T
PCM 2R
PCM 3R
PCM 3T
D01
D02
D03

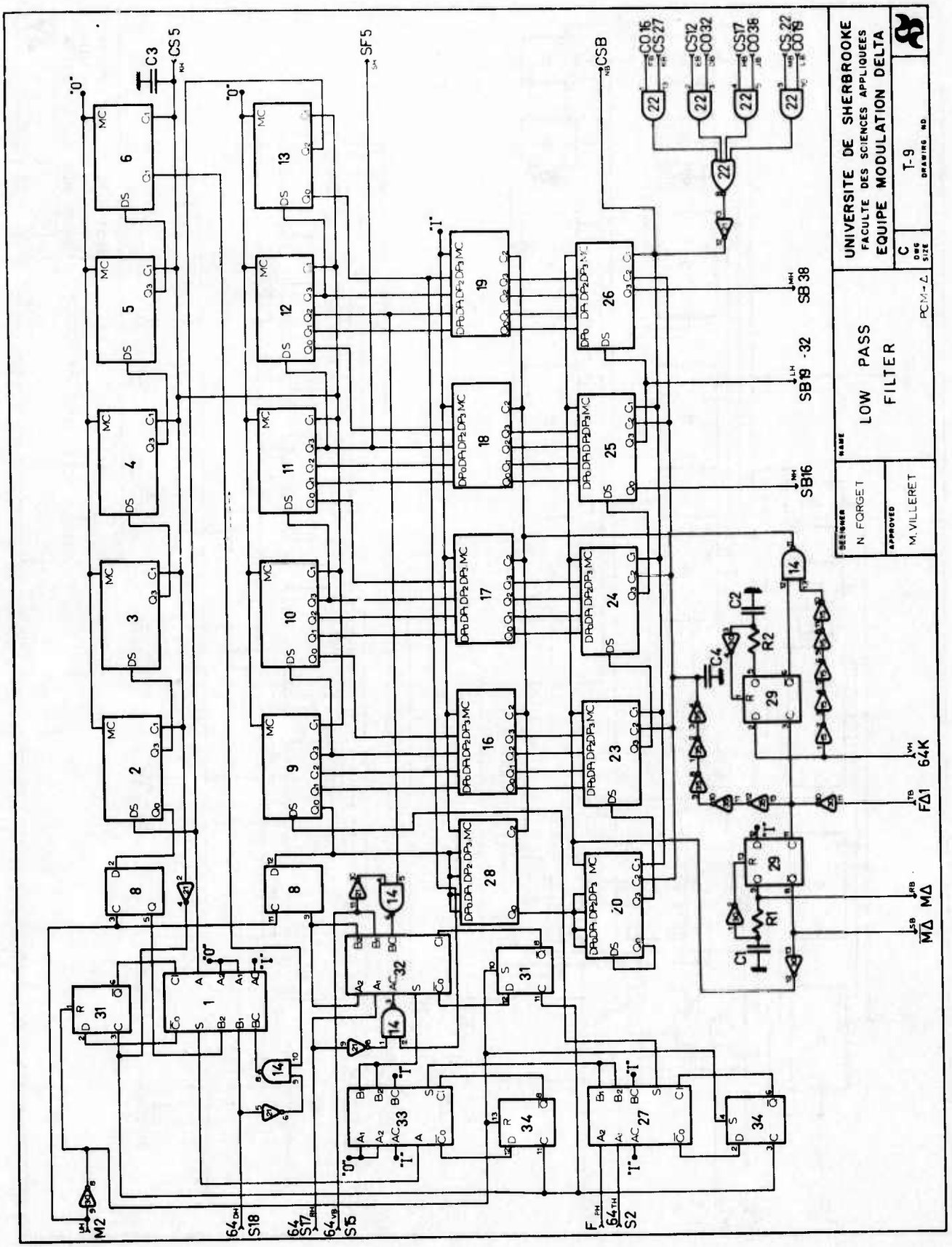

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
T3
INTERFACES
COUNTERS
PCM → Δ
L.CHARRIER
M.VILLERET
-5V
+5V
64K
8K
CS2
IN78
F3
SIG3
DF
FR1
FR2
CHN-9
CHN-5
D0
D1
D2
D3
C0
C1
C2
C3
5

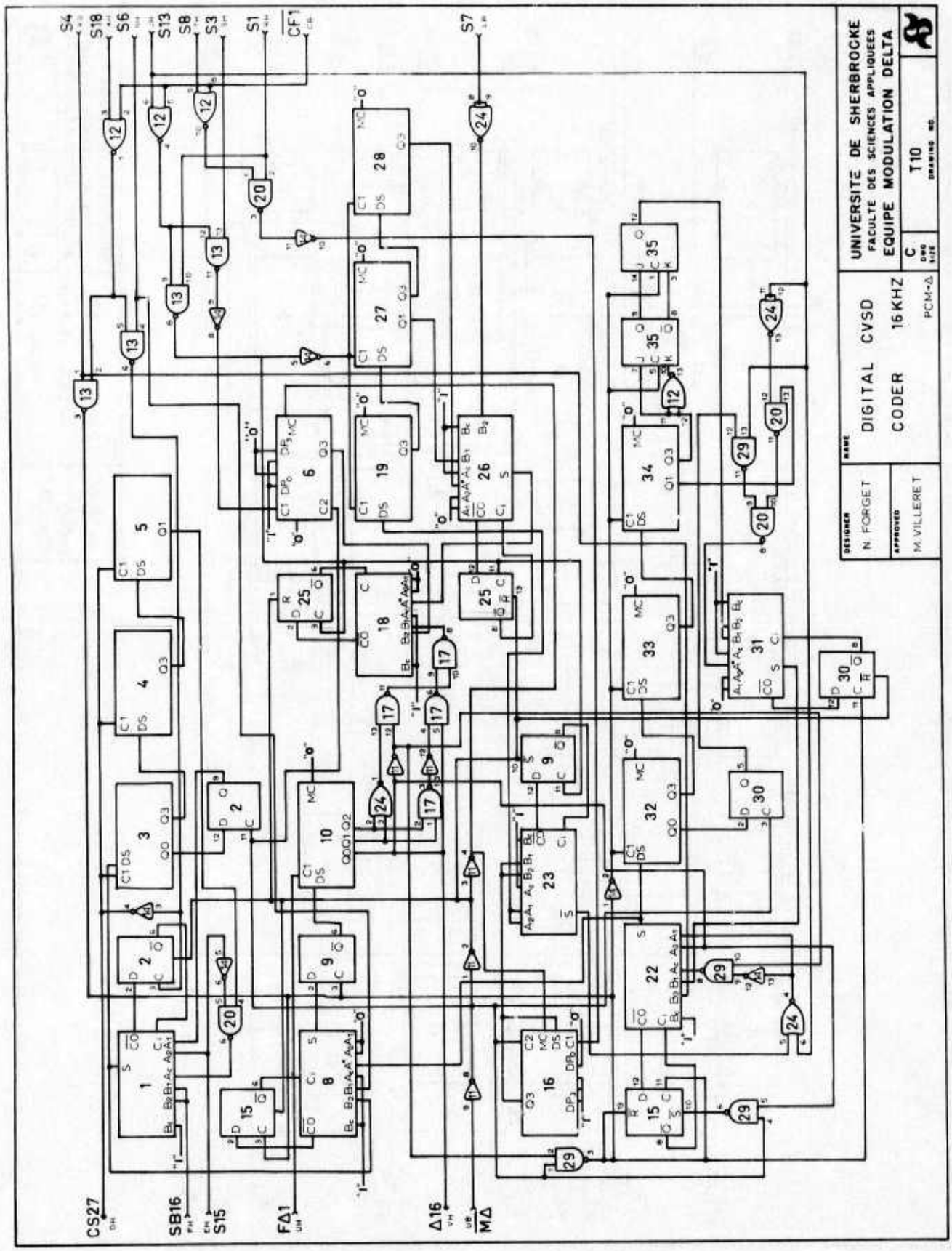

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
T 4
INTERFACES
FRAME DETECTOR
PCM — Δ
L. CHARRIER
M. VILLEFRET
F3
DF
1
FR1
3
FR2
4
PCM
CO
CH5
D0
AL
P
5V
R1
R2
R3
R4
R5
R6
C1
C2
C3
Q1
Q2

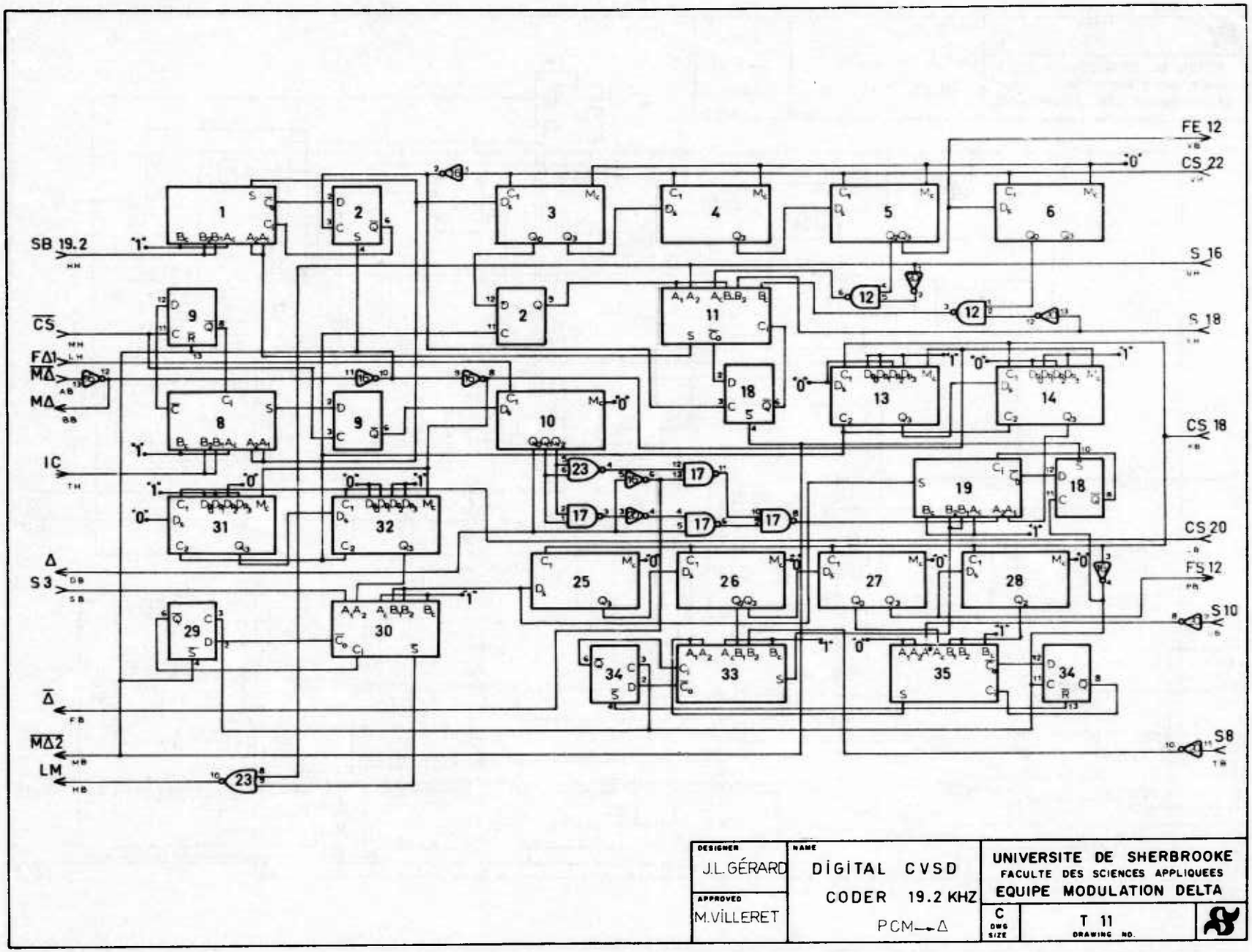

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
T-6
EXPANSEUR
PCM-Δ
JC DOMIEN
18-02-74
M. VILLERET
8 KHz
LOIS M255 A MIOO TD


UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
T 7
SIGN
AJUSTMENT
PCM-A
N. FORGET
M. VILLERET

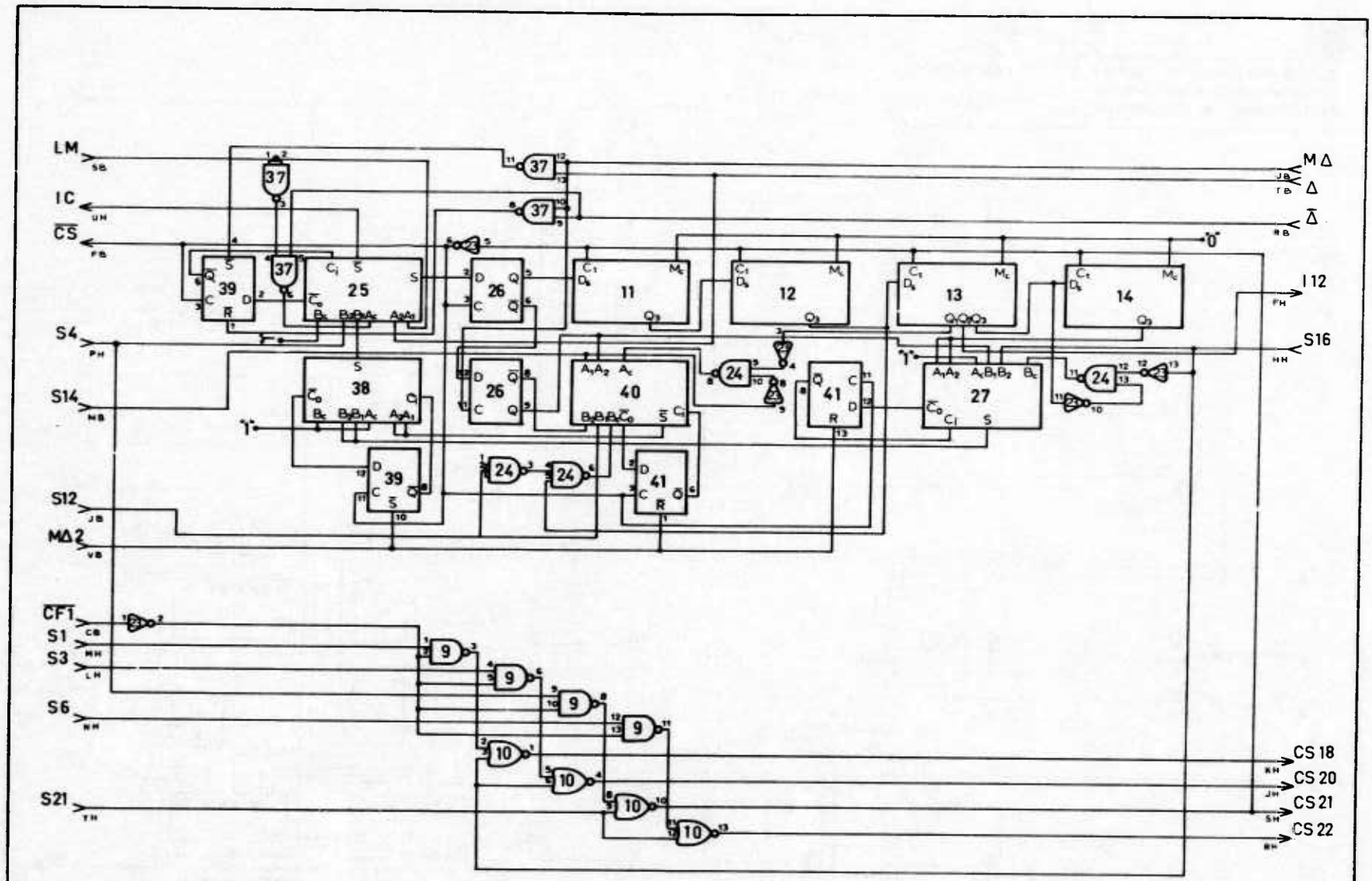

UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPL. QUÉES
EQUIPE MODULATION DELTA
INTERPOLATOR
PCM-Δ
N. FORGET
M. VILLERET
T8
CS3
CS4
I
V
M2
64 S17
F
MΔ
CF1
S1 S2 S3 S4
S5 S6 S7 S8
S9 S10 S11 S12
S13 S14 S15 S16
S17 S18 S19 S20
S21 S24
S25


UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
LOW PASS FILTER
PCM-Δ
DESIGNED N. FORGET
APPROVED M. VILLERET
T-9
C3
C2
C4
R2
R1
C1
CS5
SF5
CSB
CO15 CS27
CS12 CO32
CS17 CO36
CS22 CO16
SB38
SB19 -32
SB16
64K
FΔ1
MΔ
M2
S18
S17
S16
S2

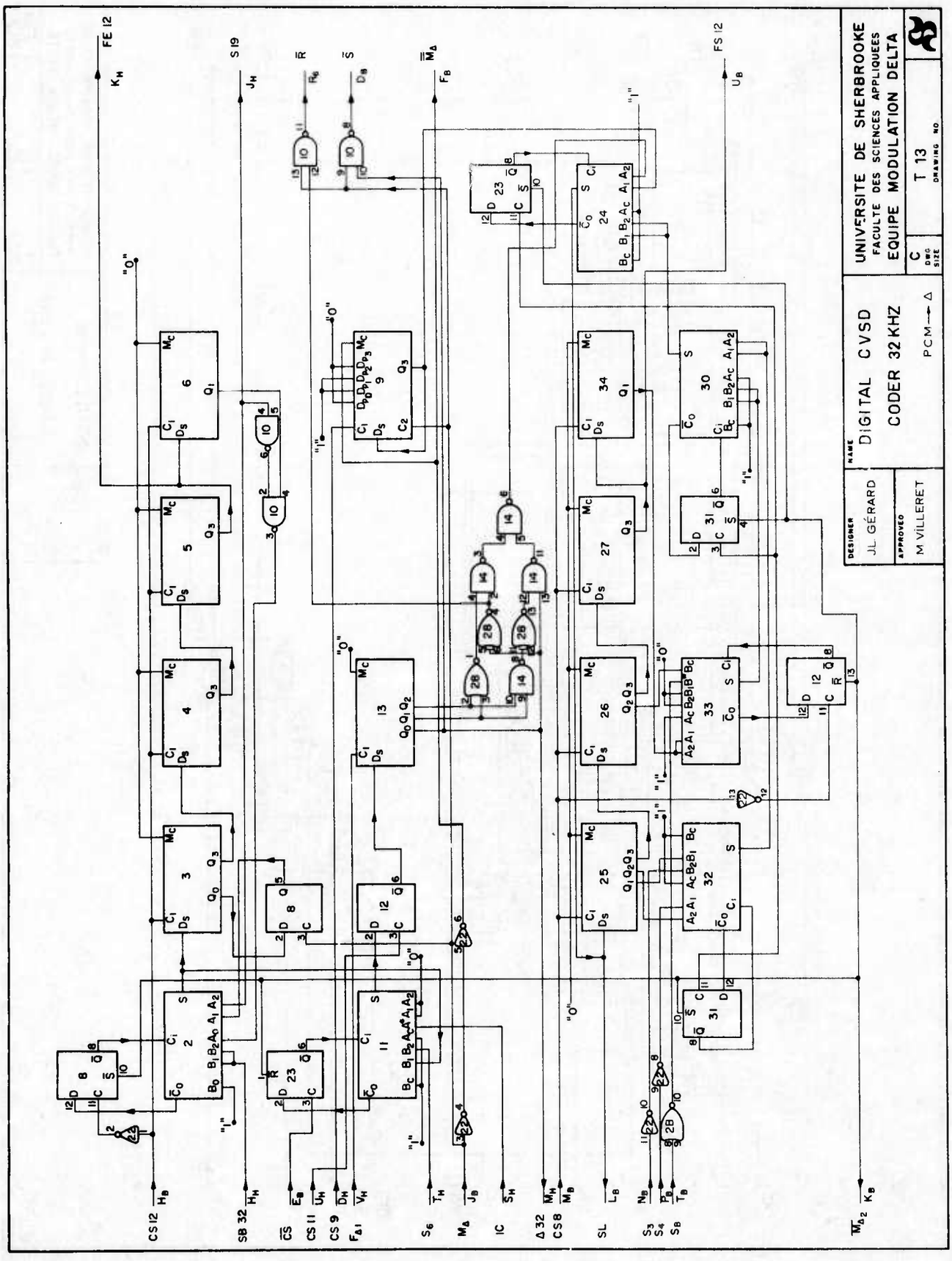

UNIVERSITE DE SHERBROCKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DIGITAL CVSD
CODER 16KHZ
PCM-Δ
T10
N. FORGET
M. VILLERET
S4
S18
S6
S13
S8
S3
S1
CF1
S7
CS27
SB16
S15
FΔ1
Δ16
MΔ

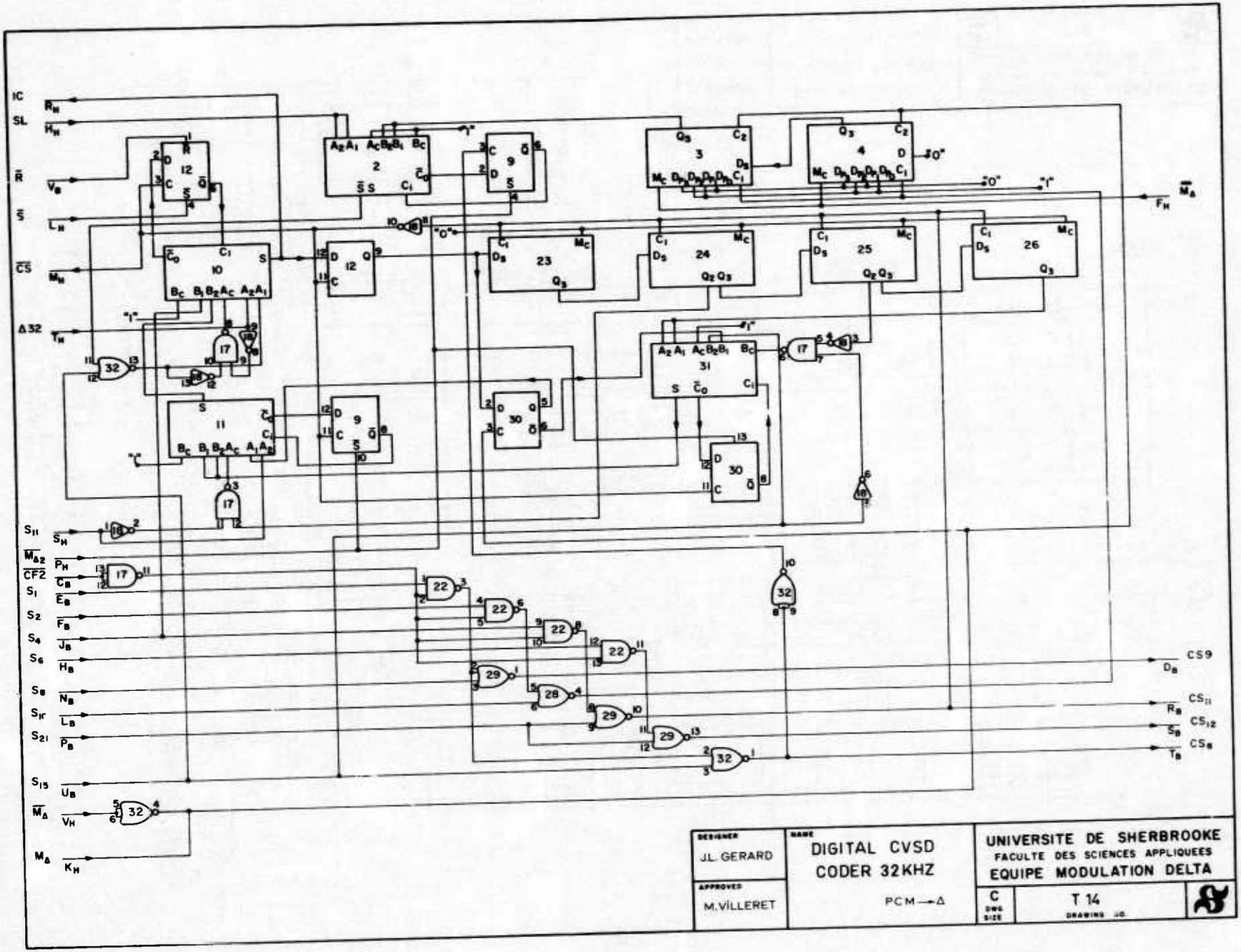


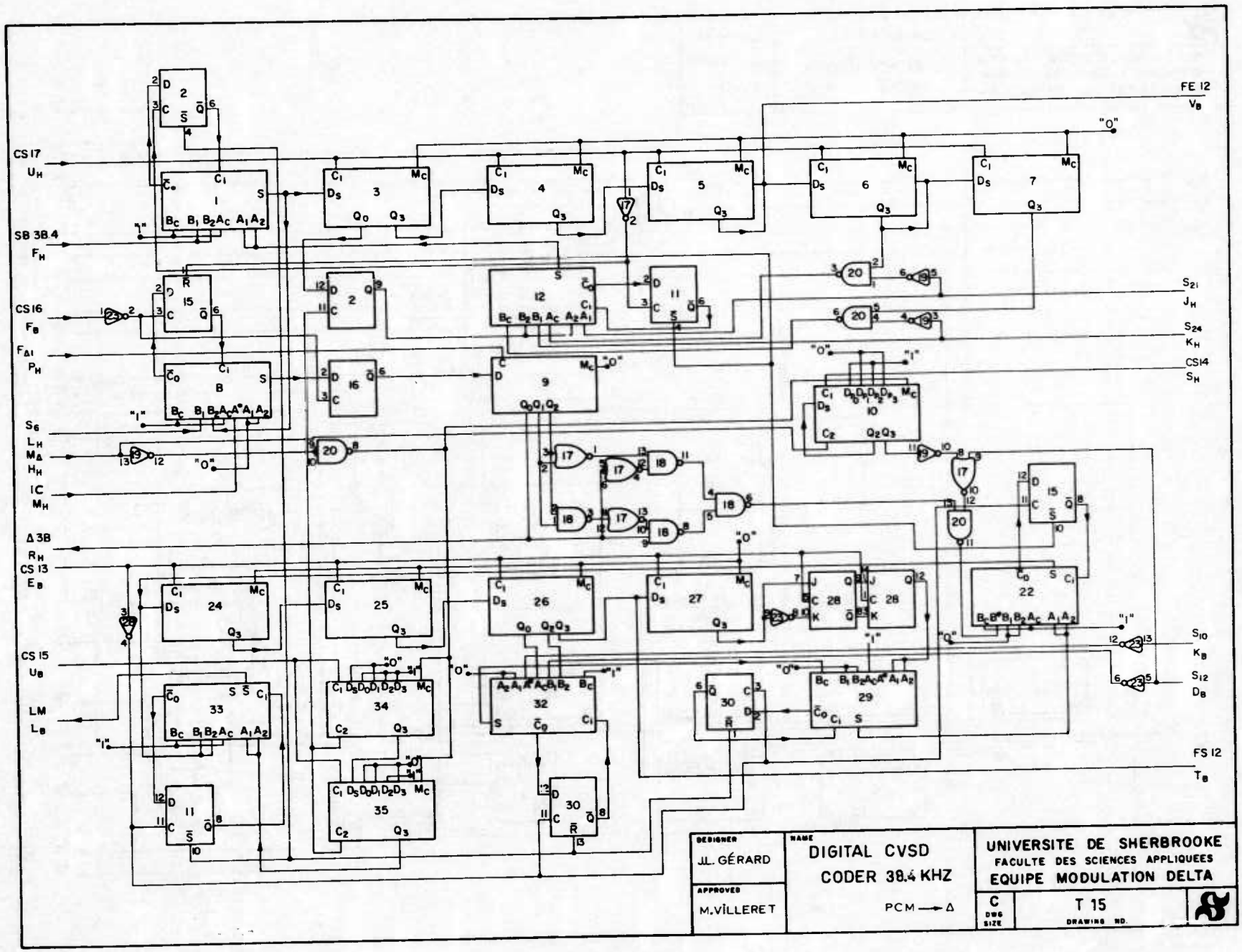
DESIGNER: J.L. GÉRARD	NAME: DIGITAL CVSD CODER 19.2 KHZ PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) — T 11 (DRAWING NO.)

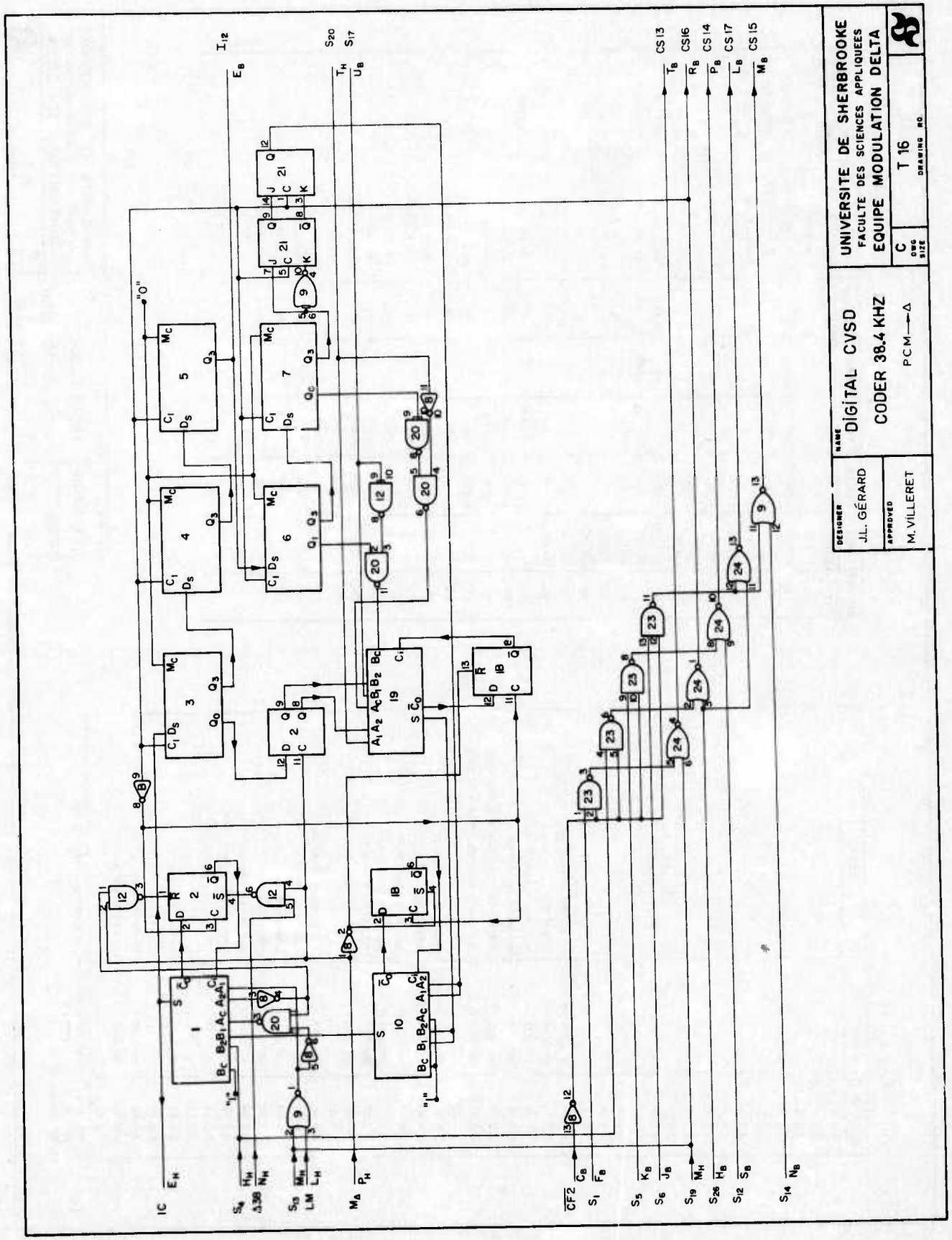


DESIGNER J.L.GÉRARD	NAME DIGITAL CVSD CODER 19.2 KHZ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED M.VILLERET		C DWG SIZE	T12 DRAWING NO.


UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
NAME
DIGITAL CVSD
CODER 32 KHZ
PCM → Δ
DESIGNER
JL GÉRARD
APPROVED
M VILLERET
SIZE
C
DRAWING NO
T 13
REV
FE 12
S 19
FS 12
CS 12
SB 32
CS 11
CS 9
CS 8
SL
CS 6


IC
SL
R̄
S̄
CS̄
Δ32
S11
M̄Δ2
CF2̄
S1
S2
S4
S6
S8
S10
S21
S15
M̄Δ
MΔ
CS9
CS11
CS12
CS8
"1"
"0"
DESIGNER
J.L. GERARD
APPROVED
M. VILLERET
NAME
DIGITAL CVSD
CODER 32KHZ
PCM → Δ
UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
C
DWG SIZE
T 14
DRAWING NO


CS17
U_H
SB 38.4
F_H
CS16
F_B
$F_{\Delta I}$
P_H
S_6
L_H
M_Δ
H_H
IC
M_H
Δ38
R_H
CS13
E_B
CS15
U_B
LM
L_B
FE12
V_B
S_{21}
J_H
S_{24}
K_H
CS14
S_H
S_{10}
K_B
S_{12}
D_B
FS12
T_B
DESIGNER
JL. GÉRARD
APPROVED
M.VILLERET
NAME
DIGITAL CVSD
CODER 38.4 KHZ
PCM → Δ
UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
C
DWG SIZE
T 15
DRAWING NO.


UNIVERSITE DE SHERBROOKE
FACULTE DES SCIENCES APPLIQUEES
EQUIPE MODULATION DELTA
DIGITAL CVSD
CODER 38.4 KHZ
PCM—Δ
T 16
J.L. GÉRARD
M. VILLERET
"0"
"1"
I12
E_B
S20
S17
T_H
U_B
CS13
CS16
CS14
CS17
CS15
T_B
R_B
P_B
L_B
M_B
E_H
H_H
N_H
M_H
L_H
P_H
M_A
CF2
C_B
F_B
K_B
J_B
M_H
H_B
S_B
N_B

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2		
IC 3		
IC 4	MC 1710 CL	COMPARATOR
IC 5		
IC 6		
IC 7		
IC 8		
IC 9		
IC 10		
IC 11	MC 7400 P	4x2 INPUTS NAND GATE
IC 12		
IC 13		
IC 14		
IC 15		
IC 16	MC 1741 CP1	OPERATIONAL AMPLIFIER
IC 17	MC 1710 CL	COMPARATOR
IC 18	MC 7479 P	DUAL TYPE D FLIP FLOP
IC 19	MC 7400 P	4x2 INPUTS NAND GATE
IC 20	MC 7401 P	4x2 INPUTS OPEN COLLECTOR NAND GATE
IC 21	MC 7401 P	4x2 INPUTS OPEN COLLECTOR NAND GATE
IC 22		
IC 23	MC 1741 CP1	OPERATIONAL AMPLIFIER
IC 24	MC 1710 CL	COMPARATOR
IC 25	MC 7400 P	4x2 INPUTS NAND GATE
IC 26	MC 7479 P	DUAL TYPE D FLIP FLOP
IC 27	MC 7400 P	4x2 INPUTS NAND GATE
IC 28	MC 7402 P	" " NOR GATE
IC 29		
IC 30	MC 7495 P	4 BITS SHIFT REGISTER
IC 31	MC 7495 P	" " " "
IC 32	MC 1710 CL	COMPARATOR
IC 33	MC 1710 CL	COMPARATOR
IC 34	MC 7400 P	4x2 INPUTS NAND GATE
IC 35	MC 7473 P	DUAL TYPE J.K. FLIP FLOP
IC 36		
IC 37		
IC 38		
IC 39		
IC 40	MC 7400 P	4x2 INPUTS NAND GATE
IC 41	MC 7402 P	4x2 INPUTS NOR GATE
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION	
T_1	NE2560V					TRANSFORMER	NORTHERN ELECTRIC
T_2	NE2560AF					TRANSFORMER	" "
L_1	S7401F	68mH	10%			VIH INDUCTANCE	NYTRONICS
L_2	S7401F	68mH	10%			VIH INDUCTANCE	NYTRONICS
CR1	IN87A				23V	SIGNAL DIODE	MOTOROLA
CR2	1N87A				"	" "	" "
CR3	IN87A				"	" "	" "
CR4	IN87A				"	" "	" "
CR5	IN87A				"	" "	" "
CR6	IN4733A	5.1V		1N	5.1V	ZENER DIODE	" "
Q1	2N4124			300mW	V_{cb} 30V	NPN TRANSISTOR	" "
Q2	2N4124			"	"	" "	" "
Q3	2N4124			"	"	" "	" "
Q4	2N4124			"	"	" "	" "
Q5	2N4124			"	"	" "	" "
Q6	2N4124			"	"	" "	" "
C1		10nF	-20+100%		40V	2222629 03103	PHILIPS
C2		100nF	±10%		250V	280AEA100K	" "
C3		10μF	-10+50%		25V	426ARF10	" "
C4		0.10nF	±2%		100V	222263870101	" "
C5		0.10nF	±2%		100V	222263870101	" "
C6		10nF	-20+100%		40V	222262903103	" "
C7		10nF	-20+100%		40V	2222 62903103	" "
C8		220nF	±10%		250V	280AEA220K	" "
C9		220nF	±10%		250V	280AEA220K	" "
C10		1nF	-20+100%		40V	222262903102	" "
C11		10μF	-10+50%		25V	426ARF10	" "
C12		10μF	-10+50%		25V	426ARF10	" "
C13		100nF	±10		250V	280AEA100K	" "
C14		2.2nF	±0.25pF		100V	222263803228	" "
C15		0.59nF	±2%		100V	222263870569	" "

DESIGNER: L.CHARRIER	NAME: INTERFACES DATA PROCESSOR PCM → Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M.VILLERET		C (DWG SIZE) — NT1 (DRAWING NO) — 1/3

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2		
IC 3		
IC 4		
IC 3		
IC 6		
IC 7		
IC 8		
IC 9		
IC 10		
IC 11		
IC 12		
IC 13		
IC 14		
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22		
IC 23		
IC 24		
IC 25		
IC 26		
IC 27		
IC 28		
IC 29		
IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(E) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION	
R1	Carbon deposit	470Ω	5%	250mW	250V	STYLE 25	PHILIPS
R2	" "	470Ω	"	"	"	" "	" "
R3	" "	1kΩ	"	"	"	" "	" "
R4	" "	2.2kΩ	"	"	"	" "	" "
R5	" "	470Ω	"	"	"	" "	" "
R6	" "	47Ω	"	"	"	" "	" "
R7	" "	1kΩ	"	"	"	" "	" "
R8	" "	4.7kΩ	"	"	"	" "	" "
R9	" "	1kΩ	"	"	"	" "	" "
R10	" "	330Ω	"	"	"	" "	" "
R11	" "	1.2kΩ	"	"	"	" "	" "
R12	" "	1kΩ	"	"	"	" "	" "
R13	" "	2.2kΩ	"	"	"	" "	" "
R14	" "	150Ω	"	"	"	" "	" "
R15	" "	1kΩ	"	"	"	" "	" "
R16	" "	15kΩ	"	"	"	" "	" "
R17	" "	4.7kΩ	"	"	"	" "	" "
R18	" "	47kΩ	"	"	"	" "	" "
R19	" "	1kΩ	"	"	"	" "	" "
R20	" "	470Ω	"	"	"	" "	" "
R21	" "	15kΩ	"	"	"	" "	" "
R22	" "	100Ω	"	"	"	" "	" "
R23	" "	1kΩ	"	"	"	" "	" "
R24	" "	1kΩ	"	"	"	" "	" "
R25	" "	1kΩ	"	"	"	" "	" "
R26	" "	47Ω	"	"	"	" "	" "
R27	" "	100kΩ	"	"	"	" "	" "
R28	" "	820kΩ	"	"	"	" "	" "
R29	" "	100kΩ	"	"	"	" "	" "
R30	" "	100kΩ	"	"	"	" "	" "
R31	" "	330Ω	"	"	"	" "	" "
R32	" "	1.2kΩ	"	"	"	" "	" "
R33	" "	100Ω	"	"	"	" "	" "
R34	" "	1kΩ	"	"	"	" "	" "
R35	" "	1kΩ	"	"	"	" "	" "

DESIGNER: L. CHARRIER	NAME: INTERFACES DATA PROCESSOR PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) — N T1 2/3 (DRAWING NO)

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2		
IC 3		
IC 4		
IC 5		
IC 6		
IC 7		
IC 8		
IC 9		
IC 10		
IC 11		
IC 12		
IC 13		
IC 14		
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22		
IC 23		
IC 24		
IC 25		
IC 26		
IC 27		
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IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(E) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION
R36	Carbon deposit	1kΩ	5%	250mW	250V	STYLE 25 PHILIPS
R37	" "	820kΩ	"	"	"	" "
R38	" "	47Ω	"	"	"	" "
R39	" "	100kΩ	"	"	"	" "
R40	" "	100kΩ	"	"	"	" "
R41	" "	100kΩ	"	"	"	" "
R42	" "	330Ω	"	"	"	" "
R43	" "	1.2kΩ	"	"	"	" "
R44	" "	1K	"	"	"	" "
R45	" "	100Ω	"	"	"	" "
R46	" "	4.7kΩ	"	"	"	" "
R47	" "	10kΩ	"	"	"	" "
R48	" "	1kΩ	"	"	"	" "
R49	" "	330Ω	"	"	"	" "
R50	" "	1.2kΩ	"	"	"	" "
R51	" "	100Ω	"	"	"	" "
R52	" "	4.7kΩ	"	"	"	" "
R53	" "	10kΩ	"	"	"	" "
R54	" "	1kΩ	"	"	"	" "
R55	" "	330Ω	"	"	"	" "
R56	" "	1.2kΩ	"	"	"	" "
R57	" "	1kΩ	"	"	"	" "
R58	" "	1kΩ	"	"	"	" "
R59	" "	1kΩ	"	"	"	" "
R60	" "	1kΩ	"	"	"	" "
R61	" "	100Ω	"	1W	500V	STYLE 52 " "
R62	" "	1kΩ	"	240mW	250V	STYLE 25 " "

DESIGNER: L.CHARRIER	NAME: INTERFACES DATA PROCESSOR PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M.VILLERET		DWG SIZE: C DRAWING NO: N T1 3/3

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7401 P	4x2 INPUTS NAND OPEN COLLECTOR GATE
IC 2	MC 7495 P	4 BITS SHIFT REGISTER
IC 3	MC 7495 P	" " "
IC 4	MC 7473 P	DUAL TYPE JK FLIP FLOP
IC 5	MC 7400 P	4x2 INPUTS NAND GATE
IC 6	MC 7493 P	4 BITS COUNTER
IC 7	NE 565 K	PHASE LOCK LOOP SIGNETICS
IC 8	MC 7402 P	4x2 INPUTS NOR GATE
IC 9	MC 7402 P	" " "
IC 10	MC 7400 P	4x2 INPUTS NAND GATE
IC 11	MC 7400 P	" " " "
IC 12	MC 7400 P	" " " "
IC 13	MC 7493 P	4 BITS COUNTER
IC 14		
IC 15	MC 7400 P	4x2 INPUTS NAND GATES
IC 16	MC7495 P	4 BITS SHIFT REGISTER
IC 17	MC 7495 P	" " "
IC 18	MC 7495 P	" " "
IC 19	MC 7495 P	" " "
IC 20	MC 7495 P	" " "
IC 21	MC 7495 P	" " "
IC 22		
IC 23		
IC 24		
IC 25		
IC 26		
IC 27		
IC 28	MC 7400 P	4x2 INPUTS NAND GATE
IC 29	MC 7402 P	4x2 INPUTS NOR GATE
IC 30	MC 7402 P	" " " "
IC 31	MC 7404 P	HEX INVERTER
IC 32	MC 7400 P	4x2 INPUTS NAND GATE
IC 33	MC 7400 P	" " " "
IC 34	MC 7404 P	HEX INVERTER
IC 35	MC 7402 P	4x2 INPUTS NOR GATE
IC 36	MC 7473 P	DUAL TYPE JK FLIP FLOP
IC 37	MC 7493 P	4 BITS COUNTER
IC 38	MC 7400 P	4x2 INPUTS NAND GATE
IC 39	MC 7479 P	DUAL TYPE D FLIP FLOP
IC 40	MC 7400 P	4x2 INPUTS NAND GATE
IC 41	MC 7492 P	DIVIDE BY TWELVE COUNTER
IC 42	MC 7400 P	4x2 INPUTS NAND GATE

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION	
C0	Ceramic	.39nF	±2%		100V	2222 629 03204	
C1	" "	1nF	+20-100%		40V	2222 629 03102	PHILIPS
C2	METALIZED	100nf	±10%		250V	280 AEA 100K	" "
C3	Ceramic	22pF	±2%		100V	2222 638 58229	" "
C4	Metalized	68nF	±10%		250V	280 AEA63K	" "
P1	Carbon deposit	1K	±10%	750mW		VARIABLE RESISTOR 3006P.1-102	TRIMPOT
Q1	2N4124			300mW	VCB 30V	NPN TRANSISTOR	MOTOROLA
R1	Carbon deposit	470Ω	5%	250mW	250V	STYLE 25	PHILIPS
R2	" "	15KΩ	"	"	"	" "	" "
R3	" "	2.7K	"	"	"	" "	" "
R4	" "	4.7kΩ	"	"	"	" "	" "
R5	" "	10kΩ	"	"	"	" "	" "
R6	" "	240Ω	"	"	"	" "	" "
R7		470Ω	"	"	"	" "	" "

DESIGNER: L CHARRIER	NAME: INTERFACES COUNTERS PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M.VILLERET		C DWG SIZE	NT3 DRAWING NO 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2	MC 7400 P	4x2 INPUTS NAND GATES
IC 3	MC 7400 P	" " " "
IC 4		
IC 5		
IC 6		
IC 7		
IC 8		
IC 9	MC 7401 P	4x2 INPUTS NANDS OPEN COLLECTOR GATES
IC 10	MC 7400 P	4x2 INPUTS NANDS GATES
IC 11		
IC 12		
IC 13	MC 7400 P	4x2 INPUTS NAND GATES
IC 14		
IC 15	MC 7402 P	4x2 INPUTS NOR GATES
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22		
IC 23	MC 7400 P	4x2 INPUTS NAND GATES
IC 24	MC 7400 P	" " " "
IC 25	MC 7402 P	4x2 INPUTS NOR GATES
IC 26	MC 7400 P	4x2 INPUTS NAND GATES
IC 27		
IC 28		
IC 29	MC 7473 P	DUAL TYPE JK FLIP FLOP
IC 30	MC 7400 P	4x2 INPUTS NAND GATES
IC 31	MC 7473 P	DUAL TYPE JK FLIP FLOP
IC 32	MC 7480 P	GATED FULL ADDER
IC 33	MC 7480 P	" " "
IC 34	MC 7480 P	" " "
IC 35	MC 7479 P	DUAL TYPE D FLIP FLOP
IC 36	MC 7400 P	4x2 INPUTS NAND GATES
IC 37	MC 7400 P	" " " "
IC 38	MC 7495 P	4 BITS SHIFT REGISTER
IC 39	MC 7495 P	" " "
IC 40	MC 7495 P	" " "
IC 41	MC 7495 P	" " "
IC 42	MC 7402 P	4x2 INPUTS NOR GATE

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION	
Q1	2N4124			300mW	VCB=30V	NPN TRANSISTOR	MOTOROLA
Q2	2N1711			800mW	VCB=45V	NPN TRANSISTOR	" "
R1	carbon deposit	470Ω	5%	250mW	250V max.	STYLE 25	PHILIPS
R2		470Ω	"	"	"	" "	" "
R3		1kΩ	"	"	"	" "	" "
R4		2.7kΩ	"	"	"	" "	" "
R5		470Ω					
R6		10K	"	"	"	" "	" "
C1	Ceramic	220pF	±10%		100V	2222 630 03221	
C2	Ceramic	470nF	±10%		"	2222 630 03471	
C3	"	220pF	±10%		100V	2222 630 03221	

DESIGNER: L.CHARRIER	NAME: INTERFACES	UNIVERSITE DE SHERBROOKE	
APPROVED: M.VILLERET	FRAME DETECTOR PCM→Δ	FACULTE DES SCIENCES APPLIQUEES	
		EQUIPE MODULATION DELTA	
		C (DWG SIZE)	NT4 1/1 (DRAWING NO)

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NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7404 P	HEX INVERTER
IC 2	1702 A	2048 BIT READ ONLY MEMORY INTEL
IC 3		
IC 4	MC 7404 P	HEX INVERTER
IC 5		
IC 6		
IC 7		
IC 8	MC 7451 P	DUAL 2-W2- INPUT A01 GATE
IC 9		
IC 10		
IC 11	MC 7400 P	QUAD 2 INPUT NAND GATE
IC 12	MC 7479 P	DUAD TYPE D FLIP FLOP
IC 13	MC 7402 P	QUAD 2 INPUT NOR GATE
IC 14	MC 7401 P	QUAD 2 INPUT NAND GATE (O.C)
IC 15	MC 7451 P	DUAL 2-W2 INPUT AD1 GATE
IC 16	MC 7400 P	QUAD 2 INPUT NAND GATE
IC 17	MC 7402 P	QUAD 2 INPUT NOR GATE
IC 18	MC 7410 P	TRIPLE 3 INPUT NAND GATE
IC 19	MC 7454 P	4 W2 INPUT A01 GATE
IC 20	MC 7400 P	QUAD 2 INPUT NAND GATE
IC 21	MC 7401 P	" " " (O.C)
IC 22	MC 7402 P	QUAD 2 INPUT NOR GATE
IC 23	MC 7479 P	DUAL TYPE D FLIP FLOL
IC 24	MC 7400 P	QUAD 2 INPUT NAND GATE
IC 25		
IC 26	MC 7402 P	QUAD 2 INPUT NOR GATE
IC 27	MC 7454 P	4 W2 INPUT A01 GATE
IC 28	MC 7454 P	" " "
IC 29		
IC 30	MC 7402 P	QUAD 2 INPUT NOR GATE
IC 31	MC 7495 P	4 BITS UNIVERSAL SHIFT REGISTER
IC 32	MC 7495 P	" " "
IC 33	MC 7495 P	" " "
IC 34	MC 7495 P	" " "
IC 35		
IC 36		
IC 37		
IC 38	MC 7495 P	4 BITS UNIVERSAL SRIFT REGISTER
IC 39	MC 7495 P	" " " "
IC 40	MC 7495 P	" " " "
IC 41	MC 7495 P	" " " "
IC 42	MC 7400 P	QUAD 2 INPUT NAND GATE

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(E) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION
C1		39CpF	10%		100V	2222 630 03391 PHILIPS
C1						NOT MARKED ON PRINTED CIRCUIT
CR1	IN5234		"	.5W	6.2V	ZENER DIODE MOTOROLA
CR2	IN4740		"	1W	10V	" " " "
R1		4.7kΩ	5%	250mW	250V	CARBON DEPOSIT TYPE STYLE 25 PHILIPS
R2		4.7kΩ	"	"	"	" " " " "
R3		4.7kΩ	"	"	"	" " " " "

DESIGNED: J.C. DOMIEN	NAME: EXPANDOR PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M.VILLERET		C (DWG SIZE)	N T6 (DRAWING NO) 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7480 P	GATED FULL ADDER
IC 2	" "	" " "
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	" "	" "
IC 5	MC 7473 P	DUAL JK FLIP FLOP
IC 6		
IC 7		
IC 8	MC 7479 P	DUAL D FLIP FLOP
IC 9	" "	" " "
IC 10	MC 7454 P	4 WIDE 2 INPUT "AND OR INVERT" GATE
IC 11	MC 7402 P	4x2 INPUT NOR GATE
IC 12	MC 7404 P	HEX INVERTER
IC 13	MC 7400 P	4x2 INPUT NAND GATE
IC 14		
IC 15	MC 7480 P	GATED FULL ADDER
IC 16	" "	" " "
IC 17	MC 7495 P	4 BITS SHIFT REGISTER
IC 18	" "	" " "
IC 19	" "	" " "
IC 20	" "	" " "
IC 21	" "	" " "
IC 22		
IC 23	MC 7479 P	DUAL D FLIP FLOP
IC 24	MC 7402 P	4x2 INPUT NOR GATE
IC 25	MC 7400 P	4x2 INPUT NAND GATE
IC 26	" "	" " "
IC 27	" "	" " "
IC 28		
IC 29		
IC 30		
IC 31		
IC 32	MC 7404 P	HEX INVERTER
IC 33	MC 7402 P	4x2 INPUT NOR GATE
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION
C1		3.9nF	+2%		63V	279 AM C3K9 PHILIPS
C2		3.9nF	"		"	" " " " "
R1		270Ω	5%	250mW	250V	CARBON DEPOSIT TYPE 25 " "
R2		270Ω	"	"	"	" " " " "

DESIGNER: N FORGET	NAME: SIGN ADJUSTMENT PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M VILLERET		C (DWG SIZE) NT7 (DRAWING NO) 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2	MC 7495P	4 BITS SHIFT REGISTER
IC 3	" "	" " "
IC 4	" "	" " "
IC 5	MC 7473 P	DUAL JK FLIP FLOP
IC 6	MC 7400 P	4x2 INPUT NAND GATE
IC 7	MC 7479 P	DUAL D FLIP FLOP
IC 8		
IC 9	MC 7495 P	4 BITS SHIFT REGISTER
IC 10	" "	" " "
IC 11	" "	" " "
IC 12	MC 7473 P	DUAL JK FLIP FLOP
IC 13	MC 7404 P	HEX INVERTER
IC 14	MC 7480 P	GATED FULL ADDER
IC 15	MC 7402 P	4x2 INPUT NOR GATE
IC 16	MC 7495 P	4 BITS SHIFT REGISTER
IC 17	" "	" " "
IC 18	" "	" " "
IC 19	MC 7473 P	DUAL JK FLIP FLOP
IC 20	MC 7400 P	4x2 INPUT NAND GATE
IC 21	" "	" " "
IC 22	MC 7495 P	4 BITS SHIFT REGISTER
IC 23	" "	" " "
IC 24	" "	" " "
IC 25	" "	" " "
IC 26	" "	" " "
IC 27	" "	" " "
IC 28	" "	" " "
IC 29		
IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35	MC 7400 P	4x2 INPUT NAND GATE
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT SHOWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNED: N. FORGET	NAME: INTERPOLATOR PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M.VILLERET		C DWG SIZE — NT8 DRAWING NO. — 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7480 P	GATED FULL ADDER
IC 2	MC 7495 P	4 BITS SHIFT REGISTER
IC 3	" "	" " "
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7		
IC 8	MC 7479 P	DUAL D FLIP FLOP
IC 9	MC 7495 P	4 BITS SHIFT REGISTER
IC 10	" "	" " "
IC 11	" "	" " "
IC 12	" "	" " "
IC 13	" "	" " "
IC 14	MC 7400 P	4x2 INPUT NAND GATE
IC 15	MC 7404 P	HEX INVERTER
IC 16	MC 7495 P	4 BITS SHIFT REGISTER
IC 17	" "	" " "
IC 18	" "	" " "
IC 19	" "	" " "
IC 20	" "	" " "
IC 21	MC 7404 P	HEX INVERTER
IC 22	MC 7454 P	4 WIDE 2 INPUT "AND OR INVERT" GATE
IC 23	MC 7495 P	4 BITS SHIFT REGISTER
IC 24	" "	" " "
IC 25	" "	" " "
IC 26	" "	" " "
IC 27	MC 7480 P	GATED FULL ADDER
IC 28	MC 7495 P	4 BITS SHIFT REGISTER
IC 29	MC 7479 P	DUAL D FLIP FLOP
IC 30	MC 7404 P	HEX INVERTER
IC 31	MC 7479 P	DUAL D FLIP FLOP
IC 32	MC 7480 P	GATED FULL ADDER
IC 33	" "	" " "
IC 34	MC 7479 P	DUAL D FLIP FLOP
IC 35	MC 7404 P	HEX INVERTER
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION
C1		3.9nF	+2%		63V	279 AHC 3K9 PHILIPS
C2		1nF	+2%		63V	" " C1K " "
C3		100pf	±2%		100V	2222 638 70101 " "
C4		.1mf	+2%		63V	279 AHC1K " "
R1		270Ω	5%	250mW	250V	CARBON DEPOSIT TYPE 25 " "
R2		100Ω	"	"	"	" " " " "

DESIGNER: N. FORGET	NAME: LOW PASS FILTER	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M. VILLERET		C (DWG SIZE)	NT9 1/1 (DRAWING NO.)

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7480 P	GATED FULL ADDER
IC 2	MC 7479 P	DUAL D FLIP FLOP
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7		
IC 8	MC 7480 P	GATED FULL ADDER
IC 9	MC 7479 P	DUAL D FLIP FLOP
IC 10	MC 7495 P	4 BITS SHIFT REGISTER
IC 11	MC 7404 P	HEX INVERTER
IC 12	MC 7402 P	4x2 INPUT NOR GATE
IC 13	MC 7400 P	4x2 INPUT NAND GATE
IC 14	MC 7404 P	HEX INVERTER
IC 15	MC 7479 P	DUAL D FLIP FLOP
IC 16	MC 7495 P	4 BITS SHIFT REGISTER
IC 17	MC 7400 P	4x2 INPUT NAND GATE
IC 18	MC 7480 P	GATED FULL ADDER
IC 19	MC 7495 P	4 BITS SHIFT REGISTER
IC 20	MC 7400 P	4x2 INPUT NAND GATE
IC 21		
IC 22	MC 7480 P	GATED FULL ADDER
IC 23	" "	" " "
IC 24	MC 7402 P	4x2 INPUT NOR GATE
IC 25	MC 7479 P	DUAL D PLIP FLOP
IC 26	MC 7480 P	GATED FULL ADDER
IC 27	MC 7495 P	4 BITS SHIFT REGISTER
IC 28	" "	" " "
IC 29	MC 7400 P	4x2 INPUT NAND GATE
IC 30	MC 7479 P	DUAL D PLIP FLOP
IC 31	MC 7480 P	GATED FULL ADDER
IC 32	MC 7495 P	4 BITS SHIFT REGISTER
IC 33	" "	" " "
IC 34	" "	" " "
IC 35	MC 7473 P	DUAL JK FLIP FLOP
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNED: N FORGET	NAME: DIGITAL CVSD CODER 16 KHZ PCM	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M VILLERET		DWG SIZE: C DRAWING NO: N T10 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7480 P	GATED FULL ADDER
IC 2	MC 7479 P	DUAL D FLIP FLOP
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	" "	" " "
IC 5	" "	" " "
IC 6		
IC 7		
IC 8	MC 7480 P	GATED FULL ADDER
IC 9	MC 7479 P	DUAL D FLIP FLOP
IC 10	MC 7495 P	4 BITS SHIFT REGISTER
IC 11	MC 7480 P	GATED FULL ADDER
IC 12	MC 7400 P	4x2 INPUT NAND GATE
IC 13	MC 7495 P	4 BITS SHIFT REGISTER
IC 14	" "	" " "
IC 15		
IC 16	MC 7404 P	HEX INVERTER
IC 17	MC 7400 P	4x2 INPUT NAND GATE
IC 18	MC 7479 P	DUAL D FLIP FLOP
IC 19	MC 7480 P	GATED FULL ADDER
IC 20	MC 7404 P	HEX INVERTER
IC 21		
IC 22		
IC 23	MC 7402 P	4x2 INPUT NOR GATE
IC 24		
IC 25	MC 7495 P	4 BITS SHIFT REGISTER
IC 26	" "	" " "
IC 27	" "	" " "
IC 28	" "	" " "
IC 29	MC 7479 P	DUAL D FLIP FLOP
IC 30	MC 7480 P	GATED FULL ADDER
IC 31	MC 7495 P	4 BITS SHIFT REGISTER
IC 32	" "	" " "
IC 33	MC 7480 P	GATED FULL ADDER
IC 34	MC 7479 P	DUAL D FLIP FLOP
IC 35	MC 7480 P	GATED FULL ADDER
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: J.L.GÉRARD	NAME: DIGITAL CVSD CODER 19.2 KHZ PCM → Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M.VILLERET		C (DWG SIZE) — N T11 1/1 (DRAWING NO)

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2		
IC 3		
IC 4		
IC 5		
IC 6		
IC 7		
IC 8		
IC 9	MC 7400 P	4x2 INPUT NAND GATE
IC 10	MC 7402 P	4x2 INPUT NOR GATE
IC 11	MC 7495 P	4 BITS SHIFT REGISTER
IC 12	" "	" " "
IC 13	" "	" " "
IC 14	" "	" " "
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22		
IC 23	MC 7404 P	HEX INVERTER
IC 24	MC 7400 P	4x2 INPUT NAND GATE
IC 25	MC 7480 P	GATED FULL ADDER
IC 26	MC 7479 P	DUAL D FLIP FLOP
IC 27	MC 7480 P	GATED FULL ADDER
IC 28		
IC 29		
IC 30		
IC 31		
IC 32		
IC 33		
IC 34		
IC 35		
IC 36		
IC 37	MC 7400 P	4x2 INPUT NAND GATE
IC 38	MC 7480 P	GATED FULL ADDER
IC 39	MC 7479 P	DUAL D FLIP FLOP
IC 40	MC 7480 P	GATED FULL ADDER
IC 41	MC 7479 P	DUAL D FLIP FLOP
IC 42		

(1) FOR NODED CERNITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNED: J.L.GÉRARD	NAME: DIGITAL CVSD CODER 19.2 KHZ PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M. VILLERET		C (DWG SIZE)	N T12 (DRAWING NO.) 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2	MC 7480 P	GATED FULL ADDER
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7		
IC 8	MC 7479 P	DUAL D FLIP FLOP
IC 9	MC 7495 P	4 BITS SHIFT REGISTER
IC 10	MC 7400 P	4x2 INPUT NAND GATE
IC 11	MC 7480 P	GATED FULL ADDER
IC 12	MC 7479 P	DUAL D FLIP FLOP
IC 13	MC 7495 P	4 BITS SHIFT REGISTER
IC 14	MC 7400 P	4x2 INPUT NAND GATE
IC 15		
IC 16		
IC 17		
IC 18		
IC 19		
IC 20		
IC 21		
IC 22	MC 7404 P	HEX INVERTER
IC 23	MC 7479 P	DUAL D FLIP FLOP
IC 24	MC 7480 P	GATED FULL ADDER
IC 25	MC 7495 P	4 BITS SHIFT REGISTER
IC 26	" "	" " "
IC 27	" "	" " "
IC 28	MC 7402 P	4x2 INPUT NOR GATE
IC 29		
IC 30	MC 7480 P	GATED FULL ADDER
IC 31	MC 7479 P	DUAL D FLIP FLOP
IC 32	MC 7480 P	GATED FULL ADDER
IC 33	" "	" " "
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: JL GERARD	NAME: DIGITAL CVSD CODER 32KHZ PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA	
APPROVED: M VILLERET		C (DWG SIZE)	NT13 (DRAWING NO) 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1		
IC 2	MC 7480 P	GATED FULL ADDER
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	" "	" " "
IC 5		
IC 6		
IC 7		
IC 8		
IC 9	MC 7479 P	DUAL D FLIP FLOP
IC 10	MC 7480 P	GATED FULL ADDER
IC 11	" "	" " "
IC 12	MC 7479 P	DUAL D FLIP FLOP
IC 13		
IC 14		
IC 15		
IC 16		
IC 17	MC 7400 P	4x2 INPUT NAND GATE
IC 18	MC 7404 P	HEX INVERTER
IC 19		
IC 20		
IC 21		
IC 22	MC 7400 P	4x2 INPUT NAND GATE
IC 23	MC 7495 P	4 BITS SHIFT REGISTER
IC 24	" "	" " "
IC 25	" "	" " "
IC 26	" "	" " "
IC 27		
IC 28		
IC 29	MC 7402 P	4x2 INPUT NOR GATE
IC 30	MC 7479 P	DUAL D FLIP FLOP
IC 31	MC 7480 P	GATED FULL ADDER
IC 32	MC 7402 P	4x2 INPUT NOR GATE
IC 33		
IC 34		
IC 35		
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: J.L. GÉRARD	NAME: DIGITAL CVSD CODER 32 KHZ PCM → Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		DWG SIZE: C DRAWING NO: N T14 1/1

NUMBER (1)	TYPE (2)	DESCRIPTION
IC 1	MC 7480 P	GATED FULL ADDER
IC 2	MC 7479 P	DUAL D FLIP FLOP
IC 3	MC 7495 P	4 BITS SHIFT REGISTER
IC 4	" "	" " "
IC 5	" "	" " "
IC 6	" "	" " "
IC 7	" "	" " "
IC 8	MC 7480 P	GATED FULL ADDER
IC 9	MC 7495 P	4 BITS SHIFT REGISTER
IC 10	" "	" " "
IC 11	MC 7479 P	DUAL D FLIP FLOP
IC 12	MC 7480 P	GATED FULL ADDER
IC 13		
IC 14		
IC 15	MC 7479 P	DUAL D FLIP FLOP
IC 16	MC 7479 P	" " "
IC 17	MC 7402 P	4x2 INPUT NOR GATE
IC 18	MC 7400 P	4x2 INPUT NAND GATE
IC 19	MC 7404 P	HEX INVERTER
IC 20	MC 7400 P	4x2 INPUT NAND GATE
IC 21		
IC 22	MC 7480 P	GATED FULL ADDER
IC 23	MC 7404 P	HEX INVERTER
IC 24	MC 7495 P	4 BITS SHIFT REGISTER
IC 25	" "	" " "
IC 26	" "	" " "
IC 27	" "	" " "
IC 28	MC 7473 P	DUAL TYPE JK FLIP FLOP
IC 29	MC 7480 P	GATED FULL ADDER
IC 30	MC 7479 P	DUAL D FLIP FLOP
IC 31		
IC 32	MC 7480 P	GATED FULL ADDER
IC 33	" "	" " "
IC 34	MC 7495 P	4 BITS SHIFT REGISTER
IC 35	" "	" " "
IC 36		
IC 37		
IC 38		
IC 39		
IC 40		
IC 41		
IC 42		

(1) FOR ADDED CLARITY, "IC" IS NOT DRAWN ON ELECTRICAL DRAWINGS AND PRINTED CIRCUIT BOARDS

(2) OR EQUIVALENT

NUMBER	TYPE	VALUE	TOL.	DISSIP.	VOLTAGE	DESCRIPTION

DESIGNER: JL. GERARD	NAME: DIGITAL CVSD CODER 38.4 KHZ PCM→Δ	UNIVERSITE DE SHERBROOKE FACULTE DES SCIENCES APPLIQUEES EQUIPE MODULATION DELTA
APPROVED: M. VILLERET		C (DWG SIZE) — NT15 (DRAWING NO) — 1/1

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APPENDIX D

TROUBLE SHOOTING CHART

This appendix will help the user to detect when and where the system is in trouble, to find out which board or part of the board is defective.

D1 PCM → Δ

The main trouble is when you hear nothing (or noise) in the CVSD decoder output. First enter a test tone (400Hz) into the PCM coder and follow the procedure:

1) Check of the analog CVSD demodulator (board B22). Put the analog CVSD back to back entering a test tone in the coder (BNC: AUDIO IN front panel). Make sure that the coder is working (SRM) and look at the demodulator output (SRDM) before the filtered output (BNC: AUDIO/OUT front panel).

2) Check of the digital CVSD decoders
Change the frequency pushbuttons on front panel.
   A) If the system is in trouble for only one of these frequencies, the corresponding digital coder does not work. To check it refer to the board description, the use of the serial D/A converter (Figure D.1) and to Table D.1.

   B) If the system is in trouble for all frequencies, the delta counter must be checked (T8 and MΔ generation). If it works the digital CVSD coders should work; follow the procedure (3).

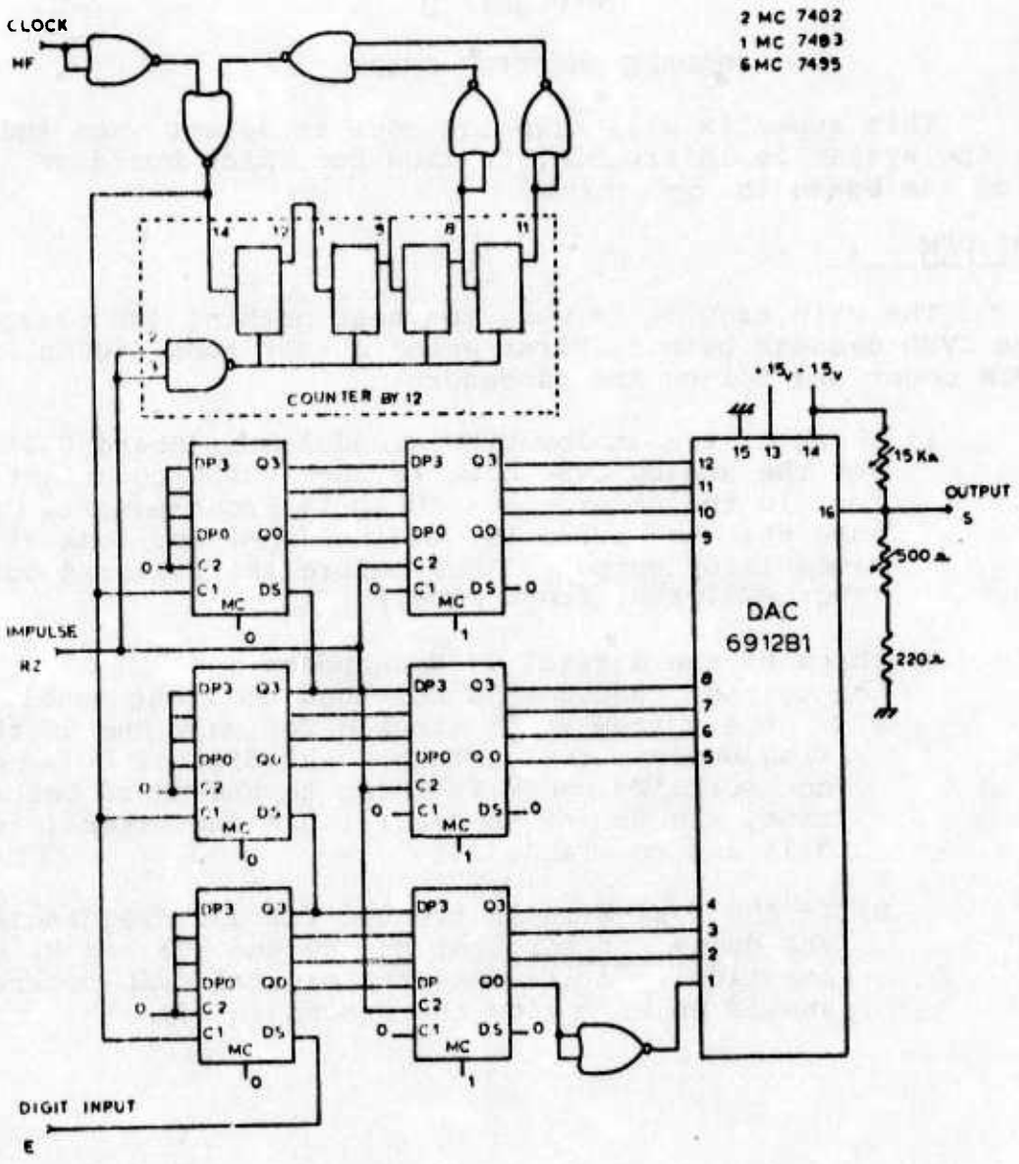


FIGURE D.1 .- Serial D/A converter

DIGITAL CVSD CODER		16kHz	19.2kHz	32kHz	38.4kHz
Input filter	board	T_{10}	T_{11}	T_{13}	T_{15}
	Digit input	$Q_3(5)$	FE12	FE12	FE12
	Clock	CS27	CS22	CS12	CS17
	Impulse	MΔ	MΔ	MΔ	MΔ
	Output	sine wave			
Syllabic filter	Board	T_{10}	T_{11}	T_{13}	T_{15}
	Digit input	$Q_3(28)$	FS12	FS12	FS12
	Clock	$C_1(28)$	CS20	CS8	CS13
	Impulse	MΔ	MΔ	MΔ	MΔ
	Output	DC function of test tone amplitude and frequency			
Integrator	Board	T_{10}	T_{12}	T_{14}	T_{16}
	Digit input	$Q_3(34)$	I_{12}	$Q_3(25)$	I_{12}
	Clock	$C_1(34)$	CS21	CS11	CS16
	Impulse	MΔ	MΔ	MΔ	MΔ
	Output	reconstructed sine wave(saw tooth)			

TABLE D.1.- Trouble shooting Table (PCM→Δ)

3) Each board may be checked, up to the expandor by using the serial D/A converter and following Table D.2.

	BOARD	DIGIT INPUT	CLOCK	IMPULSE	OUTPUT
Holder	T_9	SR19-32	CSB	MΔ	sine wave
Low pass filter	T_9	SF5	CS5	M_2	sine wave
Interpolator	T_8	F	CSI board T_7	M_2	interpolated sine wave
sign adjustment	T_7	I	CS2	8K	full sine wave
Expandor output	T_7	2^{-1}	CS1	8K	rectified sine wave

TABLE D.2.- Trouble shooting Table (PCM→Δ)

4) CHECK OF BOARD T4, T3, T1.

a) check for PCM bits on lead PCM3R, check for clock on lead Dϕ2R if no signal, see the transmitting channel bank used.

b) follow the trouble shooting table, proceed step by step. See the circuit desciption for "Trouble" use an oscilloscope or a frequency meter for checking the signal.

BOARD	PIN CHECKED	OUTPUT SIGNAL	IF NO SIGNALS: TROUBLE
T1	Dϕ3	768kHz square wave	circuits 32 or 19
T1	PCM	PCM bits multiplexed	circuits 33, 26 or 20
IF FRAME LIGHT STAY ON (first check the switch on front panel) -disconnect lead CO from pin EB board T4 -connect PIN HB board T3 to ground.			
T4	Dϕ	768kHz square wave	circuit 01 or 32
T4	$\overline{CS2}$	1.3μs pulse every 8 periods of Dϕ rate 96kHz	digit counter
T4	CHN or CH1 to CH12	10.4μs pulse every 12 periods of $\overline{CS2}$ rate 8kHz	channel counter
T3	F3	125μs pulse every 12 CH1 period rate 666Hz	frame counter (circuits 35,42)
T3	CF1 or CF2 64K	1.536MHz clock 64kHz clock	phase lock loop oscillator adjust P1 to obtain 8K synchronus of CHS.
T4	circuit 40 pin Q_3	you must see the pattern 000001101101	RBC2 circuit 38,39 or 40 or 2
DISCONNECT HBT3 from ground CONNECT CO from EBT4 HBT3			
T4	circuit 30 pin 8	pulses at Dϕ rate	circuit 35,36,24,30, or 42.

If frame light stays on after following this table, the correlator (circuit 31, 41, 34, 33, 32) or the comparator (circuit 3 Board T4) are in trouble and must be checked.

TABLE D.3.- Trouble shooting Table (PCM→Δ)

C) frame light never goes on when switching the power supplies. Check the bulb light and circuit 35 board T4.

D) check on board T1. Use test circuit 1 or 2 in Figure D2, follow Table D.4 step by step.

CHECK CIRCUIT	PIN CHECKED	OUTPUTS SIGNALS	IF NO SIGNALS
1	J3 circuit 20	sine wave	circuit 20
1	8 circuit 34	rectified sine wave	circuit 34
	CHN	high during channel N chosen	board T4 and T3
	C1 circuit 30	group of 7 pulses at Dϕ rate when CHN is high	circuit 21,41,40,28
2	E_6, E_5 E_4, E_3 E_2, E_1, E_0	compressed rectified sine wave	circuit 30 and/or 31

TABLE D.4.- Trouble shooting Table (PCM→Δ)

D.2. Δ→PCM

The main trouble is when you hear nothing (or noise) in the PCM receiving channel. Before following the procedure, make sure the PCM back to back is working. Then, put a test tone (400Hz) in the CVSD coder (BNC:AUDIOIN front panel).

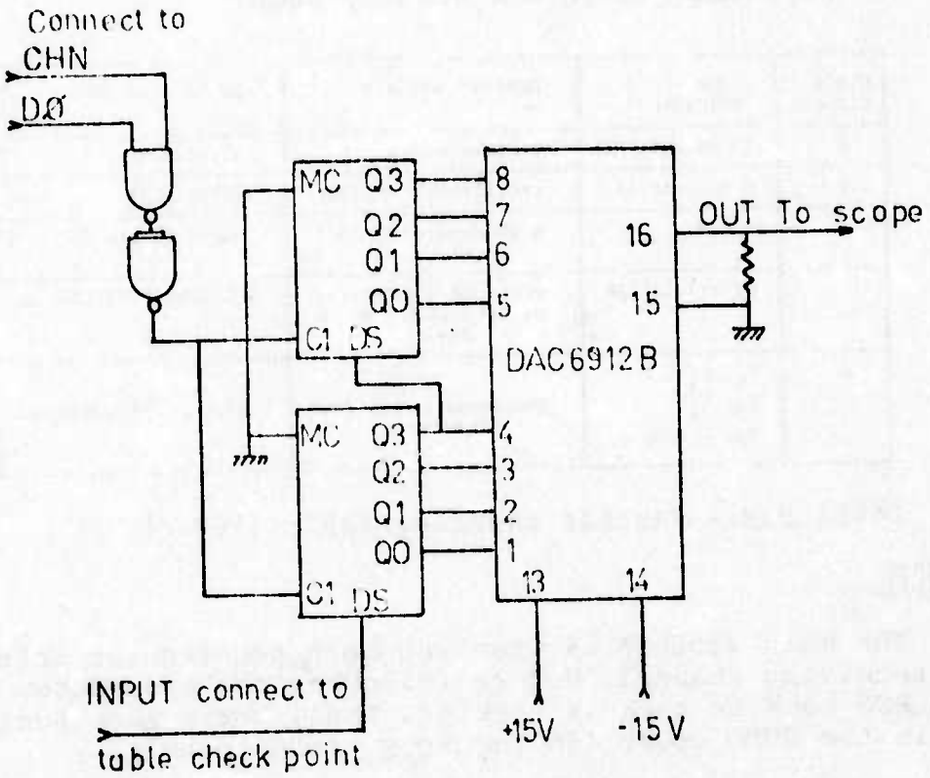
1) Be sure the analog CVSD coder is working: look at the reconstructed sine wave on the oscilloscope (SRM, B22).

2) Check of the digital CVSD decoders. Change the frequency pushbuttons on front panel.

   a) If the system is in trouble for only one of these frequencies, the corresponding digital decoder (3 boards) does not work. To check these three boards refer to the board description, the use of the serial D/A converter and Table D.5.

   b) If the system is in trouble for any frequencies, the delta counter must be checked (B9 and MΔ generation). It it works the digital CVSD decoders should work, follow the procedure (3).

TEST CIRCUIT 1



TEST CIRCUIT 2

DAC6912B used directly

FIGURE D.2.- Test circuits.

Digital CVSD decoders		16K	19.2K	32K	38.4K
Integrator	board	B10	B13	B16	B19
	digit input	SF143	Q_3(20)	SF132	SF104
	clock	CS143	CS113	CS133	CS105
	impulse	MΔ	MΔ	MΔA	MΔA
	output	reconstructed sine wave (sawtooth)			
Filter first stage	board	B11	B14	B17	B20
	digit input	SF145	Q_3(35)	SF134	SF106
	clock	CS145	CS115	CS134	CS106
	impulse	MΔ	MΔ	MΔB	MΔA
	output	reconstructed sine wave (rounded)			
Filter second stage	board	B12	B15	B18	B21
	digit input	SF147	Q_3(33)	SF136	SF108
	clock	CS147	C_1(33)	CS136	CS108
	impulse	MΔ	MΔ	MΔA	MΔA
	Output	filtered sine wave			

TABLE D.5.- Trouble shooting Table (Δ→PCM)

3) Each board must be checked, up to the compressor by using the serial D/A converter and following Table D.6.

DIGITAL CVSD DECODERS		16K	19.2K	32K	38.4K
Integrator	Board	B10	B13	B16	B19
	Digit input	SF143	Q_3(20	SF132	SF104
	Clock	CS143	CS113	CS133	CS104
	Impulse	MΔ	MΔ	MΔA	MΔA
	Output	Reconstructed sine wave (saw tooth)			
Filter first stage	Board	B_{11}	B_{14}	B_{17}	B_{20}
	Digit Input	SF145	Q_3(35)	SF134	SF106
	Clock	CS145	CS115	CS134	CS106
	Impulse	MΔ	MΔ	MΔB	MΔA
	Output	Reconstructed sine wave (rounded)			
Filter second stage	Board	B_{12}	B_{15}	B_{18}	B_{21}
	Digit Input	SF147	Q_3(33)	SF136	SF108
	Clock	CS147	C_1(33)	CS136	CS108
	Impulse	MΔ	MΔ	MΔA	MΔA
	Output	Filtered sine wave			

Table D.6.- Trouble shooting (Δ→PCM).

4) Check of the interfaces (boards B.1, B3, B4) and compressor (B5).

a) Check for PCM bits on board B1, (PCM3TOUT) during channel N used; if there are no bits, follow the check procedure with Table D.7. See descriptions for explanation of trouble.

b) Follow Table D.8 and use test circuit 2 in Figure D.2.

BOARD	PIN CHECKED	OUTPUT	TROUBLE
B4	Dϕ	768kHz square wave	Circuits 1 and/or 11
B4	$\overline{CS2}$	1.3μs pulse every 8 periods of Dϕ, rate 96kHz	Digit counter
B4	CHN or CH1 to CH12	10.4μs pulse every 12 periods of $\overline{CS2}$, rate 8kHz	Channel counter
B4	F3	125μs pulse every 12 periods of CH1, rate 666Hz	Frame counter
B4	CF1 or CF2 64K	1.536MHz clock 64kHz clock	Phase lock loop oscillator, adjust P1 to obtain 8K synchronus of CH5

TABLE D.7.- Trouble shooting Table (Δ→PCM).

BOARD	TEST CIRCUIT	PIN CHECKED	OUTPUT	TROUBLE
B5	2	PAD0 to PAD6	Rectified sine wave	Compressor board
B3	1	DQ3	Rectified sine wave	Check board B3 separatively
B1	1	Pin 9 circuit 40	Sine wave	Circuit 10 or 25 or 40
B1	/	Circuit 5 pin 13	Check for the pattern 111110010010	Circuits 3, 4 and/or 5 Circuit 24 and/or 25
B1	/	Circuit 25 pin 3	Pattern 000001101101 during negative pulse duration of circuit 26 pin 7	24, 25 or 26
B1		PCM3TOUT	Complete frame by connecting sigle from 0 to 1, signalling bits must change	Circuit composed of Q_7, Q_8, Q_9 and Q_{10}
B1		Dϕ3TOUT	768kHz square wave at TD968 levels	Circuit composed of Q_{11}, Q_{12}, Q_{13} and Q_{14}

Table D.8.- Trouble shooting Table (Δ→PCM).

APPENDIX E
POWER SUPPLIES

The TTL circuits require a 5V, 30 amp power supply and the analog components, the operational amplifiers, the ROM require a +15 and a -15 volt power supply.

Lambda regulated power supply model LXS-EE-5-OV and a TS-CA-15-15 were chosen.

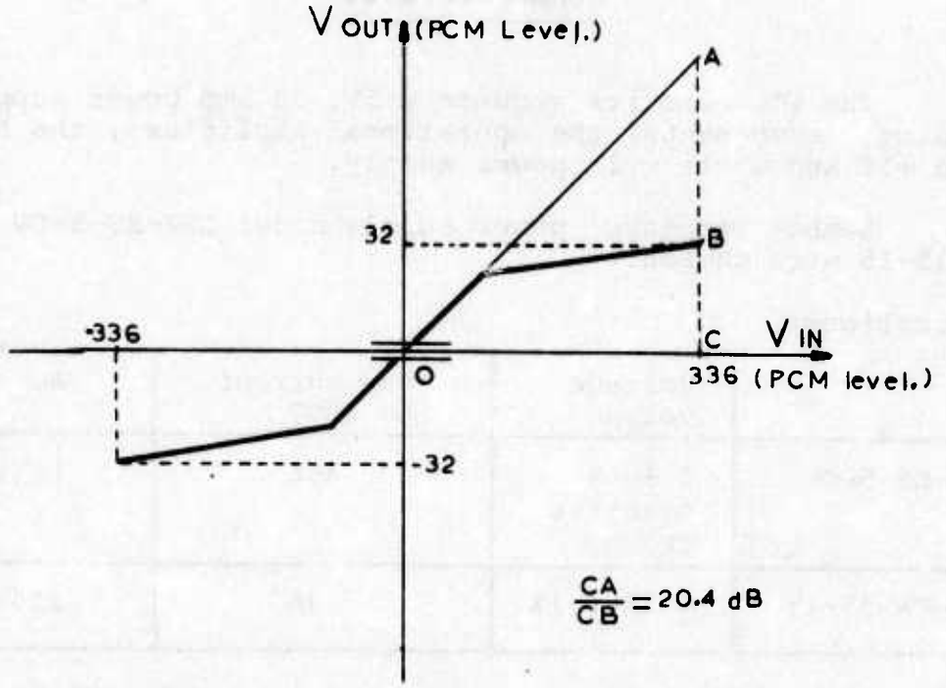
Specifications:

	Voltage volts	Max current to 40°C	AC input
LXS-EE-5-OV	5 ± 5% negative ground	45A	115V 60Hz
LTS-CA-15-15	± 15 ± 1%	4A	115V 60Hz

The power supplies are mounted in Lambda 19" rack LRA-11. A 5 amp fuse is provided on the front panel of the rack.

Remote sensing connections are made (LXS-EE-5-OV) to prevent cable drop. A 6 foot cable with connectors is furnished.

APPENDIX F
TD660 COMPRESSION LAW



The linear maximum value of the expansor output is 336 for TD660 expansion law. For M100 law, this maximum is 4096 and the common part of the DDMC is working with such a gain. So, one must multiply the expansor output, when in TD660 law and in PCM to delta conversion, by $\frac{4096}{336} = 12.19$.

Reciprocally, when in delta to PCM conversion, one must divide the input of the compressor by 12.19 in this law (12.185 is the binary truncated value of 12.19).

TABLE OF LEVELS

J	m	S	n	x_n	$\hat{y}_n$
2	16	20	32	336	326
			31	316	
			.	.	
			.	.	
			.	.	
			.	.	
			17	36	46
			16	16	26
1	16	1	15	15	15.5
			14	14	14.5
			.		
			.		
			.		
			.		
			3	3	2.5
			2	2	1.5
			1	1	0.5
			0	0	

J = segment number
m = number of steps per segment
S = step size
n = step number
x_n = decision level
$\hat{y}_n$ = quantization level

APPENDIX G

DIRECT DIGITAL FREQUENCY CONVERTER (DDFC)

This appendix presents a method for digitally converting a coded signal flowing at a predetermined rate into another coded signal flowing at another predetermined rate.

More particularly, the present method permits the linkage of a CVSD (Continuous variable slope delta modulator) to another CVSD system, the two operating at different sampling rates.

The sampling rates are 16, 32 and 38.4KHz. This interfacing is achieved through the use of a direct digital frequency converter hereinafter designated as a DDFC. The computer simulations presented herein were done on a IBM 370/145.

CONTENTS

G1. INTRODUCTION

The objective of the present appendix is to present the results of a feasibility study on a *Direct Digital Frequency Converter*, hereafter referred to as DDFC.

Direct Digital Frequency Conversion is defined as conversion from one form of digitized voice signal at one rate to the same form of digitized voice signal at another rate without reconstruction of the original analog voice signal. In this study, we will limit ourselves to one type of numerical format for voice: *delta modulation*, more specially *Continuous Variable Slope Delta Modulation* (CVSD).

The scope of this work is to determine by computer simulation the feasibility of a single CVSD-CVSD DDFC.

The first part of this report deals with the conversion principle through the General method of digital conversion.

The second chapter presents the computer simulation model of the DDFC as well as the computed results.

A conclusion finally closes the study.

G2. CONVERSION PRINCIPLE

G2.1. GENERAL CONVERTER MODEL

To interface between two different digital systems, the converter has to realize a code conversion and a sampling rate conversion (Figure 2.1).

The method for converting the code and the sampling rate of a first signal into the code and the sampling rate of a second signal is carried out by means of a first code conversion unit which receives the first signal and converts its code into an intermediate code, the rate of the intermediate code being the rate of the first signal; a rate conversion unit connected to the first code conversion unit for converting the rate of the intermediate signal into the rate of the second signal; and a second code conversion unit which receives the intermediate signal and converts its code into the second signal code.

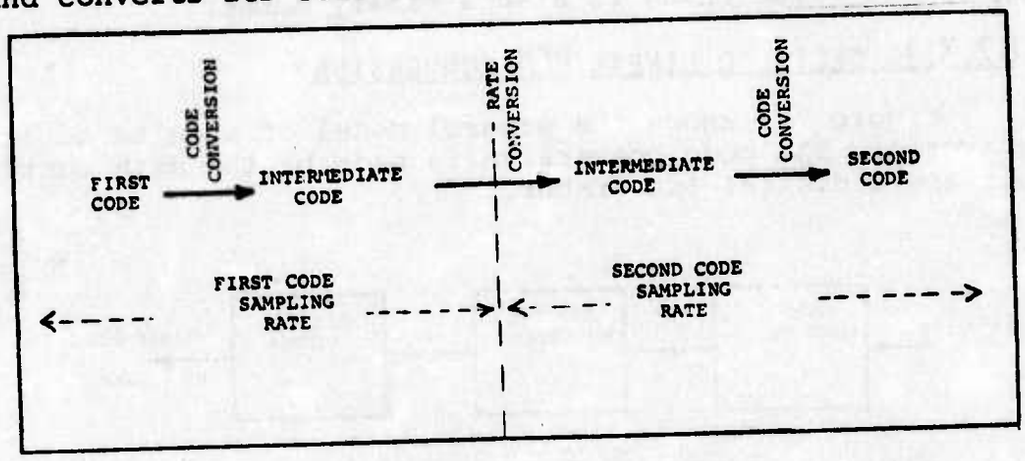


FIGURE 2.1.- General Method of Digital Conversion.

G2.2. DELTA MODULATION TO DELTA MODULATION CONVERTER

Figure 2.2 shows the general model of a delta to delta DDFC.

The first code conversion unit, when receiving a delta signal, will convert the code of the first delta signal into an intermediate code which will be a linear PCM signal, whereas the rate conversion unit will affect the conversion of the first delta sampling rate, F_2. The intermediate code at the second delta sampling rate will then be converted into the second delta code through the second rate conversion unit.

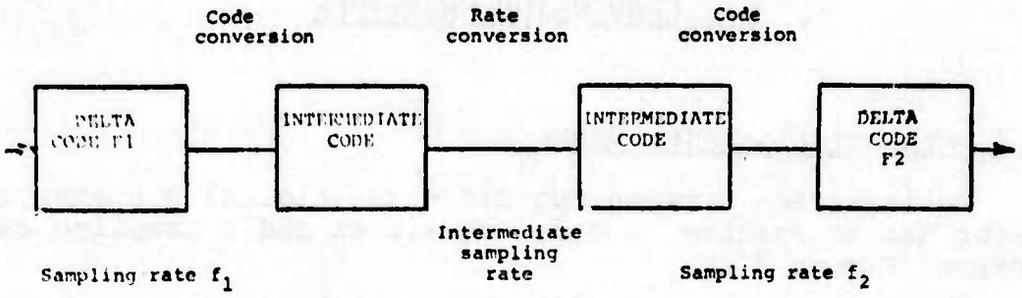


FIGURE 2.2.- General method of delta to delta DDFC.

G2.3. GENERAL MODELS

The delta to intermediate code (linear PCM) and linear PCM to delta converters are completely digital. They work with sampled signals expressed in binary form. Therefore once per sampling period each block in the following diagrams receives a binary number representing the input value and uses it to compute the output value which is also a binary number.

G2.3.1. DELTA TO LINEAR PCM CONVERSION

Figure 2.3 shows the general model of a delta to linear PCM converter. The code conversion is made by the gain control circuit and a digital integrator.

FIGURE 2.3.- General model of a delta to linear PCM converter.

The intermediate code represents the amplitude of the transmitted signal. To reconstruct at delta sampling time this amplitude, the incoming delta sequence is first fed into the *gain control* circuit which determines the delta step size. This gain control circuit is a logic circuit which utilizes an algorithm similar to the algorithm of the delta modulator. Using the delta sequence, it generates once per Δ period a binary word which represents the value of the delta step at this instant. The digital *integrator* is another logic circuit which determines the amplitude of the transmitted signal by adding the delta step values. It is a digital addition and the output is a binary word: the intermediate code word.

The digital *filter* is a logic circuit which transforms the digital version of the signal (represented by the binary intermediate code) in the same way as a continuous filter would transform the analog version of the same signal (represented by an analog voltage). It is a low-pass filter (cut-off frequency around 3.5kHz) whose purpose is to attenuate high frequency components of the delta quantizing noise. The output of the filter is again a sequence of binary words which represents the transmitted signal smoothed by the low-pass characteristic.

G 2.3.2. LINEAR PCM TO DELTA CONVERSION

The general model of a linear PCM to delta converter is shown in Figure 2.4.

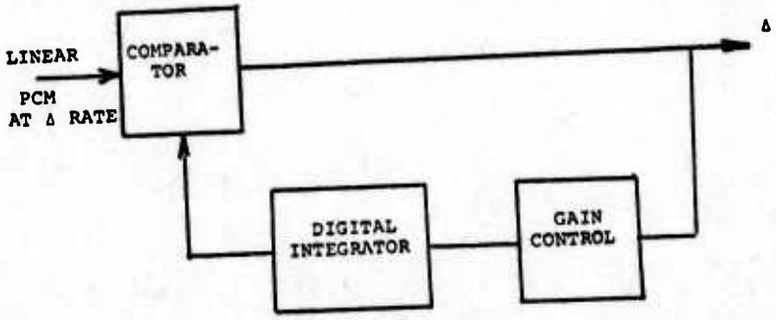


FIGURE 2.4.- General model of a linear PCM to Δ converter.

The *comparator* and the *gain control circuit* and the *digital integrator* realize the conversion from intermediate to delta codes. At each delta sampling time, the intermediate code word is compared to the binary word generated by the feedback loop (gain control and integrator). A delta bit one or zero is produced depending on the result of the comparison (positive or negative result). This delta bit is available for transmission and is also fed in the feedback loop. With this information, the gain control circuit and the digital integrator determine the value of the reconstructed signal. The gain control and the integrator have been described in Section G.2.3.1.

G 2.3.3. RATE CONVERTER

The rate conversion from delta F_1 sampling rate to delta F_2 sampling rate is done by interpolators and digital filters.

Figure 2.5 illustrates the rate converter.

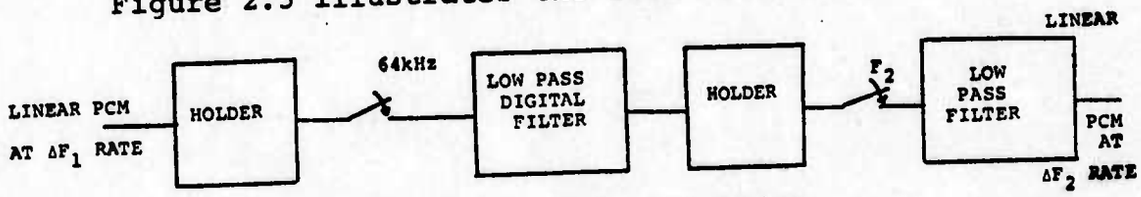


FIGURE 2.5.- Rate converter.

The linear PCM signal at delta rate F_1 is first held and sampled at 64kHz. This signal at 64kHz is then filtered by a low-pass digital filter (cut-off frequency 5kHz). This information passes through a second holder prior to being sampled at delta rate F_2 and low-pass filtered digitally. The output of this last digital filter is a linear PCM signal at delta rate F_2.

G3. COMPUTER SIMULATION

Studies were performed on an IBM 370/145 computer. A 750Hz test tone with a 40db dynamic range was used as input signal to the computer model. S/N ratios are obtained from the fast Fourier transform (F.F.T).

G3.1. MODELS

Figure 3.1 shows the block diagram of the overall system simulated on the computer. It represents the delta coder at F_1 rate, the DDFC unit and the delta decoder at F_2 rate.

In Figure 3.2 and in the following the DDFC is represented by digital filters which are defined by their Z-transfer functions. Each filter is represented by a box which contains the function with the proper coefficient values.

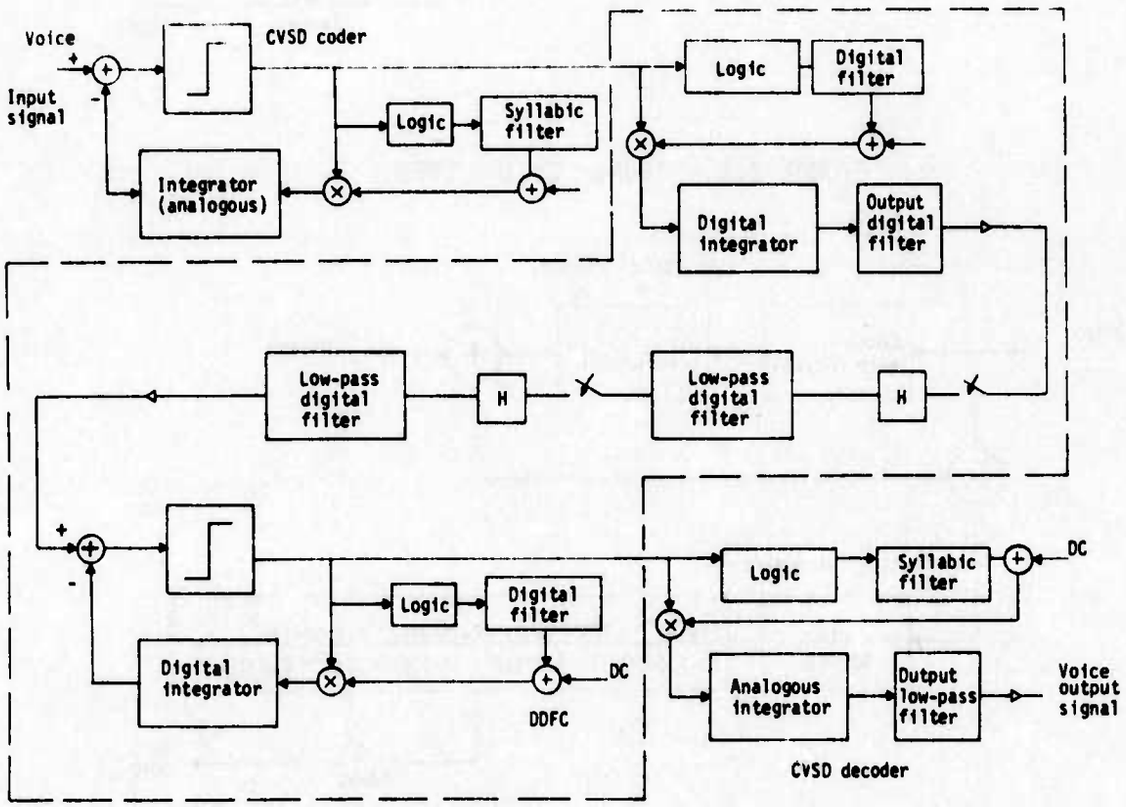


FIGURE 3.1.- Delta-delta system block diagram.

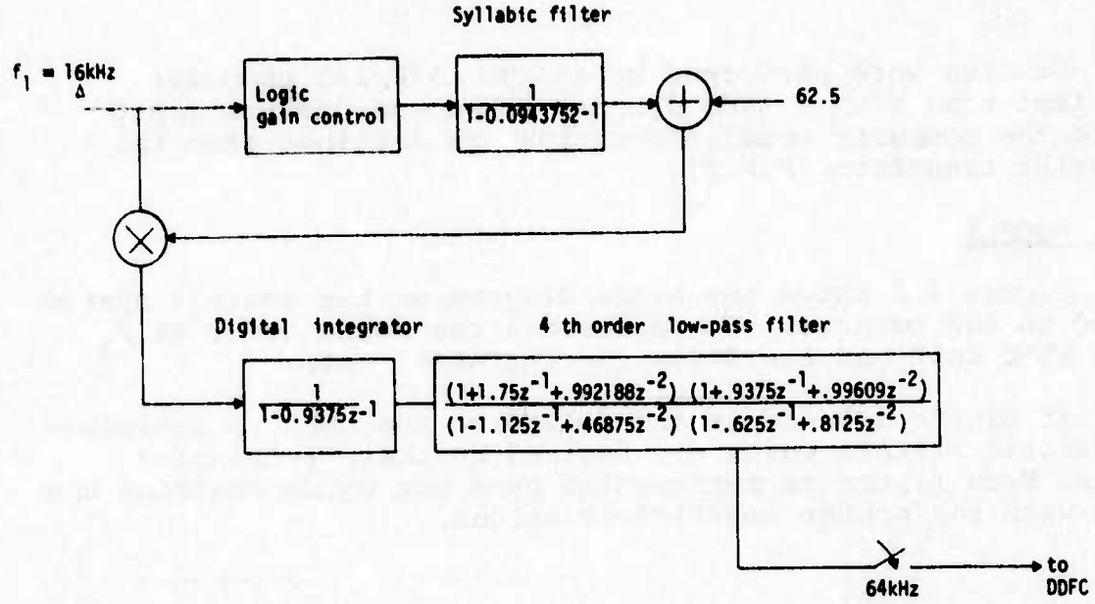


FIGURE 3.2.- 16kHz CVSD - DDFC.

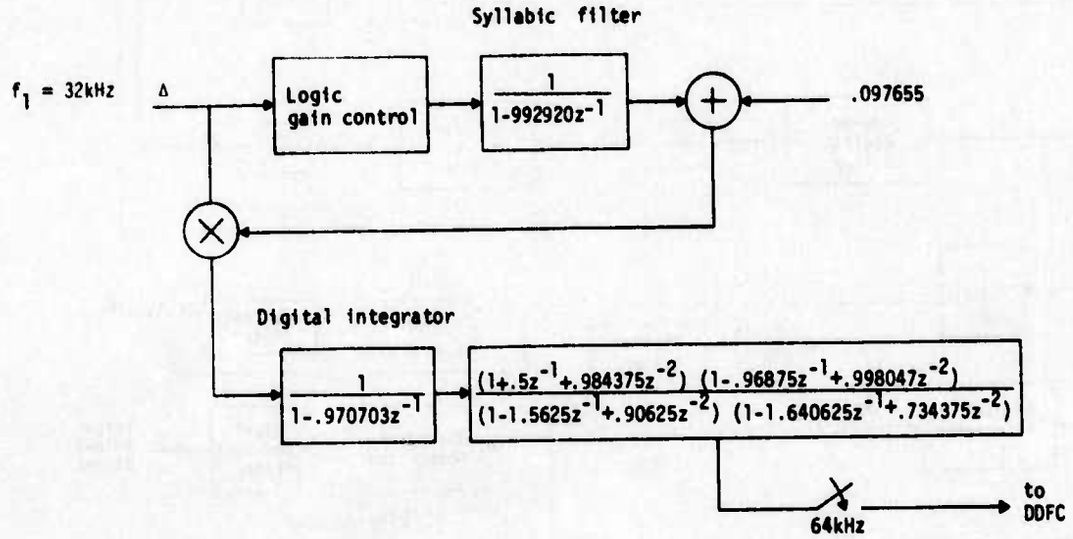


FIGURE 3.3.- 32kHz CVSD - DDFC.

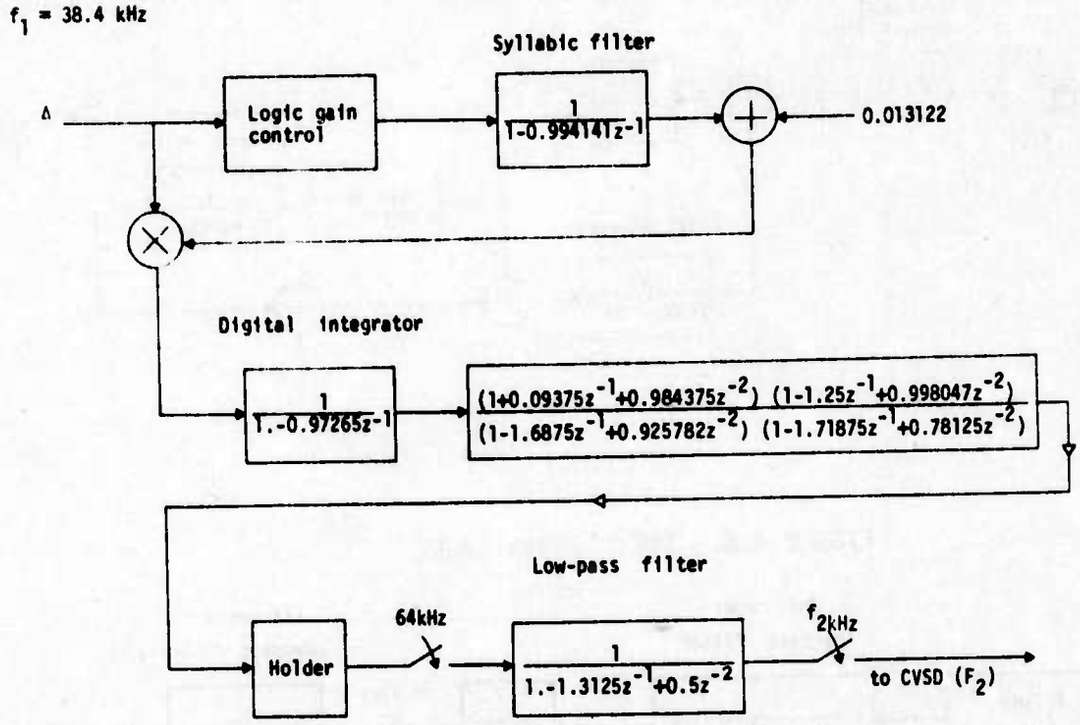


FIGURE 3.4.- 38.4kHz CVSD to DDFC.

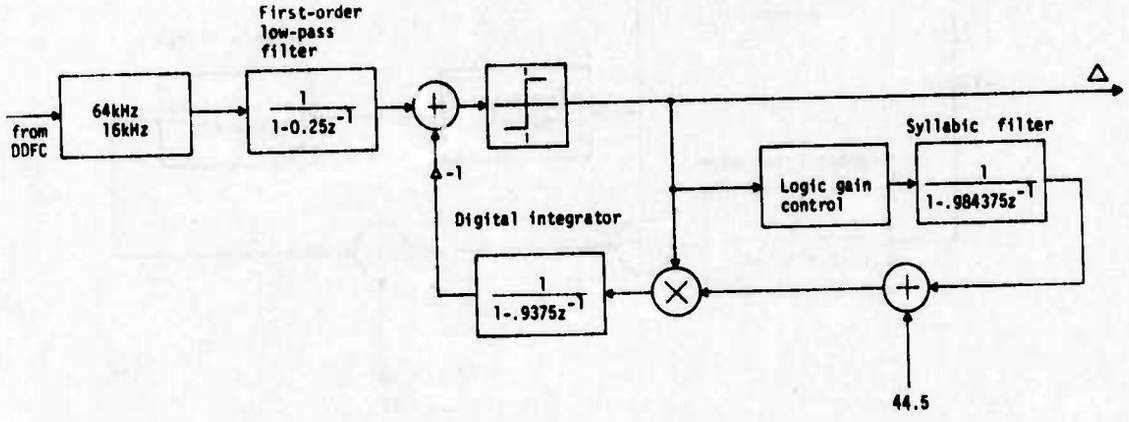


FIGURE 3.5.- DDFC to 16kHz CVSD.

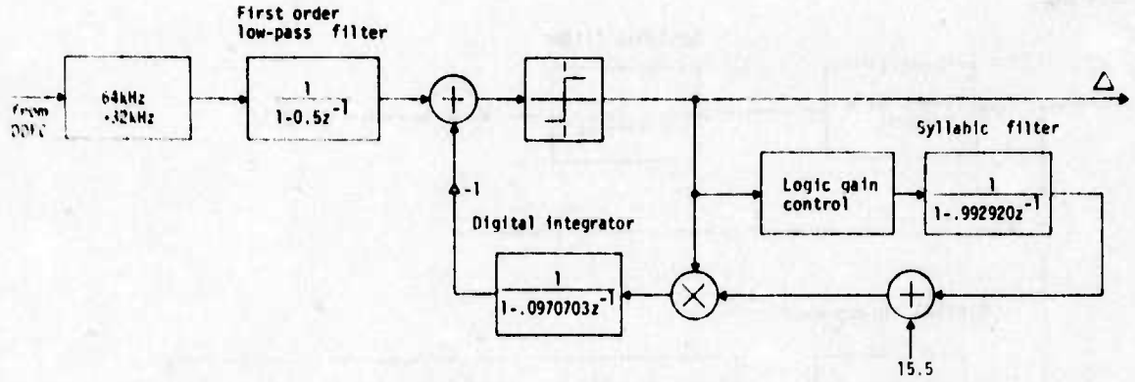


FIGURE 3.6.- DDFC -32kHz CVSD.

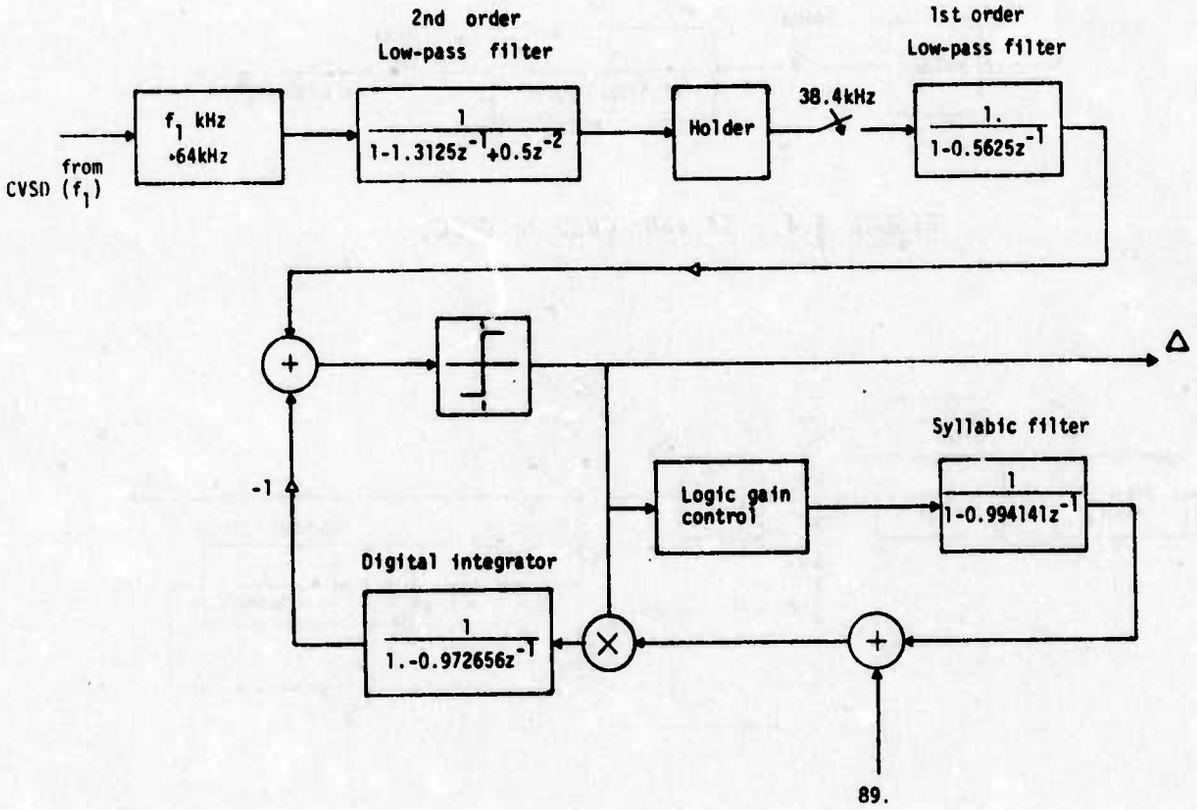


FIGURE 3.7.- DDFC to 38.4kHz CVSD.

G 3.2. SIMULATION RESULTS

Two cases were considered in the simulation:

-the first delta (transmitting) sampling rate F_1 is lower than the receiving delta sampling rate F_2 ($F_1 < F_2$).

-the receiving delta sampling rate F_2 is smaller than the transmitting delta sampling rate ($F_1 > F_2$).

G 3.2.1. F_1 DELTA RATE SMALLER THAN F_2 DELTA RATE

Let F_1 equal 16kHz and F_2 be 32 or 38.4kHz. Table 3.1 shows the S/N ratios obtained with and without the 64kHz rate converter digital filter.

	S/N (dB)				
Amplitude (Volt)	A	B	C	D	E
0.03	4.78	7.28	6.59	8.99	7.99
0.10	9.27	11.29	11.33	14.22	12.82
0.30	9.07	12.66	13.	13.44	13.77
0.60	11.14	16.32	17.01	18.43	18.25
1.00	12.89	15.86	16.20	16.46	15.85
2.00	13.97	15.01	15.16	15.00	15.13
3.00	14.08	14.11	14.41	15.71	14.75
6.00	13.77	15.37	15.26	14.55	14.36

A. reference: CVSD codec at 16kHz

B. F1 = 16K, F2 = 32K, with 64kHz low-pass filter

C. F1 = 16K, F2 = 32K, without 64kHz low-pass filter

D. F1 = 16K, F2 = 38.4K with 64kHz low-pass filter

E. F1 = 16K, F2 = 38.4K without 64 kHz low-pass filter

TABLE 3.1.- S/N ratios for $F_1 < F_2$.

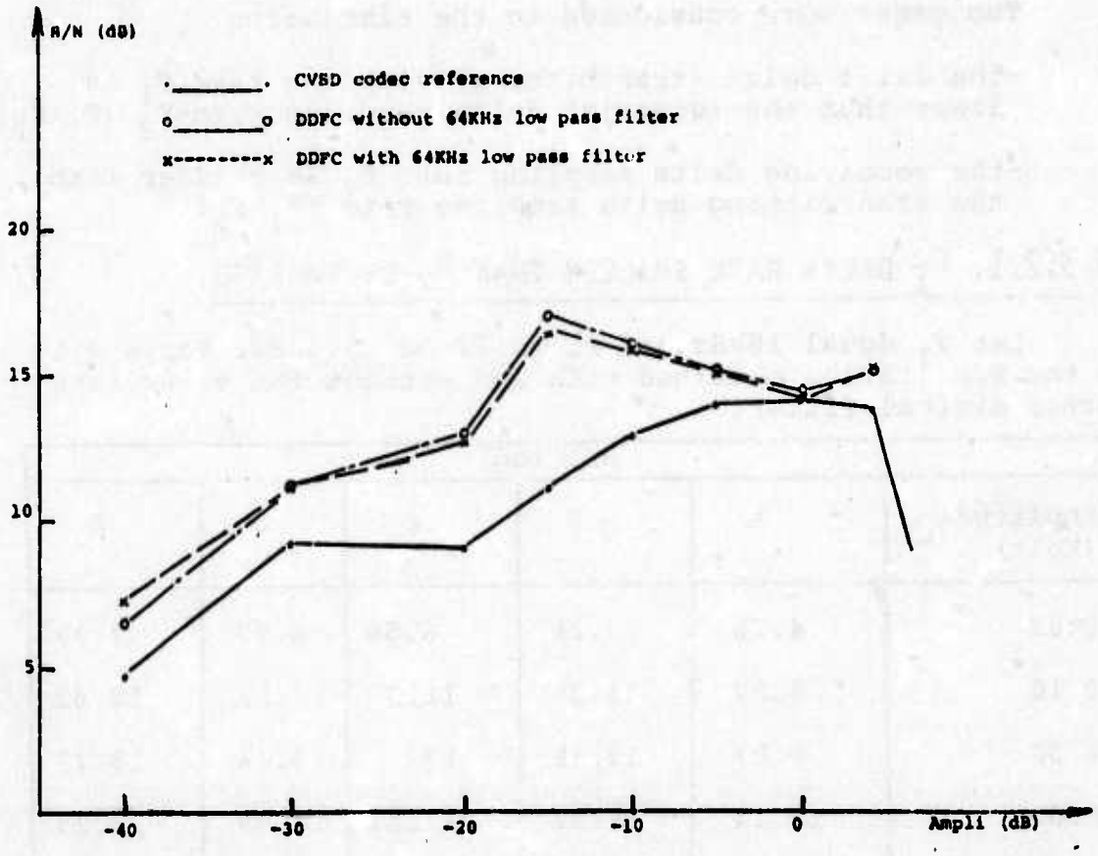


Figure 3.8.- S/N of CVSD 16-CVSD 32 System.

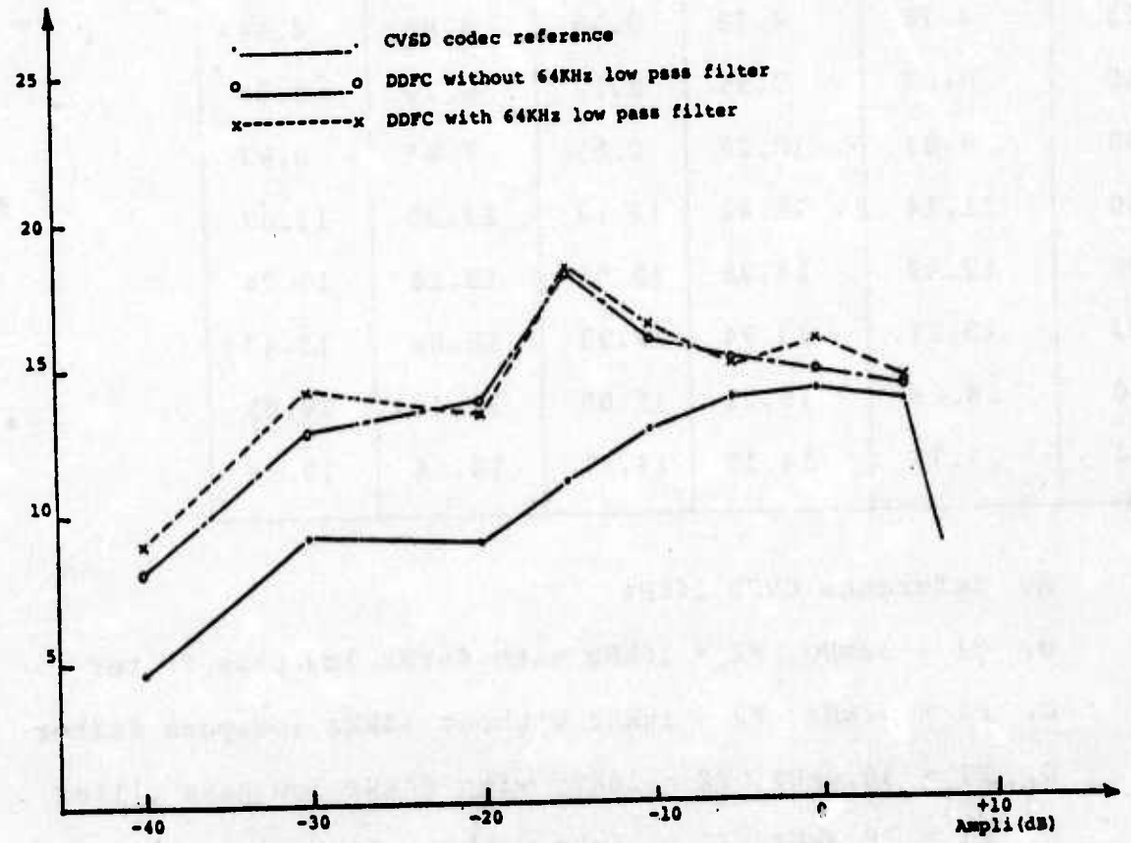


Figure 3.9.- S/N of CVSD 16-CVSD 38.4 system.

Figures 3.8 and 3.9 resume Table 3.1.

G3.2.2. F_1 DELTA RATE BIGGER THAN F_2 DELTA RATE

Table 3.2 shows the S/N ratios obtained for $F_1 > F_2$. The reference being the 32KHz delta coder-decoder back to back.

S/N					
Ampli	A	B	C	D	E
0.03	4.78	4.78	3.54	4.60	4.64
0.10	9.27	7.96	8.12	8.10	9.00
0.30	9.07	10.28	8.53	8.83	8.93
0.60	11.14	11.92	12.19	12.25	12.07
1.00	12.89	13.28	12.55	13.16	13.24
2.00	13.97	13.94	12.93	13.52	13.43
3.00	14.08	15.25	15.00	14.43	14.09
6.00	13.77	14.15	14.17	13.54	13.88

A. reference CVSD 16kHz

B. Fl = 32kHz, F2 = 16kHz with 64kHz low-pass filter

C. Fl = 32kHz, F2 = 16kHz without 64kHz low-pass filter

D. Fl = 38.4kHz, F2 = 16kHz with 64kHz low-pass filter

E. Fl = 38.4kHz, F2 = 16kHz without 64kHz low-pass filter.

TABLE 3.2.- S/N ratios for $F_1 > F_2$.

Figures 3.10 and 3.11 resume Table 3.2.

G3.3. CONCLUSION

It has been shown that the conversion from low rate delta (16kHz) to higher rate delta (32 or 38.4kHz) gives a better S/N ratio at the output, thus improving the 16kHz delta quality.

In the reverse direction from 32 (or 38.4kHz) to 16kHz the quality at the output is no longer that of the 32kHz (or 38.4 kHz) delta but more or less that of the 16kHz delta.

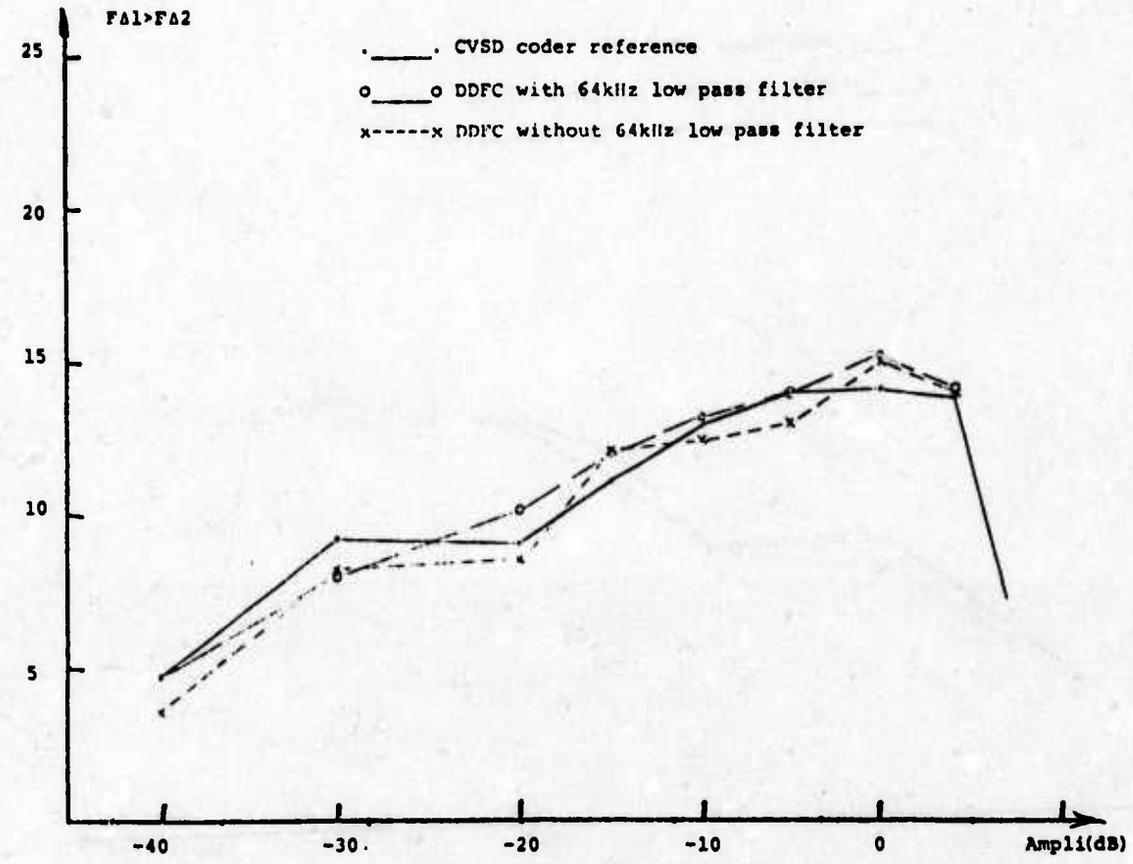


FIGURE 3.10.- S/N of CVSD 32 - CVSD 16 system.

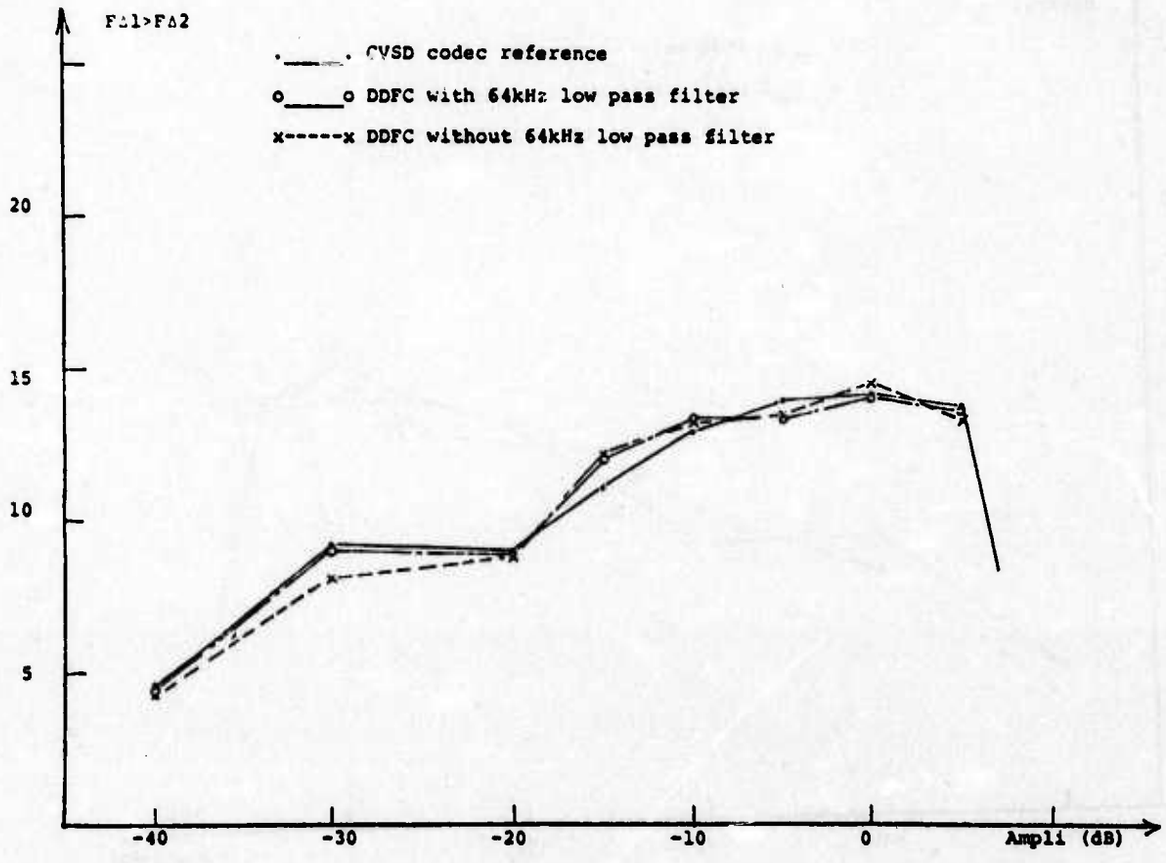


FIGURE 3.11.- S/N of CVSD 38.4 - CVSD 16 system.

G 4. CONCLUSION

The objective aimed at in this appendix on a *direct digital frequency converter* from delta to delta was to establish the feasibility of such an unit.

Computer simulation proved that the conversion is possible, with a quality equal to or better than the worse quality delta involved in the conversion process.

In this study we have reported results on a conversion system for two CVSD delta codecs at sampling rates of 16, 32 and 38.4kHz but the conception of the DDFC could be generalized for different kinds of delta modulators and for any sampling rate.

This DDFC could be incorporated in the DDMC, most of the digital functions involved in the DDFC being present in the DDMC.

APPENDIX H

SIGNAL REPRESENTATION WITHIN DDMC

H1. GENERAL MODELS

General models for a Δ to PCM and PCM to Δ DDMC are shown in Figure 1. They are valid for all types of ΔM, where companding is made inside the loop.

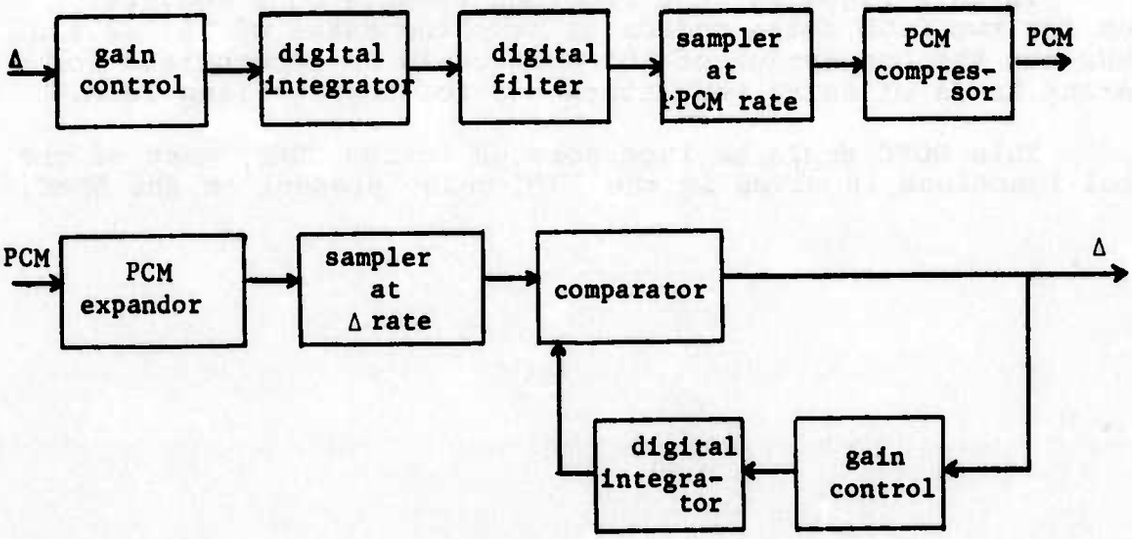


Figure 1. Converters, General Models.

The Δ to PCM and PCM to Δ DDMC's are completely digital. They are working with sampled signals expressed in binary form. Therefore, once per sampling period,each block in the diagram receives a binary number representing the input value and uses it to compute the output value which is a binary number too.

H2. ΔM TO PCM

The incoming Δ sequence is fed into the gain control circuit to determine the step size values. Steps are added in the digital integrator. The output of the integrator is thus a binary word representing the amplitude of the voice signal. The integrator could be an up-down counter or a digital filter equivalent to a leaky integrator. The latter has been chosen as it cancels the DC drift.

The voice signal, reconstructed in the integrator is then digitally filtered to remove ΔM quantizing noise. At this point, binary samples of the signal are available at Δ sampling rate.

This information must be sampled again at PCM Rate (8KHz) to be transmitted on the PCM line. When the Δ sampling frequency is 19.2KHz or 38.4KHz, intermediate values between the samples are needed and they are estimated by a curve fitting method.

A binary, linear representation of the voice signal is now available at every PCM sampling time. This linear PCM is then compressed into a non-linear 7 or 8 bit PCM according to the remote PCM channel bank characteristics.

To illustrate the principle of the Δ to PCM DDMC, values of samples found in several points of the circuit are shown in Figure 2, in the case of instantaneous Δ modulation at 19.2 KHz. It is to be understood that when the system will be built, it will be impossible to visualize the waveforms of Figure 1 with a scope because there is no analog voltage to represent the samples. All the conversion is made by means of digital operations on binary numbers. Table 1 shows these numbers and their decimal values. The sign, in the binary representation, is given by the first bit (1=+ ; 0= -). The table 1 must be read in the following manner:

- time is increasing from top to bottom,
- there is one line per sampling time.

For instance, in the first line (first period considered) the gain control circuit receives a Δ bit equal to 1 and generates the number 10100 (+4) which is sent to the digital integrator to give 10001.00 (+1.00) and so on.

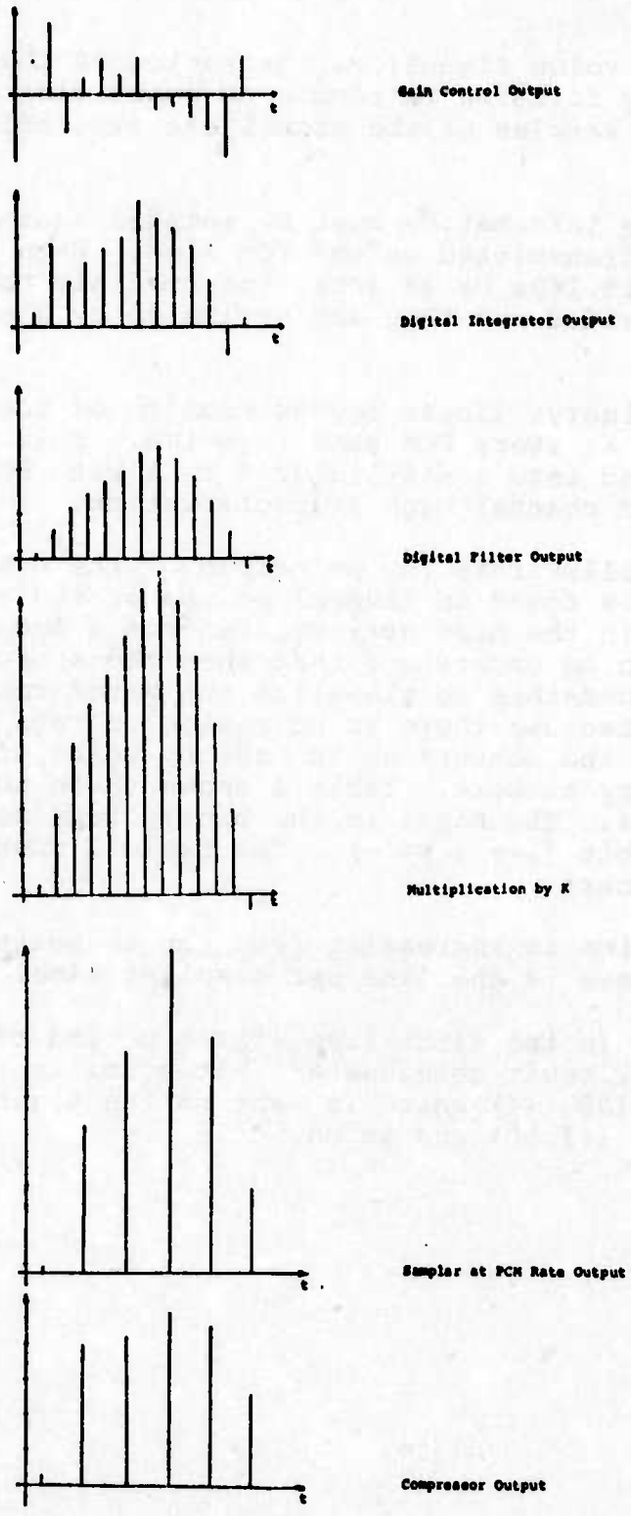


Figure 2. Δ to PCM - DDMC

	Δ bits	Gain Control Output		Digital Integrator Output		Digital Filter Output		Multiplication by K (K = 3)		Sampler at PCM Rate Output		Compressor Output	
Δ Period ↕ = 1/19200 s	1	10100	+ 4	10001.00	+ 1.00	10000.01	+ 0.25	1000000.11	+ 0.75	1000000.11	+ 0.75	1000011	+ 3
	1	11000	+ 8	11001.00	+ 9.00	10011.00	+ 3.00	1001001.00	+ 9.00				
	0	00100	- 4	10101.00	+ 5.00	10101.11	+ 5.75	1010001.01	+17.25	1010001.01	+17.25	1101000	+40
	1	10010	+ 2	10111.00	+ 7.00	10111.01	+ 7.25	1010101.11	+21.75	PCM period = 1/8000 s			
	1	10001	+ 1	11000.00	+ 8.00	11000.10	+ 8.50	1011001.10	+25.50				
	1	10010	+ 2	11010.00	+10.00	11001.11	+ 9.75	1011101.01	+29.25	1011001.10	+25.50	1101100	+42
	1	10100	+ 4	11110.00	+14.00	11011.10	+11.50	1100010.10	+34.50				
	0	00010	- 2	11100.00	+12.00	11100.01	+12.25	1100100.11	+36.75	1100100.11	+36.75	1110001	+49
	0	00001	- 1	11011.00	+11.00	11011.00	+11.00	1100001.00	+33.00				
	0	00010	- 2	11001.00	+ 9.00	11001.00	+ 9.00	1011011.00	+27.00	1011011.00	+27.00	1101101	+45
	0	00100	- 4	10101.00	+ 5.00	10110.01	+ 6.25	1010010.11	+18.75				
	0	01000	- 8	00011.00	- 3.00	10011.01	+ 3.25	1001001.11	+ 9.75	1001001.11	+ 9.75	1011001	+25
	1	10100	+ 4	10001.00	+ 1.00	00000.10	- 0.50	0000001.10	- 1.5				

Table 1. Example of Δ to PCM Conversion.

H3. PCM TO ΔM

The incoming compressed PCM word is expanded, according to the PCM system characteristics, into a binary linear representation of the signal amplitude. Linear PCM samples, expressed in binary form, are therefore available at PCM sampling rate.

The sampling circuit provides estimates of the signal amplitude at Δ rate. Intermediate (between two PCM samples) samples are estimated by a curve fitting method.

Comparisons between these samples and the output of the digital feedback loop determine the Δ sequence.

The feedback loop is made of a gain control circuit and a digital integrator similar to those of the Δ to PCM DDMC.

Figure 3 shows sample values in the PCM to Δ DDMC. It illustrates the case of a converter for 19.2KHz instantaneous Δ modulation. All the comments given above for the Δ to PCM DDMC are still valid.

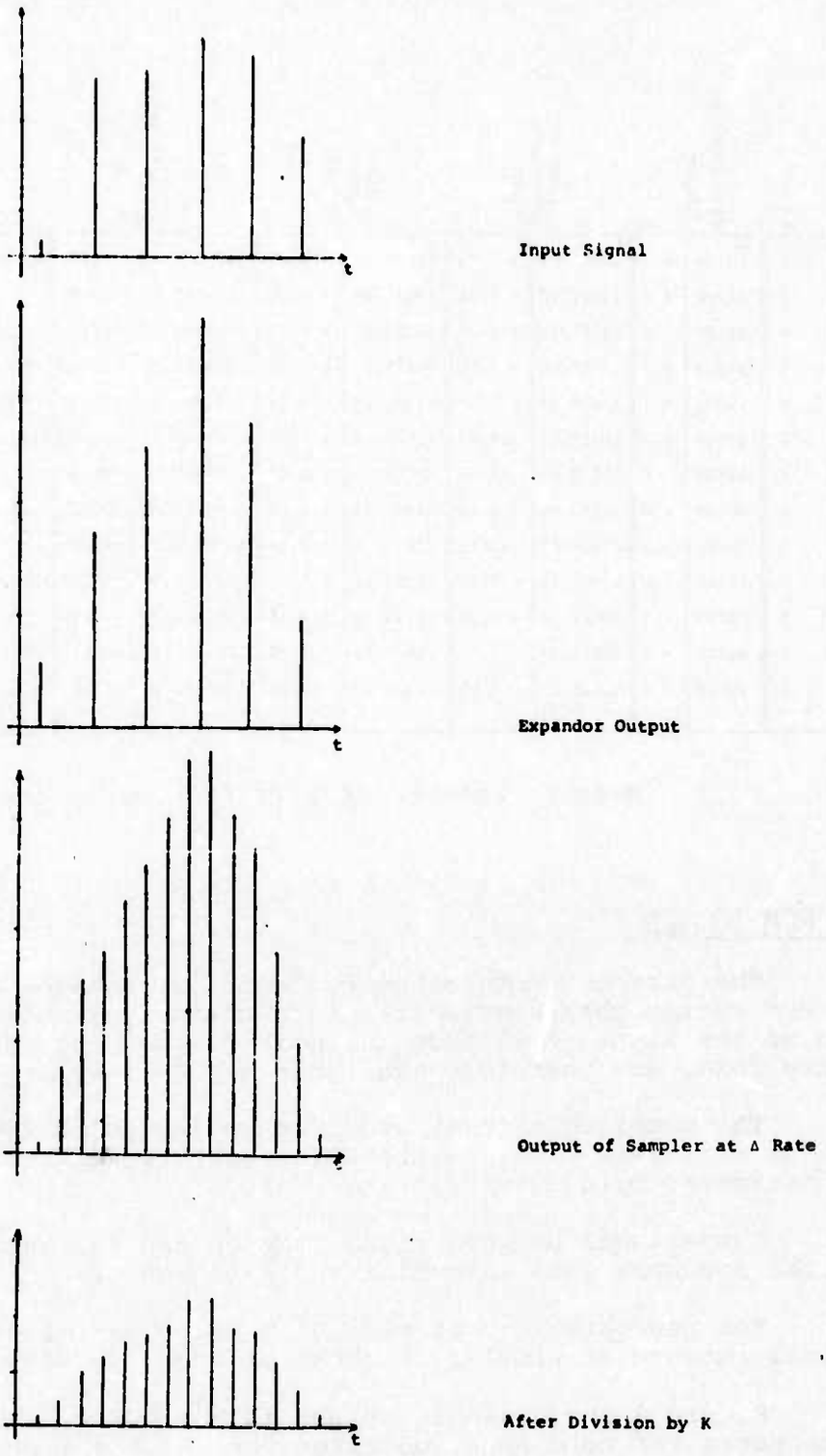


Figure 3. PCM to Δ DDMC.

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