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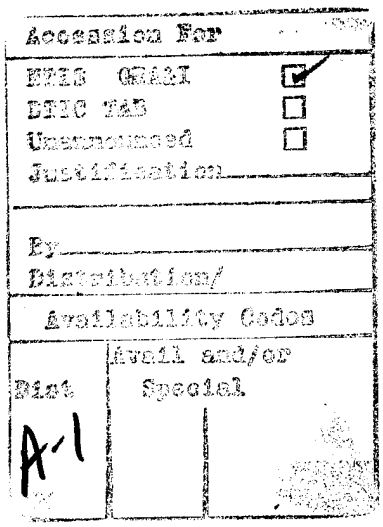

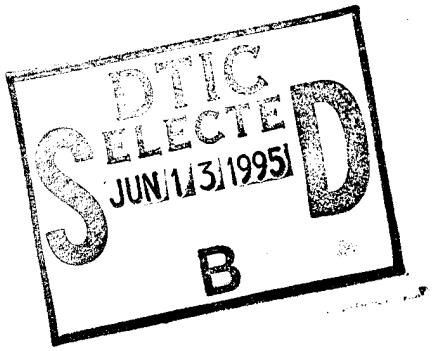

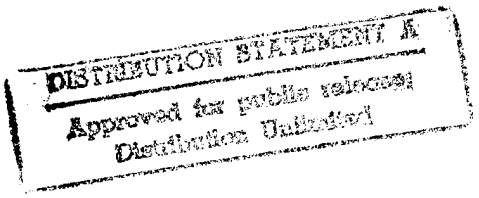

Serial No. (Unassigned) Patent Application
Applicant: Pace Attorney Docket No. 76,164

HIGH RESOLUTION ENCODING CIRCUIT AND PROCESS FOR ANALOG TO DIGITAL CONVERSION

Specification

Background of the Invention

High performance analog to digital converters typically employ a parallel configuration of analog folding circuits to symmetrically fold input signals prior to quantization by high-speed comparators. Such a circuit uses two comparator ladders, having a total of $2(2^{n/2}-1)$ comparators in the two legs together, where n is the bit resolution of the converter. The comparator ladder in each leg performs an n/2 bit binary encoding of the analog input. Because the number of levels depends exponentially on n, the number of comparators which one must employ rises exponentially with circuit resolution. This can make many engineering applications of such circuits expensive. Moreover, skew time—the time lag between receipt of analog input and delivery of quantized output—increases with increasing number of comparators; and as the number of comparators increases, the power they consume does also, leaving less system power available for signal detection, thus reducing system bandwidth.

Summary of the Invention

Accordingly, an object of the invention is to increase the bit

resolution per comparator in analog-to-digital converters significantly beyond that which is currently available.

Another object is to reduce the skew time in such circuits by reducing the number of comparators necessary for a given circuit bit resolution.

Another object is to decrease the power consumption of such circuits, and increase circuit bandwidth, by reducing the total number of comparators necessary for a given circuit resolution.

In accordance with these and other objects made apparent hereinafter, the invention concerns an analog to digital converter having N folding circuits, N being a positive, non-zero, integer greater than or equal to 2, which receive an analog input. Each of the folding circuits has an associated integer modulus m_n, n = 1, . . ., N, each of which moduli are relatively prime with respect to one another, and folds the input in accordance with a preselected folding function whose folding period is $2m_n$.

The output of the folding circuits, when detected by an associated comparator ladder having as few as m_n-1 comparators per ladder, provide a digital output which uniquely corresponds to the amplitude of the analog input, with a dynamic range equal to the product of the moduli. Because the total number of comparators needed to detect the folding circuits' outputs are on the order of the sum of the moduli, the larger the moduli, the larger the ratio of dynamic range to the number of required comparators. One can implement the invention with relatively low power comparators, and

still convert relatively high power analog signals.

These and other objects, features, and advantages of the invention are further understood from the following detailed description of particular embodiments. It is understood, however, that the invention is capable of extended application beyond the precise details of these embodiments. Changes and modifications can be made to the embodiments that do not affect the spirit of the invention, nor exceed its scope, as expressed in the appended claims. The embodiments are described with particular reference to the accompanying drawings, wherein:

Brief Description of the Drawings

Figure 1 is a graph illustrating the notion of folded waveforms.

Figure 2 is an electronic schematic showing a circuit according to an embodiment of the invention.

Figure 3 is a graph illustrating the interrelationships of folded waveforms generated by the circuit of figure 1.

Figure 4 shows another embodiment of the invention.

Figure 5 is a graph, similar to that of figure 3, illustrating additional features of the embodiment of figure 4.

Detailed Description

With particular reference to the drawing figures, figure 1 shows four exemplary waveforms as functions of input signal v_{in}, to

illustrate the notion of folded waveforms. A folded waveform is a signal, generated responsive to a monotonically increasing input (here, v_{in}), which periodically increases and decreases between maximum and minimum levels with monotonically increasing input. The waveforms are even functions, i.e. mirror image symmetrical about the vertical axis in figure 1. Waveform 20 is a triangular folded signal, waveform 22 is a rectified sinusoidal folded signal, and waveform 24 is a sinusoidal squared folded signal. The range of input magnitude over which such a folded signal repeats is the folding period v_f.

Figure 2 shows a circuit according to the invention, having an input signal v_{in} 10 fed in parallel to N folding circuits 12_n, n = 1, 2, . . ., N, N≥2. Each folding circuit 12 has a different integer modulus m_n, the meaning of which is discussed below in reference to figure 3. Each circuit 12 folds input 10 in accordance with a preselected folding function. Circuits to perform folding are known, and folding circuits *per se* form no part of this invention. The folding period of each circuit 12 is $2m_n$, i.e. $v_{f(m_n)}=2m_n$, where $v_{f(m_n)}$ is the folding period of the circuit 12_n having modulus m_n. The N moduli are relatively prime with respect to one another, i.e. no modulus has any common factor with any other of the moduli (other than 1). The N folding circuits 12 transform input signal 10 into N corresponding folded outputs which respective lines 16_1, 16_2, . . ., 16_N direct to respective detector

ladders 14_1, 14_2, . . ., 14_N. Each ladder 14 is composed of m_n-1 signal comparators, or level detectors, $C_{m_n,1}$, $C_{m_n,2}$, . . ., C_{m_n,m_n-1}. (C_{m_n,m_n-1} means the m_n-1th comparator of the nth ladder, the nth ladder being fed the output of a folding circuit of modulus m_n.) Detectors C are preferably differential amplifiers, such as operational amplifiers, biased via potentiometers 15 to trigger (change state) at appropriate input signal levels. However, detectors C could be any conventional difference amplifier, or simple diodes which are back biased at desired trigger signal levels. Output from each level detector C in signal ladders 14 is fed to decoder 18, which determines from the states of detectors C (i.e. on or off) what the magnitude of input v_{in} is, and outputs this magnitude via line 19 in digital form. The manner in which this is done is discussed below with reference to figures 3 ff. Preferably, decoder 18 is a read only memory (ROM) programmed with the truth table relating comparator input states to the magnitude of v_{in}, but more broadly could be any logical device effective to interpret a digital input and translate it according to a preset logical rule into a corresponding output.

Trigger biases of the comparators of figure 2 are set via potentiometer 15 so that comparators in each leg trigger at constant increments of input signal v_{in}. Thus, for example, in ladder 14 fed by an input from folding circuit 12 having modulus m_n, comparators $C_{m_n,l}$, l=1, 2, . . ., m_n-1, trigger at corresponding intervals $v_{t(n,l)}=l\Delta v$, i.e. Δv, 2Δ, . . ., $(m_n-1)\Delta v$ respectively,

where Δv is the least significant bit, typically in volts. Because of the symmetry of the folding functions dictated by circuits 12, and because the folding period of each folding function is $2m_n$, if the origins of v_{in} and the outputs of the folding circuits are registered (outputs of all N folding circuits 12 are zero for $v_{in}=0$), $v_{in} = m_n\Delta v$ corresponds to the maximum output of each folding circuit, and $v_{in} = 2m_n\Delta v$ corresponds to the minimum output of each folding circuit. A further consequence is that input levels v_t align from ladder to ladder, i.e. $v_{t(1,1)} = v_{t(2,1)} = \cdot\ \cdot\ \cdot = v_{t(N,1)} = \Delta v$, $v_{t(1,2)} = v_{t(2,2)} = \cdot\ \cdot\ \cdot$, $v_{t(N,2)} = 2\Delta v$, etc., with specific exceptions discussed below concerning the maxima and minima of the folding function.

Figure 3 illustrates motivation for, and the advantages of, this scheme, and in particular shows the folded outputs 30, 32, and 34, of a circuit like that of figure 2, having three folding circuits of moduli 2, 3, and 5, i.e. N=3, $m_1=2$, $m_2=3$, and $m_3=5$. As above, the folding period of each is $v_{f(m_n)}=2m_n\Delta v$. Thus for modulus 2, the folding period is $4\Delta v$, for modulus 3 the period is $6\Delta v$, and for modulus 5 the period is $10\Delta v$, which one can see also by inspection of figure 3. The comparator tree associated with each modulus has m_n-1 comparators $C_{m_n,l}$ $l = 1\ \cdot\ \cdot\ \cdot, m_n-1$, biased to trigger at $v_{in}=1\Delta v$. Thus modulus 2 has but one comparator, $C_{2,1}$, biased to trigger at $v_{in} = (1)\Delta v$, with the corresponding potentiometer bias $T_{m_n,l}=T_{2,1}$ indicated on figure 3; modulus 3 has two

comparators $C_{3,1}$ and $C_{3,2}$, biased to trigger at $v_{in} = \Delta v$ and $2\Delta v$ respectively, corresponding to biases $T_{3,1}$ and $T_{3,2}$; modulus 5 has four comparators, $C_{5,1}$, $C_{5,2}$, $C_{5,3}$, and $C_{5,4}$, with corresponding potentiometer biases $T_{5,1}$, $T_{5,2}$, $T_{5,3}$, $T_{5,4}$ set to cause the comparators to trigger at Δv, $2\Delta v$, $3\Delta v$, and $4\Delta v$ respectively. (For convenience, on figure 3 specific system comparators are listed below the value of v_{in} at which they are biased to trigger, e.g. $C_{2,1}$ with $1\Delta v$, $C_{5,4}$ with $4\Delta v$, etc.). Because of the periodic nature of folded outputs 30, 32, 34, the comparators will trigger repeatedly at fixed periods: thus e.g. $C_{2,1}$ triggers at Δv, $3\Delta v$, $5\Delta v$, etc.; $C_{3,2}$ triggers at $2\Delta v$, $4\Delta v$, $8\Delta v$, etc.; $C_{5,1}$ triggers at Δv, $9\Delta v$, etc. The only increments of Δv at which no comparator triggering in each modulus occurs is at the peaks and troughs of folded waveforms 30, 32, 34, which occur for each modulus at $km_n\Delta v$, $k = 0, 1, 2, \ldots, \infty$, e.g. for modulus 2 ($m_n=2$), 0, $2\Delta v$, $4\Delta v$, $6\Delta v$ etc.; for modulus 3, 0, $3\Delta v$, $6\Delta v$, etc.; for modulus 5, 0, $5\Delta v$, $10\Delta v$, etc. The peaks and troughs of the folded input for one leg will align with level transitions of the other legs.

The truth table for this scheme is as follows:

Normalized Input	Modulus		
	2	3	5
0	0	0	0
1	1	1	1
2	1	2	2
3	0	2	3
4	0	1	4
5	1	0	4
6	1	0	3
7	0	1	2
8	0	2	1
9	1	2	0
10	1	1	0
11	0	0	1
12	0	0	2
13	1	1	3
14	1	2	4
15	0	2	4
16	0	1	3
17	1	0	2
18	1	0	1
19	0	1	0
20	0	2	0
21	1	2	1
22	1	1	2
23	0	0	3
24	0	0	4
25	1	1	4
26	1	2	3
27	0	2	2
28	0	1	1
29	1	0	0
30	1	0	0
31	0	1	1
32	0	2	2
33	1	2	3
34	1	1	4
35	0	0	4

where the "Normalized Input" is v_{in} normalized to Δv (and rounded off to the next lower integer), and "Modulus 2, 3, 5" represent the three legs of figure 2. Integer values in the three columns under "Modulus" represent the number of comparators in the "ON" state in

each leg for a given input signal level. Thus, for v_{in} between $5\Delta v$ and $6\Delta v$, the level number is 5, and the comparator ladder for modulus 2 would have one comparator in the "ON" state, the ladder for modulus 3 would have zero comparators in the "ON" state, and the ladder for modulus 5 would have four comparators in the "ON" state. Inspection of the truth table reveals that the combination of comparators in the "ON" state does not repeat until level number 30, at which point the combinations repeat in reverse order. Thus the combinations of comparators in the "ON" state uniquely and unambiguously correspond to increments in the amplitude of v_{in}. Stated more conventionally, the dynamic range of the circuit is thirty quantization levels. Not coincidentally, this is the product of the moduli for the three folding circuits. Because the moduli are prime with respect to one another, and the folding periods of each folding function are proportional to that function's modulus, the folding functions cannot repeat the same phase relationship with respect to one another in less than a span of Δv times the product of the moduli. The number of comparators necessary to implement this circuit, however, is only 7, i.e. $\Sigma_n(m_n-1)=\Sigma_n m_n-N=10-3=7$, considerably less than the thirty which one would need to implement a conventional flash analog to digital converter of equal dynamic range. More generally, the dynamic range of the circuit of figure 2 is the product of the moduli of the its N folding circuits times Δv, the number of comparators necessary to implement the circuit is $\Sigma_n(m_n-1)$, and the number of comparators necessary to do

this will always be less than the number of input signal levels which can be resolved.

A source of error in the circuit of figure 2, or in any circuit employing comparators, is an input signal whose magnitude lies near a trigger point of one or more comparators. Circuit elements will have small performance discrepancies among components, which inevitably result in small variances in the triggering of individual comparators. The circuit of figure 2 requires triggering of a comparator in each of several legs simultaneously each time input signal v_{in} crosses $l\Delta v$, for any l. In figure 3, for example, as v_{in} crosses $2\Delta v$, comparators $C_{3,2}$ and $C_{5,2}$ should trigger to the "ON" state simultaneously. However, if the parameters or biasing of comparators $C_{3,2}$ and $C_{5,2}$ vary slightly, a magnitude of v_{in} very close to $2\Delta v$ could result in one of the comparators being triggered on, and one not, the result of which is that the code output to decoder 18 is wrong, resulting in a large output error. It is thus desirable that data resulting from an input near a comparator transition be discarded. The circuit of figure 4 does this. This circuit is identical to that of figure 2, but has associated with the comparator ladder for n=1 an additional set of m_1+1 comparators $C'_{m_1,p}$, $p = 1, \ldots, m_1+1$. (Please see, e.g., figure 5, the response curve of modulus 2.) These $2m_1$ comparators are deployed as follows: m_1-1 of them are paired with respective ones of the original m_1-1 comparators in comparator ladder 14_1, and biasing potentiometer 15, 15' set so that one

comparator in each pair will trigger just below a desired transition point, and the other just above it. By deploying the comparators in this manner, one effectively brackets each code transition point in the dynamic range of the system.

As an illustration, the original comparator threshold level for $m_1=2$ in figure 3 is replaced by two threshold levels (one slightly above the original threshold level, and one slightly below, to bracket decimation bands 36 at $1\Delta v$, $3\Delta v$, $5\Delta v$, etc.) as shown in figure 5. Also shown are the remaining two threshold levels, one just below the maximum (at $2\Delta v$, $6\Delta v$, etc.), and one just below the minimum (at $4\Delta v$, $8\Delta v$, etc.) to form decimation bands 36 disposed about the maxima and minima of folded waveform 30. In this manner each level transition, i.e. each increment of Δv in v_{in} is bracketed by a pair of comparators, throughout the entire dynamic range of the circuit.

In practice, the comparators in each pair are biased to ensure a triggering difference in v_{in} between them larger than any anticipated drift or offset due to component imperfections, etc. This triggering difference, or bracket width, is indicated by numeral 36 in figure 5. Parity check circuit 42 reads the states of these $2m_1$ comparators to determine whether an even or odd number of them are "ON." For an input signal outside any of brackets 36, i.e. distant from any level transition, but above zero, the comparator associated with the signal trough will be "ON." As v_{in} passes among the transition levels, so long as v_{in} is outside any decimation band

36, each pair of comparators associated with the various transition levels will have the same state, either on or off, and the total number of on-comparators will be odd. Upon v_{in} entering a decimation band 36, the lower biased comparator associated with the band triggers, but the higher biased comparator still remains off. Circuit 42 identifies the change in parity from odd to even, and suppresses data transmission, e.g. discards the current data point.

As just discussed, one can implement this parity checking scheme with any comparator ladder 14. Preferably one will do so with the ladder corresponding to smallest circuit modulus, to minimize the number of comparators in the circuit.

The invention has been described in what is considered to be the most practical and preferred embodiments. It is recognized, however, that obvious modifications to these embodiments may occur to those with skill in this art.

Abstract of the Invention

An analog-to-digital converter in which an analog input signal is folded by a plurality of folding circuits whose moduli, and hence half folding periods, are mutually prime with respect to one another. Each folding circuit has an associated comparator ladder having one less comparator than the modulus of the folding circuit. The collective output of the ladders, i.e. the states of the comparators in the ladders, uniquely corresponds to input signal magnitude over a dynamic range equal to the product of the folding circuits' moduli, permitting a greater dynamic range for the converter for the number of comparators used.

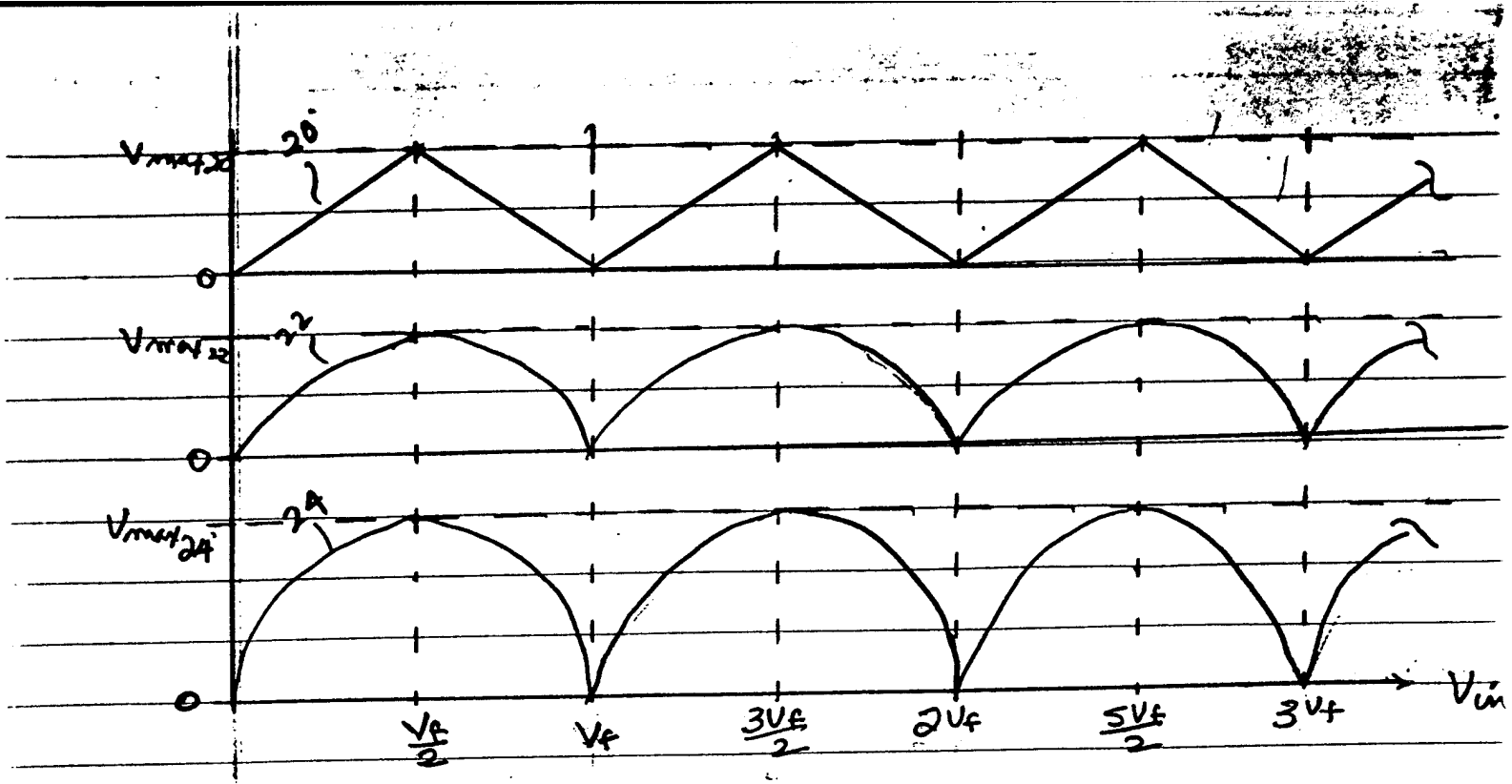
$V_{max,2^0}$
2^0
0
$V_{max,2^2}$
2^2
0
$V_{max,2^4}$
2^4
0
$\frac{V_f}{2}$
V_f
$\frac{3V_f}{2}$
$2V_f$
$\frac{5V_f}{2}$
$3V_f$
V_{in}

Figure 1

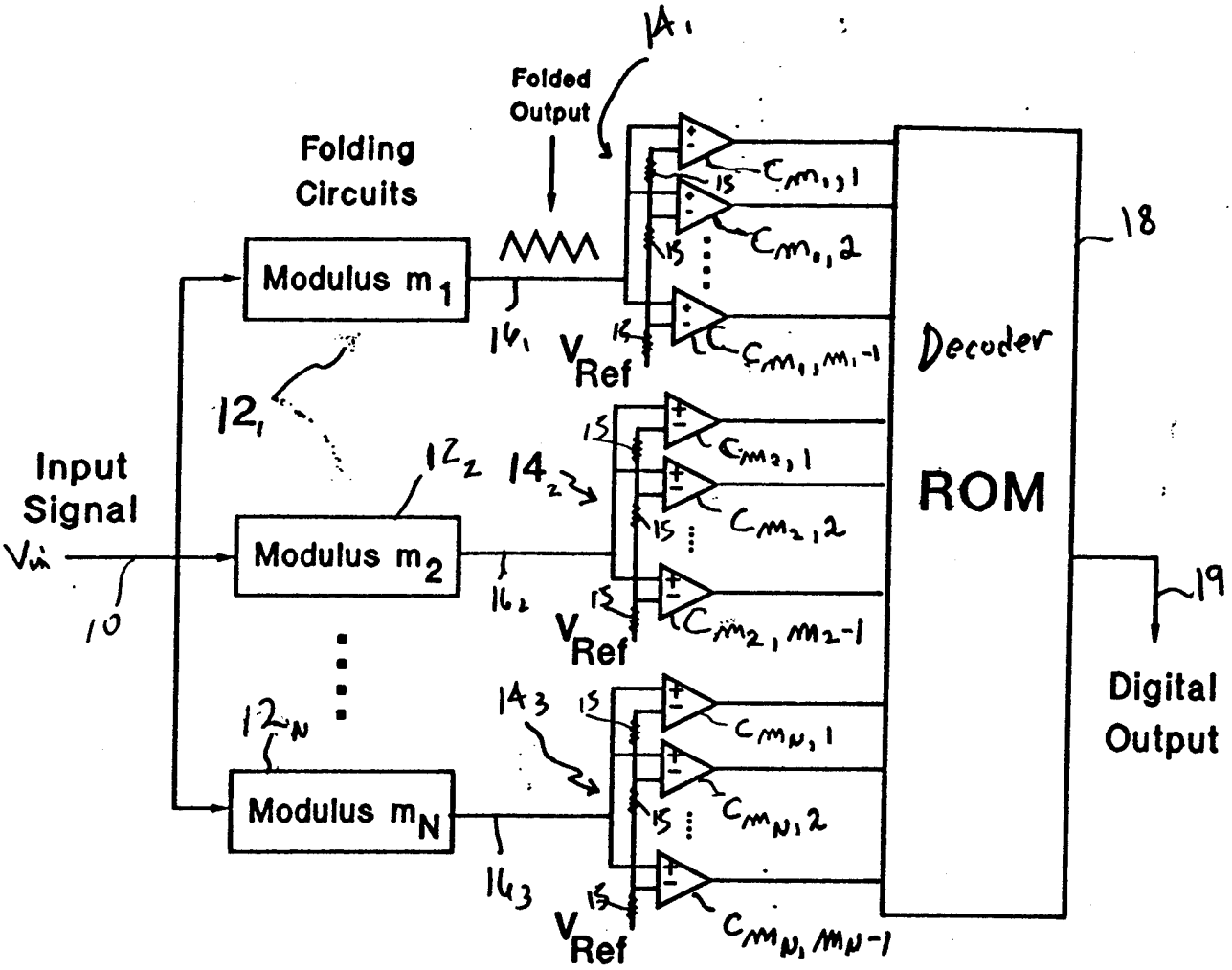
Folded Output
Folding Circuits
Modulus m_1
Modulus m_2
Modulus m_N
Input Signal
V_{in}
V_{Ref}
Decoder
ROM
Digital Output
10
12₁
12₂
12_N
14₂
14₃
16₁
16₂
16₃
18
19

Figure 2

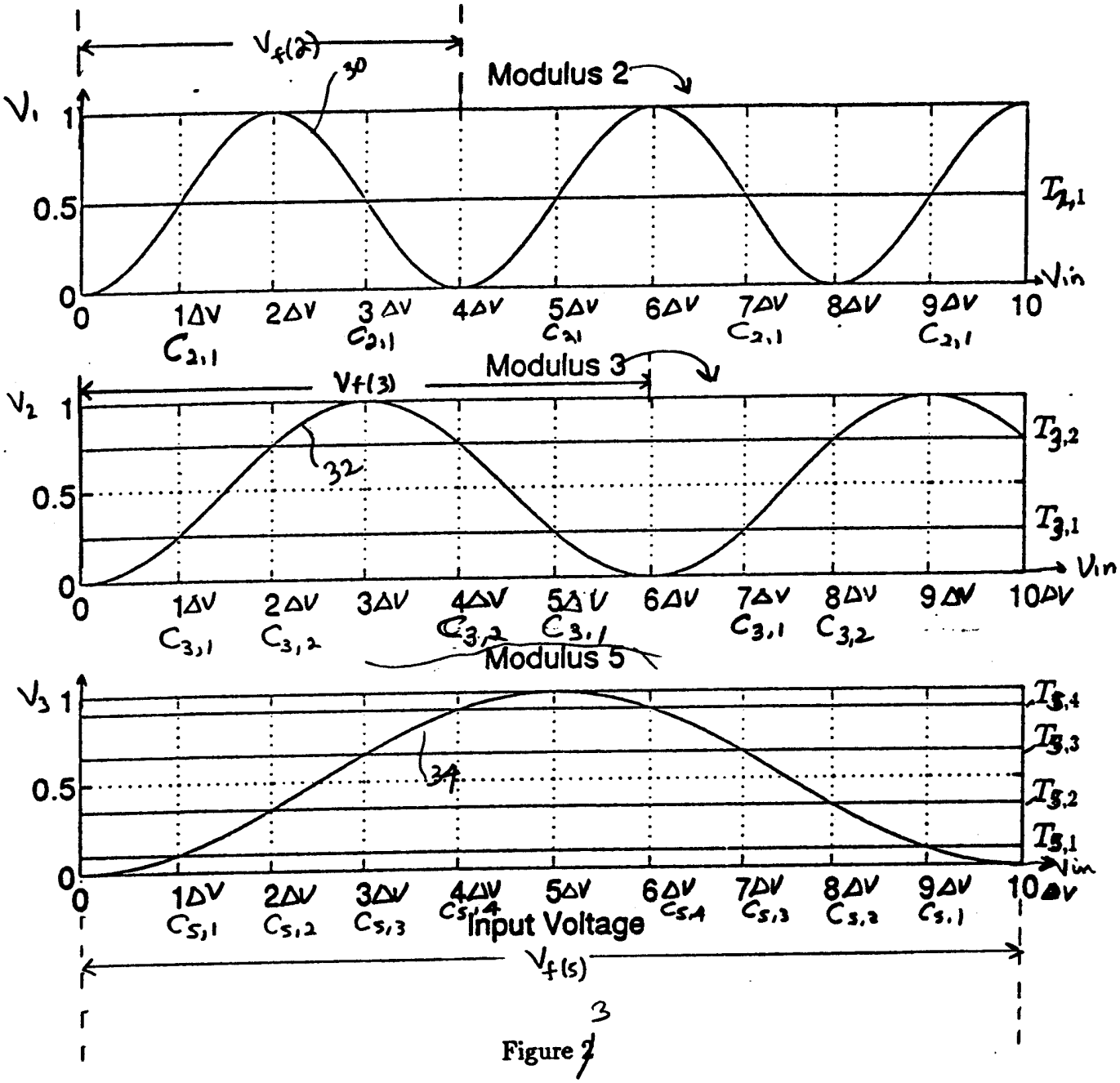
$V_{f(2)}$
30
Modulus 2
V_1
1
0.5
0
0
1ΔV
2ΔV
3ΔV
4ΔV
5ΔV
6ΔV
7ΔV
8ΔV
9ΔV
10
$C_{2,1}$
$C_{2,1}$
$C_{2,1}$
$C_{2,1}$
$C_{2,1}$
$T_{2,1}$
V_{in}
$V_{f(3)}$
Modulus 3
V_2
1
0.5
0
32
$T_{3,2}$
$T_{3,1}$
V_{in}
0
1ΔV
2ΔV
3ΔV
4ΔV
5ΔV
6ΔV
7ΔV
8ΔV
9ΔV
10ΔV
$C_{3,1}$
$C_{3,2}$
$C_{3,2}$
$C_{3,1}$
$C_{3,1}$
$C_{3,2}$
Modulus 5
V_3
1
0.5
0
34
$T_{5,4}$
$T_{5,3}$
$T_{5,2}$
$T_{5,1}$
V_{in}
0
1ΔV
2ΔV
3ΔV
4ΔV
5ΔV
6ΔV
7ΔV
8ΔV
9ΔV
10ΔV
$C_{5,1}$
$C_{5,2}$
$C_{5,3}$
$C_{5,4}$
$C_{5,4}$
$C_{5,3}$
$C_{5,2}$
$C_{5,1}$
Input Voltage
$V_{f(5)}$

Figure 3

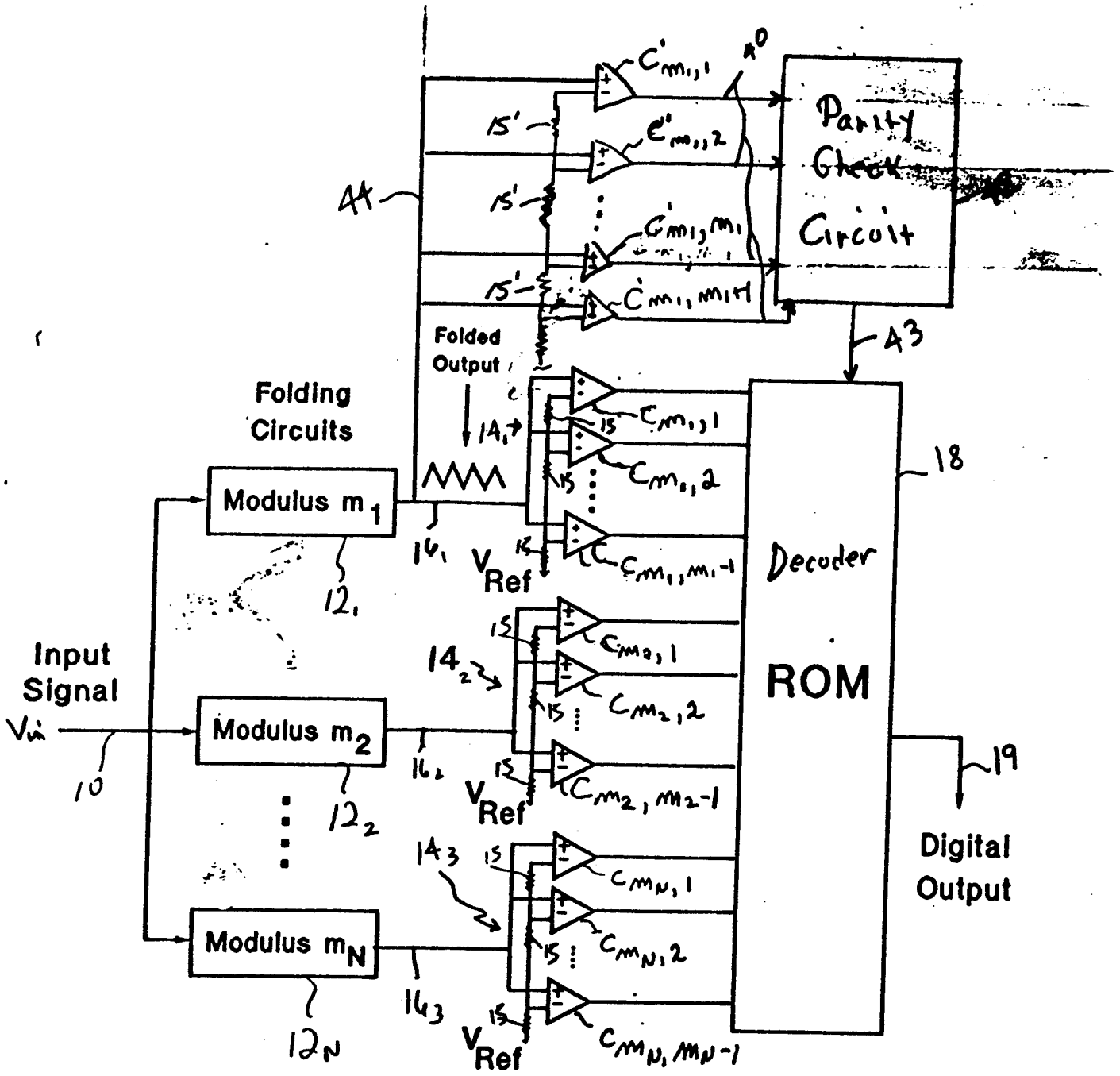
Parity Check Circuit
Folded Output
Folding Circuits
Modulus m_1
Modulus m_2
Modulus m_N
Input Signal
V_{in}
V_{Ref}
Decoder
ROM
Digital Output
$C'_{m_1,1}$
$C'_{m_1,2}$
C'_{m_1,m_1}
C'_{m_1,m_1+1}
$C_{m_1,1}$
$C_{m_1,2}$
C_{m_1,m_1-1}
$C_{m_2,1}$
$C_{m_2,2}$
C_{m_2,m_2-1}
$C_{m_N,1}$
$C_{m_N,2}$
C_{m_N,m_N-1}
10
12$_1$
12$_2$
12$_N$
14$_1$
14$_2$
14$_3$
15
15'
16$_1$
16$_2$
16$_3$
18
19
40
44
43

Figure 4

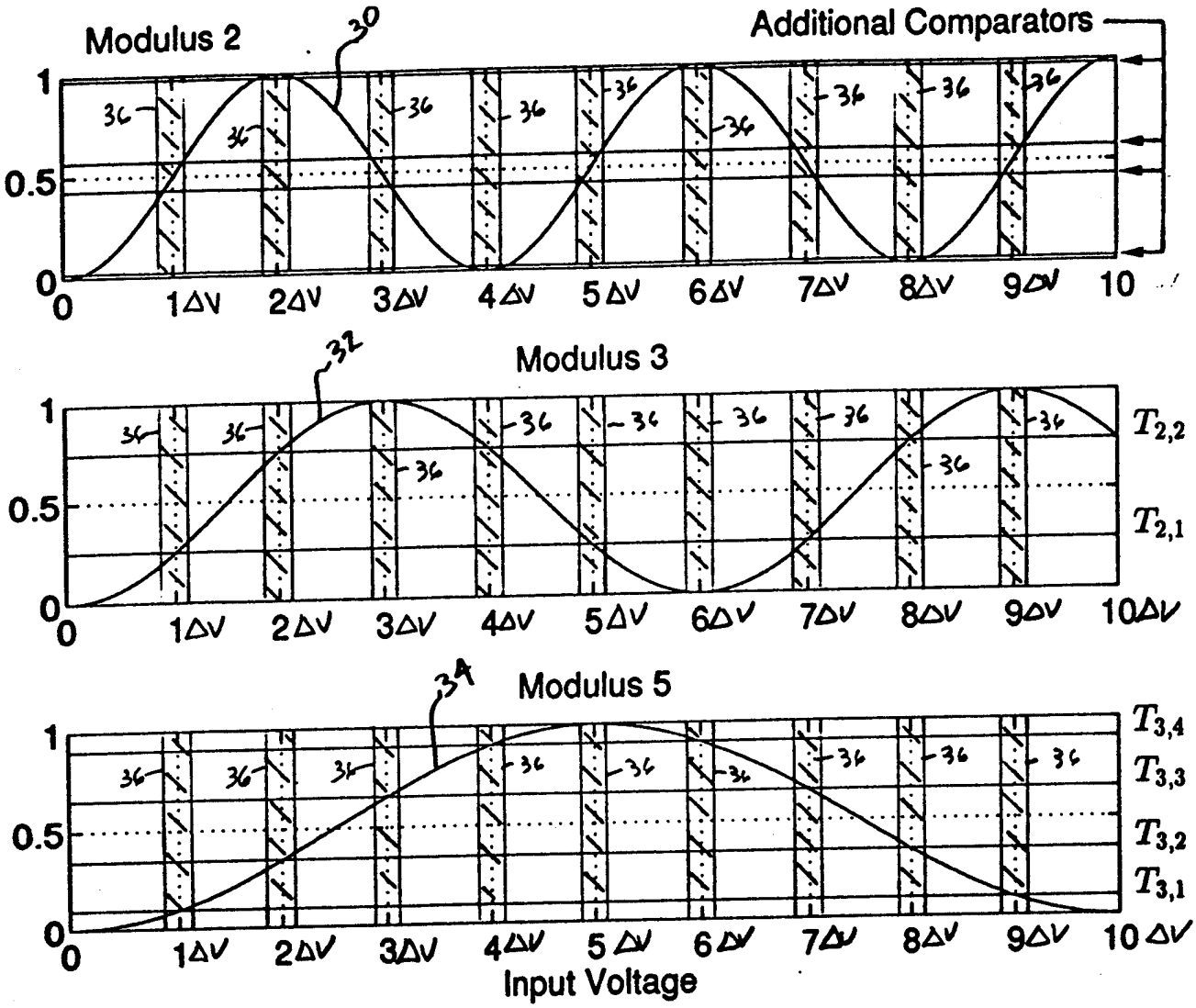
Modulus 2
30
Additional Comparators
1
0.5
0
0
1ΔV
2ΔV
3ΔV
4ΔV
5ΔV
6ΔV
7ΔV
8ΔV
9ΔV
10
36
Modulus 3
32
1
0.5
0
0
1ΔV
2ΔV
3ΔV
4ΔV
5ΔV
6ΔV
7ΔV
8ΔV
9ΔV
10ΔV
$T_{2,2}$
$T_{2,1}$
Modulus 5
34
1
0.5
0
0
1ΔV
2ΔV
3ΔV
4ΔV
5ΔV
6ΔV
7ΔV
8ΔV
9ΔV
10ΔV
$T_{3,4}$
$T_{3,3}$
$T_{3,2}$
$T_{3,1}$
Input Voltage

Figure 5