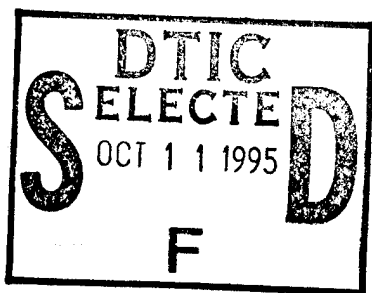


Serial No. 491,184

Filing Date 16 June 1995

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19951006 044

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ULTRA-WIDEBAND ACTIVE ELECTRONICALLY SCANNED ANTENNA

BACKGROUND OF THE INVENTION

10 Field of the Invention

This invention deals with time-delay circuits utilized for beamforming in a phased array antenna system and more particularly to a phased array antenna system utilizing switched time-delay circuits to significantly reduce the complexity of time-delay beam steering.

Description of the related Art

20 Basically, the phased-array antenna is composed of a group of individual radiators which are distributed and oriented in a linear or two-dimensional spatial configuration. The amplitude and phased excitations of each radiator can be individually controlled to form a radiated beam. The position of the beam in space is controlled electronically by adjusting the phase of the excitation signals at the individual radiators. Hence, beam scanning is accomplished with the antenna aperture remaining fixed in space without the involvement of mechanical motion in

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the scanning process. An electronically steered antenna array radar is able to track a large number of targets and illuminate some of these targets with radio-frequency energy. The antenna beamwidth may be changed electronically by means of phase spoiling to search certain areas more rapidly but with less gain. Frequency agility can be achieved through changing the frequency of transmission at will from pulse to pulse, but requires sequential phase adjustments since the beam pointing direction with phase control is narrow band and changes with frequency.

10

Phase change at the elements due to change in frequency is exploited in frequency scanned arrays, but with phased arrays it restricts the use of wide instantaneous bandwidth, which is needed to enhance radar capabilities and performance. The narrow bandwidth of phased arrays is due to phase being controlled for the antenna aperture excitation, and steered beams will scan towards broadside as the frequency is increased, and thus move off the target.

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SUMMARY OF THE INVENTION

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The object of this invention is to provide an ultra-wideband active electronically scanned antenna that utilizes compensating line lengths in cascade in an antenna branch feed line thereby providing a variable time-delay along the branch to each antenna

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element, thereby allowing smaller component structure than the prior art throughout the system.

5 The object of this invention is to enhance the performance of radar by allowing wide instantaneous bandwidth through the use of short time-delay circuitry.

Another object of this invention is to reduce the cost of radars by providing short time-delay circuits.

10

These and other objectives are obtained by utilizing an architecture utilizing simple, variable, and short time-delay circuits to significantly reduce the complexity of time-delay beam-steering. The architecture is substantially frequency independent and allows "shared apertures" concepts in both series and parallel (corporate) feed antenna arrays. The architecture may be applied to active "phased" arrays where any losses are made up by amplification on both transmit and receive.

15

20

BRIEF DESCRIPTION OF THE DRAWINGS

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Figure 1 is a schematic of the architecture for an ultra-wideband beam forming line source with a series feed having adjustable time delay modules having an odd number of antenna elements.

Figure 1a is a schematic of the architecture for an ultra-wideband beam forming line source with a series feed having adjustable time delay modules having an even number of antenna elements.

5

Figure 1b is a schematic of an adjustable time-delay module utilizing solid state components.

Figure 1c is a schematic of a transmit/receive module.

10

Figure 2 is a schematic of the architecture for an ultra-wideband beam forming line-source having adjustable time-delay modules with two-way amplification in the branch lines at one or more locations.

15

Figure 3 is a schematic of a series feed combiner network utilizing subarrays and having adjustable time-delays.

Figure 4 is a schematic of an ultra-wideband corporate feed architecture having adjustable time-delays.

20

Figure 5 is a plot of the figure of merit (FOM) versus the number of elements (N) of an ultra-wideband linear array.

25

DESCRIPTION OF THE PREFERRED EMBODIMENT

In the preferred embodiment 10, referring to Figure 1, ultra-wideband beamforming with a series feed in its simplest form is shown that is comprised of a plurality of time delay
5 circuits 18 having a means for switching in time delays from 0 to $2d/c$, where d is the inter-element spacing and c is the velocity of light. At the highest frequency the elements are spaced by $\lambda/2$ to avoid grating lobes and the delay corresponds to 360° of
10 phaseshift, as with a normal phaseshifter.

In the series feed, an electromagnetic signal is coupled at uniform intervals along the antenna feed line to radiating elements, 12 equally spaced along the aperture. For frequency
15 independent steering of the beam, the electrical pathlengths from the electromagnetic signal source 14 to each radiating element 12 to the desired equi-phasefront 16 must be the same. This is accomplished by the insertion of an adjustable time-delay circuit 18 into the antenna feedline at each element 12.

20 An electromagnetic signal generated by an electromagnetic signal source 14, such as a radar or microwave transmitter, passes through a signal splitter 22 which divides the electromagnetic signal into a plurality of electromagnetic
25 signals which are applied to the antenna elements 12 through a

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plurality of signal branches 24, 26, and 28. For an antenna array having an odd number of branches, at minimum there are three branches, a center or central branch 24, a right branch, and a left branch, 26 and 28, respectively. The center, or
5 central, branch 24 is without variable time-delay, having only a bias delay 32 of a preselected amount. Its feed length is the same as that of the other branches 26 and 28 with delay adjusted to d/c .

Dependent upon the operational frequency and power of the system,
10 these branch and element feedlines may be either waveguides, coaxial cable, or microstrip.

The time-delay circuits 18 are reciprocal so that one setting applies equally for transmitting and receiving. When the
15 time-delays are set half way, i.e., to d/c , then the various lines feeding the radiating elements 12 at the aperture have bias delays of predetermined amounts making them all equal; that setting will therefore give a broadside beam, independent of the frequency. The bias delay 32 is about $a/2c$ at the center of the
20 array, where a is the aperture size, and reduces to zero at the edge.

To scan the beam, each one of the time-delay circuits 18 in the branch 26 is ideally set to the same value $(d/c) + (d/c) \sin$
25 θ_1 , where θ_1 is the scan angle, and similarly, all the time delay

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circuits 18 in branch 28 elements are set to $(d/c) - (d/c) \sin \theta_1$, all independent of frequency. This gives both frequency independent scanning and also makes for a very simple scanning calculation with only two drivers necessary if they can handle
5 the power. Under the above conditions, the smallest change in beampointing direction is obtained by changing each one of the switchable time-delays 18 by the smallest bit. With N radiating elements 12 and n bits of time-delay, the minimal change in beampointing direction is $N/2^n$ scanned beamwidths at the highest
10 frequency. For example, when $N=64$ and $n=6$, the minimal step change in beam position is one beamwidth. Fine steering (and correction for construction errors) could be added with an additional switched time delay 18 at each module.

15 Branch time delays may be set individually and thereby forego the granular rough-plus-fine steering method discussed above. Each of the branch time-delays is set to give the closest correct value for that station, as can be achieved with the available number of bits. The most central branch 24 delay
20 circuit is set first, followed sequentially by the more outward circuits, taking into account all previous delay contributions as well as correction data from previous calibration.

Switchable time-delay of 0 to $2d/c$, with $d=\lambda/2$ at the
25 highest frequency, gives some excess in available delay, since

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this value allows scanning to $\pm 90^\circ$. Holding scanning to, for example, $\pm 60^\circ$ requires only $\sin 60^\circ = 0.866$ times that delay. Additional excess time-delay, if needed, for example, for the correction of construction errors, can be obtained by increasing
5 the time-delay circuit range from a maximum of $2d/c$ to perhaps $2.2d/c$.

For an antenna array having an even number of elements, there are two branches in the center of the array, as shown in
10 Figure 1a, one on each side of the center line and spaced $d/2$ from the center line. The switchable time-delay for those two branches 24a and 24b would have to be one half of that of the others, i.e., $1/2 d/c \pm 1/2 d/c \sin \theta_0$. The time-delays of these branches, with bias 32, and a setting of $1/4 d/c$ is the same as
15 that of the other elements with their delay adjusted to d/c .

The insertion loss for the time delay circuits is expressed in dB and is approximately proportional to the number of bits used. The total loss at the end-element is

$$L = nL_b \frac{N}{2} \text{dB} \quad (1)$$

20 where $N/2$ is the number of radiating elements 12 fed by one branch (the aperture has N or $N+1$ elements where N is an even number), n is the number of bits in each switchable branch time-delay circuit, and L_b is the loss per bit in dB. With practical

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losses per bit and the large number of bits required for low
sidelobes, this loss quickly becomes prohibitive for large
antennas. For example, if it is assumed a loss per bit of $L_b =$
0.2 dB, $n = 6$, and $N = 64$, then the maximum insertion loss at the
5 edge element is $L = 38.4$ dB. This is not acceptable, even in
view of a desirable receiver illumination edge taper.

A significant reduction in insertion loss may be obtained by
adding solid-state amplifier modules 36, Figure 1c, to each
10 branch 26, and 28, as in the series feed embodiment depicted in
40, Figure 2. The design and construction of the solid-state
amplifier module 36 is well known to those skilled in the art.

Also, the insertion loss may be reduced by dividing the
15 arrays into subarrays 54, each in the form of the preferred
embodiment as shown in Figure 1. The subarrays, as shown in
Figure 3, are then combined by a further, similar, series feed
combiner network 50. This method will give frequency independent
beam steering but at the cost of an increase in the number of
20 time-delay circuits 18. The total insertion loss to the last
antenna element in this case is

$$L_t = \left(\frac{N_s}{2}\right) nL_b + \left(\frac{M}{2}\right) n_c L_b \text{ dB} \quad (2)$$

subarray combiner

where M is the number of subarrays, N_s is the number of elements

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per subarray, n_c is the number of bits in the combining branch delay, n is the number of bits in the subarray delay, and L_s is the loss per bit in dB. This gives an improvement factor to the loss in dB of

$$\left(\frac{L}{L_s}\right) = \frac{N}{N_s + \frac{Mn_c}{n}} \quad (3)$$

5 where $N = N_s \times M$. Using the above example of $N = 64$, but with $M=8$ subarrays, each with $N_s=8$ elements, and with $n=6$ and $n_c=9$ (maximum time-delay increased from $(2d/c)$ to $(8 \times 2d/c)$), this subarray architecture gives an improvement factor $L/L_s = 3.2$ or a total insertion loss of 12 dB, which generally is considered
10 acceptable in such cases.

Another preferred embodiment, shown in Figure 4, is an active corporate, or parallel, feed architecture 60 with switchable time-delay-line circuits 18. In a parallel feed the
15 electromagnetic energy is fed in parallel to a set of delay lines, i.e., 18, each systematically shorter than the prior one. In comparison with the series architecture, shown above in Figure 1, a parallel feed architecture 60 requires longer switchable, or variable, delay-lines. The maximum time-delay required is
20 $(Nd/2c) = a/2c$, where a is the aperture size, c is the velocity of light, and N is the number of radiating elements. However, there is less insertion loss since only m time-delays are in

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series where $2^n = N$. The loss is sufficiently small so that it can be compensated by amplification in the solid state modules. For the corporate feed configurations, there is no need for bias time-delay circuits.

5

For a two-dimensional array many linear array feed networks could be stacked, say in the vertical plane and combined by one further such network. Monopulse can be added readily with a second vertical combiner and horizontal monopulse outputs.

10 Optimization monopulse outputs with low sidelobes in both sum and difference channels is possible, but requires additional complexity.

A combination of series (Figure 1) and corporate (Figure 4) architecture 10 and 60, respectively, is possible in a variety of ways, with different parts of the dividing network using different configurations. Further, the binary divisions of the corporate architecture 60 may be replaced by any multiple division network. Time-delay architecture may also be combined
20 with phase controlled subarrays. This would limit the bandwidth to that of the subarrays.

It is further possible to end-feed the array but that may lead to an asymmetric amplitude taper due to cumulative insertion
25 losses that would require compensation.

In all embodiments, the amount of switchable time-delays may be increased to allow an excess for error correction.

A figure of merit (FOM) can be derived to assess the total provided switched time-delay of a system. It is given by the

ratio

$$\text{FOM} = \frac{\text{Total switched time-delay for conventional feed system}}{\text{Total switched time-delay for proposed feed system}} \quad (4)$$

The total switched time-delay is the sum of the maximum values of all switchable time-delay networks used. The conventional system is a configuration where each radiating element has its own unique switchable time-delay. They vary from a/c at the edge to zero at the center, giving a total time delay of $Na/2c$. FOMs for the various configurations are shown in Table 1, and are plotted in Figure 5. Table 1 shows the switchable time-delay for different architectures when compared with a conventional system as known in the art. A larger FOM indicates improvement, i.e., smaller total time delay required by the system.

The ultra-wide-bandwidth active phased array architecture, described above, makes use of simple, variable, and short time-delay circuits, as previously stated, substantially no different from the standard diode phaseshifters, but makes multiple use of the same device. The architecture is substantially frequency independent and thus allows some "shared

TABLE 1. COMPARISON OF DIFFERENT ARCHITECTURES

Ultra-Wideband Architecture	Total Switchable Time Delay	
Conventional	$Na/2c$	1
Series feed, Figure 1	$2a/c$	$N/4$
Series-subarrays, Figure 3	$4a/c$	$N/8$
Corporate feed, Figure 4	$(a \log N)/(c \log 2)$	$0.15N/\log N$

apertures" concepts. It may be applied to passive "phased" arrays although the losses for that application may be prohibitive. It can be applied to active "phased" arrays where losses can be made up by amplification on both transmit and receive.

For wide instantaneous bandwidth performance, in the conventional design of the prior art, long-time delay circuits have to be added, either with sub-arrays, or for ultra-wide-bandwidth, with one circuit per antenna element. This adds greatly to the complexity and cost of the antenna. Compromises are possible where the array is broken into subarrays with phase shifters. This results in fewer switched time-delay circuits but there is a corresponding limitation in bandwidth which is reduced to that of a subarray.

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The preferred embodiments described above makes multiple use of switched time-delay circuits and thereby significantly reduce the total complexity of the system now practiced by the art. The teachings of the preferred embodiments make multiple use of
5 switched time-delays and are applicable, preferably, to active arrays, where the losses are compensated by amplification of both transmitter and receiver signals, however, as stated above, such amplification may be added to other types of systems to make utilization of the preferred embodiments feasible.

10

The ultra-wideband architectures for switchable time-delay beamsteering of an antenna array are akin to the use of tapped delay lines as described in Radar Handbook 11-1 through 11-71 and 13-10, (Skolnick ed. 1970), which is hereby incorporated by
15 reference. The same switched time-delay circuits are used for a multiplicity of antenna elements, and thereby greatly simplify wideband array scanning in comparison to conventional methods where switchable long time-delay circuits are used at each radiating element. Series feed networks are the simplest, but
20 with large arrays high insertion losses have been shown. The effect of this loss is reduced by adding amplification. Series feeds with subarrays and corporate feed systems, by comparison, have shown a much smaller insertion loss. However, their total switchable time-delays are greater than with the series
25 configuration, but still much smaller than with the conventional

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system now utilized in the art.

5 Although the invention has been described in relation to
exemplary embodiments thereof, it will be understood by those
skilled in the art that still other variations and modifications
can be affected in these preferred embodiments without detracting
from the scope and spirit of the invention.

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ABSTRACT

The architecture of this invention makes multiple use of switched time-delay circuits to reduce the complexity of both series and parallel feed antenna arrays. Each time-delay circuit can give a delay that can be switched to values between 0 and $2d/c$, where d is the inter-element spacing and c is the velocity of light. At the highest frequency of the series feed array, the elements are spaced by $\lambda/2$ to avoid grating lobes and the maximum delay corresponds to 360° of phaseshift. When the time-delays are set half way (d/c), the various lines feeding the elements of the array at the aperture have bias delays that make them all equal in length, thereby giving a broadside beam, independent of frequency. At the highest frequency, the switchable time delay gives some excess in available delay. If additional excess time-delay is needed it can be obtained by increasing the time delay circuit range. Insertion loss is proportional to the number of bits used. This could become high in large antennas, however, this loss may be compensated by the addition of two-way amplification in the branch lines with an appropriate bias length adjustment. Also the insertion loss may be reduced by dividing the array into subarrays which are then combined by a series feed combiner network. In parallel feed architecture, fewer time delay circuits are in series as compared to the series feed architecture. Therefore, there is less insertion loss and the

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loss is sufficiently small that it can be compensated for by
amplification in the solid state modules.

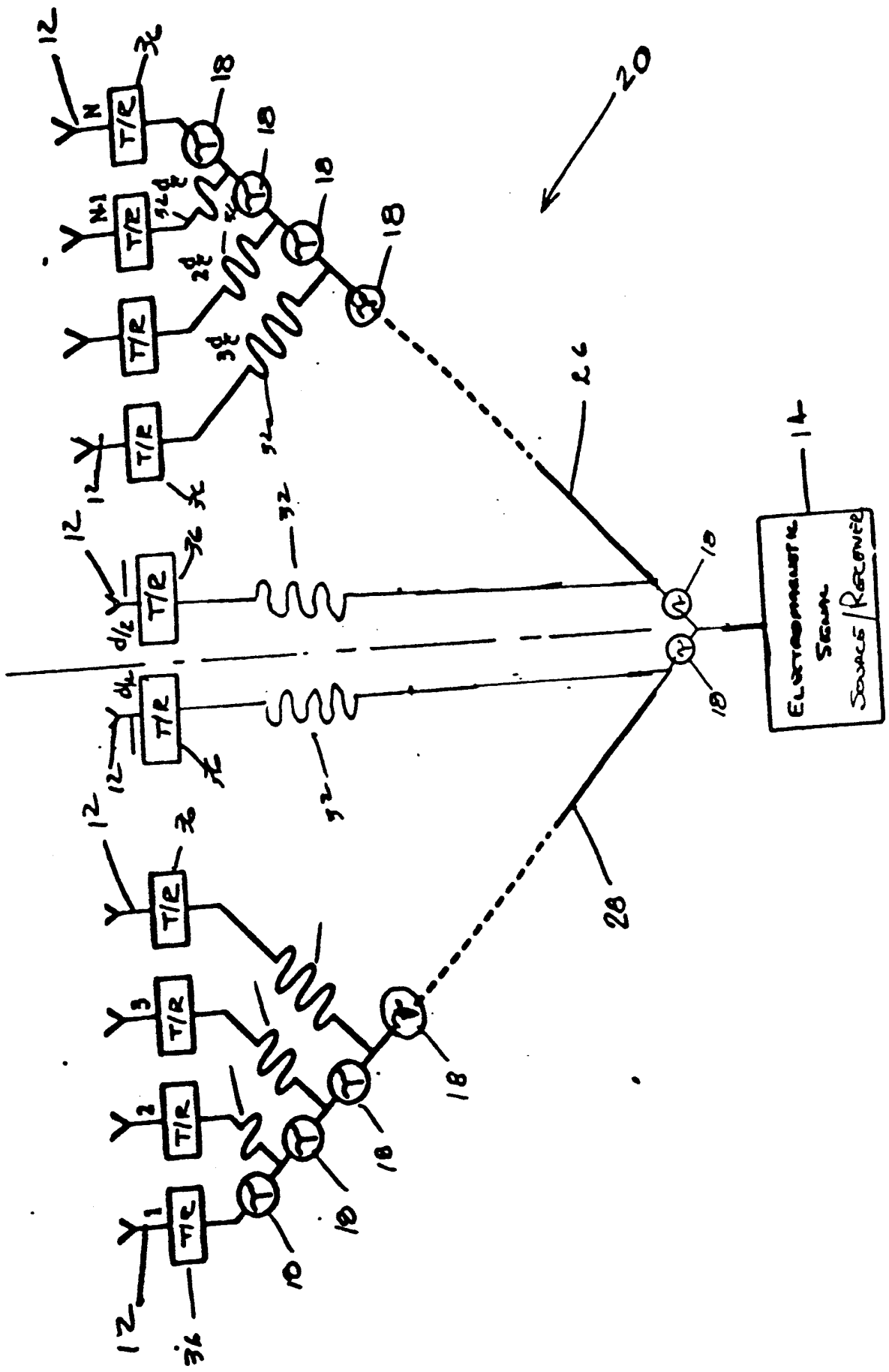
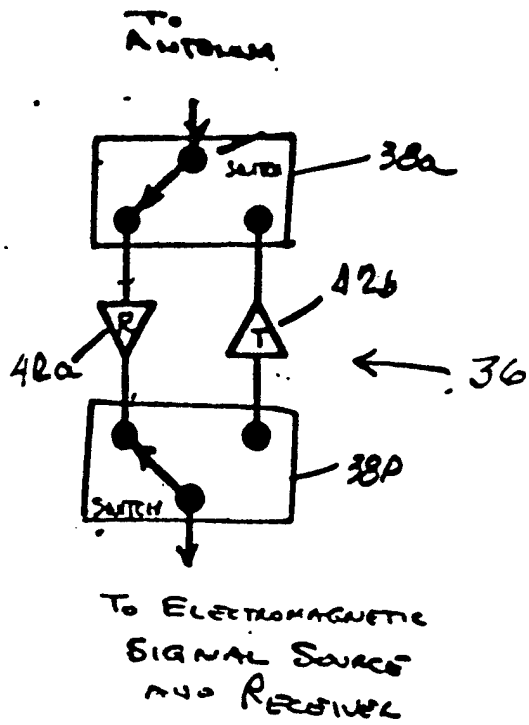


Fig. 10



TIR AMPLIFYING
MODULE

FIG 1(c)

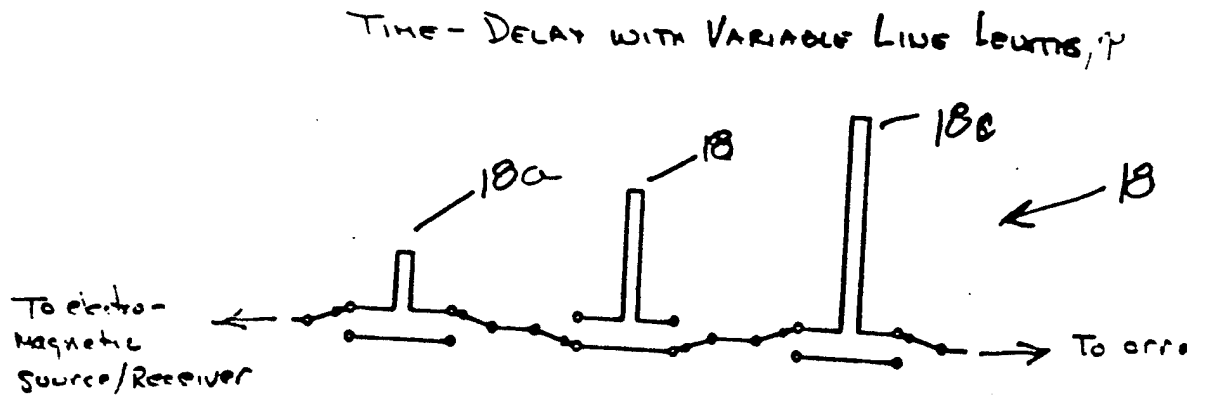


FIG
1(b)

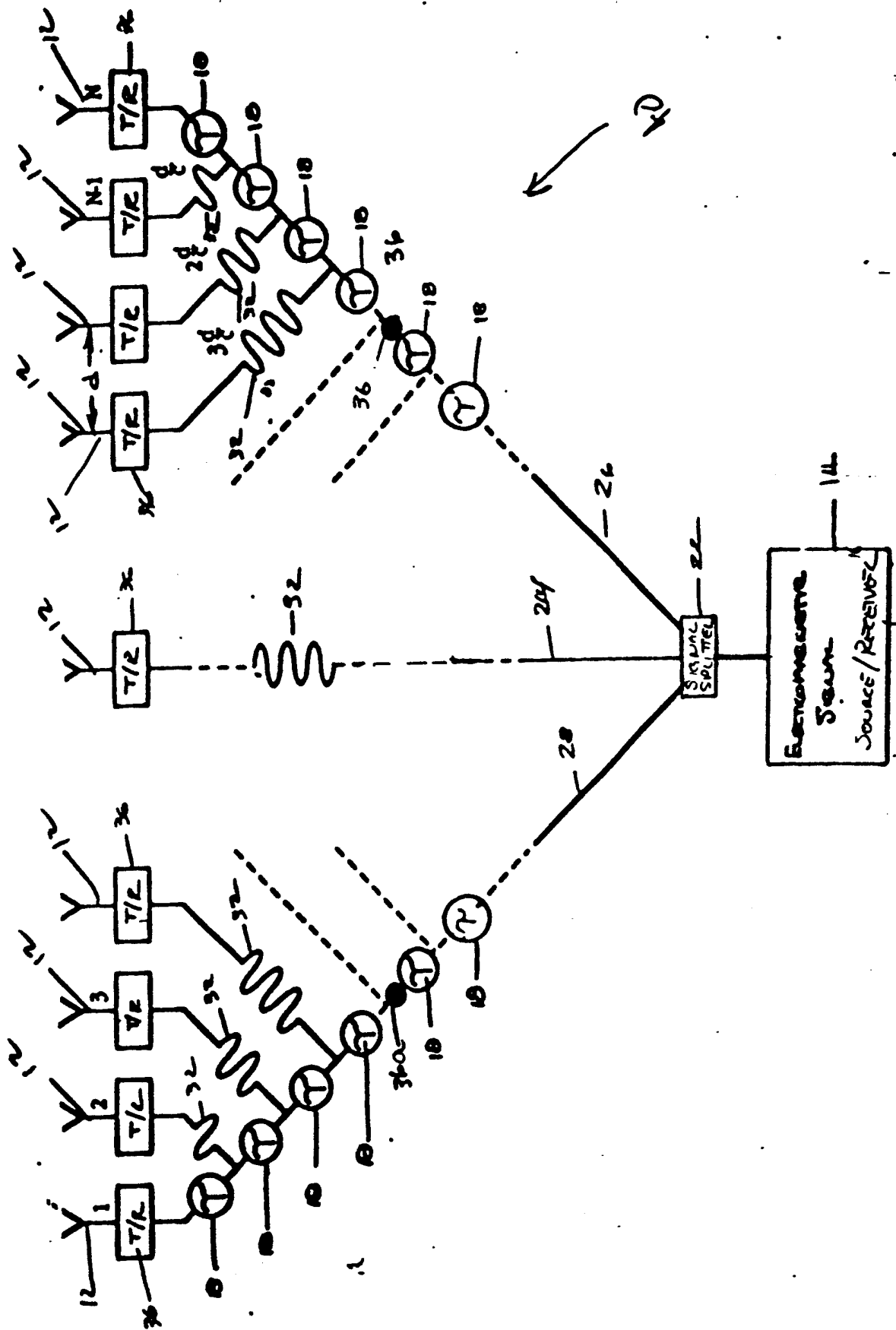


FIG. 2

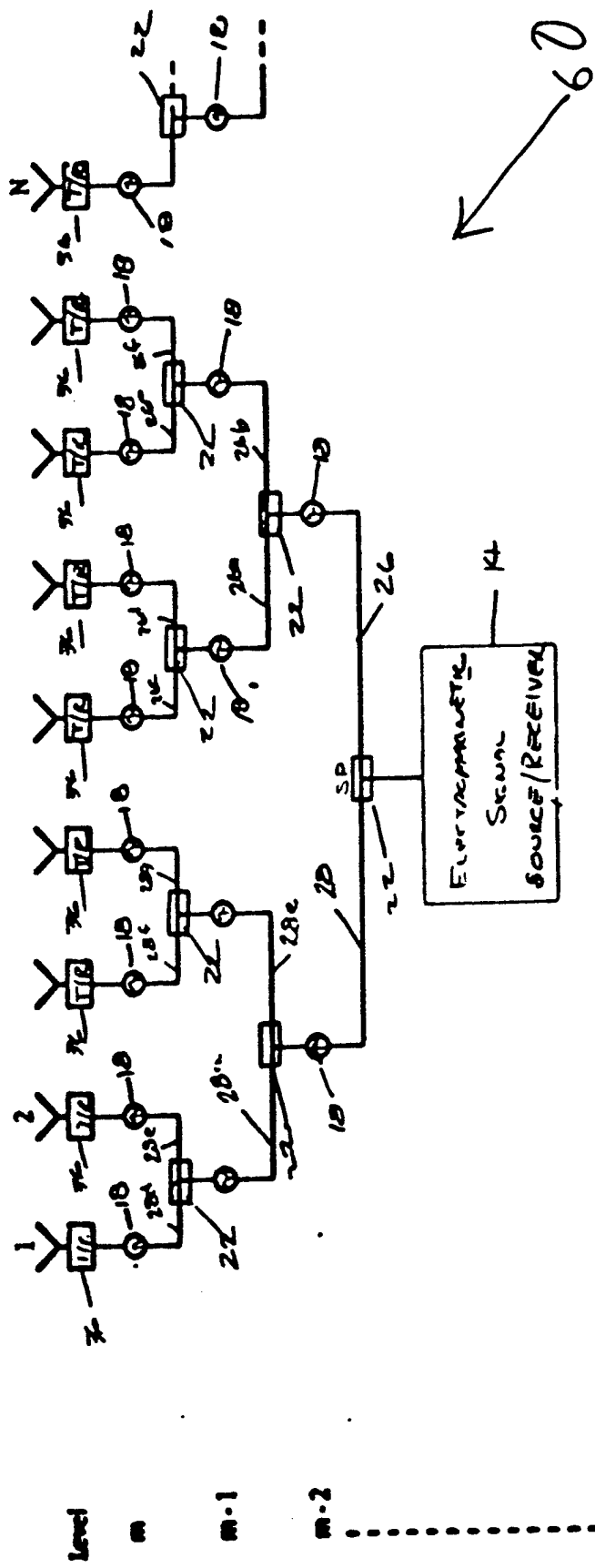


FIG. 4

N = 2^m

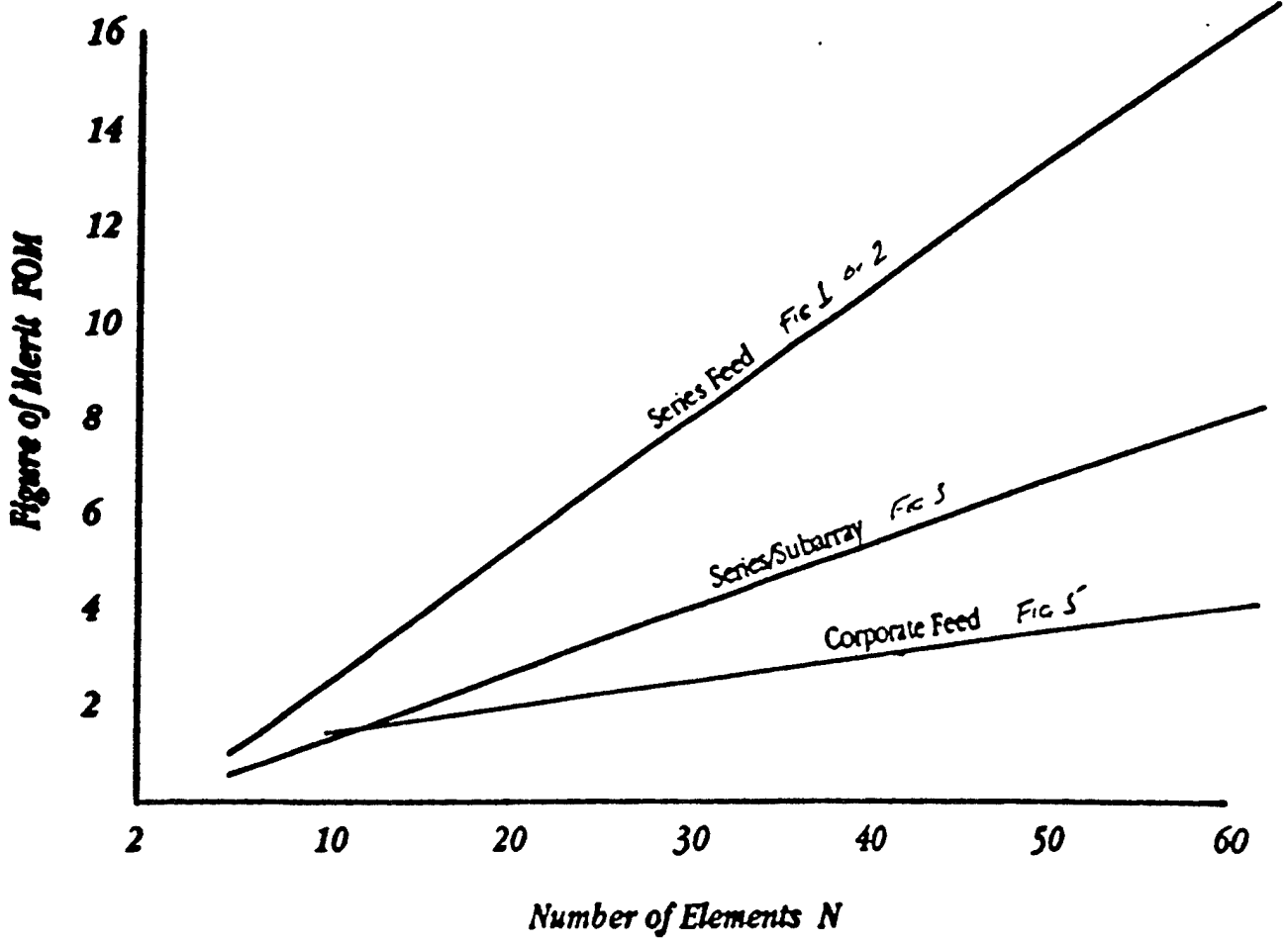


Fig. 5