Serial Number 656,494

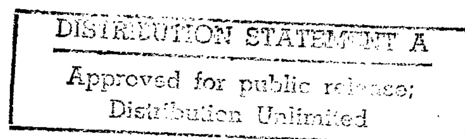
Filing Date 31 May 1996

Inventor Todd R. Weatherford
Dale McMorrow
Walter Curtice

NOTICE

The above identified patent application is available for licensing. Requests for information should be addressed to:

OFFICE OF NAVAL RESEARCH
DEPARTMENT OF THE NAVY
CODE OOCC
ARLINGTON VA 22217-5660



DTIC QUALITY INSPECTED 4

19980602 020

1

2

3 INTEGRATED CIRCUITS WITH IMMUNITY TO SINGLE EVENT EFFECTS

4

5 BACKGROUND OF THE INVENTION

6

7 Field of the Invention

8 The present invention relates to mitigating or eliminating single event effects in integrated
9 circuits that would otherwise be susceptible to single event effects. More particularly, the present
10 invention relates to decreasing the free carrier lifetime of electrons and holes that would otherwise
11 contribute to single event effects, through the use of a buffer layer.

12

13 Description of the Related Art

14 Three major types of radiation-induced effects are generally recognized as potential
15 interferents with integrated circuits: total dose effects, transient effects, and soft errors (a.k.a.
16 single event effects). Some other effects, e.g. neutron damage, are recognized by some
17 practitioners.

18 Total dose effects are related to the permanent failure of an entire integrated circuit caused
19 by an accumulation of radiation, e.g., x- or γ-rays. Such exposure can cause permanent threshold
20 voltage shifts in integrated circuits that are not hardened against total dose radiation. As the
21 name suggests, total dose radiation effects are related to the entire exposure history of integrated

1 circuits--when the total dose exceeds some threshold value, circuit failure is observed. GaAs
2 technology is inherently less susceptible to total dose effects than other technologies.

3 Transient effects are likewise caused by the exposure of an entire integrated circuit to a
4 flood of radiation, typically x- or γ-rays. However, these are typically related to a short burst
5 (10-20 ns) of high intensity radiation, such as that emitted by a nuclear detonation. Such expo-
6 sure can cause temporary, and in some case permanent, failure in integrated circuits that are not
7 hardened against transient effect radiation.

8 Single event effects are a distinct phenomenon from total dose and transient effects. *See*
9 *generally* Sherra E. Kerns, *Transient-Ionization and Single-Event Phenomena, in* IONIZING
10 RADIATION EFFECTS IN MOS DEVICES AND CIRCUITS 485-91 (John Wiley & Sons, Inc., T.P. Ma
11 et al. eds., 1989). Unlike total dose effects and transient effects, single event effects are localized
12 to a particular region of an integrated circuit. Single event effects occur when a particle (such
13 as a cosmic ray, proton, or neutron) changes the state of a particular device in an integrated
14 circuit, thereby causing an error.

15 Single event effects that take place in memory chips are referred to as single event upsets.
16 These occur when an element in a memory chip has its state changed (i.e., from a 1 to a 0 or
17 from a 0 to a 1) by the action of a high energy particle interacting with the chip. In memory
18 chips, the frequency of single event upsets will depend principally on the use environment and
19 on the configuration of the memory chip. Single event effects also will occur in other logic
20 chips, e.g., microprocessors. In these chips, the frequency of single event effects will depend on
21 the clock speed of the device, as well as on the use environment and configuration of the device.

1 This clock speed dependence arises from the fact that at higher clock speeds, the fraction of time
2 that a particular logic gate spends in transition from one state to another increases. Edge-
3 triggered devices are susceptible to soft errors in the transition region. Consequently, the larger
4 fraction of time high-speed devices spend in the transition region increases the window of
5 susceptibility to soft errors. The technological trend for the past several years has been toward
6 edge-triggered circuits and away from comparative level-triggered circuits.

7 A number of factors can contribute to the frequency of single event effects in a device.
8 The factor that has been most well documented to date is the use environment of the device.
9 Electronic devices used in outer space, for instance, are bombarded with cosmic rays and protons
10 that will induce soft errors in unhardened ICs. To date, the only effective methods for hardening
11 these circuits against cosmic rays and protons have been shielding, redundancy, and error
12 detection and correction (EDAC).

13 Likewise, neutrons, alpha particles, and other high energy particles will induce single
14 event effects in devices that are used in environments that have high concentrations of these
15 particles. It would be desirable, for example, to operate satellites within the Van Allen belts.
16 However, this is currently impossible without the use of shielding, redundancy, and/or EDAC,
17 due to the high particle concentrations within the Van Allen belts.

18 Even at elevations within the atmosphere, e.g. at elevations of 20,000 to 50,000 feet,
19 single event effects can create electronic errors. It has been established that single event effects
20 can interfere with airborne electronics.

1 Even at sea level, the concentration of single event-inducing particles is nonzero. To date,
2 this has not been a major concern because single event effects are uncommon at sea level. This
3 is due to the still relatively slow clock speeds and large device sizes in the digital electronics in
4 use today. However, high-speed supercomputers and other cutting edge technologies may already
5 be experiencing some errors that may be associated with single events. As typical clock speeds
6 increase, past 250 MHz, to 500 MHz, 1 GHz, 2 GHz, and beyond, the occurrence of single event
7 effects will increase proportionately. Aggravating this increase in clock speeds is the decreasing
8 size of the transistors in ICs. A smaller device generally has a smaller capacitance, and
9 accordingly will require a smaller charge to cause the device to change its state. Thus, it can be
10 predicted that, for example, a GaAs IC (FET technology) with a clock speed of 1 GHz, with a
11 device density of 10^6 transistors, will have an unacceptably high error rate, on the order of about
12 1-10 errors/day at sea level under normal conditions or about 10-1000 errors/day at sea level
13 during solar events.

14 It is also desired to improve the isolation of devices in ICs, reducing leakage currents.

15

16 Calawa et al., U.S. Patent No. 4,952,527, teaches the use of 2.0 μm buffer layers of low-
17 temperature grown GaAs under III-V semiconductor microwave devices, to improve their back-
18 gating effects and their resistivity, and also to improve their hardness against transient radiation.

19

1 SUMMARY OF THE INVENTION

2 Accordingly, it is an object of this invention to provide digital ICs that have improved
3 resistance to single event effects, by several orders of magnitude.

4 It is a further object of this invention to provide such resistance without the need for
5 additional shielding or redundancy.

6 It is a further object of this invention to provide such resistance in ICs that are of at least
7 MSI, LSI, or VLSI complexity.

8 It is a further object of this invention to provide such resistance in ICs that have high
9 clock speeds.

10 It is a further object of this invention to provide improved isolation of devices in ICs.

11 These and additional objects of the invention are accomplished by the structures and
12 processes hereinafter described.

13 The present invention is an electronic device having a buffer layer characterized by short
14 carrier lifetimes within the buffer layer, this buffer layer being at least about 1000 Å thick and
15 having an upper face, and an integrated circuit disposed over the upper face of the buffer layer,
16 where this integrated circuit would otherwise be susceptible to soft errors, due to its configura-
17 tion, its clock speed, its use environment, or a combination of these factors. As used herein,
18 "over", "under", "upper", "lower" and the like are used as relative terms for convenience only,
19 and do not require or imply any particular orientation with respect to gravitational fields.

20

1 BRIEF DESCRIPTION OF THE DRAWINGS

2 A more complete appreciation of the invention will be obtained readily by reference to
3 the following Description of the Preferred Embodiments and the accompanying drawings in which
4 like numerals in different figures represent the same structures or elements, wherein:

5 FIG. 1 shows the cross-section of a device of the prior art.

6 FIG. 2 shows the cross-section of an exemplary device according to the present invention.

7 FIG. 3 shows the computer simulation results of charge collection transients on a drain
8 electrode for both a conventional device and a device according to the present invention.

9 FIG. 4. shows the cross-section of a test device.

10 FIG. 5 shows the laser-induced charge collection transients measured for conventional and
11 LT GaAs HIGFETs.

12 FIG. 6 shows the 3 MeV ion-induced charge collection transients measured for n-channel
13 conventional and LT GaAs HIGFETs.

14 FIG. 7 shows the time-integrated drain charge collection measurements for conventional
15 and LT GaAs HIGFETs as a function of the laser pulse energy.

16

17 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

18 T.R. Weatherford et al., "Significant reduction in the soft error susceptibility of GaAs
19 field-effect transistors with a low-temperature grown GaAs buffer layer", *Appl. Phys. Lett.* 67(5)
20 703-05 (July 31, 1995), is incorporated by reference herein, in its entirety, for all purposes.

1 P.W. Marshall et al., "Heavy Ion SEU Immunity of a GaAs Complementary HIGFET
2 Circuit Fabricated on a Low Temperature Grown Buffer Layer", *IEEE Transactions on Nuclear*
3 *Sci.* 42(6) 1850-55 (December 1995), is incorporated by reference herein, in its entirety, for all
4 purposes.

5 D. McMorrow et al., "Elimination of Charge-Enhancement Effects in GaAs FETs with
6 a Low-Temperature Grown GaAs Buffer Layer", *IEEE Transactions on Nuclear Sci.* 42(6) 1837-
7 43 (December 1995), is incorporated by reference herein, in its entirety, for all purposes.

8 Single event upsets are governed by the relationship:

9 $$Q = cV \quad (1)$$

10 where Q is charge that interacts with the IC, c is capacitance, and V is voltage. For a device
11 with capacitance c and a threshold voltage of V (the voltage difference between the 0 state and
12 the 1 state), a charge buildup Q will cause the device to change states. If some or all of this Q
13 comes from incident high-energy particles, soft errors can be the result.

14 Referring to FIG. 1, the device **10** shown is a typical electronic structure that will be
15 referred to for illustration purposes. In this device, a transistor **12**, comprising a source **14**, gate
16 **16**, drain **18**, two n^--doped regions **20**, an n-doped region **22**, and a p^--doped region **24**, is
17 disposed over a GaAs semi-insulating layer **26** and a substrate **28**. As shown by the arrow, a
18 high-energy particle will penetrate into this GaAs layer, and will interact with this layer to
19 produce a high density of electron-hole pairs. Carriers produced by this interaction will be able
20 to migrate towards the transistor in the structure, where they may cause soft errors in the

1 structure. Charge collected at the transistor terminals will corrupt data in the IC, initiating soft
2 errors in the logic.

3 In contrast, FIG. 2 shows an exemplary device **30** according to the present invention. In
4 this device **30**, a transistor **12**, comprising a source **14**, gate **16**, drain **18**, two n^+-doped regions
5 **20**, an n-doped region **22**, and a p^--doped region **24**, is disposed over a buffer layer having a
6 short average carrier lifetime **36**, and a substrate **28**. An optional diffusion barrier **38** may be
7 disposed between the transistor **12** and the buffer layer **36**, and between the buffer layer **36** and
8 the substrate **28**. Optionally, one or more secondary buffer layers **37** may be disposed between
9 the buffer layer **36** and the transistor **12**, to facilitate growth.

10 The buffer layers **36** used in the structures of the invention will have average carrier
11 lifetimes of less than 100 picoseconds. Preferably, these buffer layers **36** will have average
12 carrier lifetimes of less than about 50 ps. More preferably, these buffer layers **36** will have
13 average carrier lifetimes of less than about 10 ps. Even more preferably, these buffer layers **36**
14 will have average carrier lifetimes of less than about 1 ps. Most preferably, these buffer layers
15 **36** will have average carrier lifetimes of less than about 500 femtoseconds.

16 As shown by the arrow, a high-energy particle will penetrate into this buffer layer, and
17 will interact with this layer to produce conduction band electron-hole pairs. However, if the
18 thickness and carrier lifetime of this buffer layer are chosen appropriately, carriers will tend to
19 recombine before soft errors occur. Buffer layers according to the invention may intrinsically
20 possess short carrier lifetimes (i.e., in their as-grown-and-annealed state), or may be modified to

1 increase the density of recombination centers (to shorten carrier lifetimes), e.g., through radiation
2 damage or through ion implantation.

3 Buffer layer materials with intrinsically short carrier lifetimes are highly preferred. Such
4 materials include low-temperature grown gallium arsenide (LT GaAs) and erbium-doped gallium
5 arsenide (GaAs:Er).

6 In the case of LT GaAs, there is a relationship between the growth temperature, the
7 annealing conditions, and the carrier lifetime. Higher growth temperatures correspond to slower
8 recombination rates and longer carrier lifetimes. Thus, a GaAs layer grown at about 200°C may
9 have an average carrier lifetime of less than 1.0 ps, a GaAs layer grown at about 300°C may have
10 an average carrier lifetime of about 10 ps, and a GaAs layer grown at about 400°C may have an
11 average carrier lifetime of about 50 ps (assuming in each case annealing after growth).

12 Skilled practitioners will recognize that adjusting annealing conditions may be needed to
13 optimize device performance and SEU hardness. Annealing low-temperature-grown GaAs made
14 with excess As will cause this excess As to precipitate out. Without wishing to be bound by
15 theory, it is suggested that these As precipitates may form recombination centers in the buffer
16 layer. Without wishing to be bound by theory, it is further suggested that precipitating excess
17 As will retard the diffusion of excess As into the IC, where this As could degrade IC perfor-
18 mance. Typical annealing temperatures are between about 600°C and about 900°C. Typical
19 annealing times are between about 1 minute and about 30 minutes. Skilled practitioners will
20 recognize that at higher temperatures, shorter annealing times may be used, and at lower
21 temperatures, longer annealing times may be used.

1 To compensate for undesirably long carrier lifetimes, thicker buffer layers preferably will
2 be employed. For example, buffer layers according to the invention may be grown at tempera-
3 tures typically below 600°C, more typically below 400°C, preferably below 350°C, more
4 preferably between about 150°C and about 300°C, and most preferably between about 190°C and
5 about 250°C. Likewise, the buffer layer preferably will be sufficiently thick to prevent single
6 event effects. Depending upon the carrier lifetime in the buffer layer, the buffer layer may be
7 between about 0.1 and 25 μm thick, between about 0.5 and about 10 μm thick, between about
8 0.5 and 5 μm thick, or between about 0.5 and 1.5 μm thick. Most preferably, the buffer layer
9 is as thin as possible to achieve the desired result, e.g., between about 0.5 and 1.0 μm thick.

10 With respect to GaAs:Er buffer layers, it has been found that higher Er content is
11 associated with faster recombination in at least the Er concentration range of $10^{17}/cm^3$ to $10^{20}/cm^3$.
12 *See* S. Sethi et al., "Backgating in Pseudomorphic $In_{0.15}Ga_{0.85}As/Al_{0.25}Ga_{0.75}$ MODFET's with a
13 GaAs:Er Buffer Layer", *IEEE Electron Device Lett.* **16**(12) 537-39 (December 1995), which is
14 incorporated by reference herein, in its entirety, for all purposes.

15 Materials such as GaAs:Er and LT GaAs having inherently high recombination rates can
16 provide buffer layers that improve the radiation hardness of ICs by multiple orders of magnitude.

17 Radiation-damaged (including neutron-damaged) buffer layers may also be used.
18 However, this approach may not provide the same level of SEU hardness as optimized LT GaAs.

19 Ion-implanted buffer layers may also be used. However, this approach may not provide
20 the same level of SEU hardness as optimized LT GaAs. Furthermore, they will tend to require
21 more processing than the as-grown materials.

1 Skilled practitioners will recognize that one way of achieving short carrier lifetimes,
2 perhaps the most direct way, is to have high recombination rates in the buffer layer. Preferably,
3 a buffer layer according to the present invention will have a recombination rate that is sufficiently
4 high to achieve the desirable short carrier lifetimes. However, skilled practitioners will recognize
5 that other factors may influence the average carrier lifetime, typically to shorten this lifetime.
6 Carrier trapping is an example of a phenomenon that will tend to shorten carrier lifetimes in
7 buffer layers.

8 In a preferred embodiment of the invention, a diffusion barrier layer is interposed between
9 the buffer layer and the IC. This diffusion barrier layer will help protect the properties of both
10 the IC and the buffer layer over time. Suitable diffusion barrier layer materials include AlAs and
11 AlGaAs. Various Al/Ga ratios may be used in AlGaAs diffusion barrier layers, e.g., $Al_{0.5}Ga_{0.5}As$,
12 $Al_{0.25}Ga_{0.75}As$, and $Al_{0.75}Ga_{0.25}As$. Such a diffusion barrier layer may be quite thin, on the order
13 of 50-500Å, typically about 100Å. Preferably, the diffusion barrier layer is not thicker than
14 necessary to prevent diffusion (especially arsenic diffusion) between the IC and the buffer layer.

15 An optional secondary buffer layer will be used to facilitate growth between layers that
16 do not grow well directly upon each other. The thickness of the secondary buffer layer **37** will
17 be limited to the level of SEU hardness desired for devices having a particular gate length and
18 clock speed. A thinner secondary buffer layer **37** will keep buffer layer **36** closer to the
19 transistor. The closer buffer layer **36** is to the transistor **12**, the more SEU hardness is provided
20 (skilled practitioners will recognize that there are trade-offs to this arrangement). E.g., for a

1 device with a 5 GHz clock rate and a 1.0 μm gate length, soft errors may result if the buffer
2 layer 36 is more than 0.5 μm from the transistor.

3 The structures of the invention include structures having complex ICs (MSI complexity
4 or higher, including LSI or VLSI complexity). It has been found that problems with single event
5 effects will be observed frequently enough to pose a serious problem in circuits with 10,000 or
6 more transistors.

7 The structures of the invention also include structures having circuits that may be less
8 complex, but are disposed in use environments that are especially hostile, i.e., environments
9 where the concentration of particles that are capable of inducing soft errors is higher than the
10 concentration of such particles at earth's surface.

11 The structures of the invention require that the IC can be disposed over the buffer layer.
12 For ICs made from semiconductors in the III-V family grown over LT GaAs or GaAs:Er buffers,
13 this is straightforward. GaAs and InGaAs ICs have been demonstrated with LT GaAs buffers.
14 Furthermore, as growth technology improves, the ability to deposit one layer over another will
15 likewise improve, even between layers with poor lattice matching. Skilled practitioners will
16 recognize that a great deal of research has been done, and continues to be done, to develop
17 techniques for semiconductor growth. For example, some success has been achieved growing
18 GaAs over Si.

19 The structures of the invention may be made using conventional deposition techniques,
20 such as molecular beam epitaxy (MBE) or organo-metallic chemical vapor deposition (OMCVD).

1 It is particularly important to keep good quality, clean interfaces between layers. Accordingly,
2 the buffer layer should be thoroughly cleaned before additional processing.
3
4 Having described the invention, the following examples are given to illustrate specific
5 applications of the invention, including the best mode now known to perform the invention.
6 These specific examples are not intended to limit the scope of the invention described in this
7 application.
8
9 Example 1:
10 Demonstration of the invention by computer simulation.
11 The operation of two 0.8 μm gate length enhancement mode MESFETs was modelled:
12 one simulated MESFET was disposed over a 3.86 μm LT GaAs buffer layer, and one simulated
13 MESFET was disposed over a 3.86 μm conventional GaAs layer. Additional experimental details
14 are given in T.R. Weatherford et al., *supra*. FIG. 3 shows the charge collection transients on the
15 drain electrode for both the conventional device and the device with the LT GaAs buffer layer,
16 where these devices were simulated to be biased near their normal operating points of V_G = 0V,
17 V_D = 2V, and V_S = 0V. It can be seen that the device with the LT GaAs buffer layer returns to
18 its baseline state within 10 ps, while the conventional device does not return to is baseline state
19 at all for the duration of the simulated experiment (500 ps). The collected charge was reduced
20 accordingly.
21

1 Example 2:
2 Demonstration of the invention by physical experiments.

3 Charge collection experiments have been performed on n-channel heterojunction insulated-
4 gate FETs (HIGFETs) both with and without an LT GaAs buffer layer. The test device is shown
5 in FIG. 4. In the test device **40**, a layer **42** that was either conventional GaAs or LT GaAs
6 (depending on the experiment) was grown over GaAs substrate **28**. Grown over this layer was
7 a GaAs layer **29**, and over the GaAs layer was an AlGaAs layer **21**. Patterned onto the AlGaAs
8 layer were a source **14**, a gate **16**, and a drain **18**. Interposed between the gate **16** and the
9 AlGaAs layer **21** was a Schottkey barrier **25**. Two doped regions **20** were formed in the AlGaAs
10 and GaAs layers, **29**,**42**, as indicated by the dashed lines. The interaction of these layers formed
11 a quantum well **27**.

12 Ion- and laser-induced charge collection experiments were performed with the NRL ion
13 microbeam facility and the ultrafast laser facility, as described in McMorrow et al., *supra*, and
14 references cited therein. Laser pulses were used to simulate cosmic ray bombardment. The use
15 of these pulses has the advantage of not damaging the transistor. However, the disadvantage is
16 that the laser pulses do not induce charge in the structure as uniformly as an ion or a cosmic ray
17 will, since laser pulses are attenuated as they travel through the structure.

18 FIG. 5 shows the laser-induced charge collection transients measured for conventional and
19 LT GaAs HIGFETs for excitation with 180 fJ laser pulses centered at 600 nm (into a 50 Ω load).
20 One sees that the LT GaAs layer provided a dramatic improvement in the laser-induced charge
21 collection transients, compared to the conventional HIGFET.

1 FIG. 6 shows the 3 MeV α-particle induced charge collection transients measured for
2 n-channel conventional and LT GaAs HIGFETs. $V_G = 0.2V$, $V_D = 1.5V$, and $V_S = 0V$. One sees
3 that the LT GaAs layer provided about a 100-fold reduction in charge collection, compared to
4 the conventional HIGFET. Error rates approximately follow the square of the charge collection.
5 FIG. 7 shows the time-integrated drain charge collection measurements for conventional
6 and LT GaAs HIGFETs as a function of the laser pulse energy. $V_G = -0.1V$, $V_D = 2V$, and
7 $V_S = 0V$. One sees that the LT GaAs layer limited the charge collection substantially.
8

9 Example 3:
10 Demonstration of the invention by physical experiments.

11 Dynamic SEU characteristics of GaAs complementary HIGFET devices fabricated on
12 conventional semi-insulating substrates were compared to the dynamic SEU characteristics of
13 devices fabricated on LT grown GaAs substrates. Experimental details may be found in Marshall
14 et al., *supra*. Heavy ion test results on shift register and flip-flop devices from the same process
15 lot demonstrated that the LT GaAs layer provides immunity from upsets, even at an LET value
16 of 90 MeV·cm^2/mg. This result is also consistent with pulsed laser measurements performed on
17 the same flip-flop circuits used in the ion test.
18

19 Obviously, many modifications and variations of the present invention are possible in light
20 of the above teachings. It is therefore to be understood that
21 the invention may be practiced otherwise than as specifically described.

Navy Case No. 76,735
Inventor(s): Weatherford et al.

PATENT APPLICATION

ABSTRACT OF THE DISCLOSURE

The present invention is an electronic structure having a buffer layer with a short average carrier lifetime, at least about 1000 Å thick with an upper face, and an integrated circuit disposed over the upper face of the buffer layer, where this integrated circuit would otherwise be susceptible to soft errors, due to its configuration, its clock speed, its use environment, or a combination of these factors. In a preferred embodiment, the preferably high recombination rate buffer layer is an LT GaAs or GaAs:Er buffer layer.

FIG. 1

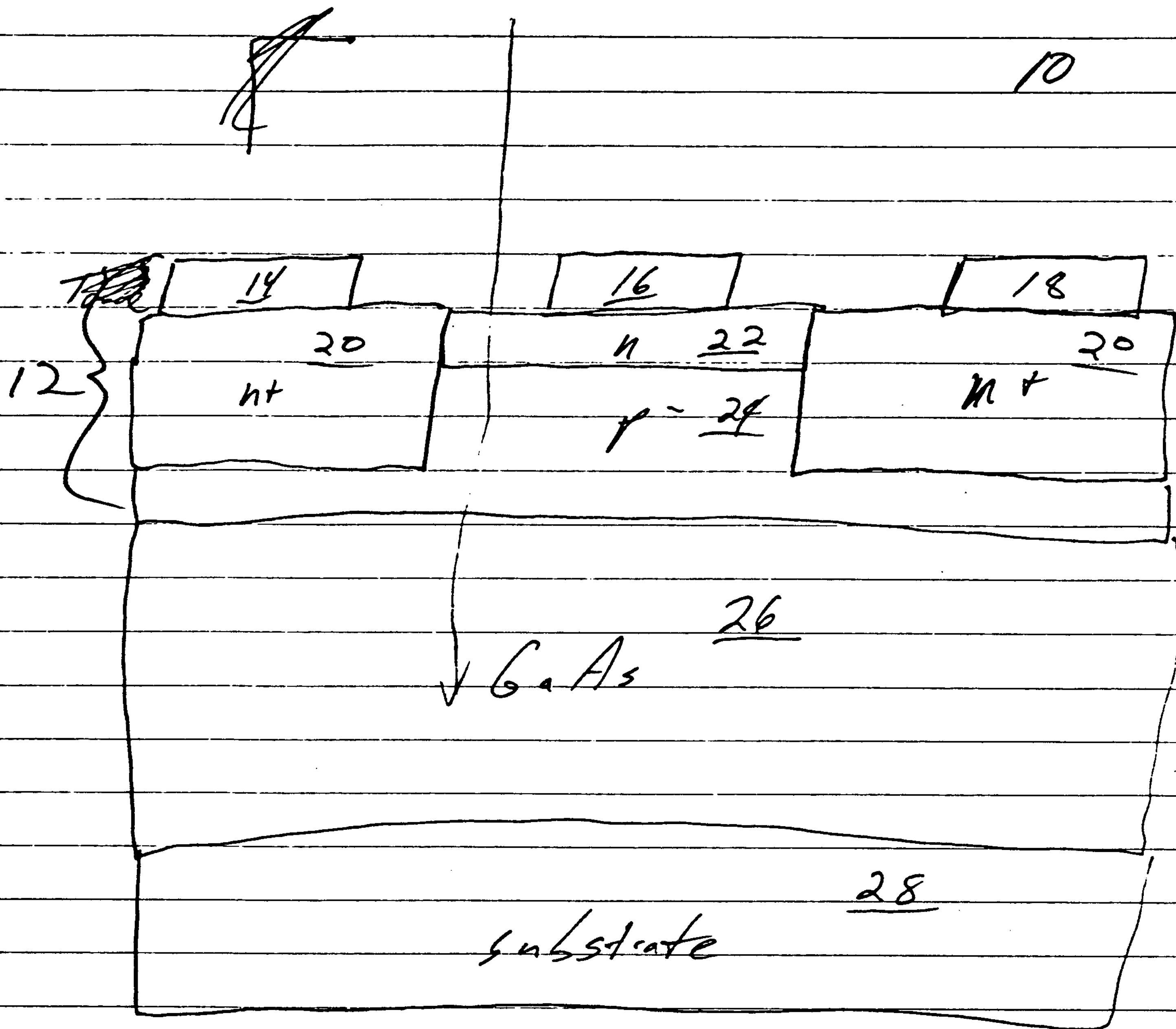


FIG. 2

30

14

16

18

12

20

22

20

24

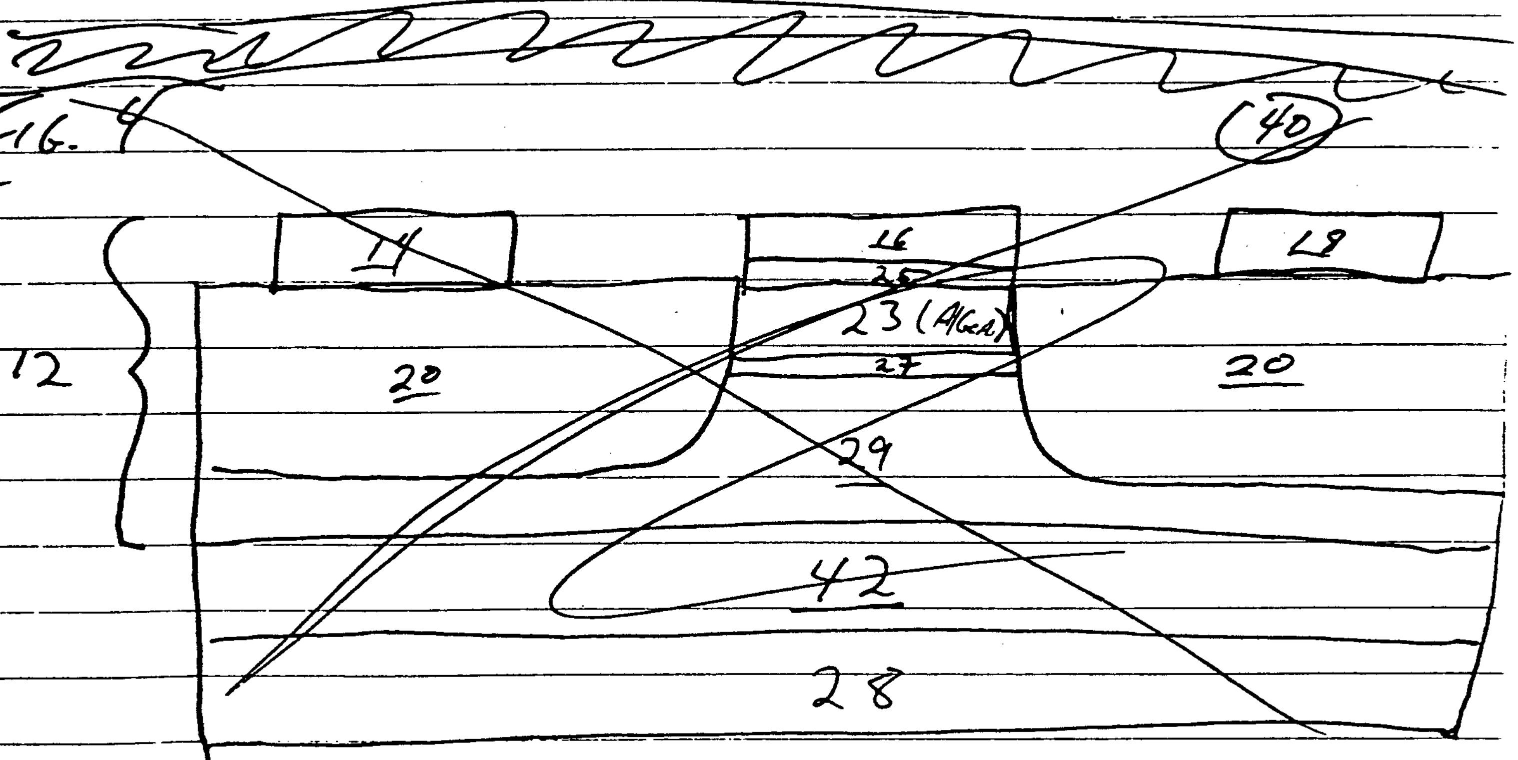
37

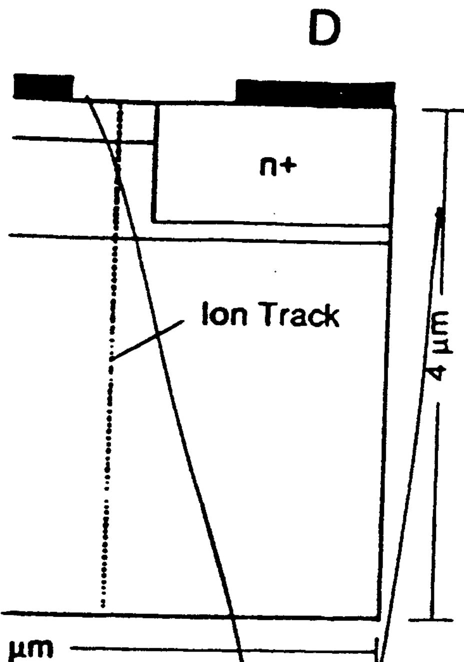
38

36

38

28





3 μm gate length enhancement-mode
n this study. The location of the ion
source-gate spacings are 1 μm.

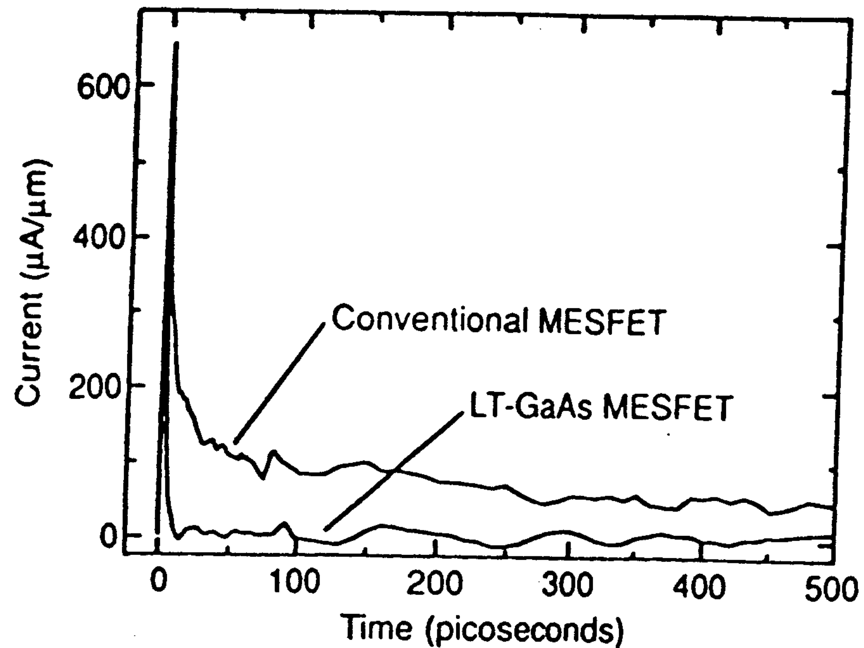


FIG. 2. Computer simulation results of charge collection transients on the drain electrode for the conventional and LT GaAs devices biased near their normal operating point of $V_G=0$ V, $V_D=2$ V, and $V_S=0$ V. The noise in the simulations is due to random fluctuations in the potential arising from the iterative solution to the discrete Poisson equation at each time step.

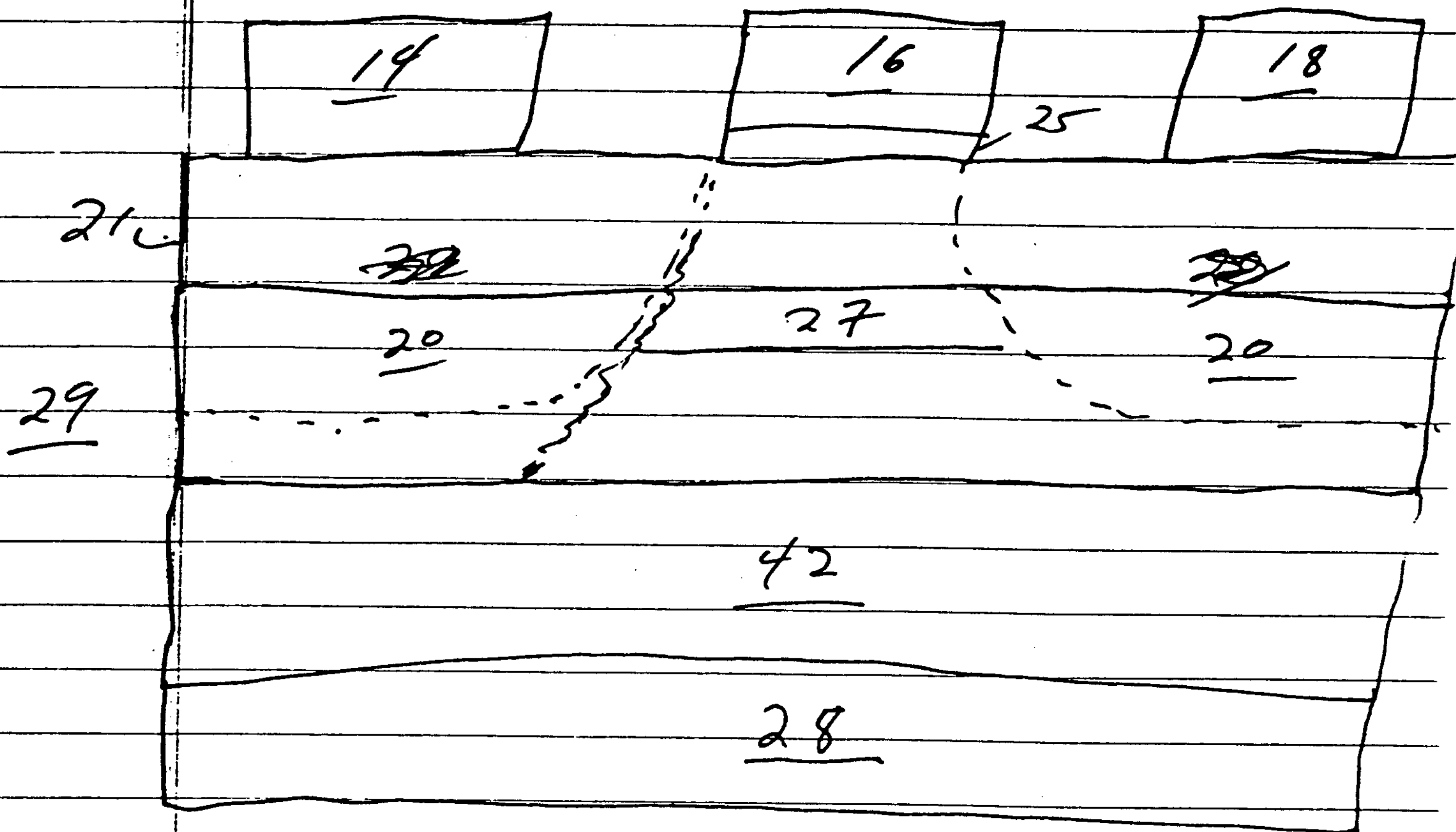
substrate (located 0.14 μm e) is replaced by a LT-grown lues of 1 ns and 1 ps are used and LT GaAs substrates, re- porate a lightly doped p im- wafer. The p implant is used l; its presence is not signifi- MeV α particle is modeled as rge with a constant electron- t $t=0$, corresponding to 25.5 4.0 μm depth of the device. d between the gate and drain nsitive region of the "off" significant at the bias used, lation.

ison of the simulated drain r the n-channel E-MESFET buffer layer. Consistent with simulation [10,11] results, the the conventional device ex-

charge-enhancement mechanisms that dominate the charge-collection dynamics of the conventional device. Additional simulations have been performed as a function of device bias and the charge density of the ion track (to simulate the effects of more energetic ions). The results are consistent with those presented here, and will be discussed in a future publication.

The SER of an IC is a complicated function of individual device characteristics, the internal circuit parameters, and the specific environment (orbit) under consideration.[17] A detailed discussion of SER calculations is beyond the scope of this letter. We have performed heavy ion SER calculations for a GaAs MESFET latch located in geosynchronous orbit utilizing the SPACE RADIATION code.[18] For a typical MESFET latch. SPICE simulations indicate that logic reversal following an ionizing event occurs on a time scale of ~2 ns,[19] and any charge collected within this 2 ns window must be considered. Extrapolation of the transients of Fig. 2 over a 2 ns window reveals that the collected charge is reduced by a factor of

FIG. 4



~~Other FIGS FROM PAPERS~~

system. This prompt response can be identified primarily with hole current being collected at the gate [31]. Following the prompt response is a distinct shoulder that decays on a timescale of about 150 ps, followed by a slowly relaxing tail that decays on a nanosecond timescale. Through computer simulation studies and experimental measurements as a function of the laser pulse energy and device bias conditions, the two slower components of the charge collection transient can be identified with current arising from a parasitic bipolar transistor mechanism, and a channel modulation mechanism, respectively [8,9,15, 16].

The LT GaAs HIGFET transient of fig. 4, in contrast, exhibits only a prompt response, with little or no evidence for the charge-enhancement mechanisms noted above. This result is in excellent agreement with the predictions of the computer simulation.

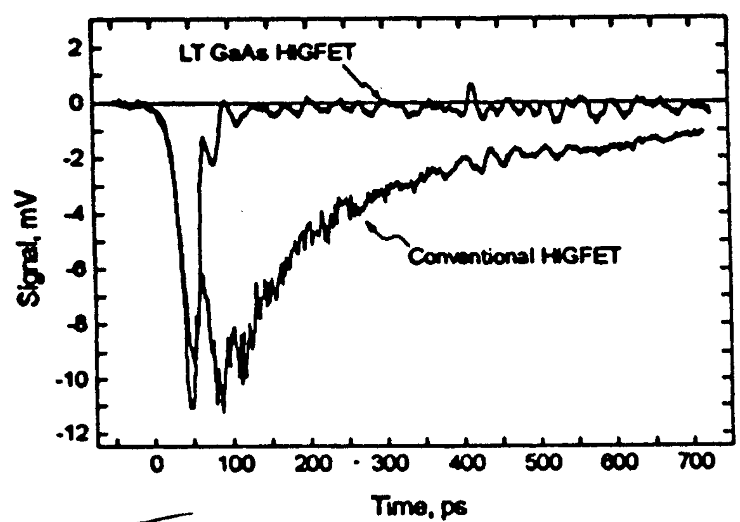


Figure 5. Laser-induced charge-collection transients measured for conventional and LT GaAs HIGFETs for excitation with 180 fJ laser pulses centered at 600 nm (into a 50 Ω load).

[illegible] is observed. We note that the LT GaAs data of fig. 5 was obtained at the triggering threshold of the HYPRES, and therefore the measured transient represents the upper bound of events induced by the ion. Integration of the curves of fig. 5 reveals that for 3 MeV α-particle excitation the LT GaAs buffer layer results in a 100-fold reduction in the collected charge.

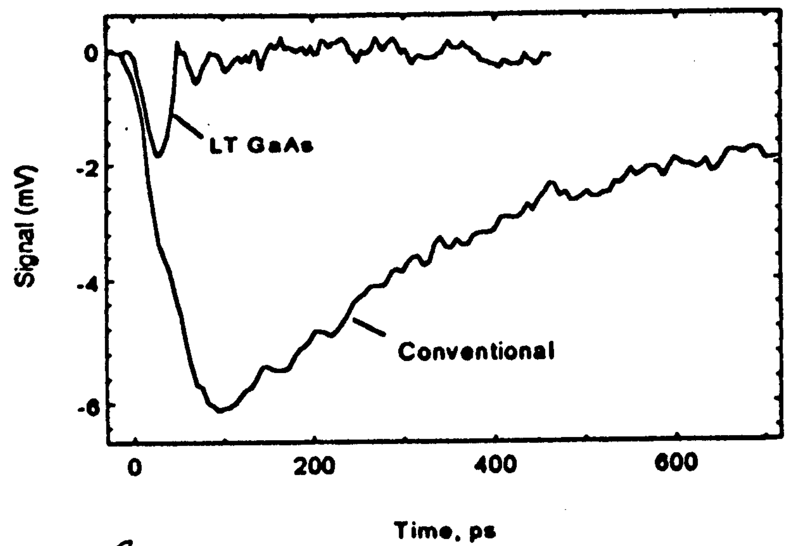


Figure 6. Charge collection transients measured for n-channel HIGFET devices of fig. 3 with and without the LT GaAs buffer layer. $V_G = 0.2\ V$, $V_D = 1.5\ V$, and $V_S = 0\ V$.

It is interesting that the charge collection efficiency is significantly reduced for 600 nm laser excitation even though 85% of the charge is produced above the LT GaAs buffer layer. This result is related to the significant contribution of charge-enhancement mechanisms to the total collected charge in GaAs FET devices. To be efficient, the charge enhancement mechanisms require the presence of excess carriers in

energy. In this report we focus on the pulse energy measurements. A complete report of these results will be presented elsewhere [32].

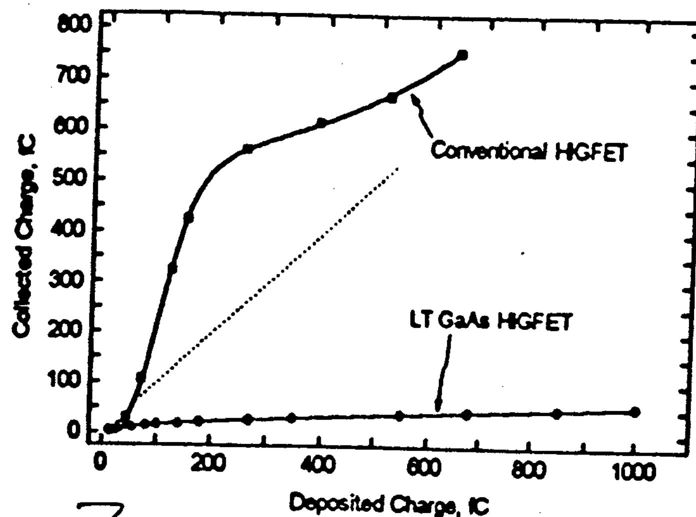


Figure 7. Time-integrated drain charge-collection measurements for the n-channel HIGFET devices of fig. 3 as a function of the laser pulse energy. $V_G = -0.1\ V$, $V_D = 2\ V$, *and*, $V_S = 0\ V$.

Figure 6 shows charge-sensitive preamplifier measurements as a function of the laser pulse energy for a bias condition of $V_G = -0.1$ V and $V_D = 2.0$ V. The dashed line corresponds to a charge-collection efficiency of unity (deposited charge = collected charge). As is evident, for most of the energy range investigated, the charge collection efficiency for the LT GaAs HIGFET is reduced by a factor of ~ 20 when compared to that of the conventional HIGFET.

Error Rate Calculations

The efficient elimination of charge-enhancement mechanisms by the LT GaAs buffer layer suggests that significant improvements in the SEU rate might be expected for LT GaAs MESFET and HIGFET-based ICs. While the current measurements and simulation results provide insight into the role of the LT GaAs buffer layer in reducing the collected charge, charge-collection measurements alone are not sufficient to