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FULL DUPLEX TRANSCEIVER

STATEMENT OF GOVERNMENT INTEREST

The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefore.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates generally to a transceiver for data communication, and more particularly to a Radio Frequency (RF) front end to a standard IF (Intermediate Frequency) modem to allow full duplex data communication at RF.

(2) Description of the Prior Art

For a full duplex communication transceiver, the transceiver's transmitter and receiver are simultaneously active, thereby allowing simultaneous data transmission and reception. Depending upon the design considerations, a full duplex transceiver's transmit and receive antennae are often the same. When transmit and receive frequencies are similar, interference

is often encountered although separate transmission and receive antennae are employed.

Methodologies and systems for avoiding transmit and receive signal interference include U.S. Patent No. 5,905,706 to Vidales wherein half-bit transmission and reception intervals are formed; U.S. Patent No. 5,715,520 to Hillock, et al, for Time Division Duplex (TDD) systems to utilize a single Local Oscillator (LO) to derive two LO signals at different times, thereafter using the two LO signals to produce an intermediate and an offset signal frequency; U.S. Patent No. 5,687,169 to Fullerton describes a pulse interleaving method and apparatus for impulse radio's ultrawide-band communications; and, U.S. Patent No. 5,533,056 to Cripps provides a duplex transceiver binary encoder/decoder.

U.S. Patent No. 5,881,369 to Dean, et al, describes a duplex receiver operational in Frequency Division Duplex (FDD) and Time Division Duplex (TDD) modes. The Dean, et al, transceiver has an up-conversion path that converts an Intermediate Frequency (IF) to a Radio Frequency (RF) in either an upper RF frequency range or a lower RF frequency range, and similarly a down-conversion path to convert the received RF frequency in either the upper or lower frequency range to a desirable IF frequency. The Dean, et al, up-conversion and down-conversion paths connect to either an upper or lower band diplexer port through a switch array. A switch controller controls the switch array based upon whether

the transceiver is operating in TDD or FDD mode. The Dean, et al, invention concentrates on cellular communication requirements and demands.

General data communication between a transmitter and receiver are less restrictive than the cellular requirements. Higher frequency data communication allows more rapid communication rates; however, typical modems for data communication operate in the IF frequency band.

There is currently no apparatus or method for a full duplex transceiver at the Radio Frequency (RF) bands, wherein RF is derived from a variable IF frequency.

What is needed is a method and apparatus to convert an IF generator output to RF for full duplex communication.

SUMMARY OF THE INVENTION

It is a general purpose and object of the present invention to provide a configurable transceiver architecture that allows simplex, half-duplex, and full duplex operation. Another object of the present invention is to provide a transceiver architecture that accepts a variable IF as input, and generates a RF output for data communication using fixed Phase Locked Oscillators (PLOs). A further object is to provide a transceiver that receives a RF signal and converts the RF signal to an IF signal using fixed PLOs. Still yet another object is to provide such

configurable transceiver architecture for single or dual antenna use, utilizing internal, external, or no diplexer, and allowing internal or external oscillator references.

Other objects and advantages of the present invention will become more obvious hereinafter in the specification and drawings.

These objects are accomplished with the present invention by a RF front end to an IF generator and post-processor whereby the IF generator output is variable. The transceiver up-conversion path includes an IF Filter, the output of which is input to a mixer with the output of a fixed Phase Locked Oscillator (PLO). The mixer output is input to a band-pass filter and amplified. With a single antenna configuration, the amplifier output connects to either an internal or external diplexer that interfaces to the antenna. With a dual antenna configuration, the amplifier output interfaces directly to the transmit antenna. Similarly, the down-conversion path includes an internal or external diplexer in the single antenna configuration, a band-pass filter, a RF amplifier, a mixer that receives the RF amplifier output and the fixed PLO as inputs, an IF Filter, IF amplifier, and an attenuator for interfacing to the IF post-processor. A user-interface allows RF TX and RX frequency selection, data rate selection, and configurable options including internal or external diplexer, internal or external

oscillator reference, and TX amplifier keying to allow simplex, half duplex, or full duplex communication.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the invention and many of the attendant advantages thereto will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings, wherein like reference numerals refer to like parts and wherein:

FIG. 1 is a block diagram of the RF transceiver for the preferred embodiment wherein the IF generator is a modem;

FIG. 2 is a block diagram of the RF transceiver up-conversion and down-conversion paths for a single antenna configuration utilizing an internal diplexer;

FIG. 3 is a block diagram of the RF transceiver up-conversion and down-conversion paths for a single antenna configuration utilizing an external diplexer; and,

FIG. 4 is a block diagram of the RF transceiver up-conversion and down-conversion paths for a dual antenna configuration.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 1, there is shown a block diagram **10** of the transceiver system, further detailing individual transceiver components. In the preferred embodiment, the transceiver **12** interfaces to a modem **14** that provides a varying IF to the transceiver **12**. The modem's **14** variable IF is specified through a user-interface **16** that allows a user to specify communication parameters. Communication parameters specified through the user-interface **16** include satellite or line-of-site (LOS) communication, RF transmit (TX) frequency, RF receive (RX) frequency, communication data rate, internal or external oscillator reference, and transmit power amplifier keying options.

An embedded controller **18** controls the user-interface **16** and initializes transceiver **12** components according to user selections. The embedded controller **18** uses the user-selected transmit (TX) and receive (RX) RF frequencies to compute respective TX and RX intermediate frequency (IF) values, and the embedded controller **18** transfers the TX and RX IF frequency values to the modem **14**. The embedded controller **18** also uses the TX and RX RF frequencies to specify the respective TX and RX band-pass filter (BPF) **20, 22** coefficients.

The embedded controller **18** accepts a user-selected data rate from the user-interface **16**, and provides the data rate to the

modem **14**. The TX amplifier **24** is additionally keyed according to user-interface designations of constant on, constant off, or RTS control, thereby providing a mechanism that allows the transceiver to perform in full duplex, half duplex, or simplex modes. In the preferred embodiment, when satellite communication is user-specified, the embedded controller enables the internal diplexer **26**. Alternately, a LOS entry indicates an external diplexer (single antenna configuration) or no diplexer (dual antenna configuration).

As will be shown in FIGS. 2, 3, and 4, the down-conversion path comprises an attenuator **28**. In the preferred embodiment, the attenuator **28** is digital and controlled by the embedded controller **18** to maintain a desired signal level at the attenuator output. The embedded controller **18** also enables the internal oscillator reference **30** depending upon whether the user selects (via the user interface) internal or external oscillator reference.

Other components comprising the transceiver **12** are the TX mixer **32**, RX Mixer **34**, TX IF Filter **36**, RX IF Filter **38**, RX Amplifier **40**, RX IF Amplifier **42**, and at least one fixed Phase-Locked Oscillator (PLO) **44**. The preferred embodiment transceiver **12** also maintains an embedded controller/user-interface interface **46** to allow user-interface control by the embedded controller, user-entered data transfer, and transmission of performance data

for user-interface display; an embedded controller/IF modem interface **48** to transfer computed IF frequencies and user-entered data rates from the embedded controller **18** to the modem **14**, and received signal levels and error rates from the modem **14** to the embedded controller **18**; an external oscillator interface **50** to allow an external oscillator reference to drive the fixed PLO(s) **44** when the internal oscillator is not selected; an external diplexer interface **52** to provide for external diplexer configurations; a single (TX/RX) antenna interface **54**; a dual antenna interface **56**; a TX IF interface **58** to accept TX IF signals from the modem **14**; and, a RX IF interface **59** to transfer down-converted RX IF signals from the transceiver **12** to the modem **14**.

Referring now to FIG. 2, there is shown the up-conversion and down-conversion paths for a single antenna configuration using the internal diplexer. The modem **14** provides an IF frequency to the transceiver **12** as directed by the transceiver's embedded controller and based upon the user-entered, TX RF frequency and fixed PLO values **44**. The modem's **14** TX IF frequency is transferred to the transceiver **12** through the TX IF interface between the modem and transceiver **58** and input to the TX IF filter **36**. The TX IF Filter output **60** provides one input to the up-conversion (TX) mixer **32**. The fixed PLO(s) **44** provide(s) the TX mixer **32** with a second input **62**. The fixed

PLO(s) **44** is selected to achieve the user-selected TX RF frequency, recalling that the TX IF provided by the modem **14** was calculated by the embedded controller **18** using the user-selected TX RF frequency and a fixed PLO **44** value.

In the preferred embodiment, the fixed PLO(s) **44** is driven by a relay **64** that maintains connections to the internal oscillator **30** and an external oscillator interface **50**. The relay **64** is activated depending upon the user selection for internal or external oscillator reference. Although FIG. 2 indicates a single fixed PLO **44**, multiple fixed PLOs may be utilized to provide a larger TX (and RX) RF frequency selection.

The IF filter output **60** and fixed PLO output **62** provide the mixer **32** with signals to achieve the desired TX RF frequency at the mixer output **66**. The mixer output **66** is input to the TX band-pass filter (BPF) **20** that is tuned by the embedded controller **18** for the appropriate TX RF frequency, and amplified **24**. In the preferred embodiment, the amplifier **24** interfaces to a relay **68**, the output of which connects to the internal diplexer **26** TX input **26a**. In the preferred embodiment, the internal diplexer **26** combined output **26b** connects to a relay **70** for interfacing to the single antenna **54**.

The FIG. 2 down-conversion path includes the internal diplexer **26**, whose RX input **26c** is connected to a relay **72** and thereafter a RX BPF **22** tuned to the user-specified RX RF

frequency. The RX RF signal is then amplified **40** before input to the down-conversion path (RX) mixer **34**. A fixed PLO **44** provides the second input to the down-conversion path mixer **34** to generate an IF signal that is filtered **38** and amplified **42** before being attenuated **28** and transferred to the modem **14** using the RX IF interface **59**.

Referring now to FIG. 3, there is shown a single antenna configuration utilizing an external diplexer. Similar to FIG. 2, the modem **14** provides the variable TX IF to the transceiver **12** through the TX IF interface **58**, and the IF signal is filtered **36** and provided as one input **60** to the up-conversion mixer **32**. A PLO **44**, driven by either an internal oscillator reference **30** or an external oscillator through the external oscillator interface **50**, provides the second mixer input **62**. The up-conversion mixer **32** provides a TX RF signal **66** that is band-pass filtered **20**, amplified **24**, and connected through relay **68** to the TX external diplexer interface **52a**. The external diplexer TX terminal **90a** accepts the TX signal, while the external diplexer combined terminal **90b** returns to the transceiver **12** through the external diplexer combined interface **52b**, connecting to a relay **70** and hence the single antenna interface **54**. The external diplexer RX terminal **90c** returns to the transceiver **12** via the RX external diplexer interface **52c**. The RX RF signal **92** begins the down-conversion path by passing through a relay **72**, RX BPF **22** tuned by

the embedded controller to the user-specified RX RF frequency, and amplifier **40**. The amplified RF signal **94** is input to the down-conversion mixer **34** with a signal from a fixed PLO **44** to convert the RF signal to IF, whereupon the IF signal is filtered **38**, amplified **42**, and attenuated **28** for transmission to the modem **14** through the RX IF interface **59**.

Referring now to FIG. 4, there is shown a dual antenna configuration wherein a first antenna designated the TX antenna, and a second antenna designated the RX antenna, are connected to the transceiver dual antenna interface **56**. The up-conversion path connected to the TX antenna is similar to the up-conversion paths of FIGS. 2 and 3, with the omission of a diplexer. Once again, the modem **14** provides a variable TX IF to the transceiver **12** through the TX IF interface **58**, whereupon the TX IF signal is filtered **36** and input to a mixer **32** with a signal from a fixed PLO **44**. A fixed PLO **44** may be driven by an internal reference **30** or by an external oscillator through the external oscillator interface **50**. The mixer output **66** is a RF signal that is input to the TX BPF **20**, amplified **24**, and connected to the dual antenna interface's TX antenna terminal **56a** through a relay **68**. The down-conversion path begins with the signal from the dual antenna interface's RX antenna terminal **56b** that is sent through a relay **72**, RX BPF **22**, and RF amplifier **40**, before being input to the RX mixer **34**. The other RX mixer input is derived from a fixed PLO

44, and the RF mixer output 96 is an IF signal that is filtered 38, amplified 42, and attenuated 28 before it is returned to the modem 14 via the RX IF interface 59 for post processing.

The advantage of the present invention over the prior art is that a RF signal can be derived from a variable IF using a fixed PLO, thereby allowing increased data rate communication.

What has thus been described is a RF front end to an IF generator and post-processor whereby the IF generator output is variable. The transceiver up-conversion path includes an IF Filter, the output of which is input to a mixer with the output of a fixed Phase Locked Oscillator (PLO). The mixer output is input to a band-pass filter and amplified. With a single antenna configuration, the amplifier output connects to either an internal or external diplexer that interfaces to the antenna. With a dual antenna configuration, the amplifier output interfaces directly to the antenna. Similarly, the down-conversion path includes an internal or external diplexer in the single antenna configuration, a band-pass filter, a RF amplifier, a mixer that receives the RF amplifier output and the fixed PLO as inputs, an IF Filter, IF amplifier, and an attenuator for interfacing to the IF post-processor. A user-interface allows RF TX and RX frequency selection, data rate selection, and configurable options including internal or external diplexer, internal or external oscillator reference, and TX amplifier

keying to allow simplex, half duplex, or full duplex communication.

Although the present invention has been described relative to a specific embodiment thereof, it is not so limited. Obviously many modifications and variations of the present invention may become apparent in light of the above teachings. For example, although the preferred embodiment indicated the presence of relays in the up-conversion and down-conversion paths, the relays may be replaced by another appropriate device, or omitted entirely. The amplifier may require a pre-amplifier depending on signal and amplifier characteristics. Multiple, fixed PLOs may be utilized to offer greater ranges of TX and RX RF selection. Although the preferred embodiment indicated a fixed PLO feeding the TX and RX mixers, depending upon the user-selected TX and RX RF frequencies, the fixed PLO output to the TX and RX mixers may be different, and may be derived from a different fixed PLO. The RF signal may be any frequency range, including but not limited to UHF, VHF, etc. Although the description provided three external diplexer interface components, these interfaces may in fact represent a single component. Similarly, the dual antenna interface may be a single interface for two antennae, or dual interfaces. The TX IF interface and RX IF interface between the transceiver and modem may also be a single interface. Although the described

transceiver operates in full duplex mode, the constant on, constant off, and RTS TX amplifier control options provide for simplex, half-duplex, or full duplex operation. Although the preferred embodiment indicated diplexer use only in single antenna configurations, diplexers may be utilized in the dual antenna configuration. The attenuator may be digital or analog. Any variable, IF frequency generator and post-processor can substitute for the modem. Although the transceiver architecture was shown in three basic configurations to encompass the configurable options within the preferred embodiment, a single configuration may be selected and implemented individually.

Many additional changes in the details, materials, steps and arrangement of parts, herein described and illustrated to explain the nature of the invention, may be made by those skilled in the art within the principle and scope of the invention. It is therefore understood that

the invention may be practiced otherwise than as specifically described.

Attorney Docket No. 79924

FULL DUPLEX TRANSCEIVER

ABSTRACT OF THE DISCLOSURE

A RF front end to an IF generator and post-processor whereby the IF generator output is variable. The transceiver up-conversion path includes an IF Filter, the output of which is input to a mixer with the output of a fixed Phase Locked Oscillator (PLO). The mixer output is input to a band-pass filter and amplified. With a single antenna configuration, the amplifier output connects to either an internal or external diplexer that interfaces to the antenna. With a dual antenna configuration, the amplifier output interfaces directly to the antenna. Similarly, the down-conversion path includes an internal or external diplexer in the single antenna configuration, a band-pass filter, a RF amplifier, a mixer that receives the RF amplifier output and the fixed PLO as inputs, an IF Filter, IF amplifier, and an attenuator for interfacing to the IF post-processor. A user-interface allows RF TX and RX frequency selection, data rate selection, and configurable options including internal or external diplexer, internal or external oscillator reference, and TX amplifier keying to allow simplex, half duplex, or full duplex communication.

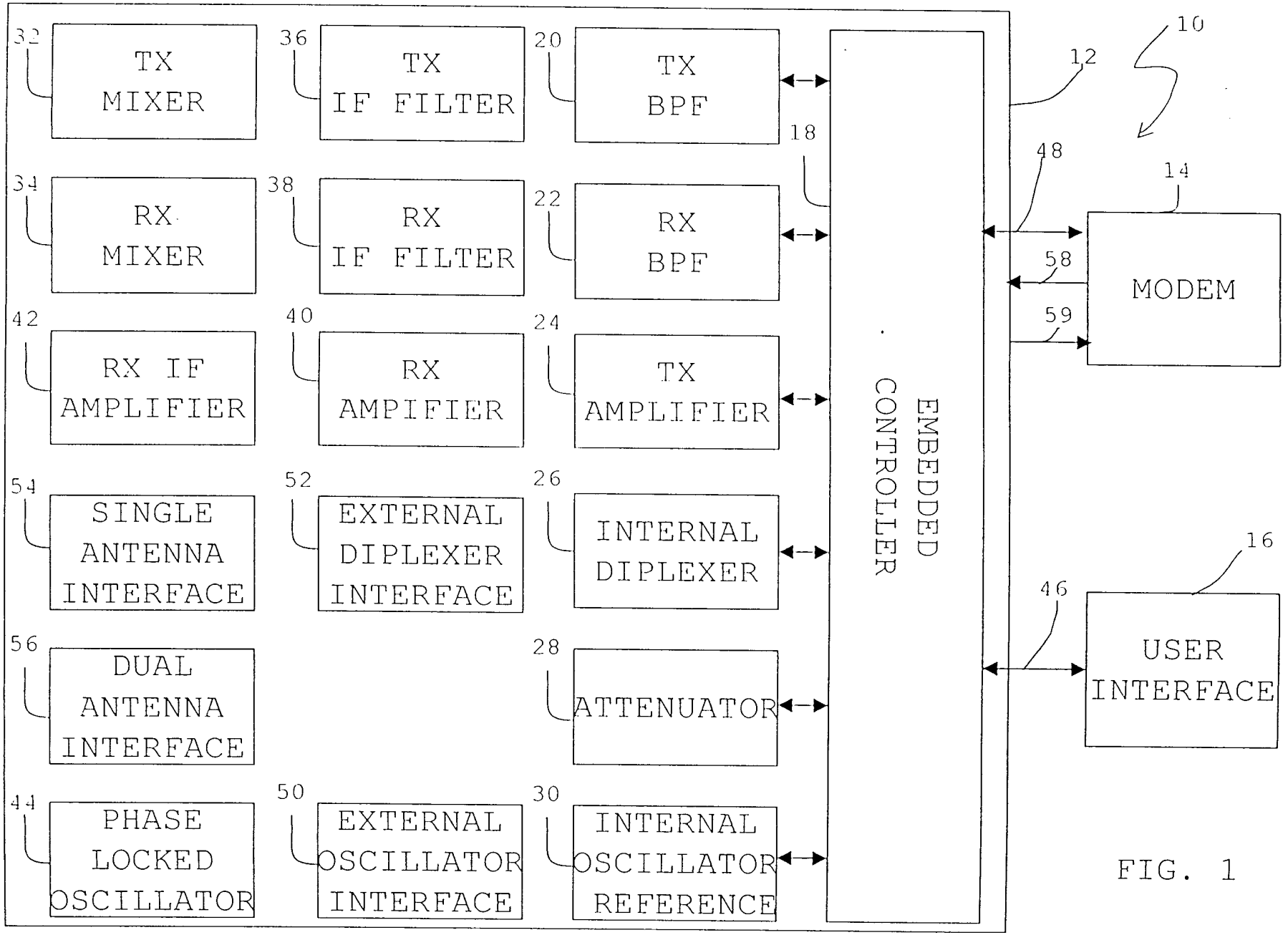
32
TX MIXER
36
TX IF FILTER
20
TX BPF
34
RX MIXER
38
RX IF FILTER
22
RX BPF
42
RX IF AMPLIFIER
40
RX AMPIFIER
24
TX AMPLIFIER
54
SINGLE ANTENNA INTERFACE
52
EXTERNAL DIPLEXER INTERFACE
26
INTERNAL DIPLEXER
56
DUAL ANTENNA INTERFACE
28
ATTENUATOR
44
PHASE LOCKED OSCILLATOR
50
EXTERNAL OSCILLATOR INTERFACE
30
INTERNAL OSCILLATOR REFERENCE
18
EMBEDDED CONTROLLER
12
10
48
14
58
MODEM
59
16
46
USER INTERFACE

FIG. 1

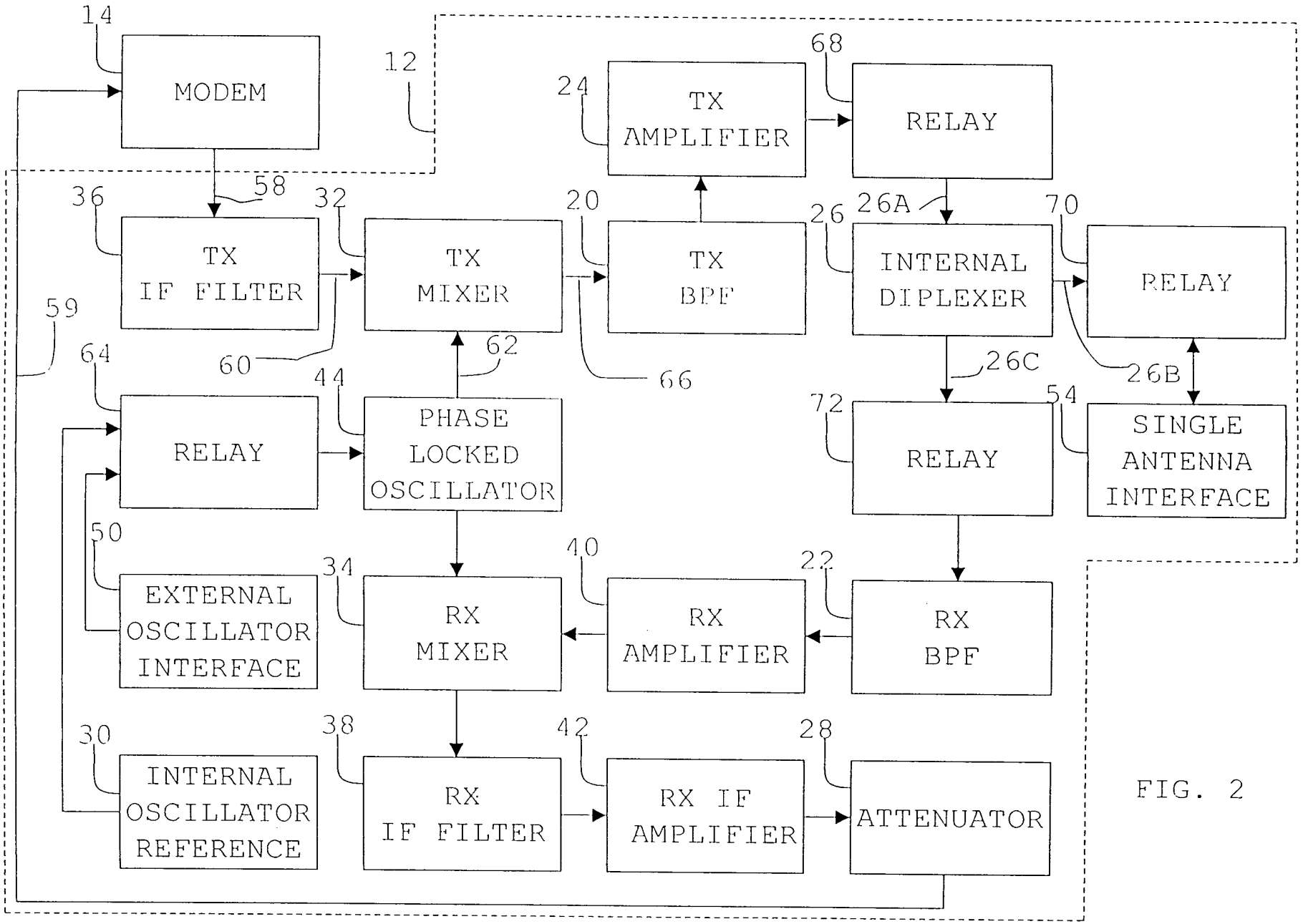
14
MODEM
12
68
24
TX
AMPLIFIER
RELAY
36
58
32
20
26
26A
70
TX
IF FILTER
TX
MIXER
TX
BPF
INTERNAL
DIPLEXER
RELAY
59
64
60
62
66
26C
26B
44
72
54
RELAY
PHASE
LOCKED
OSCILLATOR
RELAY
SINGLE
ANTENNA
INTERFACE
50
40
34
22
EXTERNAL
OSCILLATOR
INTERFACE
RX
MIXER
RX
AMPLIFIER
RX
BPF
30
38
42
28
INTERNAL
OSCILLATOR
REFERENCE
RX
IF FILTER
RX IF
AMPLIFIER
ATTENUATOR

FIG. 2

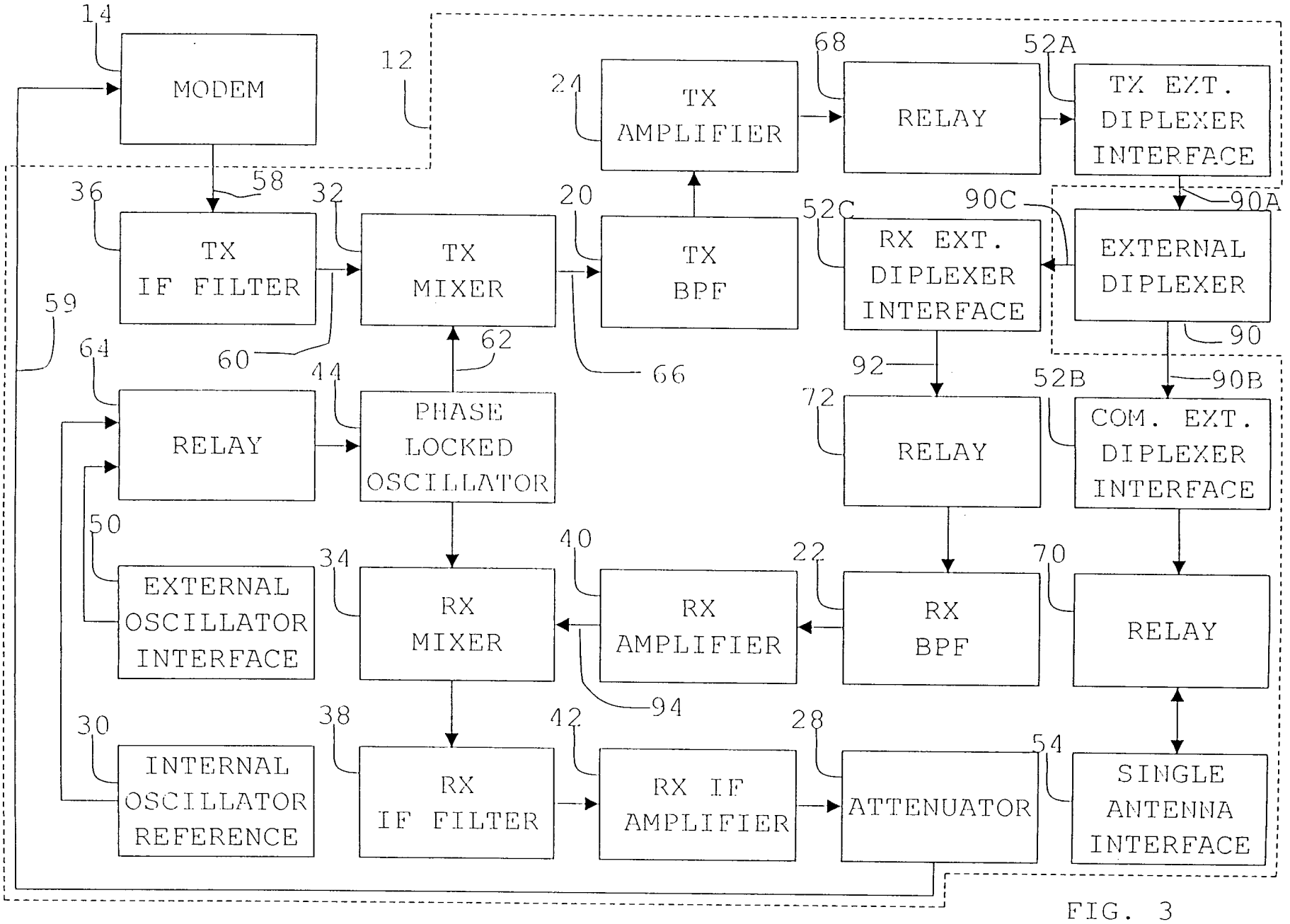
14
MODEM
12
68
52A
24
TX AMPLIFIER
RELAY
TX EXT. DIPLEXER INTERFACE
36
58
32
20
52C
90C
90A
TX IF FILTER
TX MIXER
TX BPF
RX EXT. DIPLEXER INTERFACE
EXTERNAL DIPLEXER
59
60
62
66
90
64
44
92
52B
90B
72
RELAY
PHASE LOCKED OSCILLATOR
RELAY
COM. EXT. DIPLEXER INTERFACE
50
40
34
22
70
EXTERNAL OSCILLATOR INTERFACE
RX MIXER
RX AMPLIFIER
RX BPF
RELAY
94
30
38
42
28
54
INTERNAL OSCILLATOR REFERENCE
RX IF FILTER
RX IF AMPLIFIER
ATTENUATOR
SINGLE ANTENNA INTERFACE

FIG. 3

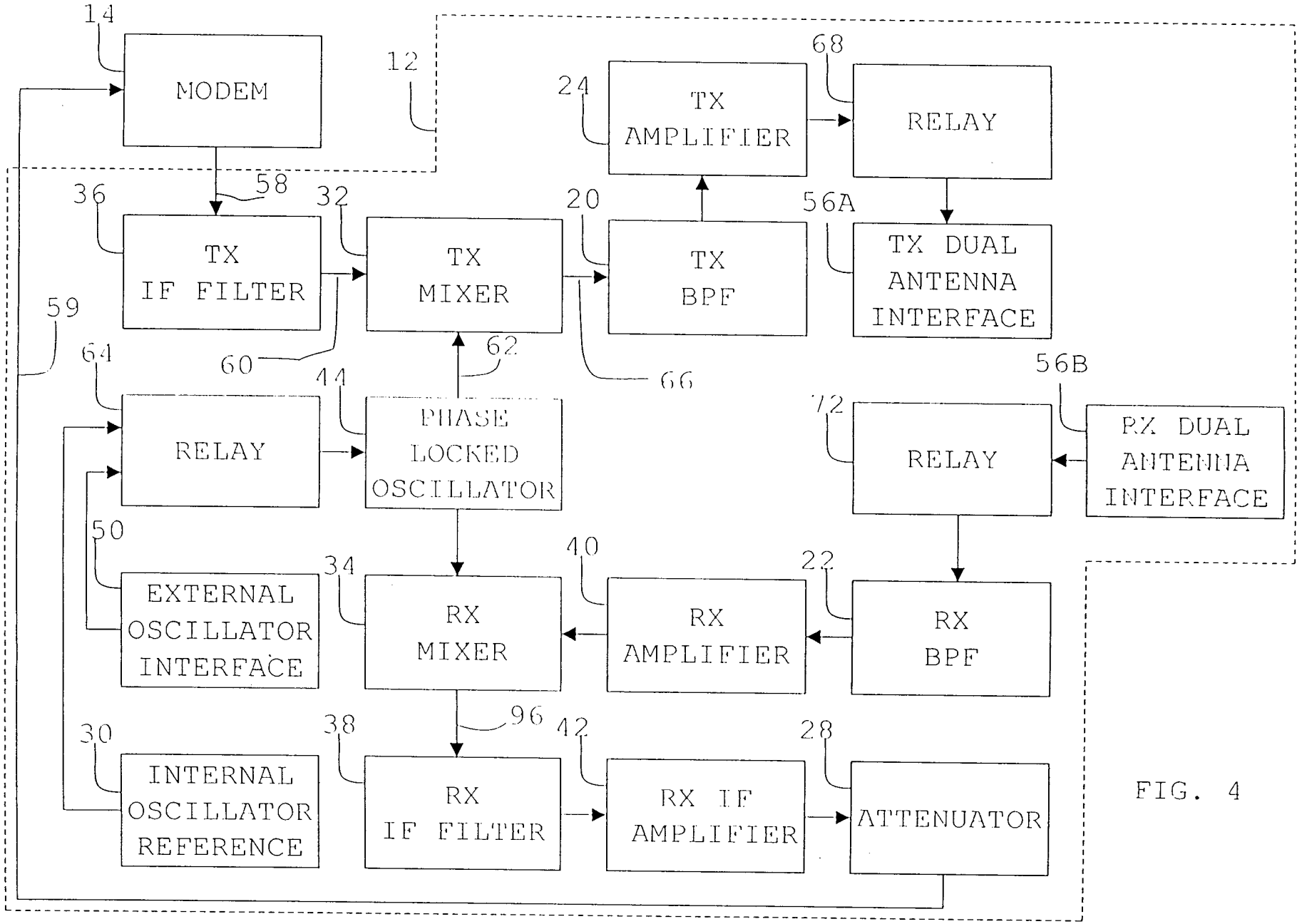
14
MODEM
12
68
24
TX
AMPLIFIER
RELAY
36
58
32
20
56A
TX
IF FILTER
TX
MIXER
TX
BPF
TX DUAL
ANTENNA
INTERFACE
59
64
60
62
44
66
56B
RELAY
PHASE
LOCKED
OSCILLATOR
72
RELAY
RX DUAL
ANTENNA
INTERFACE
50
40
34
22
EXTERNAL
OSCILLATOR
INTERFACE
RX
MIXER
RX
AMPLIFIER
RX
BPF
30
96
38
42
28
INTERNAL
OSCILLATOR
REFERENCE
RX
IF FILTER
RX IF
AMPLIFIER
ATTENUATOR

FIG. 4