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Invited Paper

High-performance thin-film transistors using Ni silicide for liquid-crystal displays

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ABSTRACT

The Ni-silicide of a sheet resistance of 7 Ω/□ can be formed at 230 °C on n^+ a-Si:H and thus can be applied to gate and source/drain contacts for high performance TFTs. Because of its low resistance it is possible to make a self-alignment between gate and source/drain, which lead to a coplanar a-Si:H TFT having a low parasitic capacitance between them. The $NiSi_2$ precipitates can be formed on a-Si:H at around 350°C and needlelike Si crystallites are grown as a result of the migration of the $NiSi_2$ precipitates though a-Si:H network. Amorphous silicon can be crystallized at 500°C in 10 minutes in a modest electric field. The low temperature poly-Si TFT with a field effect mobility of 120 cm^2/Vs has been demonstrated using the low temperature poly-Si.

Keywords: Silicide, Parasitic resistance, SMC poly-Si TFT

1. INTRODUCTION

To achieve small contact resistance and self-alignment of source/drain (S/D) to gate, silicide electrode is considered as a good candidate. Ni-silicide, mainly NiSi phase, can be formed at as low as 230°C on a-Si:H. Recently we have developed Ni-silicide S/D contacts for a-Si:H inverted staggered thin-film transistor (TFT)[1-2], a-Si:H coplanar TFT[3-4], and poly-Si coplanar TFT[5-7].

The performance of a-S:H TFT depend strongly on the S/D parasitic resistance[8-9]. In our previous work it was reduced by using the Ni-silicides on a-Si:H. To reduce the parasitic series resistance, Ching-Fa Yeh et al. performed a plasma ion implantation[10] and G. K. Guist et al. did a gas immersion laser doping [11]. The Ni-silicide formed at 230 °C on n^+ a-Si:H has a sheet resistance of 7 Ω/□, which is at least two orders of magnitude lower than that of n^+-doped poly-Si. This significantly low sheet resistance of Ni-silicide enables us to lower the contact resistance in the form of silicide-metal interface, resulting in the reduction in the parasitic resistance. The $NiSi_2$ precipitates can be formed at around 350°C on a-Si which induces a silicide-mediated-crystallization (SMC). The a-Si having an average Ni concentration of order of 10^{13} cm^{-2} can be crystallized in 10 minutes at 500°C in an electric field[12]. A SMC poly-Si TFT with a field effect of 120 cm^2/Vs has been developed.

2. NI SILICIDE FORMATION

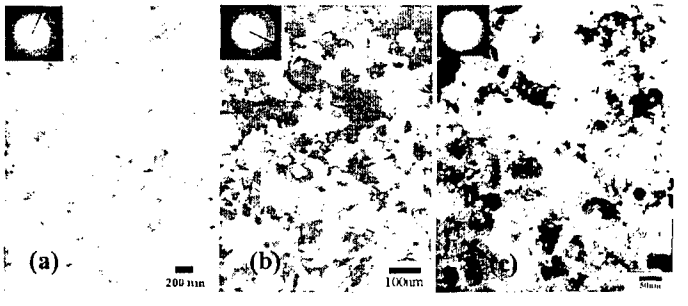

Figure 1. TEM bright-field images and their electron diffraction patterns of the Ni-silicides on a-Si:H formed at (a) 150 °C, (b) 240 °C and (c) 350°C.

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TABLE 1. Properties of the Ni-silicides on a-Si:H formed at various temperatures

	Ni_2Si	NiSi	$NiSi_2$
Formation temperature (°C)	~ 150	240 ~ 390	325 ~ 480
Phase	Orthorhombic Ni-rich	Orthorhombic	Cubic Si-rich
Sheet resistance (Ω/□)	Below 580	2.8 ~ 2.95	4.0 ~ 5.5
Crystal direction	(112), (103), (202), (020)	(211), (102)	(100), (110), (111)
Remarks		Lowest sheet resistance	Nuclei for SMC

Formation of Ni-silicides on a-Si depends strongly on the Ni/Si ratio and annealing temperature. As shown in the electron diffraction patterns shown in Fig. 1, the structure of Ni-silicide changes from amorphous to polycrystalline with increasing annealing temperature. The phase of Ni-silicide is changed as follows; $Ni_2Si \rightarrow NiSi \rightarrow NiSi_2$. The dependence of sheet resistance as a function of ion energy for various annealing temperatures is plotted in Fig. 2. Table 1 summarizes the structural and electrical properties of Ni-silicides. The sheet resistance of the Ni-silicide formed at 210 °C is about 7 Ω/□, and increases to about 13 Ω/□ at 270 °C. This increase appears to be due to the change in the Ni-silicide phase to silicon-rich silicide. Figure 3 shows the plot of Ni and Si binding energy as a function of the sputtering time, i.e., film depth. Note that there is a silicide layer of about 20nm on the a-Si:H.

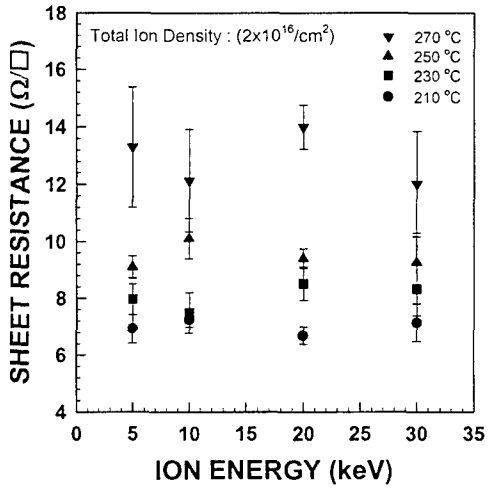

Figure 2. Sheet resistance of Ni-silicides on a-Si:H as a function of ion acceleration voltage for various annealing temperatures (total ion dose:$2\times 10^{16}cm^{-2}$).

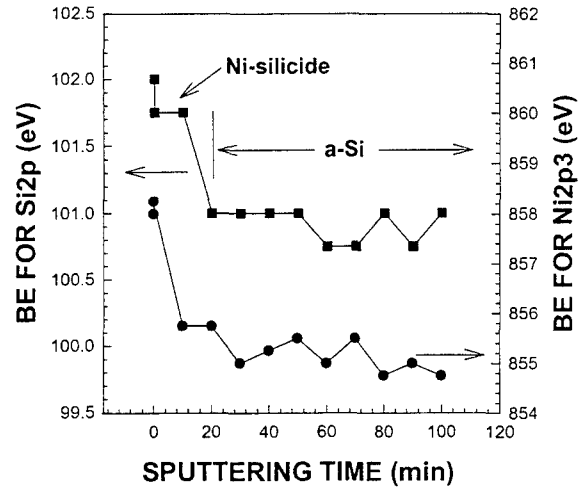

Figure 3. Variation of Ni and Si binding energy as a function of sputtering time.

3. A-SI:H TFT WITH NI SILICIDE

We fabricated a-Si:H TFTs with 3 different structures. Figure 4-(a) depicts the a-Si:H coplanar TFT in which Ni-silicide S/D is self-aligned to the gate. In the case of a-Si:H coplanar TFT[4], conventional coplanar structures employing contact windows can not be accepted because of the high resistance (~10^6 Ω/□) of n^+-doped a-Si:H, even if a process margin of ±1 μm was considered. The Ni-silicide S/D was self-aligned to a gate with a 120-nm offset[3] when the gate insulator was wet-etched in a 10%-bufferd HF solution. Thus, the series resistance could be minimized. We applied this low resistance Ni-silicide to the fabrication of a-Si:H TFTs with an etch stopper (ES) (b) and a back-channel etched (BCE) (c).

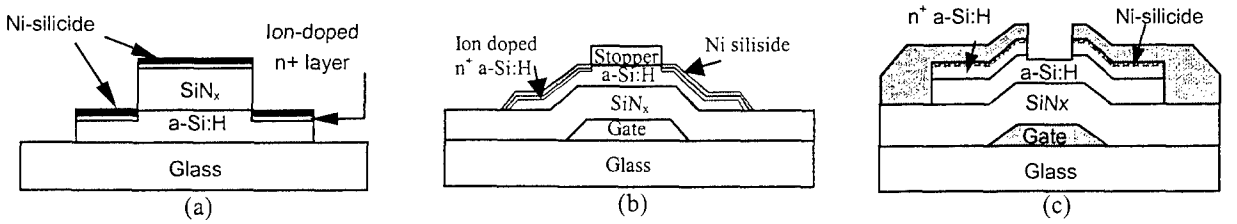

Figure 4. Cross-sectional views of the fabricated TFTs: coplanar a-Si:H (a), ES a-Si:H(b), BCE a-Si:H (c).

3.1. N^+ contact

Figure 5 shows the field effect mobility (μ_{fe}) for the a-Si:H TFT with different (Al and Ni) S/D contact materials. The field effect mobility was obtained in the saturation region. The field effect mobility increases with annealing temperature. The field effect mobility of the TFTs using Ni and Al S/D contacts increases with the same rate until 150°C annealing. This is due to the improvement in the contact resistance for the two a-Si:H TFTs[13]. However, at 200 °C annealing, the TFT mobility with Ni S/D contacts increases from 1.0 cm^2/Vs to 1.22 cm^2/Vs, while the Al contact showed a saturation in the mobility as shown in Fig. 5. This can be explained by lowering of contact resistance by the Ni-silicide formation. By measuring the drain current, I_D, in the linear region for the TFTs with different channel lengths, the Ni-silicide/n^+ a-Si:H contact resistance was obtained[14]. It decreases from $1.45\times10^5\ \Omega$ to $2.75\times10^4\ \Omega$ by increasing the annealing temperature from 150 °C to 240 °C. The Al-contacted TFT shows an increase in mobility at 220 °C in Fig. 5. But this is due to a hillrock formation[15] and Al penetration into n^+ a-Si:H degrades the off-state leakage current.

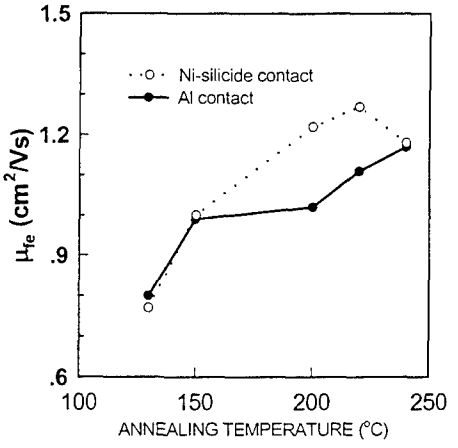

Figure 5. Changes in the field effect mobility of the a-Si:H TFTs with Ni-silicide and Al S/D contacts. W/L = 12 μm/6 μm.

3. 2. Coplanar a-Si:H TFT

Figure 6 shows the field effect mobility and transfer characteristics of the coplanar, self-aligned a-Si:H TFT at V_d= 0.1 V. The coplanar a-Si:H TFT exhibits a field effect mobility of 0.6 cm^2/Vs and a threshold voltage of 2 V. The field effect mobility and the threshold voltage were determined using the following expression for trans-conductance, g_m, in the linear region:

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d \approx 0.1} = \mu_{fe} C_i \frac{W}{L} V_d \qquad (2)$$

where, W/L, C_i, μ_{fe} are the ratio of channel width to length, gate insulator capacitance, and field effect mobility, respectively. The transfer characteristics in linear scale at V_d = 0.1V are inserted in Fig. 6. The field effect mobility and threshold voltage obtained from the inset of Fig. 6 are 0.58 cm^2/Vs and 2.5 V, respectively, using the relation in linear region at V_d= 0.1 V.

$$I_d = \mu_{fe} C_i \frac{W}{L} (V_g - V_T) V_d \Big|_{V_d \approx 0.1} \tag{3}$$

The major advantage of the new process is that in our TFT, gate and S/D Ni-silicide layers were formed simultaneously, resulting in a self-aligned structure. There is no overlap capacitance between gate and S/D, leading to a zero feed-through voltage. This is of interest since a LCD panel increases in size, making it more difficult to obtain a good quality LCD panel. The field effect mobility obtained from the trans-conductance and from the transfer characteristics at V_d = 0.1 V are almost the same. The field effect mobility, threshold voltage and the on/off current ratio of the coplanar a-Si:H TFT obtained from the present work are almost the same as those of typical inverted staggered a-Si:H TFTs. However, the present TFT has an advantage of small parasitic capacitance which is important for high performance large-area liquid crystal displays[4].

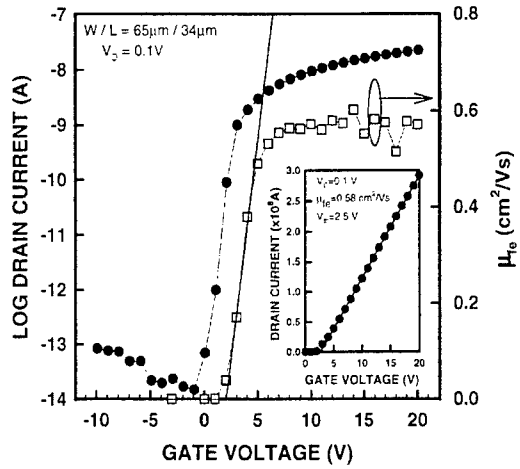

Figure 6. Plot of square root of the drain current versus gate voltage for an a-Si:H TFT using Ni-silicide and ion doped n^+ a-Si:H layers.

3. 3. 4-mask process for a-Si:H TFT array

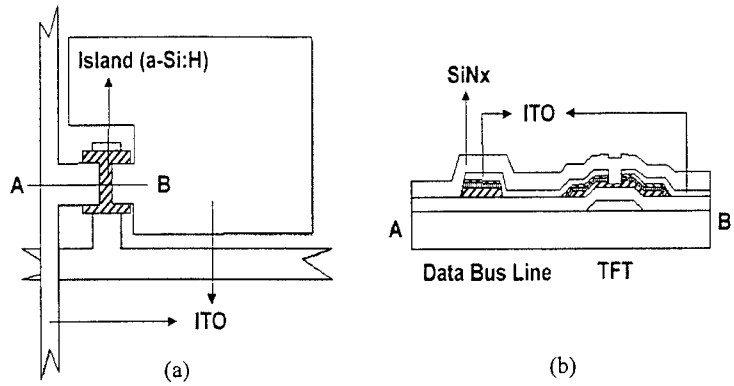

Figure 7. Schematic diagram of 4-mask TFT-arrays using Ni silicide: plan view (a), and cross-sectional view (b).

We developed a high performance, inverted staggered a-Si:H TFT, in which a thin Ni-silicide layer is inserted between an n^+ a-Si:H and an ITO. The Ni-silicide can be formed at as low as 230 °C. The fabricated TFT exhibited a field-effect mobility of 1.48 cm^2/Vs, a threshold voltage of 5.9 V, a subthreshold slope of 0.54 V/dec, an on/off current ratio of ~10^8 and an off-state leakage current of 3×10^{-14} A at the drain voltage of 5 V and the gate voltage of -5 V.

A 4 - mask TFT array process can be possible using the Ni-silicide. The fabrication procedure as follows: First, a metal film is deposited on the glass substrate (Corning 1737), then patterned for the gate bus lines (1st mask). Then, SiN_x, a-Si:H, n^+ a-Si:H are consecutively deposited by PECVD without breaking the vacuum and then the Ni layer is deposited on the top of n^+ a-Si:H and then patterned (2nd mask) for the islands and the data bus lines. The ITO was deposited by sputtering and then patterned for TFT channel and the data bus lines (3rd mask). Finally, a passivation layer of SiN_x was deposited and then it is patterned for the contact (4th mask) for the driver connections.

3. 4. Self-aligned a-Si:H TFT using a SiOF etch stopper

We used the low resistance Ni-silicide to the fabrication of a completely self-aligned a-Si:H TFT. Figure 8 shows the log I_d–V_g characteristic of the a-Si:H TFTs with different ion-stoppers, SiOF and SiN_x. The TFT with a SiOF ion-stopper has a field effect mobility of 0.52 cm^2/Vs and a threshold voltage of 4.72 V, while the TFT with a SiN_x ion-stopper has a field effect mobility of 0.42 cm^2/Vs and a threshold voltage of 4.30V. The better performance of the SiOF TFT appears to be due to the fluorine incorporation at the a-Si:H/SiN_x interface and the defect passivation by fluorine incorporation[2].

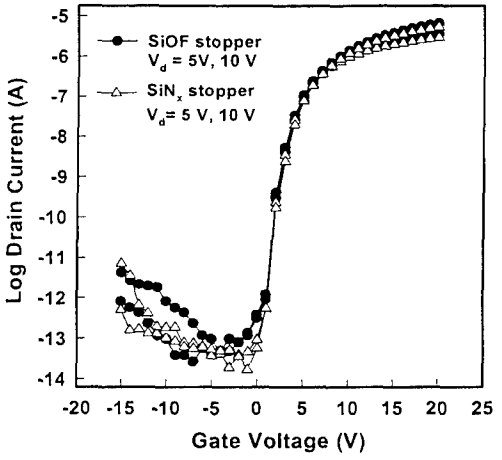

Figure 8. Transfer characteristics of the completely self-aligned TFTs.

Figure 9 shows the top and cross-sectional views of the pixel structure using a SiOF-ES. The SiOF acts as an interlayer also. The SiOF islands are formed in the TFT-regions and line-crossover regions for improving the TFT performance and reducing the line-capacitance, respectively.

The UXGA (1600×3×1200) and XGA (1024×3×768)-resolution TFT-arrays were simulated for the 3-different TFT structures of SiOF-ES, SiN_x-ES, and BCE types to compare the gate-pulse delay and the results were plotted in Fig. 9. Equivalent circuit models for a TFT-LCD can be found in the literatures [16-17]. The inset in Fig. 9 shows the simulated signal delays for the 3-different structures. The SiN_x thickness of the gate insulator was fixed at 300 nm. And the crossover area of the gate/data line was 10 μm × 8 μm. The dielectric constants of the SiN_x and SiOF were 7.4 and 3.4, respectively. The signal delay (99%-charging) for the SiOF-ES, SiN_x-ES, and BCE structures were 1.8 μs, 2.1 μs, and 2.6 μs in XGA array, and 2.2 μs, 2.6 μs, and 3.5 μs in UXGA array, respectively.

Thinning the gate insulator is important to decrease the threshold voltage of TFT and thus the driving voltage of TFT-LCD can be reduced. For bottom-gate a-Si:H TFTs, however, a thin gate insulator is unacceptable because thinning gate insulator leads to an increase in capacitance between the gate and data lines. In this case, a low dielectric constant SiOF layer that acts

as both the stopper and the line-interlayer can be much more appropriate for reducing the capacitance and thus the RC delay.

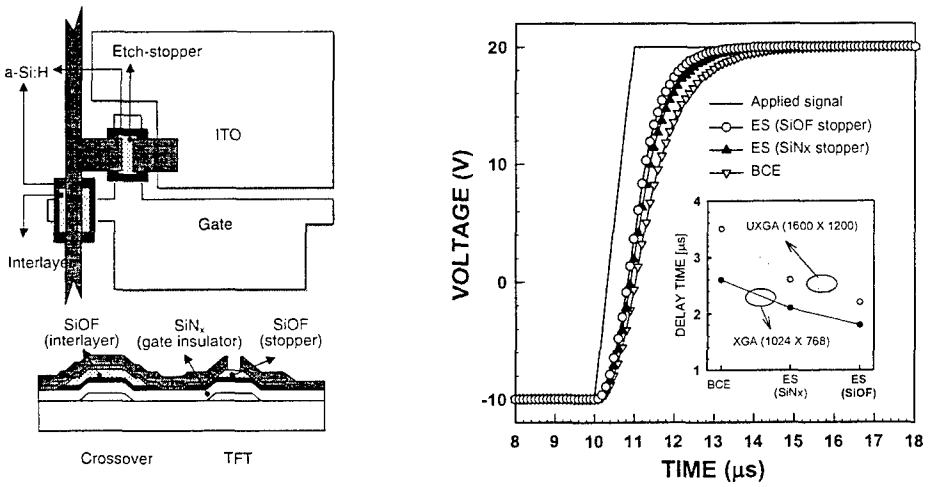

Figure 9. The plan and cross-sectional views of the pixel structure of a TFT-LCD for the application of a SiOF etch stopper (a), and the charging behavior of a pixel during gate pulse and the delay signal waveform for the three-different structures (b). A resolution of UXGA was used.

4. LOW TEMPERATURE POLY-SI TFT BY NI SMC IN AN ELCTRIC FIELD

4.1. Low temperature activation of S/D region

Figure 10 shows the Raman spectroscopy of a ELA poly-Si before (a) and after (b) an ion shower doping. The ion doping damages the lattice structure and thus an amorphous phase centered at 490 cm^{-1} appears after ion doping. Note that the Ni-silicide can be easily formed on a-Si:H than on poly-Si[18]. In our experiment, the poly-Si is amorphized after ion shower and this enhances the silicide formation. By using this method, S/D contact resistance can be reduced and thus a high performance ELA poly-Si TFT can be obtained without an addition activation of n^+ layer after ion doping.

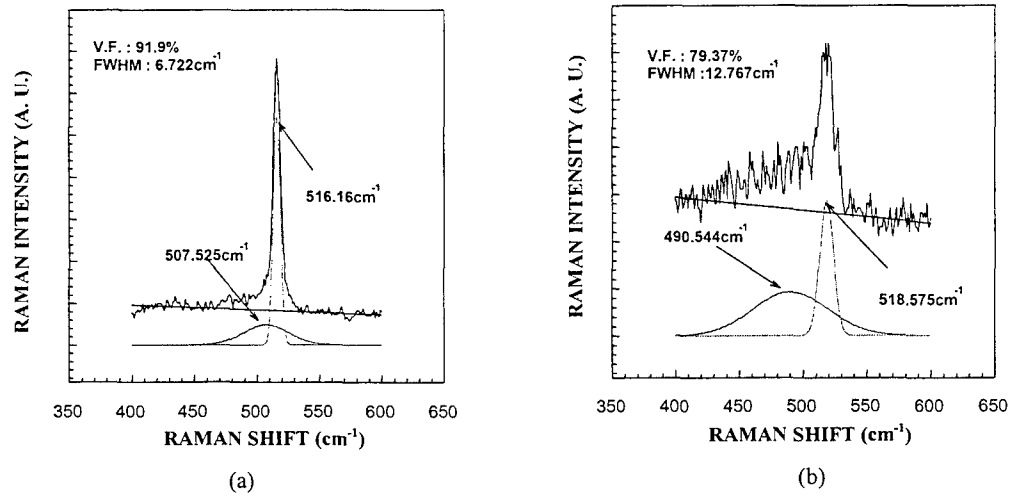

Figure 10. Raman spectra of the poly-Si before (a) and after ion shower doping (b).

4.2. High performance SMC poly-Si TFT

Poly-Si TFTs on glass substrate are of interest for active matrix liquid crystal displays (AMLCD's) and active matrix organic light emitting diodes (AMOLED's). The high field effect mobility (100 cm^2/Vs) of poly-Si TFT enables the integration of peripheral drive circuits on glass substrate and decreases the TFT area for display, thus realizing higher resolution and more compact display. A key step for a low temperature poly-Si TFT is to make a high mobility, uniform poly-Si film on glass substrate.

Recently, we developed a new crystallization method[12, 19] called a SMC. A-Si with Ni area density of $2 \times 10^{13} cm^{-2}$ can be crystallized by heating it for 10 minutes in a modest electric field[20]. It was found that the TFT performance improves with decreasing Ni density on the a-Si:H. But we need a critical density to make a complete crystallization over whole area[20]. Figure 11 shows the transfer characteristics of a SMC poly-Si TFT using an average Ni thickness of 0.15 Å. The off-state leakage current is 1.1×10^{-11} A/μm at the drain voltage of 5 V and the gate voltage of -6 V. The on-off current ratio is $> 7 \times 10^5$ at the drain voltage of 5 V. The TFT exhibited a field effect mobility of 120 cm^2/Vs, a threshold voltage of -1.5 V and a sub-threshold slope of 0.5 V/dec.

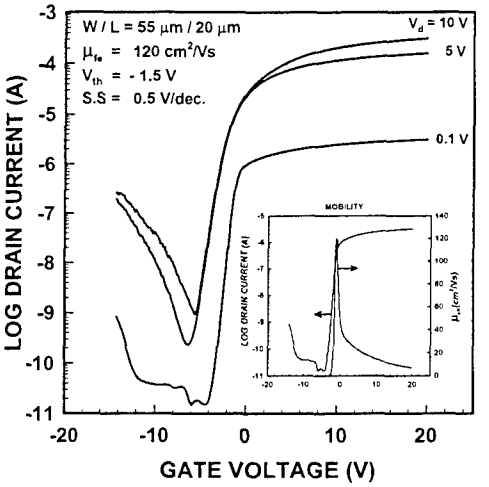

Figure 11. Transfer characteristics of a SMC poly-Si TFT using average Ni thickness of 0.15 Å. The inset shows its field effect mobility.

4.3. A comparison of a SMC poly-Si TFT with an ELA poly-Si TFT

The SMC in an electric field, a technique more compatible with batch processing than ELA, was developed for the low temperature poly-Si TFT-LCD[21].

Figure 12 shows the transfer characteristics for the poly-Si TFTs with a Ni-SMC poly-Si and an ELA poly-Si with a self-aligned coplanar structure. Both ELA and SMC poly-Si TFTs were fabricated by using the same process except for the crystallization method. The grain size of the ELA poly-Si was 400 nm, which was obtained through the optimization of laser intensity. The Ni-SMC poly-Si TFT exhibited a subthreshold slope of 0.6 V/dec and on/off current ratio of $\sim 1.1 \times 10^6$ at $V_d = 0.1$ V. The ELA poly-Si TFT exhibited a subthreshold slope of 0.5 V/dec and on/off current ratio of $\sim 2.8 \times 10^4$ at $V_d = 0.1$ V. The off-state leakage current of the SMC poly-Si TFT is $\sim 7 \times 10^{-12}$ A/μm at $V_d = 5$ V and $V_g = -6$ V and higher than that (2×10^{-12} A/μm) of an ELA poly-Si TFT. Both TFTs show similar tendency in subthreshold region and on region.

It is well known that poly-Si has many trap states in grain boundaries and these states take charge carriers and build up potential barriers to the flow of carriers. The presence of a potential barrier at a grain boundary and thus additional scattering leads to a field effect mobility degradation. The high density of trap states deteriorates a subthreshold slope, increases threshold voltage and leakage current. It is believed that the leakage current by the field-enhanced tunneling of electron from the valence band to the conduction band via grain boundary traps. But in the Ni MILC poly-Si TFT it is found

that the leakage does not depend on the Ni contamination in the poly-Si if it is not very high[22]. The Ni impurity on the off-state leakage current of the SMC poly-Si TFT is being studied in our lab and will be published.

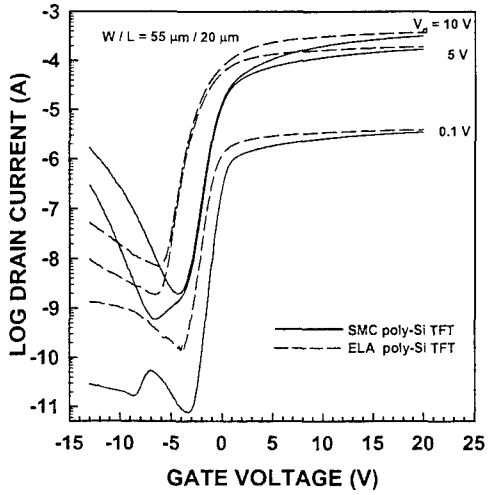

Figure 12. A comparison of a SMC poly-Si TFT with an ELA poly-Si TFT.

5. CONCLUSION

Low resistance Ni-silicides can be formed on a-Si:H at low temperatures less than 250°C and thus applied for high performance a-Si:H and poly-Si TFTs in various forms. The high field effect mobility a-Si:H TFT of > 1.4 cm^2/Vs has been obtained by using the low resistance Ni-silicide as contacts . We found that ion shower promotes the silicide formation for a TFT contact because the poly-Si was amophized by an ion shower. In addition the $NiSi_2$, having the same lattice structure as Si with only 0.4 % lattice constant difference, can be formed on a-Si at 350°C. The crystallization proceeds from these $NiSi_2$ precipitates. The crystallization of a-Si can be done at 500°C in 10 minutes in an electric field. A SMC poly-Si TFT having a similar TFT performance with an ELA-poly-Si TFT, has been developed.

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