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Metal-Induced Laterally Crystallized Polycrystalline Silicon: Technology, Material and Devices

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ABSTRACT

Polycrystalline silicon (poly-Si) has been obtained by low-temperature ($< 500^{\circ}\text{C}$), nickel-based, metal-induced crystallization (MIC) of amorphous silicon. Because crystallization outside of the nickel-covered regions is not only possible but also commonly utilized, the technique is more often called metal-induced lateral crystallization (MILC). Based on studies on the crystallization kinetics and material characteristics, a unified mechanism is proposed for MIC both under and outside of the nickel coverage. Conduction in MILC poly-Si is found to be anisotropic with respect to the MILC direction. While the material quality of MILC poly-Si is significantly better than that of solid-phase crystallized poly-Si, the performance of MILC poly-Si thin-film transistors (TFTs) is quite sensitive to and degraded by the inclusion of MIC/MILC interfaces in the device channel regions. When such interfaces are eliminated, excellent TFTs are obtained that can be used to realize high performance systems-on-panels, including sophisticated displays based on liquid crystals or organic light-emitting diodes. The application of MILC poly-Si is not limited to low-temperature electronics, it is found that high-temperature re-crystallization results in MILC poly-Si with material quality approaching that of single-crystal Si. Re-crystallized MILC poly-Si has been used to realize high performance piezo-resistors and TFTs for integrated sensor applications.

Keywords: Nickel, metal-induced crystallization, polysilicon, thin-film transistor, displays, low-temperature electronics.

1. INTRODUCTION

The mobile computing and communications market would not have been viable without the availability of portable, low power liquid crystal displays (LCDs). The demand for higher information content has been driving the switch from passive to active matrix LCDs. Low-cost production of such displays requires low-temperature (low- T) thin-film transistor (TFT) technologies that are compatible with the constraints imposed by the inexpensive but commonly used LCD glass substrates. Traditionally, this requirement has been fulfilled by using the low- T amorphous silicon (a-Si) TFT technology. However, the low field-effect mobility (μ_{FE}) of a-Si TFTs limits their applications to pixel switches within a display matrix. Clearly, a low- T polycrystalline silicon (poly-Si) technology for making TFTs with high mobility and low leakage current would be desirable for the realization of systems-on-panels (SOPs), integrating driver and other functional circuit blocks with the pixel transistors on the same glass panel.

Poly-Si with large crystallite grains has been obtained using a variety of techniques: rapid-thermal annealing (RTA) [1], Excimer laser crystallization (LC) [2], and solid-phase crystallization (SPC) [3]. RTA is a high temperature ($>600^{\circ}\text{C}$) process, resulting in films containing high densities of defects. By localizing the high temperature to the silicon layer, LC can be considered a "low- T " process. While it is capable of producing poly-Si films with low defect densities, it suffers from high initial setup cost and high process complexity. Conventional SPC is a relatively inexpensive batch process, though at around 600°C , the process temperature is still considered high.

Metal-induced crystallization (MIC) of a-Si has been proposed as a low- T crystallization technique for making high performance poly-Si TFTs [4]. MIC is superior compared to other low- T poly-Si technologies such as LC and SPC because unlike LC, it is a low-cost batch process and unlike SPC, better quality poly-Si thin films can be obtained.

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2. METAL INDUCED CRYSTALLIZATION

MIC of a-Si, amorphous germanium (a-Ge) or amorphous SiGe has been investigated with either double layers of metal and the amorphous semiconducting material or metal species implanted into Si or Ge. Studies showed that MIC could dramatically decrease the temperature necessary for the crystallization of a-Si and a-Ge. Recently, selective deposition of palladium or nickel (Ni) on a-Si thin films was found to induce crystallization of a-Si outside of the metal coverage (Fig. 1). This phenomenon is called metal-induced lateral crystallization (MILC) [5].

Thin a-Si films were deposited on oxidized Si wafers by low-pressure chemical vapor deposition (LPCVD) at 550°C. Silane (SiH_4) was used as the Si source gas. The deposition pressure was about 300mTorr. Ni films with thickness ranging from 5 to 10nm were deposited in a high-vacuum electron beam evaporator. Prior to loading the wafers into the evaporator, the native oxide on the a-Si films was removed by dipping the wafers in dilute HF. For patterned Ni samples, a lift-off process using photoresist was employed. The photoresist was patterned to expose selected regions of the a-Si thin film before the Ni evaporation. Ni deposited on the photoresist was removed together with the photoresist while Ni deposited on the a-Si was left behind. Crystallization heat treatment was done in N_2 in a conventional atmospheric pressure horizontal furnace.

The optical micro-graph of a sample heat-treated for 16 hours at 500°C is displayed in Figure 1A. Three distinct regions are visible: that with the darkest contrast (Area 1) was originally covered by Ni. This is surrounded by a region (Area 2) with the brightest contrast, which is in turn embedded in a gray region labeled Area 3. Typical Raman spectra obtained in regions equivalent to Areas 1, 2 and 3 in a sample heat-treated for 6 hours are presented in Figure 1B. The broad structure near 480cm^{-1} in the spectrum (Trace a) obtained in Area 3 indicates the film remained amorphous. Instead of the broad structure, sharp peaks near 520cm^{-1} were detected in the spectra obtained in Areas 1 (Trace b) and 2 (Trace c), indicating the a-Si in these two regions has been crystallized. This provides direct evidence that MILC and MIC have occurred in Areas 2 and 1, respectively [5]. The FWHM of the Raman peak obtained in Area 2 (MILC) is about 7.8cm^{-1} , smaller than the 8.3cm^{-1} obtained in Area 1 (MIC), indicating the average grain size in the MILC region is larger than that in the MIC region.

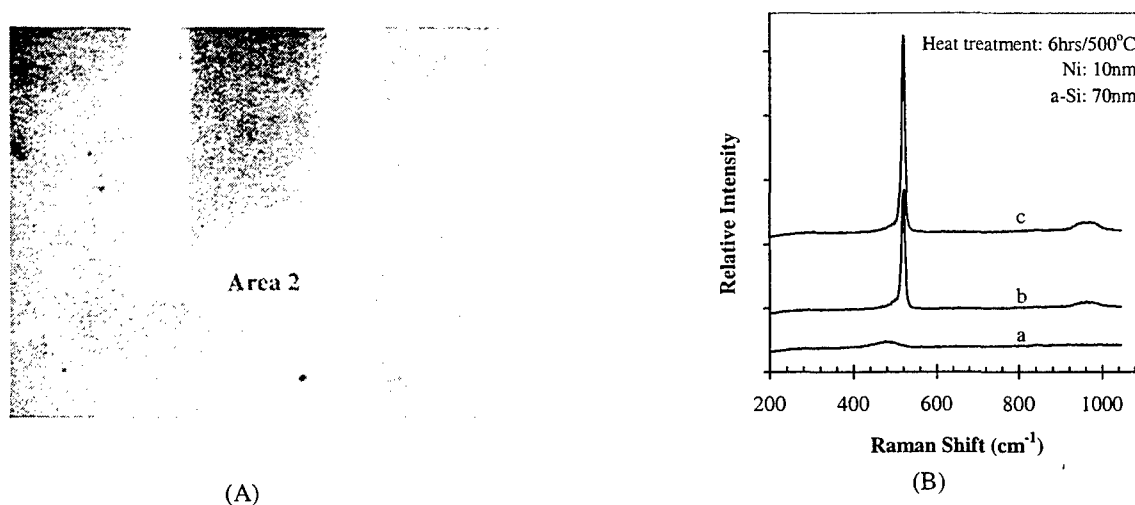


Figure 1. A) Optical micrograph of a sample with selectively deposited Ni on a-Si after heat treatment for 16 hours at 500°C. The 50 μm wide Ni-covered region (Area 1) is surrounded by a bright MILC region (Area 2). Area 3 is a-Si. B) The equivalent Raman spectra - Trace a: the a-Si region (Area 3), Trace c: the MILC region (Area 2) and Trace b: the Ni-covered region (Area 1).

The MILC rate, estimated by dividing the total MILC length by the total heat treatment time, is plotted in Figure 2 as a function of the reciprocal of the product of the absolute crystallization temperature and the Boltzmann constant. For a given temperature, a slightly lower MILC rate has been obtained on low-temperature oxide (LTO) coated glass than on oxidized silicon, with activation energy (E_a) of 1.97eV and 2.06eV [6], respectively.

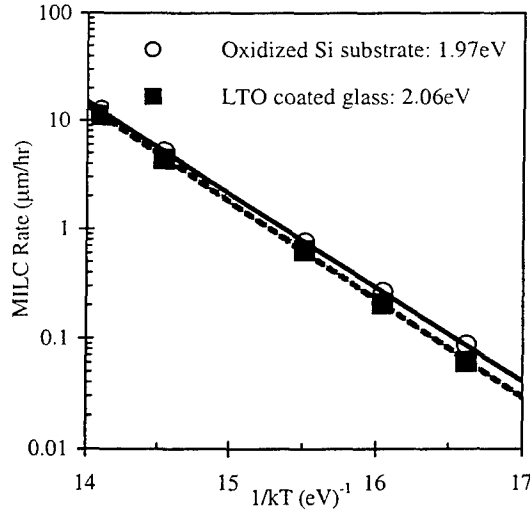


Figure 2. Dependence of the MILC rate on the reciprocal of “ kT ”, where “ k ” is the Boltzmann constant in eV/K and “ T ” is the heat-treatment temperature in K.

The MILC rate is shown in Figure 3 to decrease upon extended heat treatment. The continuous microscopic rearrangement of the atoms in the a-Si during the extended heat treatment is partially responsible for this downward drift of the MILC rate [7]. This is verified by the decrease in MILC rate (Fig. 3A) upon extended heat treatment of a-Si samples which have been pre-annealed for 70 hours at 500°C prior to the Ni deposition. Furthermore, it can be seen that the MILC rate ($\sim 1\mu\text{m/hr}$) after 70 hours of extended heat treatment of the samples and without the pre-annealing is about 20% slower than the initial MILC rate ($\sim 1.2\mu\text{m/hr}$) of the samples with the 70-hour pre-annealing. This indicates other mechanisms, in addition to the changing state of the a-Si, are needed to fully account for the decrease of the MILC rate upon extended heat treatment. It is shown in Figure 3B that after the removal of the original Ni coverage, the MILC rate became much smaller and decreased much faster upon extended heat treatment. This implies there is a supply of Ni to the crystallization front, possibly via a diffusion mechanism. In the absence of a source of Ni, Ni is gradually depleted from the crystallization front and eventually slows down the MILC rate.

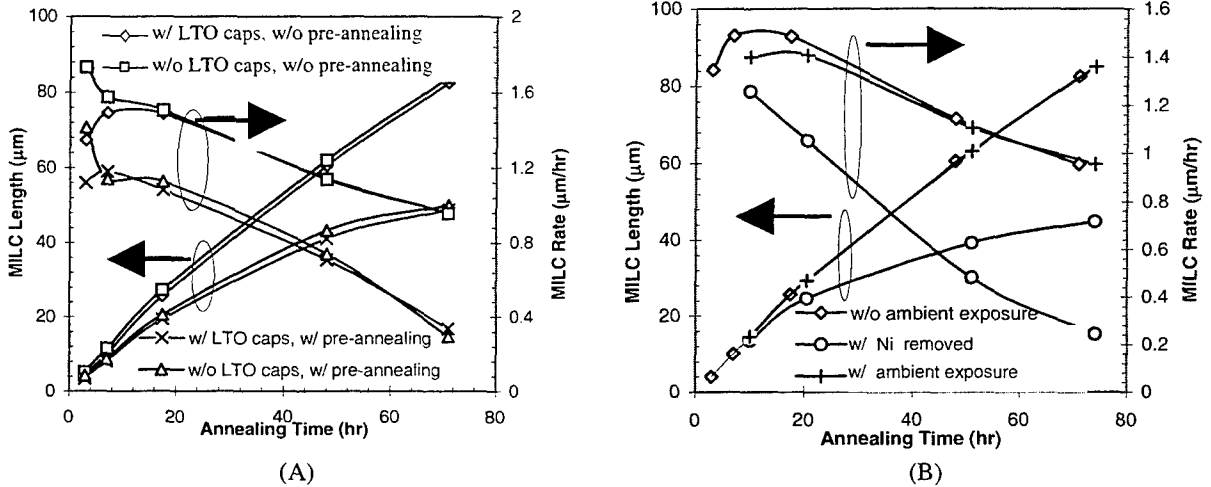


Figure 3. A) MILC length and rate with or without pre-annealing of a-Si. B) The dependence of the MILC length and rate on the heat treatment time, with or without the Ni source removed.

Ni distribution in the MIC, the MILC and the a-Si regions has been obtained using scanning secondary ion mass spectrometry (SIMS) [6]. A two-dimensional distribution of the integrated secondary Ni ion yield, expressed as brightness intensity, is plotted in Figure 4. As expected, the MIC region is the brightest, indicating the highest Ni concentration. Low

levels of Ni, as indicated by the scattered bright spots, have been detected in the MILC region. A dense population of bright spots also has been detected along the interface of the a-Si and the MILC regions, thus proving the MILC front is rich in Ni.

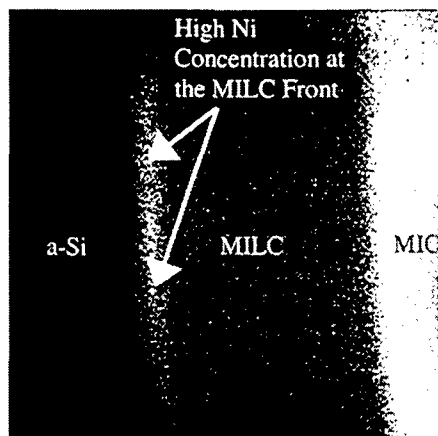
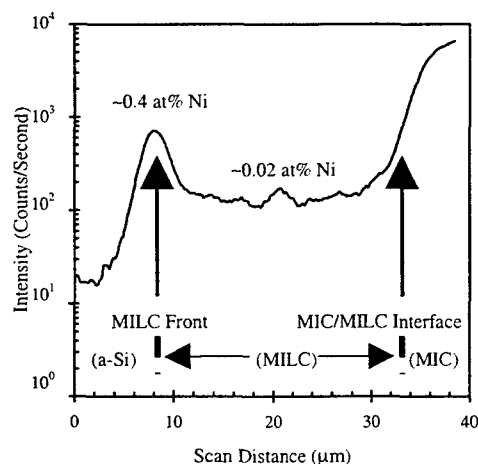
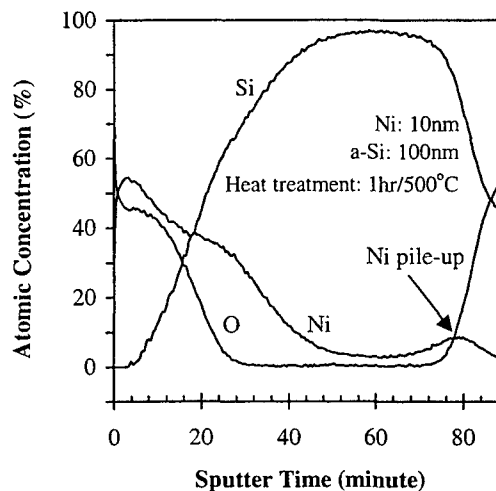


Figure 4. Two-dimensional distribution of Ni obtained by scanning micro-SIMS analysis of the MIC, the MILC and the a-Si regions. The Ni concentration is proportional to the brightness and the density of the spots. A high concentration of Ni, about 0.4 atom %, is observed at the MILC front.

The secondary Ni ion count across a line-scan is shown in Figure 5A [6]. It should be noted that the shape of this lateral Ni distribution is almost identical to that in the vertical direction shown in Figure 5B [5], obtained using x-ray photo-electron spectroscopy (XPS) in the MIC region.



(A)



(B)

Figure 5. A) Distribution of Ni across the MIC, the MILC- and the a-Si regions obtained by SIMS and B) XPS depth profiles of Si, Ni and O concentrations across an MIC region.

3. MECHANISM OF MIC

Ni induced MIC of a-Si occurs via a three-step process [5]: silicide formation, breakup of the silicide layer into small nodules, and transport of the silicide nodules through the a-Si film.

At the early stage of the MIC heat treatment, Ni readily reacts with the a-Si and converts itself into NiSi_2 . Nucleation and growth of small grains of Si crystal then take place randomly along the interface between the NiSi_2 and the underlying a-Si.

It would not be surprising that the nucleation was aided by the small lattice mismatch between NiSi_2 and crystalline Si. Further growth of the crystalline grains eventually leads to the puncturing and break up of the NiSi_2 layer. Subsequent to the break up, small nodules of NiSi_2 move away from the crystallized top region of the a-Si film. The diffusion of Ni through the nodules is responsible for the movement of the nodules away from the crystallized regions of Si into the a-Si region [8]. In the case of MIC, the fastest moving nodules will be found at the crystallization front, which is the interface between the crystallized Si and the a-Si. The slower moving nodules will be trapped inside the crystallized region, giving rise to the weak Ni XPS signal detected in the bulk of the film. Once the crystallization front reaches the bottom buried oxide, all remaining moving nodules are stopped, thus contributing to the small peak of Ni XPS signal (Fig. 5B) at the bottom interface of the crystallized silicon thin film.

Based on this model of MIC, MILC is easily explained. At the edges of a Ni covered region, certain number of the break-away NiSi_2 nodules will move laterally into the a-Si region not originally covered by Ni. As the nodules move laterally, any a-Si along the path of the moving nodules will be crystallized. As in MIC, slowly moving nodules will be trapped in the bulk of the MILC region, leaving only the fast moving nodules at the MILC crystallization front. The source of the secondary Ni ions detected by SIMS in the MILC region (Fig. 5A) is the Ni containing nodules trapped in the grain boundaries.

4. ANISOTROPIC CONDUCTION

Shown in Figure 6 are the transmission electron microscopy (TEM) and transmission electron diffraction (TED) micrographs of an MILC poly-Si region, in which elongated grains (Fig. 6B), separated by low-angle grain boundaries (GBs), are primarily aligned to the MILC direction. This relatively ordered and anisotropic micro-structure is very different from those in SPC, LPCVD and MIC poly-Si, in which random nucleation and homogenous grain growth lead to isotropic micro-structures. The TED micro-graph in Figure 6A taken in the MILC area indicates the grains are primarily (110)-oriented, while that in Figure 6C taken in the MIC area indicates a nearly random distribution of grain orientations [5].

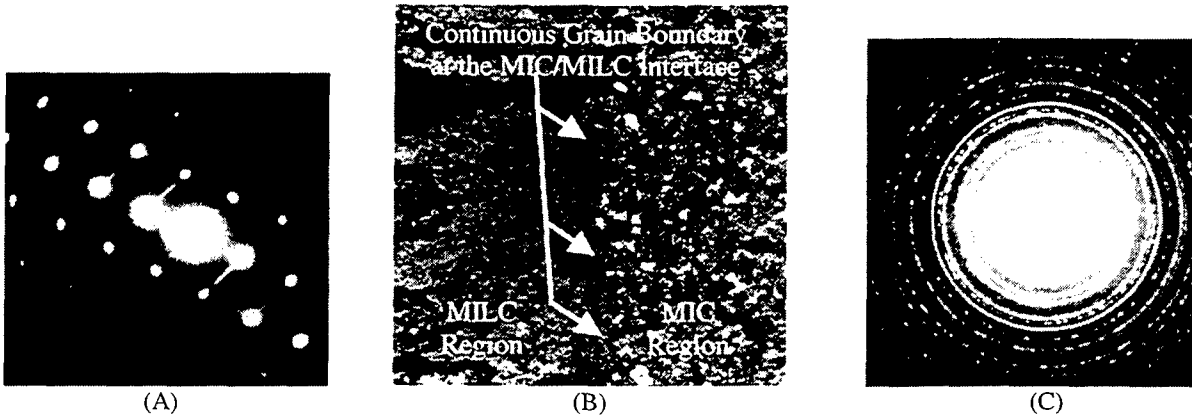


Figure 6. A) TED micro-graph in the MILC area, showing predominantly {110} orientation, B) TEM micro-graph showing elongated grains in the MILC region. A distinct grain boundary (MMGB) separates the MIC and the MILC regions, and C) TED micro-graph in the MIC area.

Arrhenius plots of ρ_t and ρ_p are shown in Figure 7B, where ρ_t and ρ_p denotes, respectively, the resistivity values for conduction parallel and transverse to the MILC direction. While linear fits can be obtained for both ρ_t and ρ_p for the lightly doped resistors, the distribution of the data for the more highly doped ones exhibits much increased influence of defect and/or GB scattering. Only in the low T range can approximate linear fits be obtained. Nevertheless, the extracted E_a is found to be inversely proportional to the doping concentration, agreeing with the GB trapping model. However, for both implant doses, higher E_a is obtained for ρ_t than for ρ_p , which is largely responsible to the observed resistivity anisotropy in MILC poly-Si [9].

The T -dependence of the resistivity anisotropy ratios (ρ_t/ρ_p) for the resistors is plotted in Figure 7A. For lightly doped resistors, ρ_t/ρ_p is quite large and consistently decreases with increasing T . Extrapolating the trend to high T yields a limiting value of 1.22. For heavily doped ones, ρ_t/ρ_p becomes relatively insensitive to T and slowly decreases from 1.25 to 1.19 with increasing T . In other words, for resistors operated at sufficiently high T , ρ_t/ρ_p approaches a similar value which is slightly larger than unity.

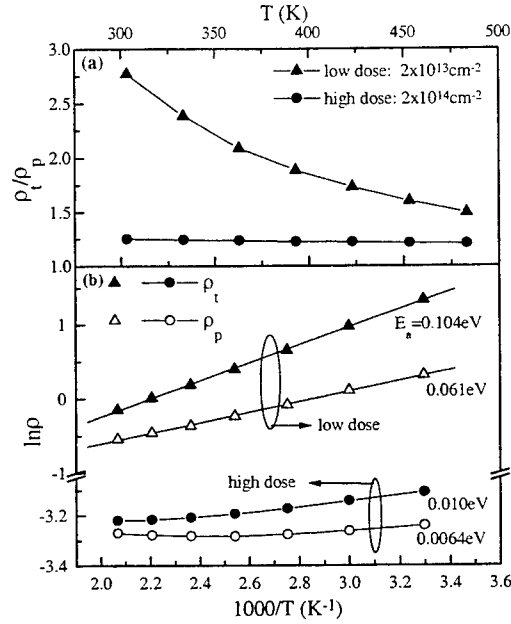


Figure 7. A) Temperature dependence of the resistivity anisotropy ratio, ρ_t/ρ_p , of MILC poly-Si at two different implant doses of 2×10^{13} (low) and $2 \times 10^{14} \text{ cm}^{-2}$ (high). B) Arrhenius plots of the corresponding ρ_t and ρ_p of the MILC poly-Si resistors. E_a of ρ_t and ρ_p for the low-dose resistors are, respectively, 0.104 eV and 0.061 eV. For high-dose resistors, the values extracted in the low T range are 0.010 eV and 0.0064 eV, respectively.

5. THIN-FILM TRANSISTORS

5.1 Device Types

Shown in Figure 8 is a micro-graph of two collided MILC regions obtained using secondary electron microscopy (SEM) in the orientation imaging mode. Also labeled in the Figure are the three major grain boundaries transverse to the MILC direction. Two of these are the MMGBs, located at the intersections of the MIC and the MILC regions. The remaining one, dubbed LLGB, is located at the intersection of the two MILC regions. SIMS (Fig. 5A) reveals that while the Ni concentration is relatively low within the MILC region, it is higher in the LLGB and still higher in the MMGBs [6].

Depending on which of these GBs are included in the channel region of a device, five different kinds of MILC TFTs can be implemented [10]. In the nomenclature used in Figure 8, each type of MILC TFT is uniquely identified by a preceding “nml” triplet. Each n, m or l takes on the value of either 1 or 0, indicating respectively the presence or absence of the corresponding transverse grain boundary. Using this nomenclature, a “111”-MILC TFT is a device with an LLGB in the middle of the channel and the MMGBs self-aligned to the edges of the gate electrode. A “110”-MILC TFT is an offset MILC-TFT [11] with one MMGB separated from the drain metallurgical junction and a “000”-MILC TFT [10] is a device without any of the three transverse grain boundaries and with the lowest concentration of Ni remaining in the active channels.

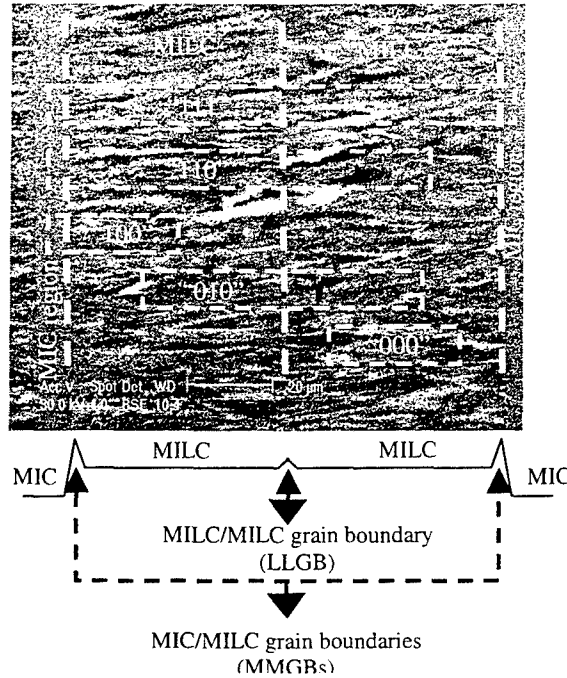


Figure 8. SEM micro-graph showing both MIC and MILC regions. A total of three GBs (two MMGBs and one LLGB) transverse to the MILC direction can be identified. The active areas of the five possible MILC TFTs are delineated by the five rectangular boxes superimposed on the micro-graph.

5.2 “111”-MILC and SPC TFTs

Compared to the processing of SPC TFTs, an additional masking step for Ni deposition is required for the realization of all but the “111”-MILC TFTs. Consequently, SPC and “111”-MILC TFTs, requiring similar process complexities, are compared. The threshold voltages (V_{th}) of the devices are defined as the gate voltages (V_g) required to achieve a normalized drain current (I_d) of $(W/L) \times 10 \text{ nA}$ at a specified drain voltage (V_{ds}), where W and L are the channel width and length, respectively. μ_{FE} was extracted from the maximum trans-conductance (g_{max}). As verified by the current-voltage (IV) characteristics presented in Figure 9, the performance of the MILC-TFTs is indeed superior to that of the SPC-TFTs.

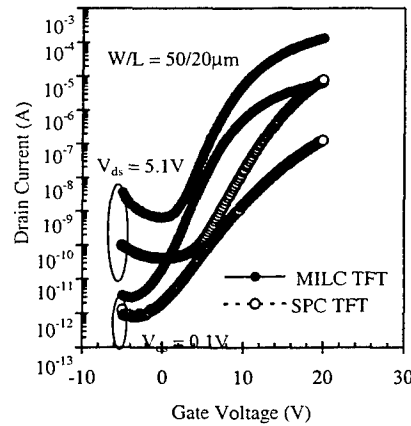


Figure 9. Transfer characteristics of “111”-MILC and SPC TFTs.

A comparison of the relevant device parameters of the two kinds of devices is summarized in Table I. Clearly, the MILC-TFTs have lower V_{th} , smaller sub-threshold slope (S), and higher μ_{FE} . However, the minimum current (I_{min}), which is a measure of the TFT leakage current, is higher for “111”-MILC [12].

Table I. Comparison of the relevant device parameters of “111”-MILC and SPC TFTs.

	V_{th} (V)	S (V/dec)	μ_{FE} (cm ² /Vs)	I_{min} (pA)
“111”-MILC TFT	6.2	1.2	74	2.9
SPC-TFT	15.6	3.3	5	0.8

5.3 Effects of MIC/MILC Interface on the Performance of “111”-MILC TFTs

Because MIC, instead of MILC, occurs in the source and drain (S/D) regions of “111”-MILC TFTs, continuous MMGBs [3] are formed which are “self-aligned” to the edges of the gate electrode. For TFTs employing self-aligned S/D doping, these MMGBs overlap the S/D metallurgical junctions (Fig. 10A) and fall within the corresponding depletion regions. Because of the overlap of the MMGBs and the S/D junctions at both ends of the channel, the MMGB traps are readily filled with charge carriers supplied by the S/D. The resulting MMGB energy barriers, the height of which is a function of the trap densities, extend into the channel region. This is depicted in Figure 10B. Since a higher V_g is required to achieve surface inversion in the regions with the MMGB barriers, it is equivalent to adding two high- V_{th} MMGB “transistors”, in series, to both sides of the intrinsic MILC transistor. This is depicted in Figure 10C.

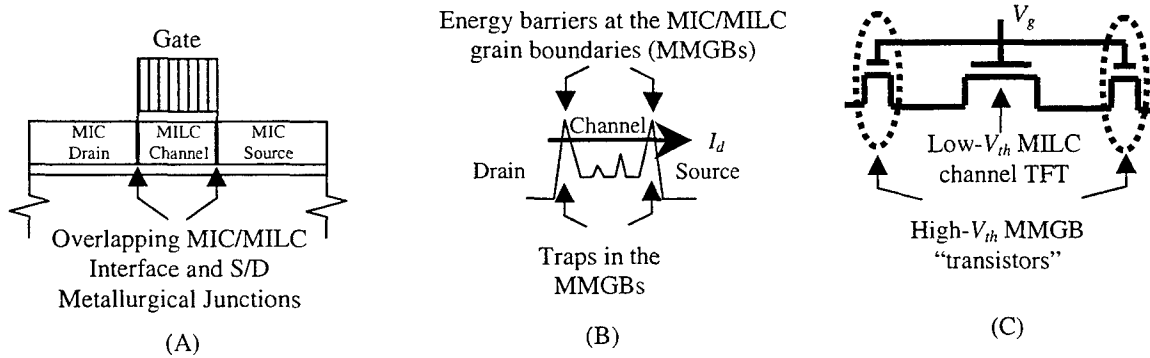


Figure 10. A) Schematic cross section of a “111”-MILC TFT showing the MMGBs self-aligned to the S/D metallurgical junctions, B) the energy barriers near the S/D metallurgical junctions and C) the device model at low V_{ds} .

While “111”-MILC TFTs are better than their SPC counterparts in many device performance measures, they suffer from higher leakage current [12], higher effective V_{th} [13], reverse short channel effect (R-SCE) [14] and lower drain breakdown voltage (kink effect) [15]. The cause of the degradation has been traced to the superposition of the MMGB, with its high densities of defects, and the depletion region of the drain junction, with its high electric field.

The leakage current and its sensitivity to L have been measured for both “111”-MILC and SPC TFTs. The leakage current of “111”-MILC TFTs is not only higher (Fig. 9) but also more sensitive to L scaling (Fig. 11A) than that of SPC-TFTs [12].

When an MMGB coincides with any one of the metallurgical junctions, it becomes part of the channel. The high density of grain boundary trap states effectively raises the local, hence also the overall, V_{th} of the device. Only by removing the MMGBs from both junctions can one effectively reduce the V_{th} . Shown in Figure 11B is the dependence of I_d on V_g of a) a “111”-MILC TFT, b) a “110”-MILC TFT with the MMGB offset from the drain-junction and c) a “010”-MILC TFT with the MMGBs offset from both source and the drain junctions. Clearly, the I_d - V_g characteristics and the apparent V_{th} values of the first two devices are almost identical, while the V_{th} value of the last device, with the double-sided offset, is clearly smaller [13].

However, it should be noted that the difference in this V_{th} is only apparent and does not lead to an increase in I_d at sufficiently high V_g . This is because an MMGB has a very small lateral extent, hence can be considered as a device with a

very short channel length, albeit with a higher V_{th} . While conduction at low V_g is limited by the high- V_{th} MMGB TFT, it is limited at high V_g by the resistance of the intrinsic MILC channel TFT, which is common to all three device structures.

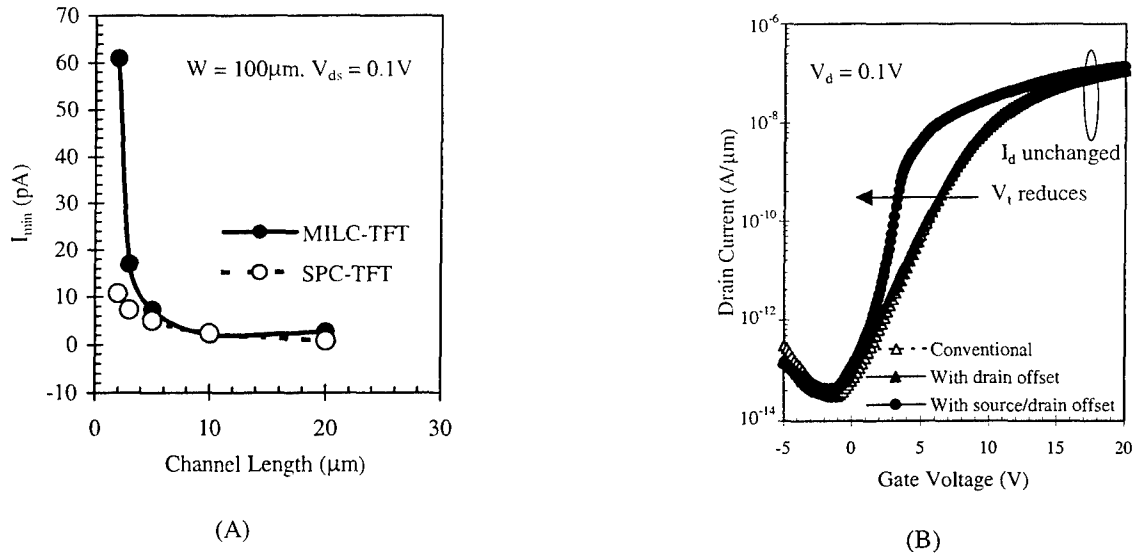


Figure 11. A) I_{min} vs L for N-channel “111”-MILC and SPC TFTs. B) I_d - V_g characteristics of the three different kinds of MILC TFTs: conventional, drain offset, and source/drain offset denote, respectively, “111”-, “110” and “010”-MILC TFTs.

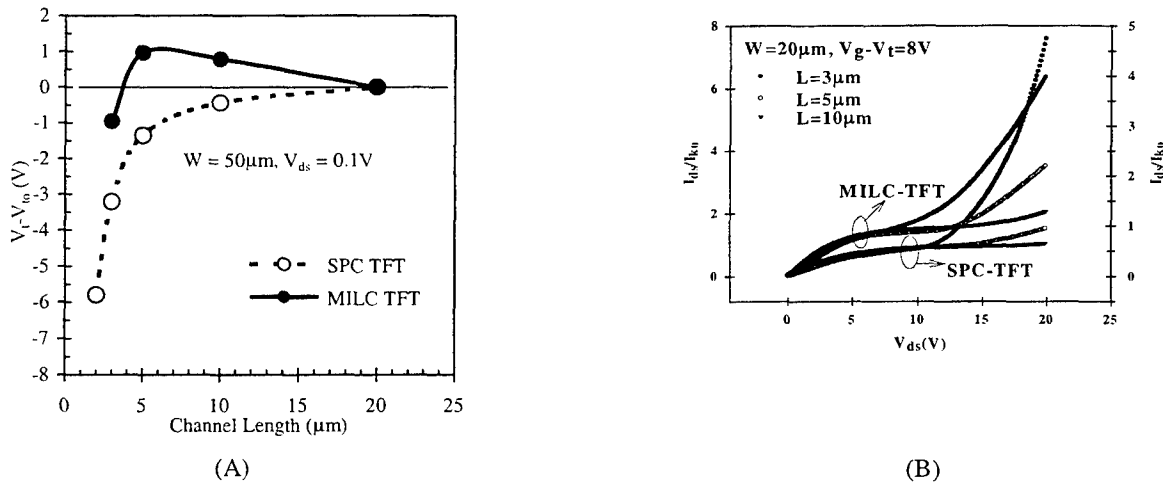


Figure 12. A) Comparison of the V_{th} scaling behavior of “111”-MILC and SPC TFTs. R-SCE is evident in the “111”-MILC TFTs. Only changes in V_{th} are plotted, with V_{tho} denoting the threshold voltage measured on the transistors with the longest channel lengths. B) Normalized output current characteristics of “111”-MILC and SPC TFTs at common gate drive. ‘ I_{ko} ’ is the drain current at the onset of soft drain breakdown (kink effect).

Shown in Figure 12A is a comparison of the L dependence of the V_{th} of “111”-MILC and SPC TFTs, It can be observed that while V_{th} of SPC TFTs decreases monotonically with L , that of “111”-MILC TFTs initially increases with L before rolling off at $L \approx 5 \mu m$, thus manifesting R-SCE [14]. When L of the intrinsic MILC transistor is reduced, a larger fraction of the channel region comes under the influence of the MMGB energy barriers, thus raising the V_{th} . Further reduction of L leads to drain-induced barrier lowering (DIBL) and conventional SCE takes over, resulting in a reduction in V_{th} with L .

Substrate current resulting from a sufficiently large V_{ds} is known to lower V_{th} via a modulated body potential. This is manifested as current kinks in the I_d - V_{ds} curves. In Figure 12B, I_d normalized by the drain current at the kink (I_k) is plotted

against V_{ds} . Because of the overlap of the defective MMGB and the high-field junction, V_{ds} at which the “kink” occurs, denoted by V_k , is lower in “111”-MILC than in SPC TFTs [15].

5.3 Metal-Induced Unilaterally Crystallized Polycrystalline Silicon

Employing metal-induced unilateral crystallization (MIUC) results in the formation of “000”-MILC TFTs (also denoted as MIUC TFTs) with the removal from the edges of and within the channel all major grain boundaries - including the MMGBs - transverse to the drain current flow [10]. Schematics of the “000”-MILC TFT, showing the associated channel potential variation in the sub-threshold regime, are shown in Figures 13A. For comparison, similar schematics for “111”-MILC TFTs are shown in Figure 13B.

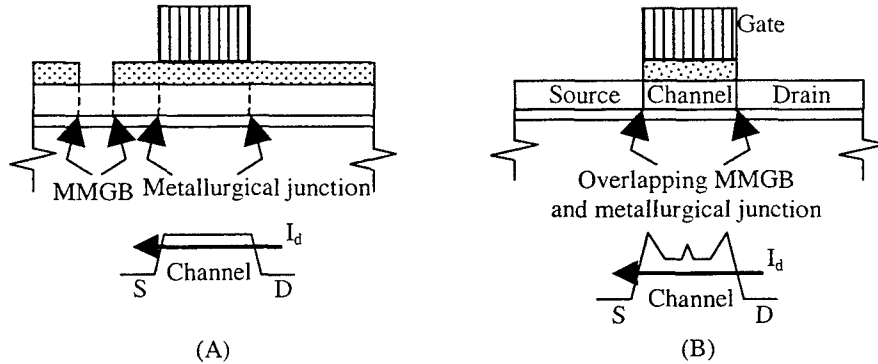


Figure 13. Schematics of the channel potential profiles of (A) a “000”-MILC TFT showing the MMGBs offset from the metallurgical junctions and (B) a “111”-MILC TFT showing the MMGBs overlapping the metallurgical junctions.

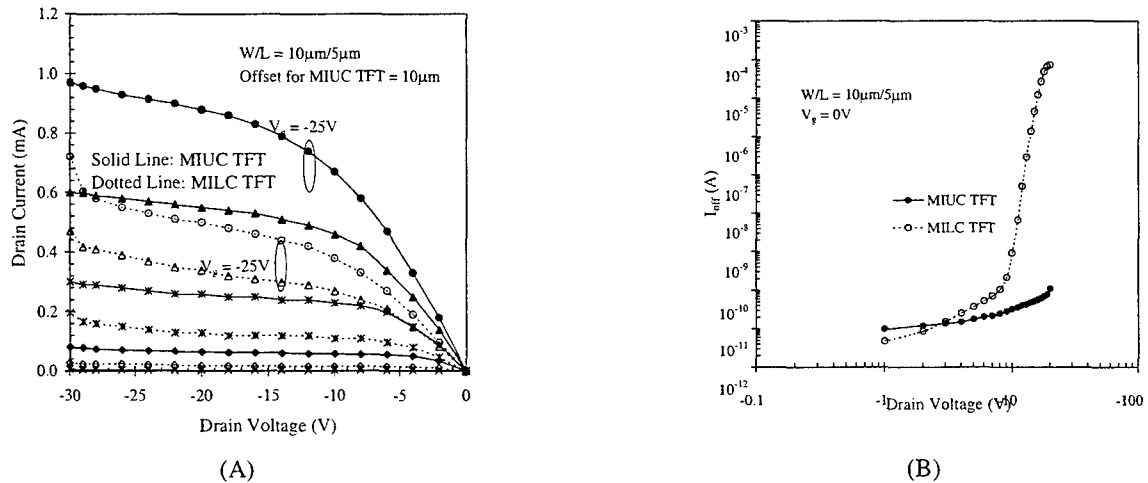


Figure 14. A) I_d dependence on V_{ds} from $V_g = -5\text{V}$ to -25V at -5V interval for p-channel MIUC (solid lines) and “111”-MILC (dotted lines) TFTs. Earlier drain breakdown can be clearly observed in the conventional MILC TFTs. B) Leakage current (I_{off}) dependence on V_{ds} .

Compared to the conventional bilaterally crystallized “111”-MILC TFTs, “000”-MILC TFTs are shown to have higher electron and hole μ_{EF} (Table II), higher drive current and better immunity to early drain breakdown (Fig. 14A), significantly reduced leakage current (Fig. 14B), as well as much improved spatial uniformity of device parameters (Fig. 15). All of these positive attributes make “000”-MILC TFTs particularly suitable for SOP applications requiring low-temperature processed TFTs over a large area.

Table II. Comparison of the device parameters of both n- and p-type MIUC ("000"-MILC) and MILC TFTs.

	N-type		P-type	
	"000"-MILC	"111"-MILC	"000"-MILC	"111"-MILC
μ_{EF} (cm ² /Vs)	78	70	98	75
V_{th} (V) @ $ V_d = 5V$	3.0	3.8	-4.2	-5.7
S (V/decade)	1.1	1.4	1.0	1.5
I_{off} (pA/ μ m) ($ V_{ds} = 5V$)	1.8	17	0.8	470
I_{on}/I_{off} ($ V_{ds} = 5V$)	1.4×10^7	9.3×10^5	3.4×10^7	3.6×10^4

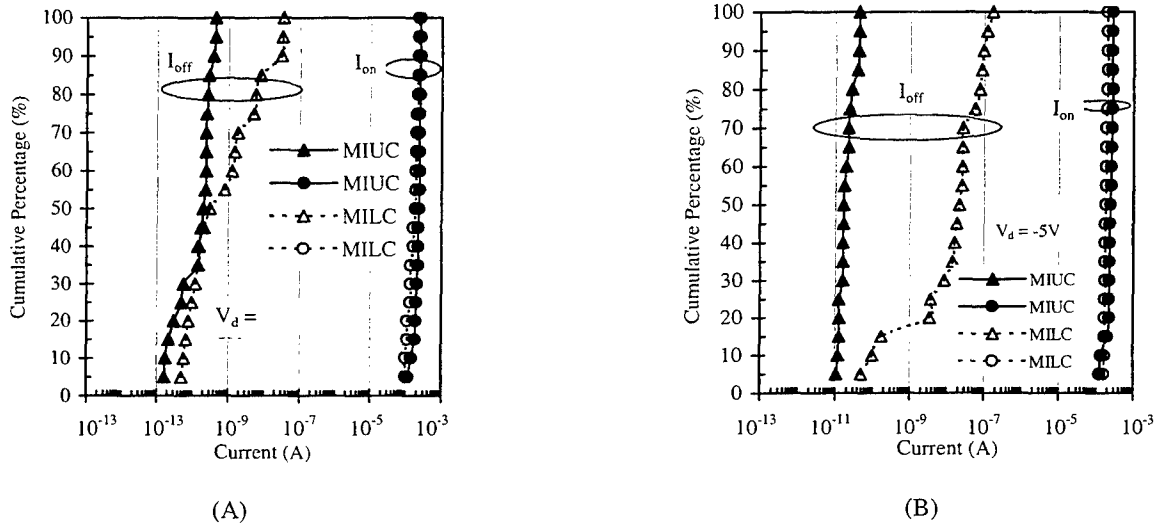


Figure 15. Statistical distributions of I_{on} and I_{off} for (A) n-type and (B) p-type MIUC ("000"-MILC) and "111"-MILC TFTs with $W/L = 10/5\mu$ m.

6. RE-CRYSTALLIZED MILC POLYCRYSTALLINE SILICON

Outside of flat-panel displays, hence free from the low temperature constraint, high temperature processed poly-Si devices have been employed in other important applications such as micro-electro-mechanical systems (MEMS) [16] and 3-dimensional (3D) integrated circuits (ICs) [17]. Early work on the re-crystallization (RC) of conventional low-pressure chemical vapor deposited (LPCVD) poly-Si thin films showed that high temperature processing generally led to a small amount of grain growth and limited improvement in the crystallinity of poly-Si. This occurs because poly-Si has a higher free energy than single-crystal Si, and heating provides the necessary thermal activation energy required for the micro-structure transformation.

Compared to the micro-structure of conventional poly-Si with random fine grains, that of MILC poly-Si consists of relatively ordered elongated grains separated by low-angle grain boundaries (GBs) [5]. A high- T anneal leads to RC of MILC poly-Si and significant material enhancement [18]. The improvement can be traced to the evolution of the unique grain structure of MILC poly-Si during the high- T anneal. The longitudinal grains (Fig. 6B) are no longer discernable in the TEM micro-graph (Fig. 16) of the RC-MILC poly-Si.

Shown in Figure 17A is the dependence of the room temperature resistivity (ρ) on the doping concentration (N_A) of MILC poly-Si, LPCVD poly-Si and single-crystal Si. With a slope ($\delta\rho/\delta N_A$) of -5.4 decades/decade, ρ of the conventional fine-grain poly-Si exhibits the most sensitive dependence on N_A . At -3.0 decades/decade, the slope for low- T MILC poly-Si is significantly reduced, thus reflecting a reduced trap density and a considerable improvement in the material quality relative

to conventional poly-Si. After a high- T anneal, the slope of -1.0 decade/decade for high- T MILC poly-Si is only slightly larger the -0.77 decade/decade reported for single-crystal Si [19]. This result is consistent with the TEM observation that the material quality of high- T MILC poly-Si approaches that of single-crystal Si.

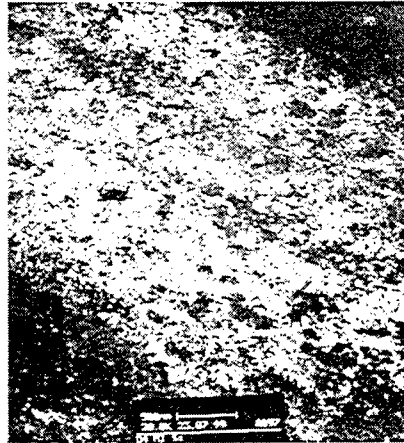
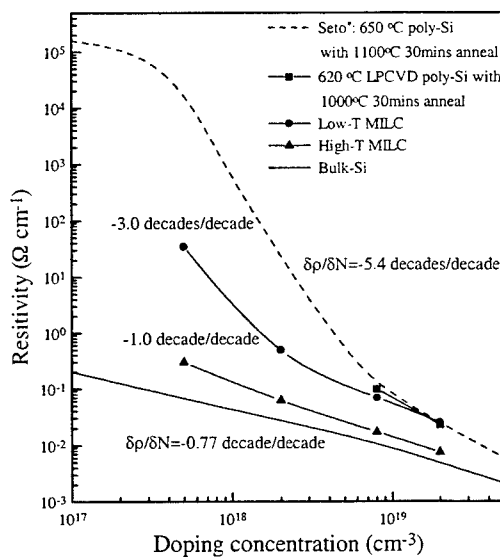
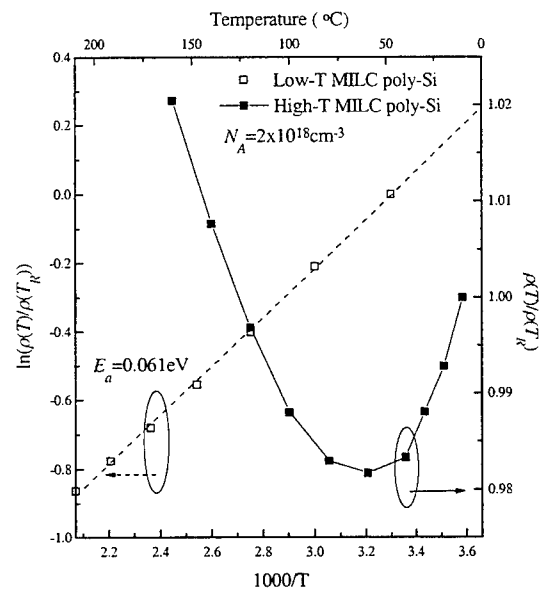


Figure 16. Typical TEM micro-graph of RC-MILC poly-Si. Distinct elongated grains are no longer discernable, leaving only long-range stress-induced and short-range micro-defect induced contrast variations.



(A)



(B)

Figure 17. A) The dependence of the room temperature resistivity on doping concentration for LPCVD poly-Si, bulk Si and low- and high- T MILC poly-Si. B) The temperature dependence of ρ of both low- and high- T MILC poly-Si with the same doping concentration of $2 \times 10^{18} \text{ cm}^{-3}$.

Additional evidence of the good crystallinity of high- T MILC poly-Si was obtained by studying the T dependence of ρ . The data are presented in Figure 17B for both low- and high- T MILC poly-Si resistors, implanted with the same boron dose of $8 \times 10^{13} \text{ cm}^{-2}$. Clearly, ρ for low- T MILC poly-Si exhibits an exponential dependence on $1/T$, with E_a of 0.061 eV. This behavior is consistent with the mechanism of thermionic emission over GBs, commonly used to model conduction in

conventional poly-Si. On the other hand, the behavior of the high- T MILC poly-Si resistor is rather more complicated. In the low T range, ρ still depends weakly exponentially on $1/T$ as in low- T MILC poly-Si, though with a significantly reduced E_a of 0.0043eV. However, as T is increased beyond $\sim 60^\circ\text{C}$, the dependence is reversed, with ρ increases with increasing T . This turn-around indicates that instead of thermionic emission over the GBs, intra-grain phonon scattering, which controls the conduction behavior in bulk-Si at elevated T , also appears to dominate that of high- T MILC poly-Si.

The piezo-resistive effect of boron-doped RC-MILC poly-Si [20] has been characterized and the longitudinal gauge factor (k) compared to those of LPCVD and LC poly-Si (Figure 18). In the N_A range from 5×10^{17} to $2 \times 10^{19} \text{ cm}^{-3}$, k of RC-MILC poly-Si typically varies from 43 to 55. Not only are these values significantly larger than those measured in conventional LPCVD poly-Si (30-40 [21], 24-20 [22] and 20-26 for the control samples), they are even better than the 50-35 [22] reported for LC poly-Si.

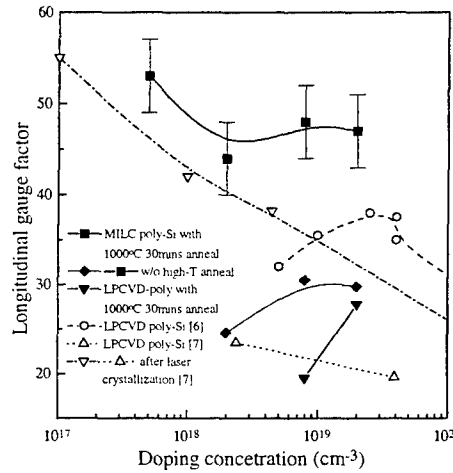


Figure 18. Longitudinal gauge factor vs. doping concentration for boron-doped MILC poly-Si. Results of conventional LPCVD poly-Si, the control samples and LC poly-Si are included for comparison.

The greatly improved material and electrical properties also make it possible to fabricate high performance active electronic devices. Typical TFT parameters of low- and high- T MILC TFTs, including μ_{FE} , V_{th} , S , minimum I_{off} , I_{on}/I_{off} are summarized and compared in Table III. It is worth noting that while the maximum I_{on}/I_{off} of both low- and high- T MILC TFTs exceed 10^7 , only for the high- T devices can this ratio still exceed 10^7 at more practical biased conditions, such as $|V_{ds}| = 5\text{V}$ and $|V_g| = 5\text{V}$.

Table III. Comparison of typical TFT parameters of low- and high- T MILC devices.

	N-type		P-type	
	Low- T	High- T	Low- T	High- T
$\mu_{EF} (\text{cm}^2/\text{Vs})$	70	150	90	100
$V_{th} (\text{V}) (V_{ds} = 0.1\text{V})$	5.0	3.4	-6.0	-3.8
$S (\text{V/decade})$	0.35	0.33	0.40	0.28
Min. $I_{off} (\text{pA}/\mu\text{m}) (V_{ds} = 5\text{V})$	2.0	1.7	1.6	1.6
Max. $I_{on}/I_{off} (V_{ds} = 5\text{V})$	1.3×10^7	3.4×10^7	1.6×10^7	2.3×10^7
$I_{on}/I_{off} @ (V_{ds} = 5\text{V}, V_g = 5\text{V})$	5×10^6	3.2×10^7	1.0×10^6	1.5×10^7

7. CONCLUSION

Polycrystalline silicon (poly-Si) has been obtained by low-temperature ($< 500^{\circ}\text{C}$), nickel-based, metal-induced lateral crystallization (MILC) of amorphous silicon. MILC is superior compared to other low-temperature poly-Si technologies such as laser crystallization (LC) and solid-phase crystallization (SPC) because unlike LC, it is a low-cost batch process and unlike SPC, better quality poly-Si thin films can be obtained. Anisotropic grain growth in MILC poly-Si leads to anisotropic conduction with respect to the MILC direction. While the material quality of MILC poly-Si is significantly better than that of SPC poly-Si, the performance of MILC poly-Si thin-film transistors (TFTs) is quite sensitive to and degraded by the inclusion of MIC/MILC interfaces in the device channel regions. When such interfaces are eliminated using metal-induced unilateral crystallization, excellent TFTs are obtained that can be used to realize high performance systems-on-panels, including sophisticated displays based on liquid crystals or organic light-emitting diodes. The application of MILC poly-Si is not limited to low-temperature electronics, it is found that high-temperature re-crystallization (RC) results in MILC poly-Si with material quality approaching that of single-crystal Si. RC-MILC poly-Si has been used to realize high performance piezo-resistors and TFTs for integrated sensor applications.

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