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EPITAXIAL TERNARY AND QUATERNARY III-V ANTIMONIDE SUBSTRATES

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Abstract: Modified liquid-phase epitaxy (LPE) techniques can be adapted for the growth of relatively thick (50 to 500 micron) epitaxial layers of ternary and quaternary III-V antimonide alloys, including InAsSb, InGaSb, AlGaAsSb, InGaAsSb, and InAsSbP. These structures can function as 'virtual' substrates with adjustable lattice constants for epitaxy of various optoelectronic devices such as mid-infrared photodiodes. A variety of substrate structures can be realized either by effecting gradual, continuous compositional grading of thick epilayers, or by growing multilayers with abrupt but incremental compositional changes between adjacent layers. Both approaches can be combined with selective removal of the seeding substrate and wafer bonding techniques. Low-defect alloy substrates with increased functionality, and with lattice constants and bandgaps significantly different than available with binary compound wafers (e.g., InAs or GaSb), appear feasible.

1. Introduction and Background

'Customized' substrates comprised of ternary and quaternary III-V compound alloys—in the form of either thick, self-supporting structures or else as epilayers transferred from the seeding substrate and bonded to a surrogate substrate—would enable much new device technology for mid-infrared optoelectronics. Such alloy substrates may also be useful for high-speed electronics. In particular, the III-V antimonide-based compound semiconductors (ABCS) have a wide range of bandgaps and valence or conduction band offsets in their heterojunctions, and extremely high electron mobilities. Consequently, the low-bandgap III-V antimonides are of increasing interest for infrared (2- to 12-micron wavelength) detectors, LEDs, and laser diodes; high-frequency (>100 GHz) analog, digital, and mixed analog / digital circuits with extremely low power consumption (< 1 fJ per operation) and low power supply voltage levels (< 1 V); and novel devices that operate in the THz to IR frequency range [1]. There is an acute need for improvements in substrate technology to facilitate epitaxial growth of these materials.

Compared to conventional elemental or binary compound substrates such as silicon or GaAs wafers—which are of invariant lattice constant and bandgap for a given temperature, alternative substrates made of ternary or quaternary alloys provide one or two extra degrees of freedom for 'tuning' the lattice constant and/or bandgap. The additional latitude in selecting the lattice constant and bandgap of the substrate would open up new device designs and applications that until now have been severely hindered by certain materials limitations. For example, the performance ranges of semiconductor detectors based on III-V antimonide alloys (e.g., InAsSbP, InGaAsSb, and AlGaAsSb) are limited by lattice-matching constraints, as epitaxial device layers should generally be closely lattice-matched (< 1%) to their substrate in order to avoid excessive defect levels. Thus, epilayer compositions that would nominally satisfy bandgap specifications for particular wavelength bands of operation are eschewed due to the inavailability of a substrate with the desired lattice constant. Lattice matching considerations are one of the most important criteria in formulating an epitaxy process, especially with regard to reducing threading dislocation concentrations; maintaining smoothness, thickness uniformity, and homogeneity of epilayers and avoiding corrugated surface morphologies; and controlling or exploiting strain effects that influence optical and electrical properties. The lattice mismatch between substrate and epilayer determines the critical thickness that delimits whether the epilayer is relaxed (with dislocations) or coherent (strained or pseudomorphic), an aspect of growth which is especially important in quantum well or superlattice structures.

In epitaxy of many III-V alloys, lattice matching constraints are further exacerbated by miscibility gaps that can preclude alloys with compositions (and bandgaps) prone to spinodal decomposition. Consequently, miscibility considerations may impose additional restraints on alloy compositions suitable for lattice-matched III-V semiconductor device designs. To a certain degree, lattice-matched epitaxial layers with compositions inside the miscibility gap can be stabilized against decomposition; the strain energy that a homogeneous layer incurs by separating into lattice-mismatched phases impedes decomposition. In many instances, a wider selection of substrate lattice constants would help circumvent limitations associated with miscibility gaps.

Semi-insulating substrates are useful for device isolation and for reducing substrate capacitance effects that can limit device speed. A significant drawback of the low-bandgap III-V antimonides is the lack of semi-insulating substrates, such as are available with GaAs and InP. The low bandgaps of InAs, InSb, and GaSb result in relatively high room-temperature thermal carrier generation, and consequent high substrate conductivity. On the other hand, substrates with wide bandgaps ($> \text{approx. } 1.3 \text{ eV}$) can be rendered semi-insulating provided the residual doping and certain background impurities are kept sufficiently low such that conductivity is dominated by intrinsic carriers. Close donor-acceptor compensation, control of electrically active defects and impurities such as oxygen, and/or the introduction of deep donor or acceptor levels can also increase resistivity. Nevertheless, the techniques used to produce very high resistivity in GaAs, InP, and GaP substrates have not been effective with GaSb, InAs, or InSb—or with Ge or Si for that matter. Thus, the growth of wide-bandgap antimonide alloy layers, especially compositions rich in AlSb ($E_g = 1.5 \text{ eV}$), in combination with techniques for inducing semi-insulating behavior, may present a route for producing semi-insulating wafers suitable for lattice-matched growth of III-V antimonides. Some caution is warranted here, however, since the more complex field of defects in ternary and quaternaries may contribute to electrical conduction mechanisms that are difficult to control. A more promising approach for achieving substrate isolation is perhaps provided by wafer bonding techniques whereby an epilayer is transferred to an insulating surrogate substrate.

2. Some Prior Relevant Work on Alloy Substrates

As a general rule, the only readily available substrates are wafers sliced from ingots of bulk-grown elemental semiconductors (Ge and Si) or congruently melting, stoichiometric binary compounds (e.g., InAs, InSb, GaSb, GaAs, ZnSe, and SiC). The potential advantages of ternary and quaternary alloy substrates as discussed above have been appreciated for quite some time, and the production of new alloy semiconductor wafers has been an area of long standing interest with considerable potential applications [2-13]. "Bulk" photon or particle detectors with tunable bandgaps and optical absorption edges can be directly fabricated in such alloy substrates. Still, of much greater interest is the use of such alloy substrates for epitaxial growth of semiconductor device structures. As an example of a purely optical application, 2- to 3-mm thick plates of ternary and quaternary III-V antimonide alloys can be used as window materials with tunable optical absorption edges in mid-infrared laser protection schemes.

We note some limited successes in growing bulk ternary crystals of InAsSb, HgZnTe, and HgMnTe for certain composition ranges using the Bridgman-Stockbarger technique (directional melt freezing); or through solid-state recrystallization or zone melting growth of quenched or sintered charges [14]. Nevertheless, growth of ternary and alloy semiconductor is typically hampered by severe segregation effects, sensitivity of solid composition to fluctuations in growth temperature, and the high vapor-pressure of components resulting in evaporative losses and changes in melt composition. In spite of these difficulties, much effort has been directed toward making alloy substrates using adaptations of bulk crystal growth, such as Czochralski crystal pulling or horizontal boat directional solidification, from three-component melts to produce boules or ingots of the ternary alloy. This is reasonable since crystallization rates from the melt are sufficiently fast enough to grow large crystals that can be cut into free-standing wafers with thickness of 100 to 1000 microns. In contrast, vapor-phase or vacuum growth (e.g., CVD or MBE) is usually considered much too slow to achieve crystals with millimeter thicknesses. (However, there are some notable exceptions such as vapor-phase growth of bulk AlSb [15] and ZnS.)

While most semiconductor substrates are made by slicing wafers from boules grown from congruently-solidifying stoichiometric melts, the *epitaxial growth* of substrate wafers, either from the vapor-phase or from non-stoichiometric liquid solutions as will be described shortly, is not unprecedented. For example, commercial ultrabright light-emitting diodes utilize a 100-micron thick AlGaAs "transparent substrate" grown by liquid-phase epitaxy [16]. Moreover, SiC substrates are grown by what is essentially a vapor-phase sublimation process. Sumitomo, Inc. (Japan) is producing ZnSe wafers made by vapor-phase transport processes, and Crystal Photonics, Inc. (Sanford, FL) is developing a GaN substrate made by vapor-phase epitaxy. In general, however, the application of epitaxial growth methods for substrate production would normally be considered uneconomic due to the slow growth rates (< 0.1 to 1 microns / min) resulting in very low throughput. (Evidently, in the instances cited above the advantages gained by epitaxial growth with respect to material quality are so compelling that the slow growth rates are acceptable, and that at least for certain materials, a premium will be paid for high-quality substrates made by unconventional or specialized techniques.) Solution growth methods, specifically liquid-phase epitaxy (LPE), might also be dismissed as too slow for the practical growth of bulk crystals. LPE is usually effected by precipitation from a molten metal solution that is dilute in at least one component of the crystallized material. For instance, the LPE growth of AlGaAs occurs from Ga-rich solutions with As and Al concentrations on the order of 1 atomic-% and 0.01 atomic-%, respectively; and growth rates are typically in the 0.1 micron / min range. Nevertheless, there are at least several III-V antimonide alloy semiconductors where the LPE melt is relatively rich in all components. For example, for GaInSb solidified at ~ 550 °C the liquid-phase atomic fractions are $X_{Ga} \sim 0.3$, $X_{In} \sim 0.5$ and $X_{Sb} \sim 0.2$. These ternaries generally exhibit fast LPE growth rates (1 to 5 microns / min), and in such cases, the distinction between melt growth and solution growth is not sharp.

Thick (> 50 micron), low-defect, compositionally-graded epitaxial layers of ternary and quaternary alloys, termed "virtual substrates" by MAO and KRIER [17], would effectively satisfy many of the same specification objectives that are sought in substrate wafers sawed from ternary ingots. Assessment and applications of thick LPE layers, and specifically, the use of a thick continuously compositionally-graded single layer or step-graded multilayers, often in for low-bandgap III-V antimonide alloy detector or LED structures have been reported by several groups [18-23]. As mentioned, the seeding substrate can be selectively removed and/or the epitaxial layer can be transferred to an insulating surrogate superstrate, thus increasing its functionality for device applications benefiting from a transparent or electrically isolating substrate.

3. Technical Approach

Our approach is based on adaptations of liquid-phase epitaxy (LPE) technology for the production of so-called *virtual substrates*. These virtual substrates are essentially thick (> 100 micron), potentially self-supporting epitaxial structures of ternary or quaternary III-V antimonides grown from liquid-metal solutions by a modified LPE process. Multiple growths; i.e., separate LPE steps where the epitaxial structure is cooled to room temperature, removed from the LPE system, and used as a substrate for another LPE growth; are feasible. Each LPE step adds a layer and increases the total thickness of the stack. The associated compositional step-gradings at each growth interface contributes to the total lattice constant deviation from the binary substrate upon which the stack is seeded and supported. Epilayers are added until the desired lattice constant targeted for the ultimate top layer is achieved.

An overview of two basic but closely related options is shown in FIGURE 1. A III-V binary compound substrate (e.g., InAs, GaSb, or GaAs) is used to seed the epitaxial growth of the virtual substrate. The epitaxial virtual substrate layer(s) can be transferred to a surrogate substrate, such as a semi-insulating GaAs wafer, using bonding and etching techniques already demonstrated or currently in development for silicon and other III-V semiconductors. Alternatively, if foregoing a bonded surrogate substrate, then the epitaxial layers of the virtual substrate are made sufficiently thick to be self-supporting and do not need the binary seeding substrate for mechanical support. In either case, the binary seeding substrate can be removed by post-growth selective or controlled etching, yielding a free-standing wafer of a ternary or quaternary alloy.

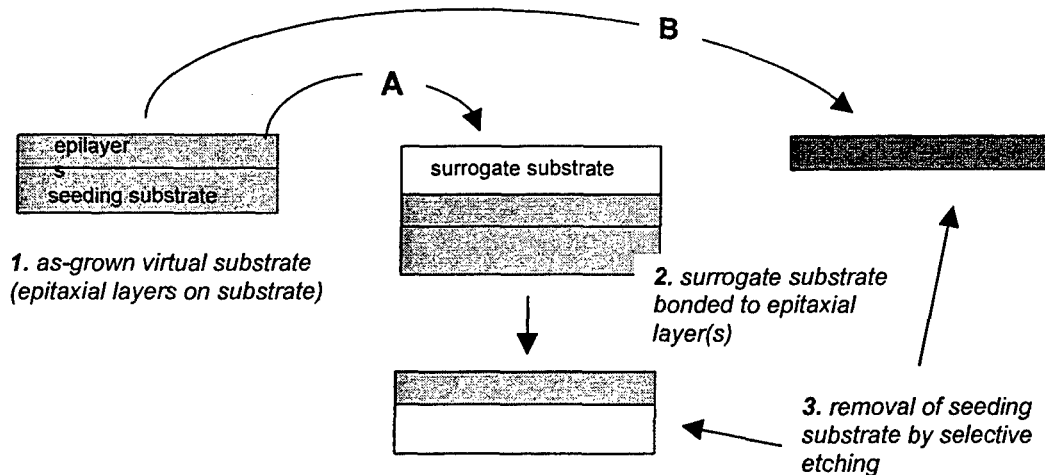


FIGURE 1: Options for virtual substrates: 1. epitaxial growth of thick multilayers on a binary compound seeding substrate (e.g., GaSb, InAs, InSb, or GaAs); Option A: 2. a surrogate substrate (e.g., semi-insulating GaAs, oxide-coated silicon, or a thermal-expansion matched insulating material) is bonded to the exposed surface of the epitaxial layers, 3. which is then removed by selective etching. Option B: the epitaxial virtual substrate is grown sufficiently thick to be self-supporting, in which case, 3. the seeding substrate can be removed by etching.

4. Experiments and Results

An important advantage of the proposed work is the ability to make ternary and quaternary substrates with lattice constants significantly different than that currently available with the wafers of binary compound such as GaSb, InAs, InSb, and GaAs. By growing multiple layers with a small composition change and related lattice constant change (0.1 to 0.3 %) at each interface, the cumulative effect is a top layer alloy with a lattice constant significantly different than that of the binary seeding substrate. Thus, the bandgap in which a device is fabricated, or the lattice constant of the surface upon which a device structure is grown in a subsequent MBE or MOCVD epitaxy step can be parameterized over some range, hopefully without generating excessive defects. The change in lattice constant at each interface must be sufficiently small to maintain low densities of misfit dislocations [24]. Additionally, such thick LPE layers tend to "anneal-out" defects [25], which is an important advantage gained by the high growth rates inherent in LPE. Details of III-V antimonide LPE processes can be found in ref. [26] and references contained therein.

For the LPE we use a graphite slideboat technique in a horizontal, three-zone, resistively heated, 55-mm diameter fused-silica tube furnace. All of the systems are microprocessor-controlled and can be programmed with elaborate time-temperature schedules. The growth ambient is 1-atm pressure, Pd-membrane purified hydrogen with a flow rate of 30 ml/min. Growth temperatures are in the range of 400 to 650 °C. Upon contact with the melt, the substrate is ramp-cooled at a rate of 1 °C / min. Our research epitaxy normally uses 1 cm x 1 cm substrates, but substrate sizes up to 5 x 5 cm can also be used. Typically, such an LPE system is used for one epitaxy run per day, although two or three epitaxy experiments per system per day is feasible. One technician can operate as many as four systems simultaneously, and various heterostructures based on InGaAsSb, AlGaAsSb, InAsSbP alloys are routinely grown. Substrates are polished wafers of (100) oriented GaSb:Te and InAs:S and are obtained from a number of vendors including Firebird Semiconductor (British Columbia), MCP Wafer Technology (Milton Keynes, UK), Galaxy Compound Semiconductors, Inc. (Spokane, WA) and Princeton Scientific (Princeton, NJ). (111)-oriented GaSb wafers were used in some experiments. Pieces of these wafers were also used as source materials for the melts. All metals are six-9's purity obtained from Alfa Aesar (Ward Hill, MA) or Atlantic Metals & Alloys, Inc. (Stratford, CT). Prior to growth, metals are baked out for sixteen hours at a temperature of 100 °C above the highest growth temperature in flowing hydrogen to remove residual impurities and reduce oxides. In the

following, we present results for thick epilayer growths of several antimonide-based III-V alloys. The top surface(s) and cross sections of the epitaxial structures are characterized by optical, scanning electron, and atomic force microscopy, defect etching, energy-dispersive x-ray analysis, electron microprobe analysis, Raman spectroscopy, photoluminescence, and high-resolution x-ray diffraction.

4.1 Thick InAsSb LPE Layers

We first studied the characteristics of liquid-phase epitaxy of thick InAsSb layers on InAs substrates. The substrates are polished (100) oriented InAs wafers diced into 1-cm x 1-cm rectangles. We start with melt compositions (i.e., indium saturated with InAs) and growth temperatures that produce thick (> 200 micron) layers of InAs on InAs substrates, followed by experiments wherein the relative antimony content of the melt is increased incrementally with the objective to empirically determine the effect of increasing antimony content on growth characteristics. Although lattice mismatch is perhaps most important in determining the quality of growth, substrate dissolution, solute mass transfer in the melt, and effective supercooling are also contributing factors. We are able to grow InAsSb layers of several hundred microns on InAs substrates in a single LPE step by cooling In-As-Sb melts from 650 °C to 530 °C over a course of 2 hours.

4.2 Thick LPE Layers of InGaSb and AlGaAsSb

We have developed modified LPE techniques for the growth of thick, closely-lattice matched epilayers of InGaSb and AlGaAsSb. FIGURES 2 and 3 show cross-sections of >100-micron thick epilayers of $\text{In}_{0.04}\text{Ga}_{0.96}\text{Sb}$ on GaSb and AlGaAsSb on GaSb. This demonstrates that very thick layers of these III-V antimonide alloys can be grown by conventional methods of LPE. In many cases, LPE of alloy epilayers appears straightforward, however, in general such growth of a ternary or quaternary epilayer on a binary substrate is a complex process involving initial dissolution of the substrate (a binary substrate can never be in equilibrium with a 3- or 4-component melt), formation of an interlayer, solid-state diffusion, or changes in the saturation of the solution [27,28]. FIGURE 4 indicates an example of this behavior, showing a plot of growth thickness for several growth times (separate epitaxy experiments with varying growth times) for a ramp-cooling mode of growth (1 °C/min). Initially, there is melt back of the substrate ("negative" growth thickness) as the non-equilibrium conditions are relieved by dissolution of the GaSb substrate. After sufficiently long times, there is a net growth of quaternary alloy on the substrate. The growth rate then diminishes, and the epilayer attains an ultimate thickness. Such melt back and regrowth invariably results in rough interfaces. These effects are not inevitable and can be minimized by proper selection of melt composition and growth parameters (temperature, initial supersaturation, and ramp cooling rates). As Figure 3 demonstrates, a thick AlGaAsSb epilayer on a GaSb substrate with a smooth interface is attainable.

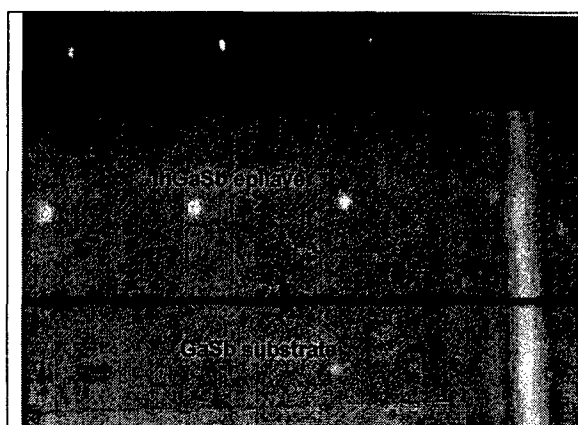


FIGURE 2: $\text{In}_{0.04}\text{Ga}_{0.96}\text{Sb}$ epilayer on GaSb substrate cross-section. Thickness of epilayer is 160 microns.

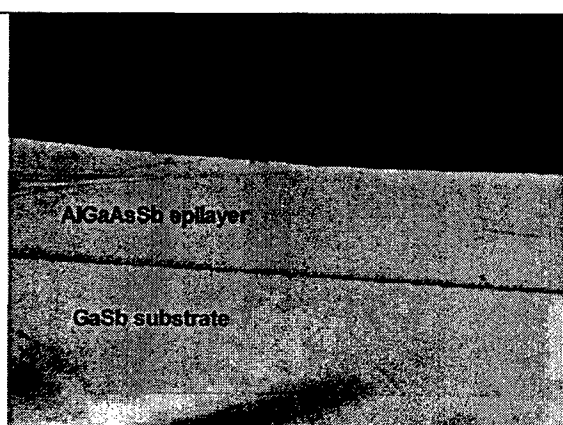
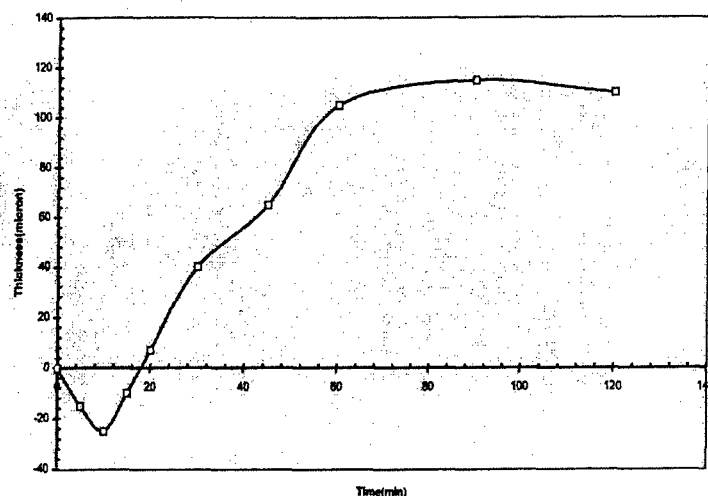


FIGURE 3: AlGaAsSb on GaSb substrate cross-section. (Epilayer is 200 microns thick. Ramp-cooling mode of growth).

Figure 4: AlGaAsSb epilayer thickness as a function of contact time for growth on a (100)GaSb substrate. Growth solution is ramp-cooled at a rate of 1 °C/min from an initial temperature of 515 °C. Negative thickness corresponds to dissolution of the substrate ("melt back"). After sufficiently long times (≈ 20 mins), there is a net growth of the AlGaAsSb quaternary alloy.



4.3 Thick LPE Multilayers of InAsSb

Stacks of thick ($> 50 \mu\text{m}$) compositionally step-graded $\text{InAs}_{1-x}\text{Sb}_x$ layers on (100) InAs substrates, where x increases with each layer, are also feasible. To make such and similar structures, we found it was feasible and convenient to grow each thick ternary (or quaternary) layer in separate, successive LPE steps. For LPE of III-V antimonides, cleaning and surface preparation are evidently not overly critical for the success of these multi-step LPE processes: we can routinely and consistently use samples with epitaxial layers as substrates for subsequent LPE growth without surface cleaning or etching between growths. FIGURES 5a and 5b are cross-sections after the three-step growth of three InAsSb epilayers. Each layer has a successively higher antimony fraction. This is effected by increasing the relative proportion of antimony in the In-Sb-As melt. The melt compositions for the two samples for which stained cross-sections are shown in FIGURES 5a and 5b are summarized in TABLE 1. All layers were grown at 650 °C for 120 minutes. Excess InAs in the form of a wafer floating on the melt was used as the source of arsenic. The step grading is dictated by the maximum abrupt lattice change at each growth interface that can be tolerated to maintain epitaxial growth and thus single-crystal layers (see refs. 24-26 for elaboration). If the difference in lattice constants of adjacent layers is too large, non-optimum nucleation is likely. On the other hand, higher antimony in the melt probably inhibits melt back of the underlying layer. This then suggests an optimum antimony fraction for each layer.

Each layer is approximately 100 microns thick so that the thickness of the composite structure (not including the substrate) is about 0.3 mm. The interfaces are smooth and abrupt. In the sample shown in FIGURE 5a, the top layer is rough and polycrystalline. We interpreted this as due to excessive lattice mismatch between the second and third layer. We then reduced the amount of antimony in the melt used to grow the third layer (from 1.6 g to 1.53 grams). This resulted in a smooth third layer. Energy-dispersive x-ray spectroscopy (EDS) indicates the composition of the top layer is $\text{InAs}_{0.8}\text{Sb}_{0.2}$. X-ray diffraction indicates the layers are completely relaxed. The lattice constant difference between the top $\text{InAs}_{0.8}\text{Sb}_{0.2}$ and the InAs substrate is $\approx 1.5\%$.

The desired change in composition in step-graded LPE-grown structures raises the issue of lattice *pulling* or *latching*. In some systems, there is a tendency for a lattice-matched composition of the ternary or quaternary to grow in preference to the composition predicted by the phase diagram [25-27]. The stabilization of lattice-matched compositions against small changes in melt composition is advantageous in some applications. On the other hand, for step-graded, multilayer virtual substrates this phenomena might imply a minimum supersaturation and associated composition/lattice-constant step is required to overcome the tendencies of lattice pulling.



FIGURE 5a: Cross-sectional view of three layers of InAsSb on InAs substrate. Total thickness of three epilayers is ~ 0.3 mm.

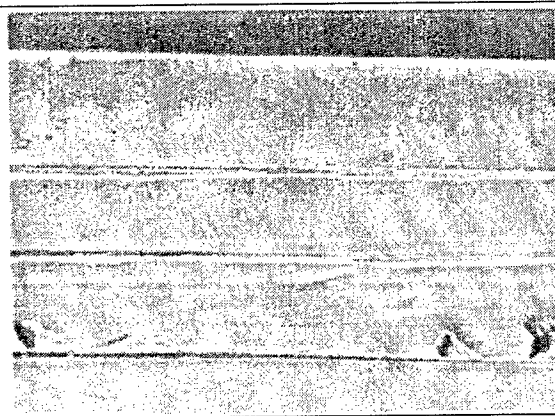


FIGURE 5b: Cross-sectional view of three layers of InAsSb on InAs substrate. Total thickness of three epilayers is ~ 0.3 mm.

TABLE 1: SUMMARY OF STEP-GRADED THREE-LAYER InAsSb GROWTHS (SHOWN IN FIGURES 5a AND 5b)

		Composite structure shown in FIGURE 5a	Composite structure shown in FIGURE 5b
top layer	indium in melt (g)	4.40	4.47
	antimony in melt (g)	1.60	1.53
	epilayer composition	$\text{InAs}_{0.8}\text{Sb}_{0.2}$	$\text{InAs}_{0.8}\text{Sb}_{0.2}$
	lattice mismatch	approx 1.5%	approx 1.5%
middle layer	indium in melt (g)	4.60	4.60
	antimony in melt (g)	1.40	1.40
	epilayer composition	$\text{InAs}_{0.85}\text{Sb}_{0.15}$	$\text{InAs}_{0.85}\text{Sb}_{0.15}$
	lattice mismatch	approx. 1.0%	approx. 1.0%
bottom layer (next to substrate)	indium in melt (g)	4.80	4.80
	antimony in melt (g)	1.20	1.20
	epilayer composition	$\text{InAs}_{0.93}\text{Sb}_{0.07}$	$\text{InAs}_{0.93}\text{Sb}_{0.07}$
	lattice mismatch	approx. 0.5%	approx. 0.5%

notes: melts are saturated with an InAs source; epilayer compositions determined by EDS or electron microprobe to approx. ± 2 atomic percent resolution.

4.4 Multi-Layer LPE Growth of InGaSb, InGaAs, and InAsSbP

The cross-section of a two-layer $\text{In}_x\text{Ga}_{1-x}\text{Sb}$ ($x \approx 0.05$) structure grown on a (100) GaSb substrate is shown in FIGURE 6. The InGaSb layers are grown in two separate LPE steps each at a starting ramp temperature of 500 °C. Similarly, two-layer InGaAs structures with a total epitaxial layer thickness of 0.25 mm were grown in two LPE steps both with starting ramp temperatures of 600 °C. Layers with thicknesses on the order of 100 microns require about 1 to 1.5 hours growth time. A cross-section of a three-layer stack of InAsSbP on an InAs substrate is shown in FIGURE 7. In this case, for each of the three LPE steps, the melt atomic fractions are $X_{\text{In}} = 0.589$, $X_{\text{Sb}} = 0.40$, $X_{\text{As}} = 0.01$ and $X_{\text{P}} = 0.00088$ and the growth temperature is 565 °C which yields an epitaxial layer with a composition of $\text{InAs}_{0.6}\text{Sb}_{0.2}\text{P}_{0.2}$. As before, in each successive LPE step we change the melt composition to effect a small lattice change at each interface, and again, in principle multiple LPE steps can be performed several times to achieve a desired lattice constant substantially different than the binary seeding substrate wafer (GaSb or InAs). The defect density of the last-grown epilayer of the stack will depend on the lattice constant steps and epilayer thicknesses.

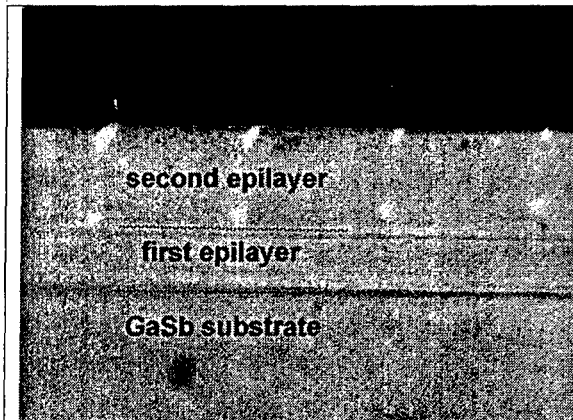


FIGURE 6: Cross-section of a two-layer InGaSb structure on a GaSb substrate. The total thickness of the layers is 250 microns.

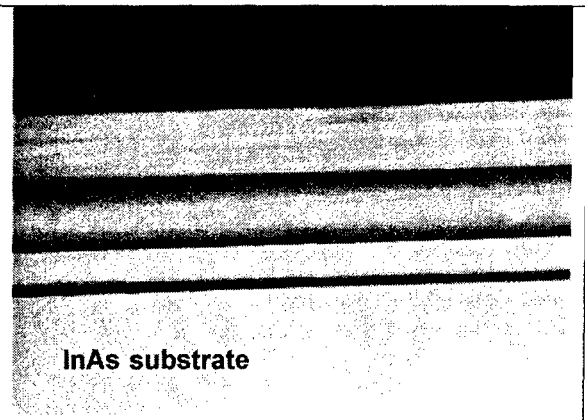


FIGURE 7: Cross-section of a three-layer InAsSbP structure on an InAs substrate. The total thickness of the layers is 150 microns.

The utility of step-graded ternary and quaternary alloy multilayers for virtual substrates is contingent upon the simultaneous achievement of two objectives: 1. the lattice constant of the top layer should be significantly different than the underlying binary substrate upon which the first layer was seeded and this needs to be achieved in a reproducible and consistent manner with negligible variation over the entire area of the top layer, and 2. the defect density due to misfit and threading dislocations must be sufficiently low ($\ll 10^3$ or 10^4 cm^{-2}), preferably comparable to that of GaAs wafers. FIGURE 8 shows the high-resolution x-ray diffraction for a composite structure of two InAsSbP layers, each approximately 40 microns thick, on an (100) InAs substrate. The compositions of the LPE layers are adjusted to effect a modest lattice mismatch at each interface. Modeling indicates an approximate 2% lattice mismatch between the top InAsSbP epilayer and InAs substrate. FIGURE 9 is an atomic force microscope scan showing the exceptionally smooth surfaces produced by this LPE process: the root mean square roughness is $\sim 0.2 \text{ nm}$. Defect etching studies on these layers indicate an etch pit density of less than 10^4 cm^{-2} .

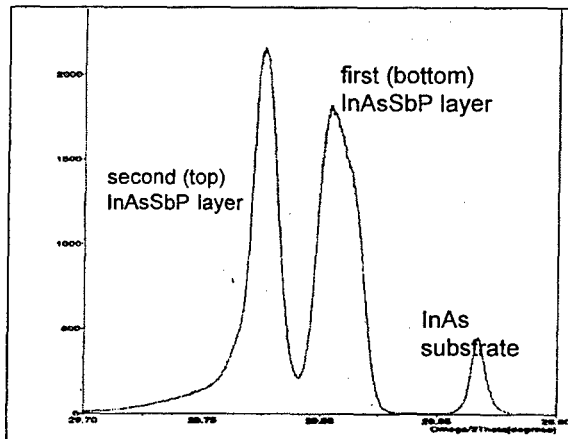


FIGURE 8: High-resolution double crystal x-ray diffraction peaks for a two layers of InAsSbP on InAs substrate, (004) peaks shown.

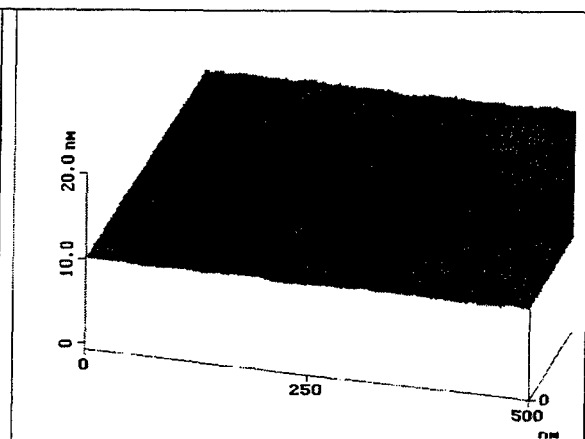


FIGURE 8: AFM surface profile of three layer InAsSbP/InAs structure similar to that shown in FIGURE 7.

LPE-grown layers can be bonded to a superstrate such as, for example, a metal sheet, a glass slide, an oxidized silicon wafer, a semi-insulating GaAs substrate, or a GaSb wafer coated with an insulating dielectric film. The binary seeding substrate can be removed by controlled and/or selective wet etching, and the resulting epilayer/surrogate substrate composite can be polished as needed. FIGURE 10 shows a top-view of a 20-micron thick InAsSbP epilayer bonded to a glass slide after the GaSb has been etched away. As an indication of the potential for a scaled-up implementation of these ideas, but demonstrated for AlGaAs rather than III-V antimonides, FIGURE 11 shows a 3-inch (75-mm) diameter, 50-micron thick, LPE-grown $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ epilayer (which is semitransparent) epoxied to a glass superstrate after the GaAs seeding substrate was removed by wet chemical etching. More sophisticated wafer bonding techniques could be applied to the structures described here. Some relevant related work in this area includes the demonstration of 100-GHz InGaAsP photodiodes formed on sapphire substrates [30]. A spin-on sodium silicate glass was used to bond InGaAsP /InP epitaxial structures to sapphire followed by removal of the InP substrate by wet etching.

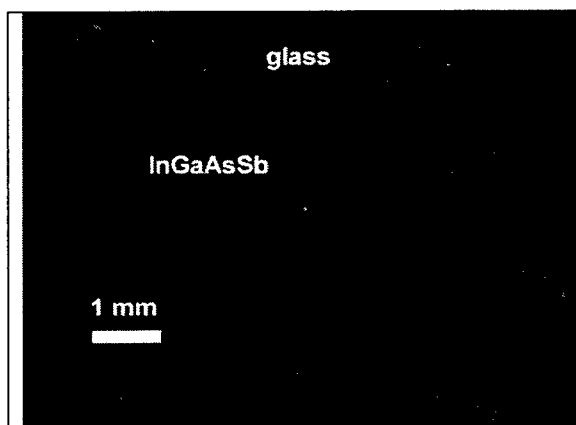


FIGURE 10: 20-micron thick InGaAsSb epilayer bonded to a glass superstrate with GaSb substrate removed by wet etching. (See text for description).

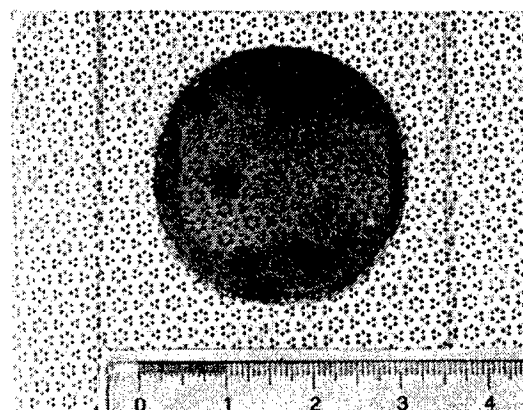


FIGURE 11: 75-mm diameter, 50-micron thick $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ epilayer bonded to glass superstrate. (GaAs seeding substrate removed.)

5. Summary and Discussion

Liquid-phase epitaxy techniques can be used to produce thick (50 to 500 micron) layers of ternary and quaternary alloys including InAsSb, InGaSb, AlGaAsSb, InGaAsSb, and InAsSbP. LPE of the III-V antimonides exhibits remarkably high growth rates (1 to 10 microns / min), thus making very thick layers feasible. Using gradual- or step-compositional grading, low-defect layers with lattice constants and bandgaps significantly different from the binary substrate on which the thick layer(s) are seeded can be achieved. Additionally, the thick epitaxial layer can be bonded to a surrogate (insulating) substrate and the seeding binary compound substrate can then be removed by selective etching, yielding a semiconductor-on-insulator structure. These techniques are applicable to a practically all III-V compound alloys that can be grown by LPE and are sufficiently versatile to enable a wide assortment of structures suited for various device applications. The most profitable near-term applications appear to be mid-infrared detectors. These devices will also serve as excellent test structures to evaluate material quality. We are currently exploring alternative LPE methods, such as piston-boat techniques [31] for making virtual substrates. Although the customized substrates described here will cost more than commercially available wafers, e.g. GaSb or InAs, we believe they will be considerably less expensive than some recently developed niche substrates such as SiC or GaN wafers, and further, the added cost of III-V antimonide virtual substrates will be justified by improved performance and new regimes of device operation for mid-infrared optoelectronics.

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